Superconducting Magnetic Energy Storage Based DC Unified Power Quality Conditioner with Advanced Dual Control for DC-DFIG

Ruohuan Yang, *Student Member*, *IEEE*, Jianxun Jin, *Fellow*, *IEEE*, Qian Zhou, Shuai Mu, and Ahmed Abu-Siada, *Senior Member*, *IEEE*

***Abstract*—The development of DC custom power protection devices is still in infancy that confines the sensitive loads integrated into medium-voltage (MV) and low-voltage (LV) DC networks. Considering the DC doubly-fed induction generator (DC-DFIG) based wind energy conversion system (WECS), this paper proposes a dual active bridge (DAB) based DC unified power quality conditioner (DC-UPQC) with the integration of superconducting magnetic energy storage (SMES) to maintain the terminal voltage of DC-DFIG and regulate the current flow. The principle of the proposed DC-UPQC has three parts, i.e., parallel-side DAB (PDAB), series-side DAB (SDAB), and SMES, used for the voltage compensation, current and power regulation, and energy storage, respectively. The circuit principle of the PDAB and SDAB and the modeling of SMES are analyzed in this paper. A DC dual control strategy is also proposed to deal with the DC voltage oscillation generated by the AC-side asymmetrical fault. A case study of DC-DFIG interfaced with DC power grid is carried out, integrated with the proposed SMES-based DC-UPQC to verify the high-power applications of the proposed structure. Finally, an experiment is implemented, and the results demonstrate the correctness of the theoretical analysis and the feasibility of the proposed structure.**

***Index Terms*—DC network, unified power quality conditioner (UPAC), DC doubly-fed induction generator (DC-DFIG), power quality.**

I. Introduction

THE medium-voltage (MV) and low-voltage (LV) DC distribution systems have attracted increased attention in the past few years, owing to the advantages of concise structure, high economy, and convenient interface to energy storage devices (ESDs) and renewable power generators (RPGs) [1], [2]. However, the penetration of power-electronic-controlled DC RPGs will lead to power quality issues [3]. Among DC RPGs, the DC doubly-fed induction generator (DC-DFIG) based wind energy conversion system (WECS) has been widely investigated in [4]-[7], which mainly consists of a DFIG, a diode rectifier, and a rotor-side converter (RSC). Compared with the traditional DFIG, the DC-DFIG-based WECS has a more economical structure since the grid-side converter (GSC) is no longer needed. However, the uncontrolled commutation of the diode rectifier makes the DC-DFIG-based WECS lack the low-voltage ride through (LVRT) capability and thus vulnerable to DC grid faults. What is worse, when an asymmetrical fault occurs at the AC side, there will be a voltage sag accompanied by a 100 Hz voltage oscillation in the DC voltage. If not adequately considered, the voltage oscillation will lead to highly unbalanced current and power, resulting in significant losses of power system revenue and sensitive loads [8], [9].

To improve the LVRT capability of DFIG-WECS, many solutions have been proposed [10]-[15], which can be approximately classified into two categories, i. e., software-based solutions and hardware-based solutions. Software-based solutions can be further divided into two parts. Some of the software improvements, such as demagnetizing control [10], flux linkage tracking control [11], and current reversely tracking control [12], [13], aim at improving the control strategies of DFIG RSC. When a DC fault occurs, the software-based solutions are still applicable for DC-DFIG, but a concern is raised in [14], [15] that the DC current will rapidly increase with a considerable amplitude in a short time. Such a DC fault current will seriously cause damage to the assailable equipment such as diode rectifier and insulated gate bipolar transistor (IGBT) switches used in DC-DFIG-based WECS.

Some software-based methods are proposed to regulate the DC voltage profile of the DC microgrids, such as hierarchical control, which has been widely investigated. Inside the hierarchical control, the secondary control is responsible for the voltage regulation and current sharing among renewable energy sources [16], [17]. However, when a severe grid fault occurs, software-based solutions are ineffective in sustaining load voltage due to the limited capacity of the converters. In addition, software modifications lack the capability to protect a certain sensitive load. Therefore, hardware-based solutions should be considered.

Manuscript received: June 2, 2021; revised: September 13, 2021; accepted: November 18, 2021. Date of CrossChecked: November 18, 2021. Date of online publication: February 4, 2022.

R. Yang, J. Jin (correspongding author), Q. Zhou, and S. Mu are with the School of Electrical and Information Engineering, Tianjin University, Tianjin 300072, China (e-mail: yrh9312@163. com; jxjin@tju. edu. cn; zhou_qian@tju. edu.cn; mushuai1108@tju.edu.cn).

A. Abu-Siada is with the Department of Electrical and Computer Engineering, Curtin University, Perth, WA 6102, Australia (e-mail: a.abusiada@curtin.edu. au).

DOI: 10.35833/MPCE.2021.000354

Among hardware-based solutions, crowbar protection circuits are the most widely used and have been already commercially adopted in many DFIG-based WECSs [18], [19]. But the problem of the crowbar protection circuit is that the pulsation of the electromagnetic (EM) torque cannot be confined. Custom power protection devices such as dynamic voltage restorer (DVR) [20], [21], series GSC (SGSC) [22], [23], superconducting fault current limiter-magnetic energy storage (SFCL-MES) [24], and unified power quality conditioner (UPQC) [25]-[27] are proposed for AC DFIG-based WECSs, but they are not suitable for DC-DFIG-based WECSs due to the architectural difference of the two systems. Various types of non-superconducting fault current limiters (FCLs) [28]-[30] and SFCLs [31], [32] also provide good hardware-based solutions, due to their advantages of low cost and straightforward structure. However, several issues should be noted: ① the load voltage cannot be accurately compensated to the rated voltage; ② without the utilization of energy storage, the intermittency of the renewable power sources cannot be well-addressed; ③ various modified controls are not suitable for FCLs, which limit its ability to suppress the voltage and current oscillations.

Relying on the development of the dual active bridge (DAB) [33]-[35], some DC custom power protection devices have been proposed. Based on the structure, the DC custom power devices (CPDs) can be categorized into two main classifications, i.e., series CPD (SCPD) and parallel CPD (PCPD). PCPDs including various kinds of energy storage interfaced to power grid via power-electronic-based converters [36]-[38], active power filter [39], and power flow controller [40]-[42] provide an additional shunt path to regulate the current quality of the DC transmission line. They can filter the DC current ripple or smooth the time-varying stochastic power caused by the intermittent renewable energy sources. In contrast, SCPDs are utilized to solve the voltage quality issue. The typical SCPDs in DC systems include intelligent uninterruptible power supply (IUPS) [43], DC-DVR or series voltage regulator (SVR) [44], [45], and superconducting magnetic energy storage (SMES) based transformerless SVR (TLSVR) [46]. Although these hardware systems are used for DC voltage restoration, a little concern is raised when the abovementioned SCPDs are used.

In the field of voltage quality, the DC voltage swell always appears along with the DC voltage sag [47], [48]. Therefore, the SCPDs are required to have a bidirectional voltage compensation capability. However, the voltage direction of each side of the traditional DC/DC DAB is inherent, which limits the ability to deal with either voltage sag or voltage swell. For instance, the DC-DVR proposed in [44] can only mitigate the voltage sag. To acquire the bidirectional voltage compensation capability, additional converters are required, such as the IUPS proposed in [43] and the SVR proposed in [45], but the increased number of converters will result in a compliable control issue. The AC/AC matrix converter [49] provides a more straightforward structure and a more concise control for bidirectional voltage output. Matrix-converter-based devices are presented in [50]-[52], and their performances in voltage restoration are initially validated in [46].

Combining the advantages of the DAB and matrix converter and synthesizing the functions of PCPD and SCPD, a DAB-based DC-UPQC is proposed in this paper to simultaneously improve the LVRT capability of the DC-DFIG and regulate the output DC current and power. As an ESD for smoothing the time-varying wind power, the SMES is adopted at the DC bus of DC-UPQC. The system configuration of the DC-DFIG-based WECS with the integration of the DAB-based DC-UPQC is shown in Fig. 1. The proposed DC-UPQC comprises three parts: ① a series-side DAB (SDAB) for the voltage regulation, serving as an SCPD; ② a parallel-side DAB (PDAB) for the power management and current quality improvement, serving as a PCPD; and ③ an SMES serving as an energy storage system to carry out the energy exchange with the two DABs, for storing the surplus energy from the DC-DFIG under high wind speed and low load demand, and releasing energy under low wind speed and high load demand.

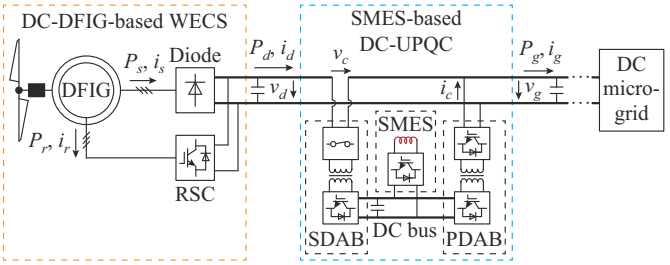

Fig. 1. System configuration of DC-DFIG-based WECS with integration of DAB-based DC-UPQC.

The unbalanced oscillation of DC voltage should also be considered. In AC systems, the dual control can be adopted in dealing with the unbalanced AC voltage. The core concept of this control system is to decompose the voltage/current signals into positive- and negative-sequence components and control these two signals separately [53], [54]. However, this control system calls for additional phase-locked loop (PLL) and three-phase (abc) to *dq* rotation coordinate transformation (abc/*dq* transformation). If the dual control is introduced into the control strategy of DC converter, the control system will be significantly complicated. The proportional-integral plus resonant (PI-R) controller is also an alternative method for precisely tracking the AC current references [55]. Nevertheless, there are some defects in the PI-R controller. Firstly, the parameter estimation of the R regulator will become more complex since the R regulator is in parallel with the PI controller. Once the R controller is not precisely designed, the compensation accuracy will be influenced. Secondly, the utilization of PI-R controller will result in longer recovery time [56]. In this paper, to simplify the control strategy and effectively suppress the DC voltage oscillation generated by asymmetrical fault, a band-pass filter based DC dual control utilized in the SDAB and PDAB is proposed. The complicated PLL and abc/*dq* transformation are not required in the proposed DC dual control, but the voltage and current oscillations can be well-suppressed.

In summary, the contributions of this paper are listed as follows.

1) A DC-UPQC is proposed to simultaneously enhance

the DC voltage and current qualities. Based on the modified structure and the support of ESDs, the proposed DC-UPQC has a wide range of four-quadrant *V-I* compensation. Meanwhile, the DC dual control is proposed in this paper to suppress the second-order voltage and current ripples.

2) An SMES is adopted as an ESD to regulate the power exchange via the two DABs of DC-UPQC. The structure, inductance, critical current, and capacity of SMES are estimated in this paper for the systematical application.

3) A DC-DFIG-based case study is carried out. The LVRT mechanism is analyzed in this paper, and the effectiveness of the proposed DC-UPQC in improving the LVRT capability and smoothing the output power is verified via simulation analysis.

4) Experimental analysis is also conducted to validate the circuit principle of the SDAB and PDAB, and demonstrate the feasibility of the proposed DC dual control.

The remainder of this paper is organized as follows. Section II introduces the modeling of DC-DFIG-based WECS and its parameter responses under the DC voltage sag and 100 Hz DC voltage oscillation. Section III presents the structure and circuit principles of the proposed DC-UPQC. Section IV introduces the control strategies of the proposed DC-UPQC. Section V shows the simulation and experimental results of the protection performance of DC-DVR in the DC-DFIG system. Section VI concludes the key findings of this paper.

II. Modeling of DC-DFIG and System Analysis

A. Behaviors of DC-DFIG Under DC Voltage Oscillation

Assuming that the DC-DFIG works under the normal operation and the terminal voltage v_d can be regarded as a constant, the AC-side stator voltage v_s of the DC-DFIG can be rectified by the diode rectifier as a three-step AC square wave, as shown in Fig. 2. Neglecting the initial phase, the three-phase stator voltages v_{sa}, v_{sb}, and v_{sc} can be expressed according to Fourier decomposition as [57]:

$$\begin{cases} v_{sa}(t)=\dfrac{2V_d}{\pi}\left\{\sin(\omega_s t)+\displaystyle\sum_{n=1}^{\infty}\frac{1}{6n\pm1}\sin\left[(6n\pm1)\omega_s t\right]\right\} \\ v_{sb}(t)=\dfrac{2V_d}{\pi}\cdot \\ \qquad\left\{\sin\left(\omega_s t-\dfrac{2}{3}\pi\right)+\displaystyle\sum_{n=1}^{\infty}\frac{1}{6n\pm1}\sin\left[(6n\pm1)\left(\omega_s t-\dfrac{2}{3}\pi\right)\right]\right\} \\ v_{sc}(t)=\dfrac{2V_d}{\pi}\cdot \\ \qquad\left\{\sin\left(\omega_s t+\dfrac{2}{3}\pi\right)+\displaystyle\sum_{n=1}^{\infty}\frac{1}{6n\pm1}\sin\left[(6n\pm1)\left(\omega_s t+\dfrac{2}{3}\pi\right)\right]\right\} \end{cases} \tag{1}$$

where V_d is the amplitude of DC bus voltage; and ω_s is the stator angular frequency.

Similar to the AC-DFIG system, the fundamental stator/rotor voltage and flux linkage equations of the DC-DFIG-based WECS can be established in the stationary $\alpha\beta$ frame [25], [58] as:

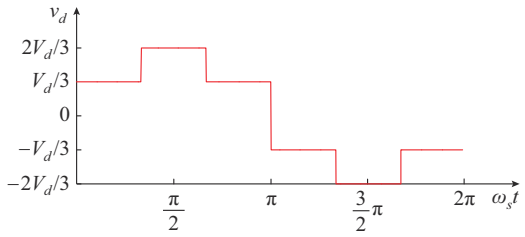

Fig. 2. Waveform of single-phase stator voltage of DC-DFIG.

$$\begin{cases} \boldsymbol{v}_{s\alpha\beta}=R_s\boldsymbol{i}_{s\alpha\beta}+\dfrac{\mathrm{d}\boldsymbol{\psi}_{s\alpha\beta}}{\mathrm{d}t} \\ \boldsymbol{v}_{r\alpha\beta}=R_r\boldsymbol{i}_{r\alpha\beta}+\dfrac{\mathrm{d}\boldsymbol{\psi}_{r\alpha\beta}}{\mathrm{d}t}-\mathrm{j}\omega_r\boldsymbol{\psi}_{r\alpha\beta} \end{cases} \tag{2}$$

$$\begin{cases} \boldsymbol{\psi}_{s\alpha\beta}=L_s\boldsymbol{i}_{s\alpha\beta}+L_m\boldsymbol{i}_{r\alpha\beta} \\ \boldsymbol{\psi}_{r\alpha\beta}=L_m\boldsymbol{i}_{s\alpha\beta}+L_r\boldsymbol{i}_{r\alpha\beta} \end{cases} \tag{3}$$

where R and L are the resistance and inductance, respectively; v, i, ψ, and ω are the voltage, current, flux linkage, and angular frequency, respectively, of which the space vector forms are bold; subscripts s and r are the stator and rotor of DC-DFIG, respectively; subscripts α and β represent α- and β-axis values, respectively; and L_m is the mutual inductance.

Combining (2) and (3), the space vector of dynamic rotor voltage can be expressed as:

$$\boldsymbol{v}_{r\alpha\beta}=\left(R_r-\mathrm{j}\omega_r\sigma L_r\right)\boldsymbol{i}_{r\alpha\beta}+\sigma L_r\frac{\mathrm{d}\boldsymbol{i}_{r\alpha\beta}}{\mathrm{d}t}+\underbrace{\frac{L_m}{L_s}\left(\boldsymbol{v}_{s\alpha\beta}-R_s\boldsymbol{i}_{s\alpha\beta}-\mathrm{j}\omega_r\boldsymbol{\psi}_{s\alpha\beta}\right)}_{\boldsymbol{e}_{r\alpha\beta}} \tag{4}$$

where $\boldsymbol{e}_{r\alpha\beta}$ is the transient electromotive force (EMF) introduced by stator flux linkage; and σ is the leakage coefficient, which can be expressed as:

$$\sigma=1-\frac{L_m^2}{L_sL_r} \tag{5}$$

According to (1), the space vector of stator voltage $\boldsymbol{v}_{s\alpha\beta}$ can be expressed as:

$$\boldsymbol{v}_{s\alpha\beta}=\frac{2V_d}{\pi}\left[\mathrm{e}^{\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{1}{6n\pm1}\mathrm{e}^{\pm\mathrm{j}(6n\pm1)\omega_s t}\right] \tag{6}$$

Neglecting the stator resistance, the space vector of flux linkage $\boldsymbol{\psi}_{s\alpha\beta}$ can be expressed as:

$$\boldsymbol{\psi}_{s\alpha\beta}=\int\boldsymbol{v}_{s\alpha\beta}\mathrm{d}t=\frac{2V_d}{\pi}\left[\frac{1}{\mathrm{j}\omega_s}\mathrm{e}^{\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{\pm1}{\mathrm{j}(6n\pm1)^2\omega_s}\mathrm{e}^{\pm\mathrm{j}(6n\pm1)\omega_s t}\right] \tag{7}$$

The space vector of rotor voltage can be then calculated after the manipulation of (4) and (7) as:

$$\boldsymbol{v}_{r\alpha\beta}=\left(R_r-\mathrm{j}\omega_r\sigma L_r\right)\boldsymbol{i}_{r\alpha\beta}+\sigma L_r\frac{\mathrm{d}\boldsymbol{i}_{r\alpha\beta}}{\mathrm{d}t}-\frac{L_m}{L_s}R_s\boldsymbol{i}_{s\alpha\beta}+\frac{2L_mV_d}{L_s\pi}\left[s\mathrm{e}^{\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{(s-1)}{6n\pm1}\left(1\pm\frac{1}{6n\pm1}\right)\mathrm{e}^{\pm\mathrm{j}(6n\pm1)\omega_s t}\right] \tag{8}$$

where $s=\left(\omega_s-\omega_r\right)/\omega_s$ is the slip of DC-DFIG.

Considering that an asymmetrical fault occurs in the AC grid, the connected DC voltage will experience a 100 Hz DC voltage oscillation along with the voltage sag [59]. As-

suming that a DC voltage oscillation occurs at $t=0$ and by ignoring the high-frequency harmonics, the space vectors of dynamic equation of stator voltage under the pre-fault condition ($t<0$) and after the fault occurrence ($t\geq 0$) can be expressed as [4]:

$$\boldsymbol{v}_{s\alpha\beta}=\frac{2V_d}{\pi}\left[\mathrm{e}^{\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{1}{6n\pm 1}\mathrm{e}^{\pm\mathrm{j}(6n\pm 1)\omega_s t}\right]\quad t<0 \tag{9}$$

$$\boldsymbol{v}_{s\alpha\beta}=\underbrace{\frac{2V_{d1}}{\pi}\left[\mathrm{e}^{\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{1}{6n\pm 1}\mathrm{e}^{\pm\mathrm{j}(6n\pm 1)\omega_s t}\right]}_{\boldsymbol{v}_{s\alpha\beta+}}+\underbrace{\frac{2V_{d2}}{\pi}\left[\mathrm{e}^{-\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{1}{6n\pm 1}\mathrm{e}^{\mp\mathrm{j}(6n\pm 1)\omega_s t}\right]}_{\boldsymbol{v}_{s\alpha\beta-}}\quad t\geq 0 \tag{10}$$

where V_{d1} is the amplitude of the DC voltage; and V_{d2} is the amplitude of the AC components after a voltage dip. Equation (10) elaborates that the behavior of DC-DFIG under AC-side asymmetrical fault is similar to that of AC-DFIG. The positive- and negative-sequence stator voltages $\boldsymbol{v}_{s\alpha\beta+}$ and $\boldsymbol{v}_{s\alpha\beta-}$ will induce positive- and negative-sequence stator flux linkages, respectively. Meanwhile, a decayed DC component of the stator flux linkage will also be introduced under the DC voltage oscillation conditions [54], [55].

According to (7) and (9), the steady-state space vectors of stator flux under the pre-fault condition ($t<0$) and after the fault occurrence ($t\geq 0$) can be expressed as:

$$\boldsymbol{\psi}_{s\alpha\beta}=\frac{2V_d}{\pi}\left[\frac{1}{\mathrm{j}\omega_s}\mathrm{e}^{\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{\pm\mathrm{e}^{\pm\mathrm{j}(6n\pm 1)\omega_s t}}{\mathrm{j}(6n\pm 1)^2\omega_s}\right]\quad t<0 \tag{11}$$

$$\boldsymbol{\psi}_{s\alpha\beta}=\frac{2V_{d1}}{\pi}\left[\frac{1}{\mathrm{j}\omega_s}\mathrm{e}^{\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{\pm\mathrm{e}^{\pm\mathrm{j}(6n\pm 1)\omega_s t}}{\mathrm{j}(6n\pm 1)^2\omega_s}\right]+\frac{2V_{d2}}{\pi}\left[\frac{-1}{\mathrm{j}\omega_s}\mathrm{e}^{-\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{\mp\mathrm{e}^{\mp\mathrm{j}(6n\pm 1)\omega_s t}}{\mathrm{j}(6n\pm 1)^2\omega_s}\right]\quad t\geq 0 \tag{12}$$

Note that the stator flux linkage cannot be abruptly changed when a fault occurs. Assuming that the RSC provides no excitation voltage for the DC-DFIG and is open-circuit, the dynamic changes of the stator flux linkage after the fault occurrence can be derived as:

$$\frac{\mathrm{d}\boldsymbol{\psi}_{s\alpha\beta}}{\mathrm{d}t}=\boldsymbol{v}_{s\alpha\beta}-\frac{R_s}{L_s}\boldsymbol{\psi}_{s\alpha\beta} \tag{13}$$

Combining (9)-(13), the transient stator flux can be expressed as:

$$\boldsymbol{\psi}_{s\alpha\beta}=\frac{2V_{d1}}{\pi}\left[\frac{1}{\mathrm{j}\omega_s}\mathrm{e}^{\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{\pm\mathrm{e}^{\pm\mathrm{j}(6n\pm 1)\omega_s t}}{\mathrm{j}(6n\pm 1)^2\omega_s}\right]+\frac{2V_{d2}}{\pi}\left[\frac{-1}{\mathrm{j}\omega_s}\mathrm{e}^{-\mathrm{j}\omega_s t}+\sum_{n=1}^{\infty}\frac{\mp\mathrm{e}^{\mp\mathrm{j}(6n\pm 1)\omega_s t}}{\mathrm{j}(6n\pm 1)^2\omega_s}\right]+\frac{2(V_d-V_{d1})}{\pi}\left[\frac{1}{\mathrm{j}\omega_s}\mathrm{e}^{\mathrm{j}\omega_s t_0}+\sum_{n=1}^{\infty}\frac{\pm\mathrm{e}^{\pm\mathrm{j}(6n\pm 1)\omega_s t_0}}{\mathrm{j}(6n\pm 1)^2\omega_s}\right]\mathrm{e}^{-t/\tau_s}+\frac{2(0-V_{d2})}{\pi}\left[\frac{-1}{\mathrm{j}\omega_s}\mathrm{e}^{-\mathrm{j}\omega_s t_0}+\sum_{n=1}^{\infty}\frac{\mp\mathrm{e}^{\mp\mathrm{j}(6n\pm 1)\omega_s t_0}}{\mathrm{j}(6n\pm 1)^2\omega_s}\right]\mathrm{e}^{-t/\tau_s}\quad t\geq 0 \tag{14}$$

where $\tau_s=L_s/R_s$ is the time constant of stator; and t_0 is the fault occurrence time. In (14), we set $t_0=0$.

By substituting (14) into (8), transferring the space vector of rotor voltage into rotor reference frame, and ignoring the influence of the stator current, the EMF in (4) under the DC bus voltage sag with oscillation can be re-written as:

$$\begin{aligned}\boldsymbol{e}^r_{r\alpha\beta}=\frac{L_m}{L_s}\Bigg\{&\frac{2V_{d1}}{\pi}\left[s\mathrm{e}^{\mathrm{j}\omega_{slip}t}+\sum_{n=1}^{\infty}\frac{s-1}{6n\pm 1}\left(1\pm\frac{1}{6n\pm 1}\right)\mathrm{e}^{\pm\mathrm{j}(6n\pm 1)\omega_{slip}t}\right]+\\&\frac{2V_{d2}}{\pi}\left[(2-s)\,\mathrm{e}^{-\mathrm{j}(2-s)\omega_s t}+\sum_{n=1}^{\infty}\frac{(1-s)\mathrm{e}^{\mp\mathrm{j}(6n\pm 1)\omega_{slip}t}}{6n\pm 1}\left(1\pm\frac{1}{6n\pm 1}\right)\right]-\\&\frac{2(V_d-V_{d1})}{\pi}\left[(1-s)\mathrm{e}^{\mathrm{j}\omega_s t_0}+\sum_{n=1}^{\infty}\frac{\pm(1-s)}{(6n\pm 1)^2}\mathrm{e}^{\pm\mathrm{j}(6n\pm 1)\omega_s t_0}\right]\mathrm{e}^{-t/\tau_s}\mathrm{e}^{-\omega_r t}-\\&\frac{2(0-V_{d2})}{\pi}\left[(s-1)\mathrm{e}^{-\mathrm{j}\omega_s t_0}+\sum_{n=1}^{\infty}\frac{\mp(s-1)}{(6n\pm 1)^2}\mathrm{e}^{\mp\mathrm{j}(6n\pm 1)\omega_s t_0}\right]\mathrm{e}^{-t/\tau_s}\mathrm{e}^{-\omega_r t}\Bigg\}\end{aligned} \tag{15}$$

where $\omega_{slip}=\omega_s-\omega_r$. Equation (15) shows that the dynamic process of rotor voltage is significantly complex. Neglecting the high-frequency component, three compositions can be observed in the transient rotor EMF $\boldsymbol{e}^r_{r\alpha\beta}$: ① an AC component that rotates anticlockwise at a speed of ω_{slip}; ② an AC component that rotates clockwise at a speed of $(2-s)\omega_s$; and ③ an AC component that rotates clockwise at a speed of ω_r, and decays with the time constant τ_s. The second and third components are transient signals that will also lead to a massive oscillation of the EM torque and damage of the gearbox and converter.

B. Behaviors of DC-DFIG Output Power under DC Voltage Oscillation

Under the DC voltage oscillation, the amplitude of DC voltage will be changed from V_d to $V_{d1}+V_{d2}\sin(2\omega_s t)$, by only considering the $2\omega_s$ frequency oscillation. Accordingly, the output current of DC-DFIG can be expressed as $I_{d1}+I_{d2}\sin(2\omega_s t+\varphi_0)$ with consideration of the nonlinear elements in the DC transmission cable, where φ_0 is the shifting phase between the DC voltage and current oscillations. The output power of DC-DFIG-based WECS can be then derived as:

$$P_d=\left(V_{d1}+V_{d2}\sin\left(2\omega_s t\right)\right)\left(I_{d1}+I_{d2}\sin\left(2\omega_s t+\varphi_0\right)\right)=P_{d1}+P_{d\sin 2}\sin\left(2\omega_s t\right)+P_{d\sin 4}\sin\left(4\omega_s t\right) \tag{16}$$

where subscripts 1, sin2, and sin4 of P_d represent the DC, $2\omega_s$, and $4\omega_s$ components of the output power, respectively. Since the amplitudes of DC voltage and current oscillations (V_{d2} and I_{d2}) are generally small, the $4\omega_s$ component can be neglected in the analysis. Equation (16) reveals that there will be no oscillation of voltage, current, and power in the transmission line under the normal conditions. With unbalanced disturbances, conversely, these coefficients are not equal to zero, and the main power oscillation is with a frequency of $2\omega_s$.

Synthesizing the above analysis, a hardware device is required for power compensation due to the intermittent and

volatility of wind energy. The regulation of DC terminal voltage is also necessary to improve the LVRT capability of the DC-DFIG. Meanwhile, an advanced control strategy is also required to suppress the voltage, current, and power oscillations.

III. Circuit Principle of DAB-based DC-UPQC

A. System Configuration

The detailed model of DC-UPQC is shown in Fig. 3, where v_d, v_g, and v_c are the DC-DFIG-side, grid-side, and SDAB-side volages, respectively; i_d, i_g, and i_c are the DC-DFIG-side, grid-side, and PDAB-side currents, respectively; v_{dc} is the bus voltage of ESD; i_{SC} is the SMES current; v_{H1}-v_{H4} and i_{H1}-i_{H4} are the voltages and currents of the bridges 1-4 at the high-frequency side, respectively; v_2 and i_4 are the output voltage and current of bridges 2 and 4, respectively; and v_{lf2} is the inductance voltage of L_{f2}. The system consists of two main parts: SDAB and PDAB. The output port of PDAB is serial with the DC transmission line near the DC microgrid, while the output port of SDAB is in parallel with the DC transmission line in front of the terminal of the DC-DFIG-based WECS. The input ports of the two DABs are connected, formulating an ESD bus, where the SMES and its converter are connected.

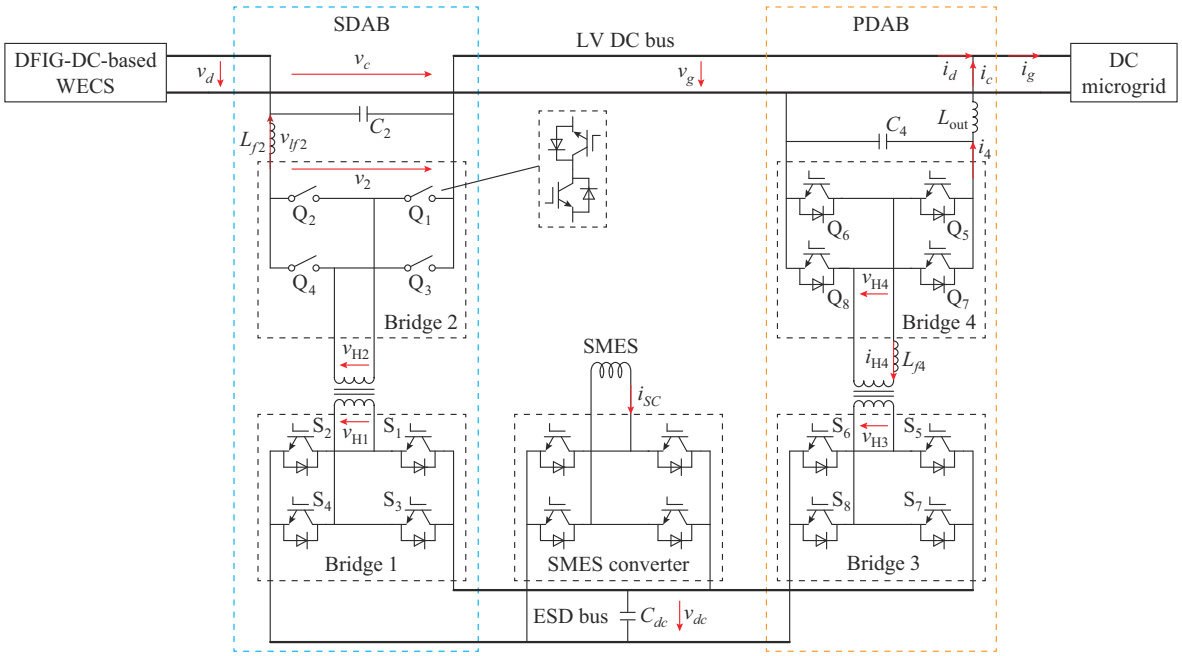

Fig. 3. Detailed configuration of proposed SMES-based DC-UPQC.

The SDAB is to maintain the voltage profile under grid faults. According to Fig. 1, the relationship of the DC-DFIG-side voltage v_d, grid-side voltage v_g, and compensation voltage v_c is:

$$v_d = v_g + v_c \tag{17}$$

Equation (17) reveals that the SDAB can introduce a certain DC voltage in series with the DC cable under DC voltage quality events. It can improve the LVRT capability of the DC-DFIG and protect crucial elements of the system.

The PDAB has two functions: ① compensating the variable output power of DC-DFIG under wind gust situations; and ② enhancing the current and output power qualities of DC-DFIG under DC fault events. As shown in Fig. 1, the relationships of the current and power at the DC-DFIG side, PDAB side, and grid side can be expressed as:

$$i_d + i_c = i_g \tag{18}$$

$$P_d + P_c = P_g \tag{19}$$

B. SDAB

To simplify the analysis of the circuit principle, the SDAB and PDAB are considered as single phase-shifting (SPS) control strategies. Figure 4 shows the crucial parameter responses of the SDAB, where T_{hs} represents the half period; and φ_s is the ratio of shifting phase in SDAB. Under the control by the SMES and DC/DC converter, the DC bus voltage of DC-UPQC V_{dc} can be considered as a constant. The relationship among of φ_s, v_c, and V_{dc} can be expressed as:

$$v_c = -2\left[\varphi_s n_s V_{dc} + \left(\frac{1}{2} - \varphi_s\right)\left(-n_s V_{dc}\right)\right] = \left(4\varphi_s - 1\right) n_s V_{dc} \tag{20}$$

where n_s is the turn ratio of the high-frequency transformer in the SDAB. Equation (20) claims that φ_s is correlated linearly with the output voltage of SDAB v_c. When φ_s is equal to 0.5, the output voltage of SDAB is equal to zero. When φ_s is in a range of [0, 0.5), a backward voltage compensation can be provided by the SDAB in a range of $[-nV_2, 0)$ for voltage sag compensation, as shown in Fig. 4(a). When φ_s is in the range of (0.5, 1], a forward voltage compensation will be generated by the SDAB, and the compensation is in a range of $(0, nV_2]$ for voltage swell suppression, as shown in Fig. 4(b).

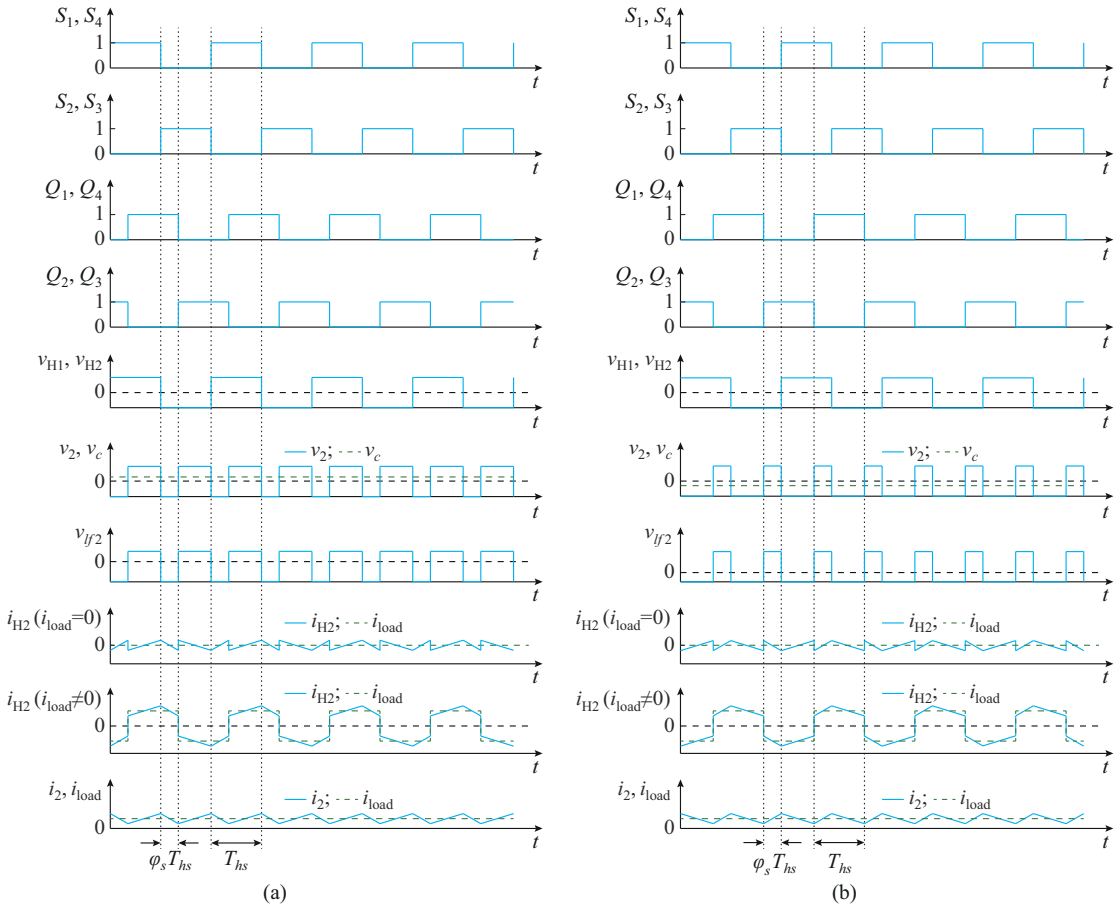

Fig. 4. Operation of SDAB for voltage sag compensation and voltage swell suppression. (a) Voltage sag compensation. (b) Voltage swell suppression.

There is an external inductance L_{f2} that can be used to limit the rate of current increment and confine the current stress of SDAB. The current stress is equal to the peak value of i_{H2}, defined as I_p, which can be also observed in Fig. 4. Assuming that i_{load} is zero, the value of I_p can be calculated as:

$$\begin{cases} L_{f2}\dfrac{-I_p-I_p}{\varphi_s T_s}=v_{lf2}-2n_2V_{dc} \\ L_{f2}\dfrac{I_p-\left(-I_p\right)}{\left(0.5-\varphi_s\right)T_s}=v_{lf2} \end{cases} \tag{21}$$

$$I_p=\varphi_s\left(1-2\varphi_s\right)\frac{n_2V_{dc}}{L_{f2}f_s} \tag{22}$$

where $T_s=1/f_s$ is the switching period, and f_s is the switching frequency; and v_{lf2} is the voltage across the inductance L_{f2}. According to (22), the inductance L_{f2} can be used to control the current stress of the SDAB.

The relationships among the output voltage of SDAB v_c, inductance voltage v_{lf2}, and output voltage of bridge 2 v_2 can be expressed as:

$$v_c=v_2-v_{lf2} \tag{23}$$

C. PDAB

The working principle of PDAB is consistent with the traditional DAB investigated in [60]-[62]. There is a series inductor L_{f4} that controls the current rise and decides the power level of PDAB. The operation of PDAB under the backward and forward current flow conditions is shown in Fig. 5. The compensation current i_c can be obtained from i_4 with the function of LC filter C_4 and L_{out}.

The inductance current $i_{H4}(t)$ can also be expressed as:

$$\frac{\mathrm{d}i_{H4}(t)}{\mathrm{d}t}=\frac{v_{H4}(t)-v_{H3}(t)}{L_{f4}} \tag{24}$$

Considering that the average current flowing through the inductance L_{f2} in a period is considered as zero; the power delivery of PDAB in a period of T_s can be derived by:

$$P_{H4}=\frac{1}{T_s}\int_0^{T_s}v_{H4}i_{H4}(t)\,\mathrm{d}t=\frac{n_pv_dV_{dc}}{f_sL_{f4}}\varphi_p\left(1-2\varphi_p\right) \tag{25}$$

where n_p is the turn ratio of the PDAB; and $\varphi_p\in[-0.5, 0.5]$ is the ratio of shifting phase in PDAB. During the normal operation, the magnitudes of V_{dc} and v_d can be considered as constants. The filter inductance L_{f4} controls the current rise and can be used to estimate the capacity of PDAB.

D. Design of SMES

As one of few current sources, SMES is an emerging technology that can store the magnetic energy in a superconducting coil (SC), and release the stored energy when required. Compared with other commercial ESDs such as battery energy storage (BES) with a low-power capacity, the high-power capacity of SMES makes it more suitable for MW-class applications.

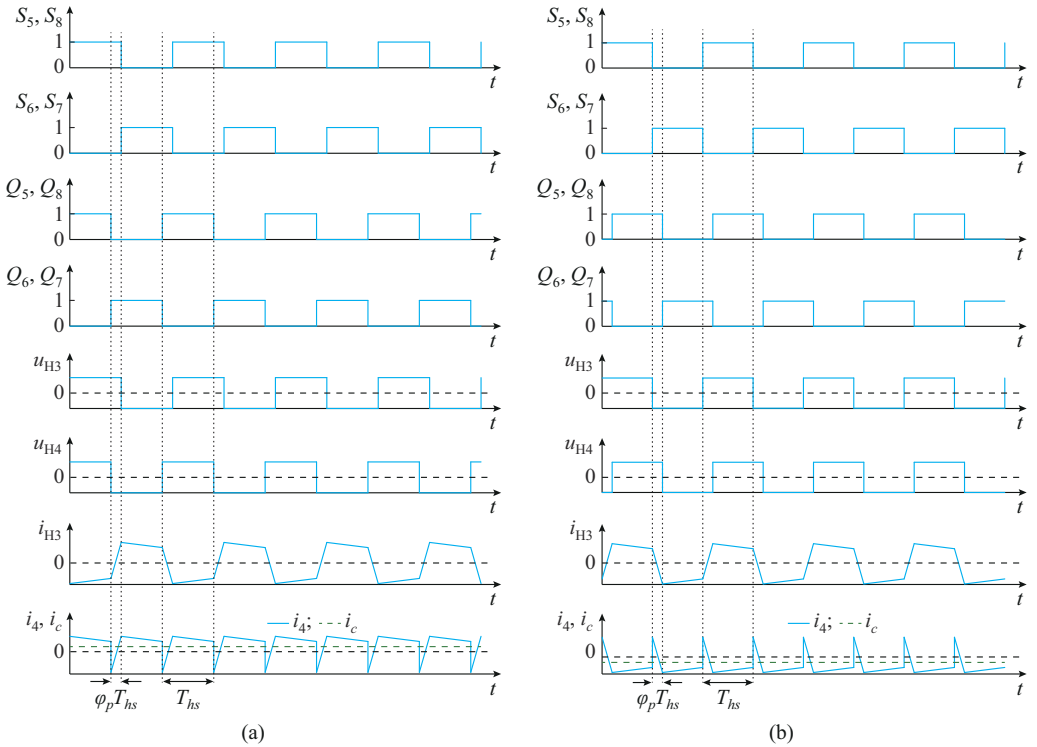

Fig. 5. Operation of PDAB under backward and forward current flow conditions. (a) Under backward current flow condition. (b) Under forward current flow condition.

Moreover, the cost of power loss in the battery is considerable. As for the supercapacitor, it is necessary to keep the energy uniformity of each cell, so the additional cost of the online condition monitoring and the voltage/current balancing control should also be considered. In comparison, the SMES is actually an individual SC. Therefore, the voltage balancing control and condition monitoring are not necessary. Moreover, if one supercapacitor component breaks, the performance and stabilization of supercapacitor will be influenced. Conversely, the SMES has better stability as an ESD due to its individual structure [63], [64].

The expensive capital cost of SMES is always criticized. Recently, many new structures of SMES have been designed to increase the critical current, reduce the usage of superconducting tape, and lower the cost. Among the existing investigations, the step-shaped solenoidal coil obviously enlarges the critical current (1.4 times that of the rectangular-shape coil) and decreases the amount of tape usage (80% of the rectangular-shape coil) [65], [66]. However, the above structures are based on 1G superconducting strip. As the newest research achievement, the 2G-strip-based varying-axial-gap structure proposed in [67] and adopted in this paper is proven to enlarge around 40% energy capacity for an MJ-class SMES case compared with the regular-shape coil.

Figure 6(a) shows a structure of a designed varying-axial-gap solenoidal SC among certain pancakes. The designed SC is made up of Q single pancakes. Among them, $2m$ single pancakes have a fundamental gap of g and a gap increment of Δx; while $Q-2m$ single pancakes have a constant axial gap of d. The wire of each single pancake is winded using N turns, and the inner radius and outer radius of each pancake are R_i and R_o, respectively.

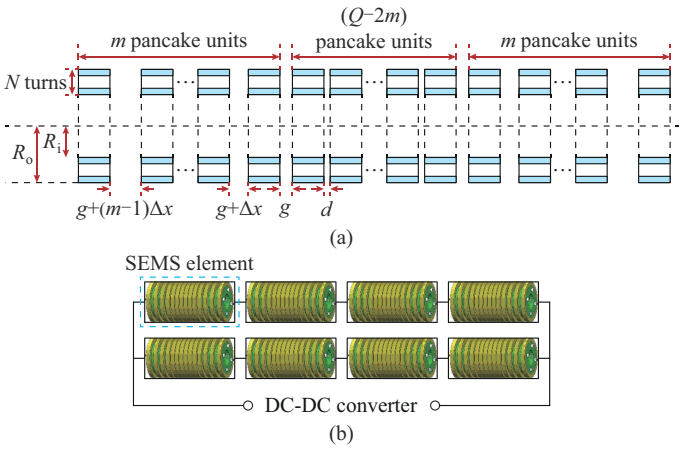

Fig. 6. Design of SMES. (a) Structure of designed varying-axial-gap solenoidal SC. (b) Electrical connections of eight SMES elements.

After the optimal design and calculation, the structural parameters of the designed varying-axial-gap solenoidal SC are $Q=80$, $N=19$, $R_i=0.5$ m, $R_o=0.5076$ m, $m=11$, $\Delta x=1$ mm, $g=1$ mm, and $d=0$, respectively. However, due to the internal packaging issue of the strip in practice, the constant axial gap can be considered as $d\approx 0.8$ mm. The usage of the superconducting tape is about 5 km. With these parameters, the critical current of the designed SMES element is about 900 A, and the inductance and capacity of the designed SMES element are 2.57 H and 1.04 MJ, respectively.

In this paper, the adopted SMES device contains eight designed SMES elements. The electrical connections of the designed SMES are shown in Fig. 6(b). The eight SMES ele-

ments are firstly divided into two components, and each component consists of four SMES elements connected in series. The critical inductance and current of each component are 10.28 H/900 A, respectively. The two components are further connected in parallel to compose a 5.14 H/1800 A SMES unit, whose capacity is 8.32 MJ. The designed composite SMES element can meet the capacity requirement considering the demanded wind power compensation capacity.

IV. Control Strategies

It is necessary to introduce an oscillation regulator to mitigate the DC voltage, current, and power oscillations under unbalanced AC-side grid faults. Figures 7 and 8 show the control strategies of the proposed SMES-based DC-UPQC.

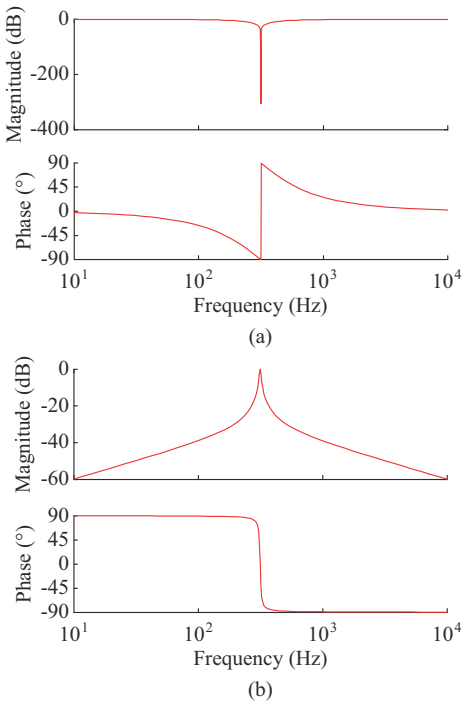

Fig. 7. Filters used in proposed SMES-based DC-UPQC. (a) Bode diagram of band-trap filter. (b) Bode diagram of band-pass filter.

A. Control of SDAB

To separately regulate these two voltage components, as depicted in Figs. 7 and 8, the terminal voltage of sampled DC-DFIG v_d can be decomposed to a DC component v_{d1} by the band-trap filter, and an oscillatory component v_{d2} by the band-pass filter. The two filters are used to implement the error-free tracking control. The open-loop transfer function of the band-trap filter can be expressed as:

$$G(s)=\frac{s^2+(2\pi f)^2}{s^2+\omega_0 s+(2\pi f)^2} \tag{26}$$

where $f=100$ Hz; and ω_0 is the cut-off frequency, which can be adjusted to decrease the sensitivity of the frequency fluctuation. Figure 7(a) shows the bode diagram of the band-trap filter when ω_0 is equal to $2\sqrt{2}\,\pi f$ rad/s. The difference between the actual and reference signals (v_{d1} and v_{d1}^*) is considered as the input signal of PI controller, while the reference signal v_{d1}^* is assumed to be equal to the rated terminal voltage of DC-DFIG.

To precisely obtain the oscillatory signal, a band-pass filter is introduced, and the open-loop transfer function of the band-pass filter is expressed as:

$$G(s)=\frac{2\pi fs}{s^2+\omega_0 s+(2\pi f)^2} \tag{27}$$

The bode diagram of the open-loop band-pass filter is shown in Fig. 7(b) with the cut-off frequency of $\omega_0=10$ rad/s. The oscillation signal v_{d2} is then carried out from a virtual $\alpha\beta/dq$ transformation, which is adopted via a $\pi/2$ transport delay model. The process can be expressed mathematically as:

$$\boldsymbol{v}_{d2dq}=\boldsymbol{v}_{d2\alpha\beta}e^{-j\omega t} \tag{28}$$

The obtained signals v_{d2d} and v_{d2q} are DC signals, which are easy to be regulated by PI controllers. Since the generated dq signals v_{d2d} and v_{d2q} are separately regulated, the input angle frequency of the dq transform does not call for the initial angle phase and PLL to track the oscillatory voltage. The reference dq signals of the oscillation components v_{d2d}^* and v_{d2q}^* are equal to zero.

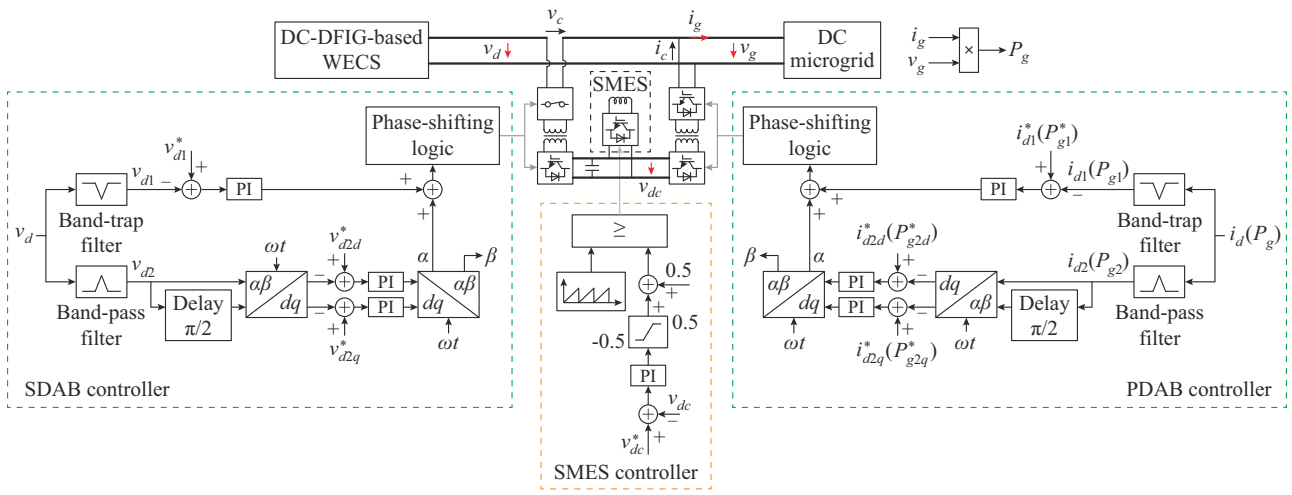

Fig. 8. Control diagram of proposed SMES-based DC-UPQC.

After the PI regulation, a $dq/\alpha\beta$ inverse transformation is utilized, and the obtained α-axis component is used as the output signal of the oscillation regulator. The phase-shifting control can be implemented by adding the output signals of the DC regulator and the oscillation regulator. Note that the α-axis component is an AC signal with a rotating frequency of 100 Hz. When a voltage oscillation occurs, the ratio of the shifting phase contains two components, i.e., a DC component for voltage magnitude compensation and an AC component for voltage oscillation suppression.

B. Control of PDAB

The PDAB also uses the similar control structure as SDAB. There are two alternative control targets designed for power compensation and current quality enhancement, respectively: ① target 1: constant power control; and ② target 2: constant current control.

Under the constant power control, the grid-side power P_g is considered as the input signal; while under the constant current control, the output current of DC-DFIG i_d is assumed as the input signal. Similar to the control of SDAB, the reference signals of the DC power and current (P^*_{g1} and i^*_{d1}) are equal to the rated power and current of the DC-DFIG, respectilvely, and the reference signals of the oscillation components (P^*_{g2d} and P^*_{g2q} or i^*_{d2d} and i^*_{d2q}) are equal to zero.

C. Control of SMES

The function of SMES is to sustain the DC bus voltage as a DC power supply of DC-UPQC. The control of the DC-DC converter is shown in Fig. 8. The DC bus voltage v_{dc} is sampled, and the difference of the actual and reference signals (v_{dc} and v^*_{dc}) is fed into the PI controller. Finally, a duty cycle can be generated in the range of [0, 1] by adding the output signal of the PI controller to an offset constant of 0.5.

V. Simulation Results

A 1.5 MW DC-DFIG-based WECS with the integration of the proposed SMES-based DC-UPQC using MATLAB/Simulink is shown in Fig. 1. In the study model, the DC-DFIG is connected to a 1 kV DC source. Initially, the DC-DFIG works at a steady state, and the output power is the rated power (1.0 p.u.). The slip of the DC-DFIG is set to be –0.2. The inductance, critical current, and capacity of the SMES are 5.14 H, 1800 A, and 8.32 MJ, respectively, and the initial current of SMES is 1272 A. The turn ratios of the SDAB and PDAB n_p and n_s in the DC-UPQC are both 2: 1, which means the DC bus voltage of DC-UPQC is 500 V. The filter inductances of bridegs 2 and 4 L_{l2} and L_{l4} are 200 μH and 10 μH, respectively. The current compensation range is about [–1250 A, 1250 A] with the adopted filter inductances. It means that the unsteady output power resulting from the volatility of wind energy can be smoothed by the PDAB when the output power of DC-DFIG fluctuates in the range of [0.25 MW, 2.75 MW].

To give a round performance validation of the proposed targets, three cases are analyzed in the simulation and listed as follows: ① Case 1: without any control system; ② Case 2: with the proposed DC-UPQC but without the DC dual control; and ③ Case 3: with the proposed DC-UPQC and DC dual control.

A. Behaviors of DC-DFIG with Variable Wind Speeds

Under variable wind speeds, the PDAB plays a leading role in smoothing the output power of DC-DFIG. The two control targets are both available for output power mitigation since the DC source voltage can be regarded as a constant during the normal operation. Figure 9 shows the wind speed variation, power conditions of the DC-DFIG, DC-UPQC, and DC source, and the response of the SMES current with variable wind speeds. The 60 s emulated wind speed data varying from 11 m/s to 19 m/s based on the Kaimal wind speed model [68] are adopted in the simulation. Besides, some assumptions are made with variable wind speeds: ① there is no power quality disturbance with variable wind speeds; ② an average wind speed of 14 m/s is considered as the nominal speed of DC-DFIG; and ③ there is no extremely high-speed wind gust or breezeless condition.

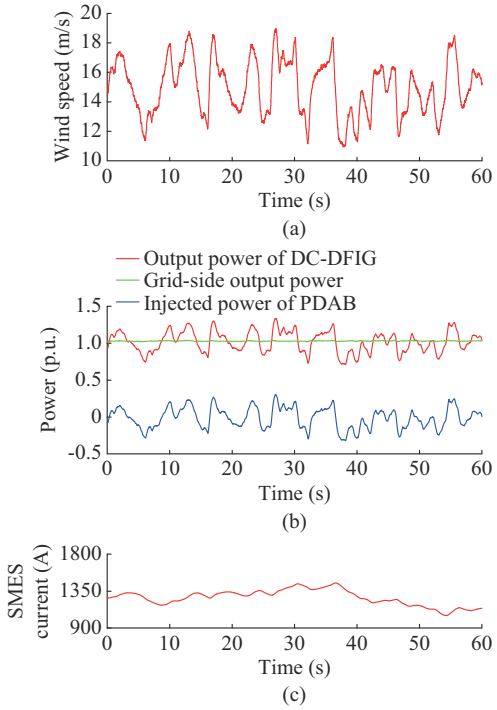

Fig. 9. Wind speed variation, power of DC-DFIG, DC-UPQC, and DC source, and SMES current with variable wind speeds. (a) Wind speed. (b) Responses of output power of DC-DFIG, grid-side output power, and injected power of PDAB. (c) SMES current during power compensation process.

As illustrated in Fig. 9(b), the output power of DC-DFIG will fluctuate in the range of [0.8 p.u., 1.4 p.u.] following the wind speed variations. With the proposed compensation strategy, the PDAB of DC-UPQC will inject a specific current to keep the total output power of DC-DFIG and DC-UPQC at a constant level (1.0 p.u.), smoothing the unsteady output power and eliminating the potential system stability issues. Reflected by the SMES current, the state of charge (SOC) of SMES will fluctuate between 10% and 90% to adjust the total output power with variable wind speeds. Figure

9(c) reveals that the designed SMES has a sufficient capacity and a compelling performance in dealing with the power fluctuation with time-varying wind speeds.

B. Behaviors of DC-DFIG Under AC-side Line-to-line Fault

Figure 10 shows the parameter responses of the DC-DFIG under DC voltage sag with oscillation. At $t=0.5$ s, 80% voltage depth is assumed to take place due to line-to-line fault in phases A and B. Without any controller, the terminal voltage of DC-DFIG falls from 1 kV to 466.7 V. Meanwhile, a 100 Hz voltage oscillation appears with the amplitude of 176.3 V.

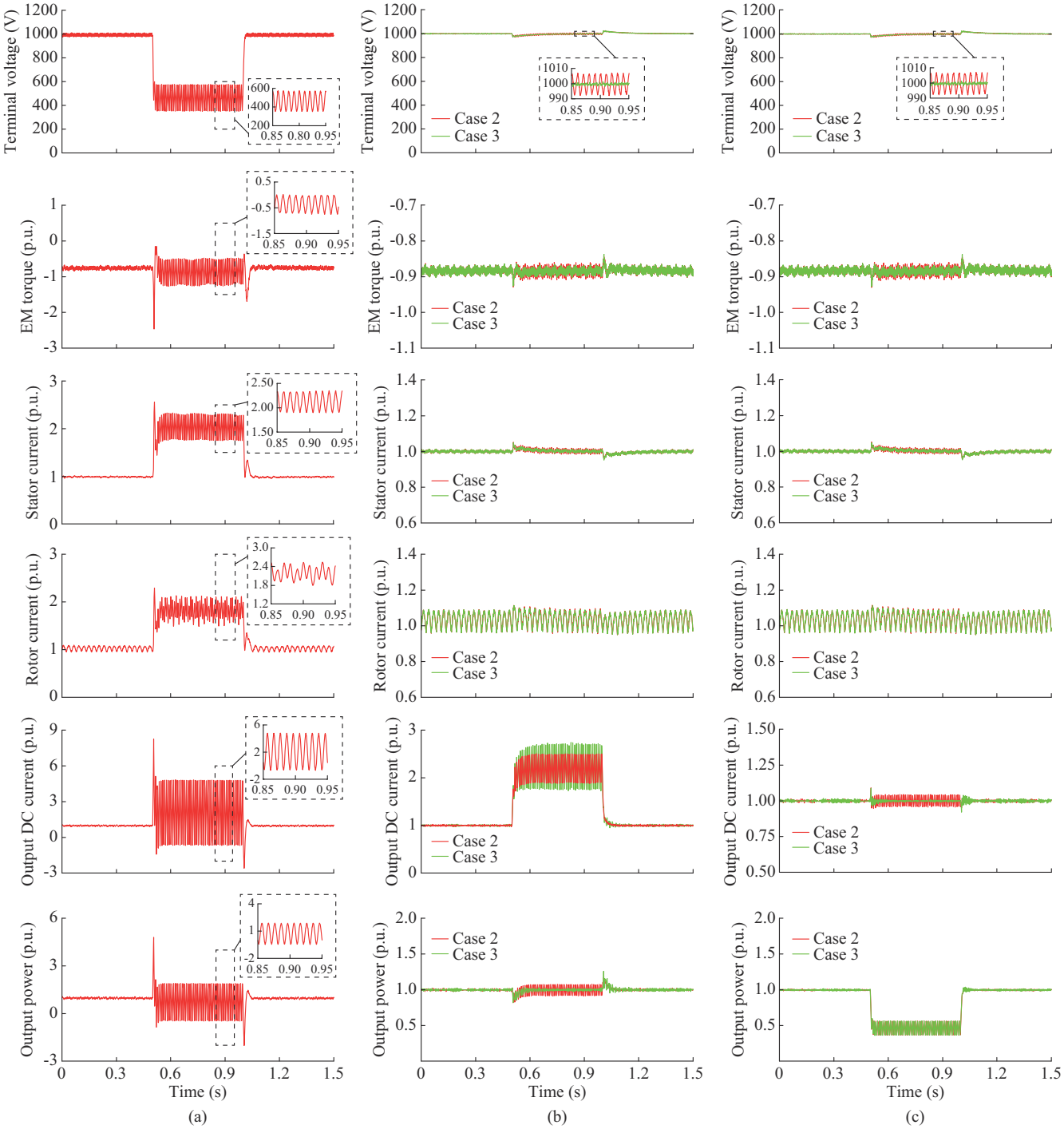

Fig. 10. Responses of terminal voltage, EM torque, magnitudes of stator and rotor currents, output current and power of DC-DFIG under DC voltage sag with oscillation. (a) Without any controller in Case 1. (b) Under constant power control in Cases 2 and 3. (c) Under constant current control in Cases 2 and 3.

As shown in Fig. 10(a), the crucial parameters, including EM torque, stator current, and rotor current, are all beyond the maximum permitted values (2.0 p.u.) along with significant oscillations. Such oscillations will lead to a severe heating problem in the machine and may damage the expensive gearbox of the wind turbine. As a result, there is a substan-

tial spike in the output DC current and power at the beginning of the fault occurrence. Meanwhile, there is also a huge 100 Hz oscillation in the output DC current and power.

As shown in Fig. 10(b) and (c), the application of the DC-UPQC considerably improves the LVRT capability of DC-DFIG and the qualities of DC current and power. However, without the DC dual control, the oscillations of the DC voltage, current, and power cannot be eliminated (red curves in Fig. 10(b) and (c)). The total harmonic distortion (THD) spectrum of the DC voltage, output current, and power is shown in Fig. 11. Under the constant power control in Case 2, there is still a 100 Hz oscillation in the DC output power, and its THD is about 7.75% of the DC component. Under the constant current control in Case 2, the DC output current contains a 100 Hz current oscillation, whose THD is about 4.05% of the current DC component. Without the DC dual control, the THD of the DC-DFIG terminal voltage is 1.83%, which still has a potential possibility of system component destruction.

With the DC dual control, the DC power and current quality can be further enhanced under the constant power and current control, respectively (green curves in Fig. 10(b) and (c)). It can be observed from the THD spectrum that the 100 Hz oscillations of the DC current and power are almost cleared. The THD of the DC power is 1.33% under the constant power control, while the THD of the DC current is 0.44% under the constant current control. With the DC dual control in SDAB, the THD of the DC-DFIG terminal voltage is only about 0.06%, which reduces the tripping risk of the DC-DFIG and protects the crucial elements within the system.

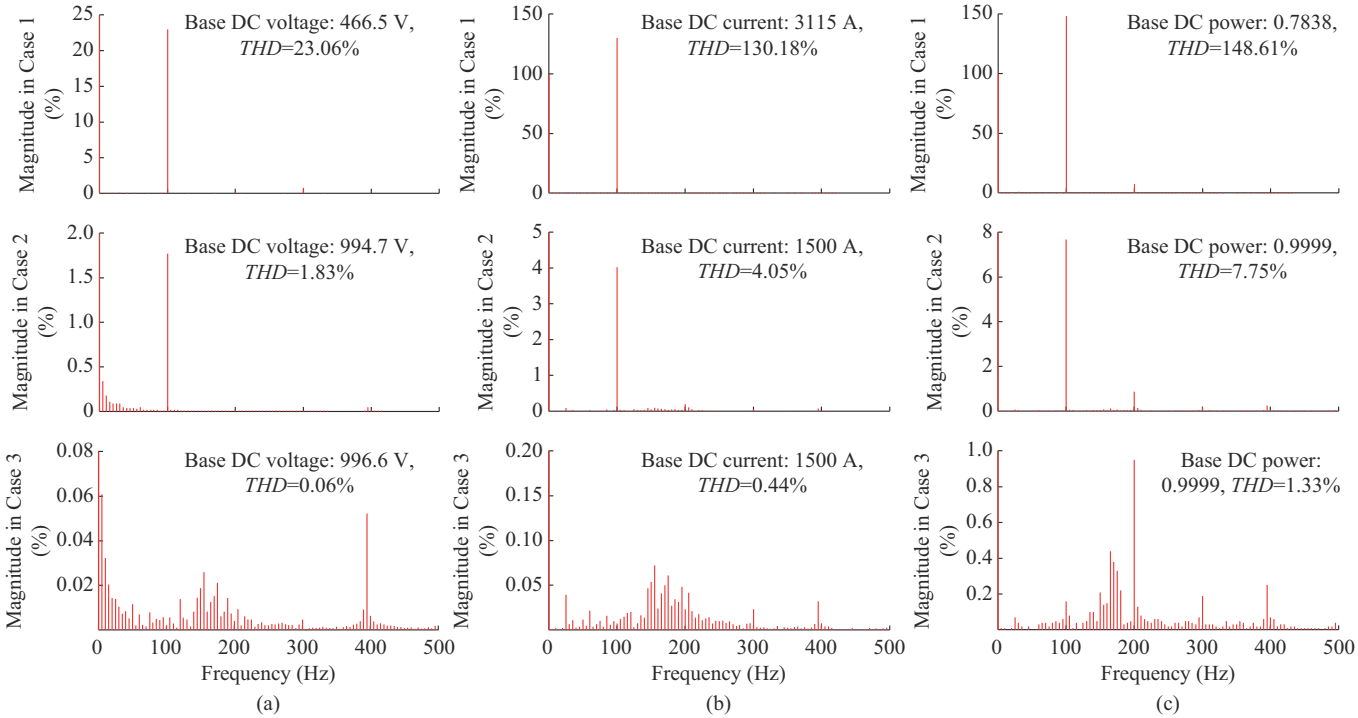

Fig. 11. THD spectrum in Cases 1-3. (a) DC voltage of DC-DFIG. (b) Output current under constant current control. (c) Output power under constant power control.

Figure 12 shows the responses of SMES current with the two control targets in Cases 2 and 3. Under the constant power control, the absorbed energy will be simultaneously released by PDAB to keep the output DC power at its rating level. Therefore, the SMES current is almost unchanged, varying from 1271.8 A to 1274 A during the whole transient process, as shown in Fig. 12(a). Under the constant current control, the output DC current to the DC source is controlled as the rated current, and no compensation power is injected from the PDAB. The SMES only absorbs the surplus energy from the SDAB, and the SMES current raises from 1272 A (at $t=0.5$ s) to 1331 A (at $t=1$ s). Meanwhile, the SMES current slightly fluctuates due to the power fluctuation caused by the DC voltage oscillation, as shown in Fig. 12(b).

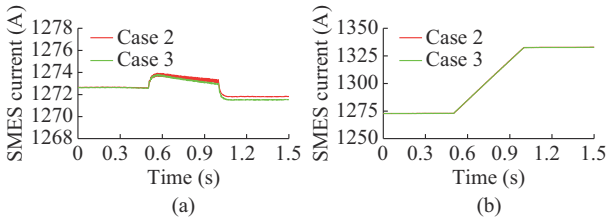

Fig. 12. Response of SMES current in Cases 2 and 3. (a) Under constant power control. (b) Under constant current control.

C. Experimental Results

A 50 V/5 A experimental setup is established to prove the effectiveness of the proposed DC dual control. The platform is shown in Fig. 13. To simplify the experimental setup, a DC source is served as the DC power supply of the DC-UP-

QC. Circuit principles of these two structures are also verified in this experiment. To avoid unnecessary risks in the experiment, the voltage sag and swell are generated via a voltage divider instead of the short-circuit fault. In this experiment, the turn ratio of the high-frequency transformer is 2:1; the DC power supply of the DC-UPQC is set to 25 V; the filter inductances L_{f2} and L_{f4} are 200 μH and 100 μH, respectively, which means the maximum power output capacity of the PDAB is in the range of [–625 W, 625 W].

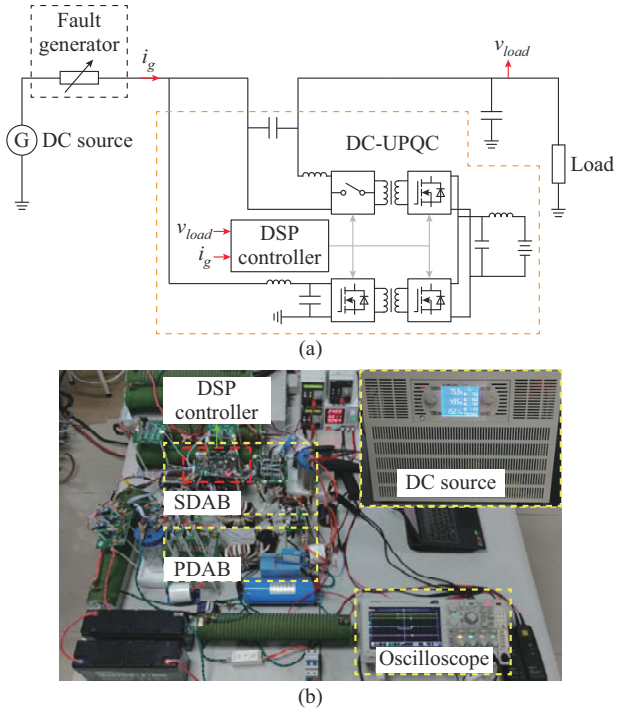

Fig. 13. Experimental setup. (a) Schematical diagram of UPQC. (b) Experimental platform of DC-UPQC.

1) Circuit Principle

Figure 14 shows the experimental results of the SDAB under the normal operation and PDAB under 5 A current compensation. As can be observed, the waveforms of the SDAB and PDAB are consistent with the theoretical waveforms shown in Figs. 4 and 5, respectively. Therefore, the experiment proves the correctness of the basic principles of the SDAB and PDAB introduced in Section III.

2) Voltage and Current Compensation

Figure 15 shows the parameters of load voltage v_{load}, compensation voltage v_c, grid-side current i_g, and compensation current i_c under voltage sag/swell compensation and load variation condition with the protection of DC-UPQC. The control targets of the PDAB and SDAB in DC-UPQC are constant source current and constant load voltage, respectively.

As shown in Fig. 15(a) and (b), under disturbances of 25% voltage sag and 25% voltage swell, respectively, the load voltage v_{load} can be well-maintained via SDAB to the nominal value. In Fig. 15(c) and (d), a ±2.5 A load variation is introduced, lasting for 200 ms. At that time, the PDAB will introduce a compensation current into the DC bus, and the grid-side current can be maintained at 5 A.

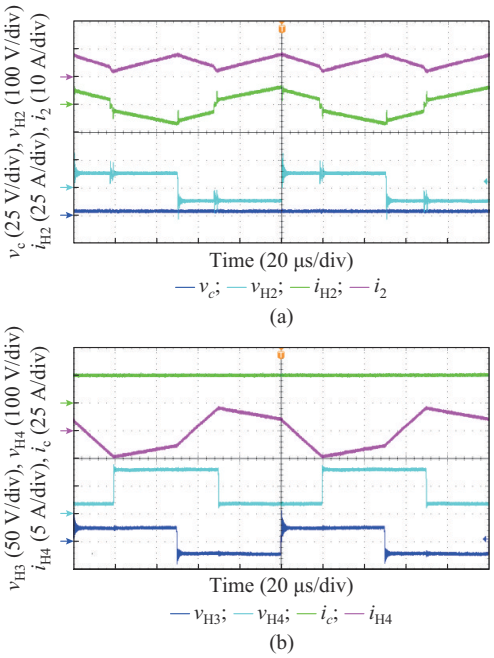

Fig. 14. Experimental results of circuit principle. (a) Circuit principle of SDAB under normal operation. (b) Circuit principle of PDAB under 5 A compensation.

3) Oscillation Suppression

Figure 16 shows the responses of SDAB parameters (grid-side voltage v_g, compensating voltage v_c, load voltage v_{load}, and load current i_{load}) under the DC voltage sag with oscillation.

In Fig. 16(a), the DC dual control is not used. As can be observed, although the amplitude can be accurately enhanced to the rated value, the oscillation cannot be well-suppressed. With the DC dual control, both the DC voltage amplitude and the voltage oscillation can be well-compensated within 100 ms, as shown in Fig. 16(b). Therefore, the proposed DC dual control has a better dynamic performance than the traditional control when dealing with the second-order voltage ripple.

Figure 17 shows the responses of PDAB parameters (grid-side current i_g, compensation current i_c, load current i_{load}, load voltage v_{load}, and load power P_{load}) under DC voltage oscillation sag. Figure 17(a) and (b) shows the results of constant power control in Cases 2 and 3, respectively. Whereas, Fig. 17 (c) and (d) show the results of constant current control in Cases 2 and 3, respectively. It is evident that the load current and power oscillations cannot be precisely eliminated with traditional control methods. With the DC dual control, the oscillations of the load current and power can be cleared rapidly, and only a few high-order harmonics exist in the waveforms of load current and load power. The experiment results for PDAB prove the effectiveness of the two control targets and the DC dual control in PDAB.

D. Comparison with Other DC Control Strategies

Table I shows a comparison between the proposed DC-UPQC and other existing DC control strategies, including the control method in [39], DC-PFC in [40], IUPS in [43], SVR in [45], and SMES-TLSVR in [46].

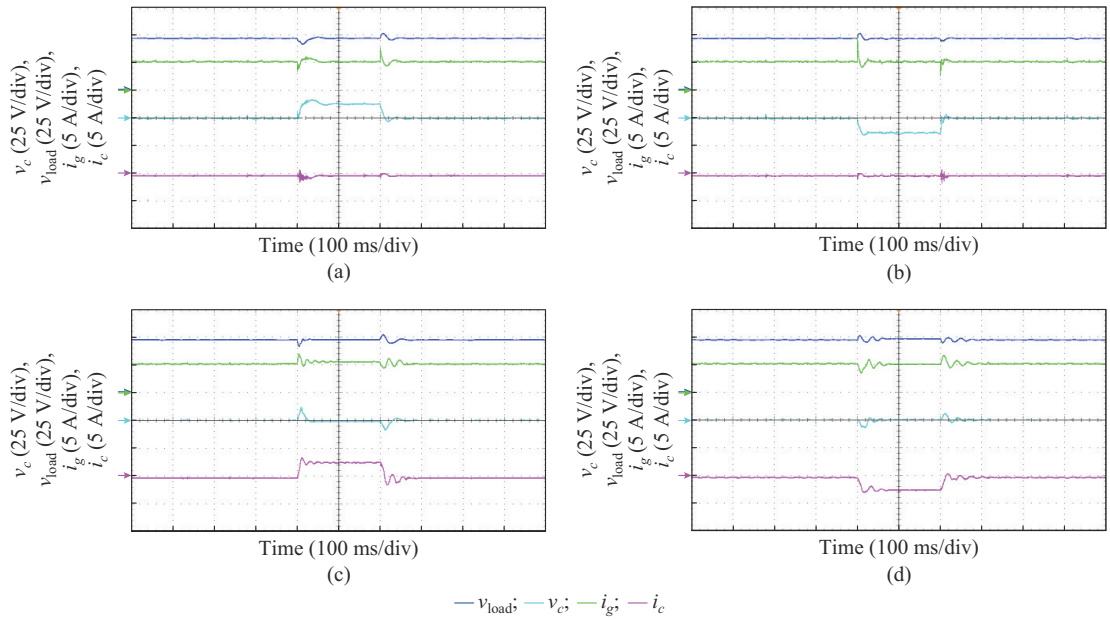

Fig. 15. Experimental results of voltage disturbances and load variations. (a) 25% voltage sag. (b) 25% voltage swell. (c) 250 W load connection compensation. (d) 125 W load removal compensation.

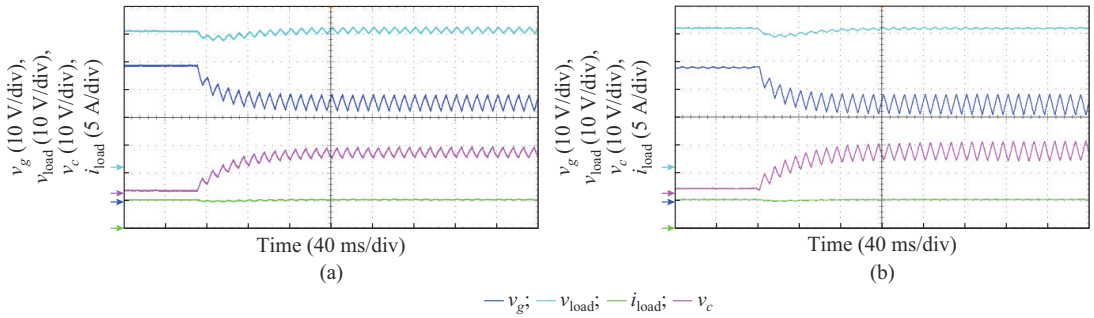

Fig. 16. Experimental results for SDAB under DC voltage sag with oscillation (under either constant power or current control). (a) Case 2. (b) Case 3.

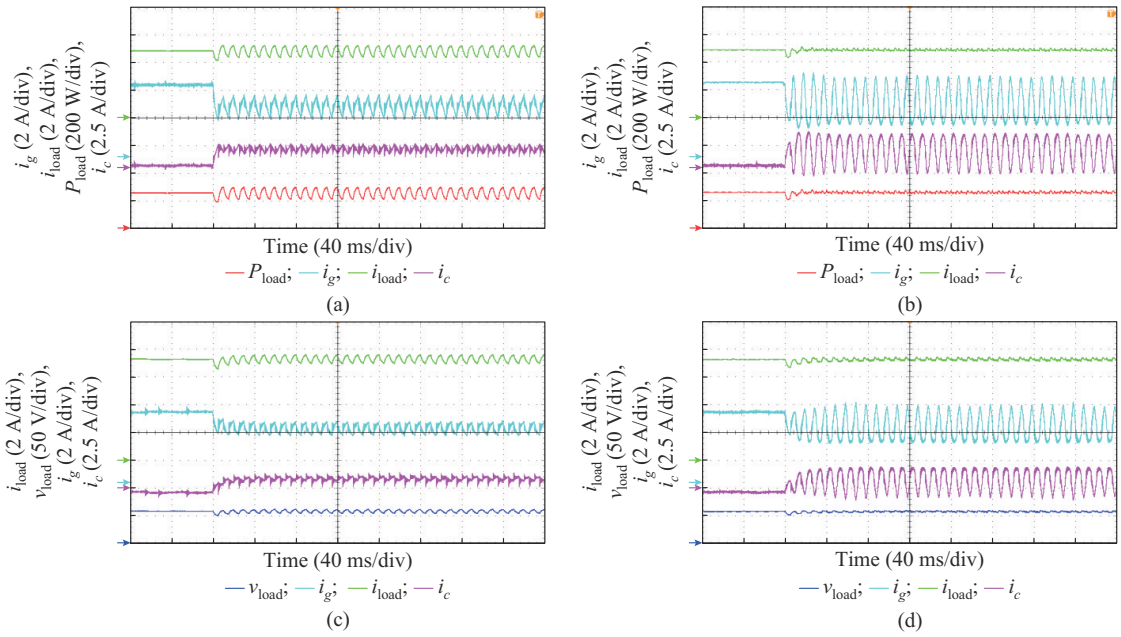

Fig. 17. Experimental results for PDAB under DC voltage sag with oscillation. (a) Constant power control in Case 2. (b) Constant power control in Case 3. (c) Constant current control in Case 2. (d) Constant current control in Case 3.

The attractive features of the proposed DC-UPQC can be summarized as follows.

1) Unlike other traditional DC controllers, the proposed DC-UPQC system has superior features in terms of performing the functions of voltage sag/swell mitigation, power supplement, and voltage and current harmonics elimination.

2) The proposed DC-UPQC system provides a new strategy for ESDs such as SMES to interface with the LV DC microgrid to simultaneously improve the voltage quality simultaneously, smooth the fluctuated power of renewable energy, and suppress voltage and current oscillations during AC voltage unbalance events.

TABLE I
COMPARISON BETWEEN PROPOSED DC-UPQC AND EXISTING DC CONTROL STRATEGIES

Strategy	Voltage sag	Voltage swell	Power regulation	Voltage oscillation	Current oscillation
Method in [39]	×	×	×	√	√
DC-PFC [40]	×	×	√	×	×
IUPS [43]	√	√	×	×	×
SVR [45]	√	√	×	×	×
SMES-TLSVR [46]	√	√	×	×	×
Proposed DC-UPQC	√	√	√	√	√

Note: "×" and "√" represent the device is without and with this function, respectively.

VI. CONCLUSION

An SMES-based DC-UPQC is proposed in this paper. The topologies of its compositions, i. e., SDAB, PDAB, and SMES, are fully described. The DC dual control strategies of the DC-UPQC with consideration of DC and oscillation regulators are presented.

Parameter responses of the DC-DFIG and grid-side power oscillations under DC voltage sag with oscillation are analyzed. With the connection of the proposed controller, simulation results show that all crucial parameters of the DC-DFIG can be well constricted within their maximum permitted values. With the large-power SMES, the proposed DC dual control of the SDAB and PDAB can also be well-implemented under DC voltage oscillations.

An experiment is carried out to verify the proposed DC dual control of the DC-UPQC. Experimental results verify the correctness of the circuit principle of the SDAB and PDAB, and the effectiveness of the modified control strategies is also validated.

Conclusively, the proposed scheme has several outstanding features over other existing DC protection devices. This includes straightforward structure, capability of simultaneously handling the DC voltage and current quality with wide compensation range, and providing improved control strategy for voltage, current, and power oscillation suppression.

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Ruohuan Yang received the B. S. and M. S. degrees from the College of Electrical Engineering, Sichuan University, Chengdu, China, in 2016 and 2019, respectively. He is currently working toward the Ph. D. degree with the School of Electrical and Information Engineering, Tianjin University, Tianjin, China. His current research interests include applied superconductivity, wind energy conversion system, power quality, power electronic converters, and DC microgrid.

Jianxun Jin received the B. Eng., M. Sc., and Ph.D. degrees from University of Science and Technology Beijing, Beijing, China, The University of New South Wales, Sydney, Australia, and University of Wollongong, Wollongong, Australia, in 1985, 1994, and 1997, respectively. He is currently a Professor with the School of Electrical and Information Engineering, Tianjin University, Tianjin, China. He is the Guest Editor-in-Chief of the IEEE Transactions on Applied Superconductivity ASEMD special issue, Chair of the IEEE China Council Council of Superconductivity Chapter (CCCSC), and General Chair of the 2020 International Conference on Applied Superconductivity and Electromagnetic Devices (ASEMD). His current research interests include applied superconductivity, superconducting material characterization and application modelling, superconductors in strong current and electrical power application, electromagnetic devices, electric machine, energy efficiency and green energy generation, electric vehicle, and control and measurement technologies.

Qian Zhou received the B.S. degree from the School of Electrical and Electronic Engineering, Hubei University of Technology, Wuhan, China, in 2020. She is currently working toward the M.S. degree with the School of Electrical and Information Engineering, Tianjin University, Tianjin, China. Her current research interests include applied superconductivity, power electronic converter, and DC microgrid.

Shuai Mu received the B.S. degree from the College of Electrical Engineering, Zhengzhou University, Zhengzhou, China, in 2018. He is currently working toward the M.S. degree with the School of Electrical and Information Engineering, Tianjin University, Tianjin, China. His current research interests include applied superconductivity, AC loss, superconducting magnetic energy storage (SMES), and DC microgrid.

Ahmed Abu-Siada received the B.Sc. and M.Sc. degrees from Ain Shams University, Cairo, Egypt, in 1998, and the Ph.D. degree from Curtin University, Perth, Australia, in 2004, all in electrical engineering. Currently, he is the Discipline Lead of the Electrical and Computer Engineering at Curtin University. He is Editor-in-Chief for the international journal of Electrical and Electronic Engineering. He is the Vice-chair of the IEEE Computation Intelligence Society, WA Chapter and IEEE Senior Member. His research interests include power electronics, power system stability, condition monitoring, and power quality.