# Supply Boosting Technique for Designing Very Low-Voltage Mixed-Signal Circuits in Standard CMOS

Ali Mesgarani, Mustafa N. Alam, Fan. Z. Nelson, Suat U. Ay
Department of Electrical and Computer Engineering,
University of Idaho, Moscow, ID, USA
*suatay@uidaho.edu*

***Abstract*—This paper presents a technique called supply boosting for designing sub-1V analog/mixed-signal circuits. Supply boosting technique (SBT) is suitable for sub-micron CMOS processes containing MOSFET transistors with threshold voltages comparable to the supply voltage. SBT is based on the idea that if current consumption of the circuit block is very low, in the order of nanoamper, supply voltage could be boosted locally to higher levels during a period that the processing of input signals is done. This technique is very suitable for very-low power clocked and continuous time circuits such as level shifters, operational amplifiers, and comparators. Design of a 10-bit supply boosted (SB) SAR ADC is presented as an example of the technique. SB-SAR ADC simulated using 0.5µm CMOS process that has high-$V_T$ NMOS and PMOS devices. Simulations show that the SB-SAR ADC achieves 0.24pJ/conv-step figure of merit (FOM) when operating ADC at 10KS/sec and 1.2V supply.**

## I. INTRODUCTION

Supply voltage level, power consumption and most importantly energy efficiency of mixed-signal subsystems used in energy-limited applications such as wireless sensor networks, portable biosignal acquisition devices, and energy-harvesting systems are critical issues that need to be addressed. Using advanced CMOS technologies in such applications becomes a topic of debate in terms of cost and loss of energy efficiency due to the sub-threshold leakage current in deep-submicron CMOS devices [1]. Besides, necessary scaling of core supply voltages degrades the gate overdrive voltage making threshold reduction necessary [2,3]. However, threshold voltages of mixed-signal/RF devices do not scale as fast as the supply voltages as can be seen in Fig.1. This makes analog and mixed-signal design more difficult in deep-submicron CMOS technologies. This is mainly due to limited circuit techniques and topologies available to accommodate sub-1V supply operation especially when threshold voltages are comparable with supply voltages. Thus, new analog and mixed-signal design techniques addressing both technology and circuit design issues are needed.

One possible approach might be to design sub-1V analog/mixed-signal circuits exploring new circuit design venues by using low cost, mature, and relatively low leakage standard CMOS technologies ($L_{min}$>150nm). Some of these techniques were explored in the past using advanced CMOS technologies or specialized processes that provide devices with reduced threshold voltages [4]. These techniques include bootstrapping [5], charge pump based circuits [6-8], switched opamp technique [9], floating gate based circuits [10], and threshold modulation techniques [11-12]. Low-leakage mature CMOS processes have their own drawbacks especially for sub-1V supply designs. Typically, the sum of threshold voltages of NMOS and PMOS devices in these processes are in the order of 1V or more which makes analog design difficult. Operating the devices in weak inversion region or using unique circuit design techniques are currently used to address overdrive voltage degradation.

In this paper, a new design technique to realize sub-1V mixed-signal circuits called supply boosting technique (SBT) is presented. SBT is discussed in section II. A unique SB comparator topology utilizing both supply and clock boosting techniques is presented in section III. SBT is used for designing a 10-bit SAR ADC in a 0.5µm CMOS process. Design and simulation results of the supply boosted SAR ADC are presented in section IV and section V is designated for discussions and conclusion.

## II. SUPPLY BOOSTING TECHNIQUE

In supply boosting technique (SBT), supply voltage is boosted locally when analog signal processing such as level shifting, amplification or comparison is performed without compromising reliability margins of the process in use. SBT is well suited for designing clocked comparators due to the fact that the comparison of the input signals is performed in concurrent phases during which supply voltage has to be stable. SBT could also be used if very low power signal processing operations are performed continuously by source follower based level shifters, opamps, or comparators. SBT was used in designing continuous time operational amplifiers [6, 7] and clocked comparators [8] before.

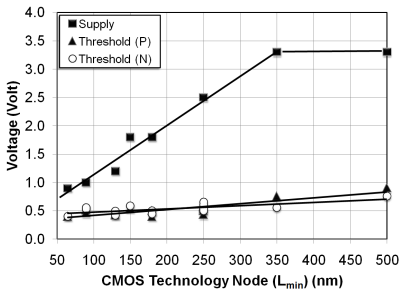


Fig. 1. Supply voltage and threshold voltages versus technology node of commercially available mixed-signal/RF CMOS processes

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Major benefits that can be achieved by boosting supply voltage in SB circuits include: expansion of the input signal range, improved speed and supply voltage range, and operation of all transistors in strong inversion region. The major drawback in SBT is that the capacitor(s) used for supply boosting has to be large enough to provide adequate charge during signal processing. Tradeoff between booster capacitor and speed and, hence power consumption, exists. Boosting circuit also consumes extra power reducing overall energy efficiency of the SB circuits. Another drawback is related to device reliability due to using boosted supply voltages. This issue may not be critical if a larger feature size CMOS processes with higher voltage rating (i.e. 0.5µm/5V) is used while operating circuits in sub-1Volt supply levels.

## III. SUPPLY BOOSTED COMPARATOR DESIGN

Comparators are used as the main building blocks of most analog-to-digital converters (ADC). Design of high resolution, high speed, and low power comparators with wide dynamic range has a significant effect on ADC performance. Especially designing comparators in low voltage regime becomes quite challenging because of the reduced dynamic range. Although different low voltage design techniques have been proposed to improve the performance of analog circuits in this regime none of them address the dynamic range issue. Fig. 2 shows the idea behind the proposed supply boosted comparator (SBC). It composes of single phase supply and clock booster (SCB) or charge pump circuit (M1-M3), supply boosted level shifter (SBLS) (M4-M7), supply boosted latched comparator (SBLC) (M8-M14), second latched comparator (LC) (M15-M21), and bias network (M22-M24). SBC works in two phases like a typical discrete time latched comparator; reset and compare. Supply and clock are boosted during compare period as shown in Fig.3. The main idea is to increase the supply voltage during the comparison phase so that the input signal range can be increased up to $V_{AA}$ covering rail-to-rail input range. The circuit works as follows. During the reset phase, $V_{RST}$=0, $V_{AAB}$ equals to $V_{AA}$ and the output nodes of SBLC and LC are charged to $V_{AA}$. When clock goes high, SCB boosts clock and $V_{AAB}$ approximately to $2V_{AA}$ and the comparators enter the compare phase. In this phase voltage difference between the two inputs is amplified by the two stage comparator. SBLS are included to provide the required overdrive voltage to keep input NMOS devices (M7, M8) in strong inversion regime. Latched comparators are biased with constant tail currents. Although this biasing

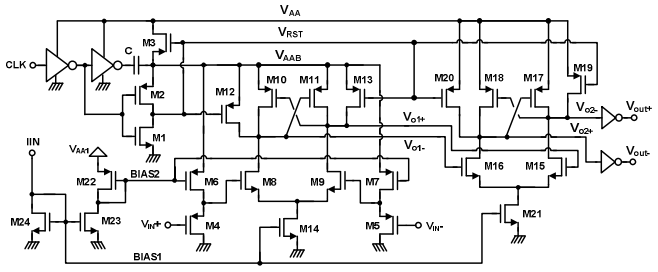


Fig. 2. Proposed supply boosted comparator (SBC)

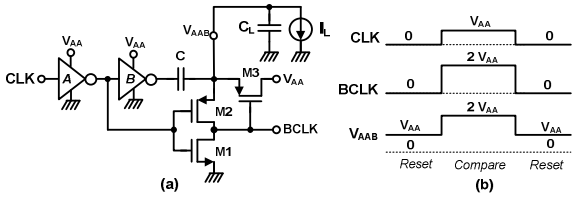


Fig. 3. Supply and clock booster (SCB) circuit; a) schematic, b) timing.

scheme leads to static current consumption form the power supply it has a better performance than the case where the tail transistor is clocked. If the tail transistor is clocked large glitches in the tail current might be introduced during the comparison phase. These glitches drain high currents from the boosted supply leading to faster discharge of boosting node, $V_{AAB}$, and eventually failure of the circuit.

SBC does not consume much power since its output is not a regulated DC voltage. Moreover if an array of such comparators is used in an ADC, a single SCB can be shared among all of them. Assuming no load is connected to the outputs, the voltage at $V_{AAB}$ during compare phase is the sum of the output voltage of inverter *B* and capacitor voltage in reset phase, which is ideally equal to $2V_{AA}$. However, if there is a load capacitance $C_L$ and a load current $I_L$, the voltage at $V_{AAB}$ becomes;

$$V_{AAB} = V_{AA} + \frac{C}{C + C_L} \cdot V_{AA} - \frac{I_L \cdot T}{C + 2 \cdot C_L} \tag{1}$$

where T is compare time. If $C_L$=0.2C and $I_L$ is small, $V_{AAB}$ will be $1.83V_{AA}$ which is more than 90% of the required output. It is necessary that the bulks of M3 and M2 are connected to $V_{AAB}$. Also inverter B has to be designed stronger than inverter A, due to the fact that the bottom plate of pump capacitance, C, has to be connected on inverter B side to achieve better efficiency as given in (1).

Although this technique improves the dynamic range of the comparator, it should be designed carefully according to speed limitations. The regeneration time constant of this comparator can be found as (2) [12].

$$\tau_R = \frac{C_L}{g_{m,p}} = \frac{C_L}{\sqrt{2K'_p\left(\frac{W}{L}\right)_p \cdot I_D}} \tag{2}$$

where $g_{m,p}$ is the transconductance of cross coupled PMOS devices and $I_D$ is their bias current. To reduce the regeneration time constant $g_{m,p}$ must be increased by increasing the bias current. On the other hand, increasing the bias current drops the boosted supply voltage with a higher rate and may cause failure of supply boosting technique unless the boosting capacitor is large enough. Since the size of boosting capacitor cannot exceed a certain value due to limited area, this comparator can only be used for low power, medium speed applications. For example consider the SB comparator supplied from a single 1V power supply. For reliable operation of the comparator, the boosted supply must not fall below a certain level.

$$V_{AAB} = \left|V_{TP}\right| + 3V_{od} \tag{3}$$

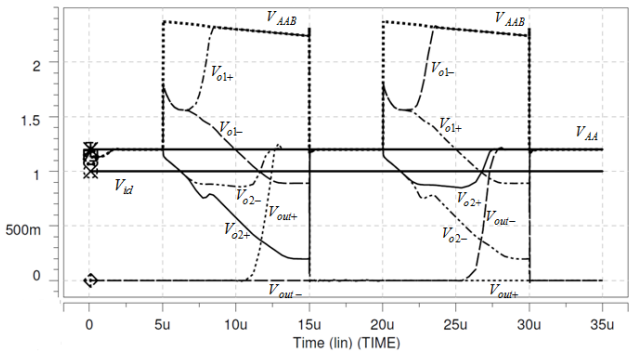


Fig. 4. Simulation result of supply boosted comparator (SBC). ($V_{AA}$=1.2V, Vin-=1.0V, dVin=±0.25mV)

where $V_{od}$ is the overdrive voltage of devices and $V_{AAB}$ can be found from (1). In (3), it is assumed that all devices have the same overdrive voltages. Hence the voltage drop ΔV across the boosting capacitor during the compare phase must not fall below a certain value given in (4)

$$\Delta V < V_{AAB} - |V_{TP}| - 3V_{od} \tag{4}$$

Since the comparison phase takes at least one time constant of the comparator, $\tau_d$, during this time we have

$$\frac{I_{tot} \cdot \tau_d}{C} < V_{AAB} - |V_{TP}| - 3V_{od} \tag{5}$$

Replacing $\tau_d$ in (2) and defining α as the ratio of current in the comparator to the total current, the maximum current that can be drained from the boosted supply can be found as (6).

$$I_{tot} < 2 \cdot K'_p \left(\frac{W}{L}\right)_p \alpha \cdot \left(\frac{C}{C_L}\right)^2 \left(V_{AAB} - |V_{TP}| - 3V_{od}\right)^2 \tag{6}$$

The latter equation gives the upper limit of the total current for a given boosting capacitor.

The supply boosted comparator has been designed and simulated in 0.5µm standard CMOS process in HSpice. The comparator is supplied from a single 1.2V power supply and operates at 65 KHz clock frequency. A current of 50nA has been assigned to boosted level shifters and 100nA to each of the latched comparators. Fig. 4 shows the waveforms at different nodes of the SBC when a 0.5mV differential signal with 1V common mode input voltage is applied. Total delay time in this case is 6.9µs. During comparison time the boosted supply level drops to 2.29V and performance of the comparator does not degrade. SBC was also simulated at sub-1V supply levels. It was working with better than 8-bit resolution with input common mode range of 0.4V for supply voltage of 0.85V. At low supply voltages, as expected speed reduces around 1KConv.-sec.

## IV. Supply Boosted SAR ADC Design

A 10-bit SAR ADC was designed using supply and clock boosting techniques. Overall circuit diagram of the SAR ADC is shown in Fig.5. It is composed of SAR logic blocks (SARL), dynamic shift registers (DSR), supply boosted comparator (SBC), clock phase generators, clock boosting

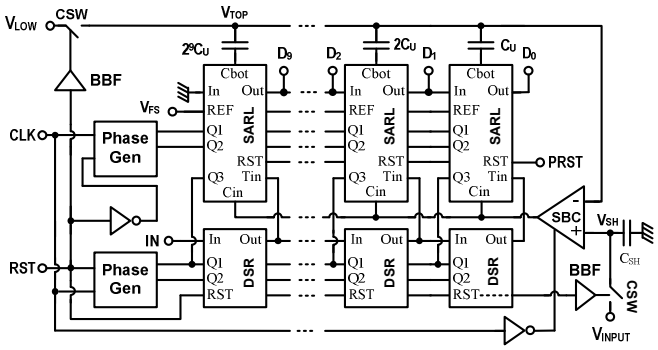


Fig. 5. Circuit diagram of the 10-bit supply boosted SAR ADC.

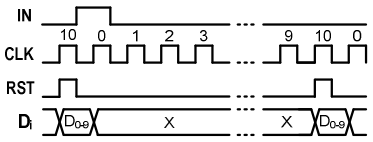


Fig. 6. Timing diagram of the 10-bit supply boosted SAR ADC.

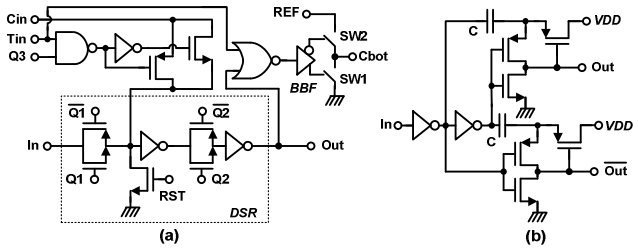


Fig. 7. Schematic diagram of: a) SARL and DSR, b) boosting buffer (BBF).

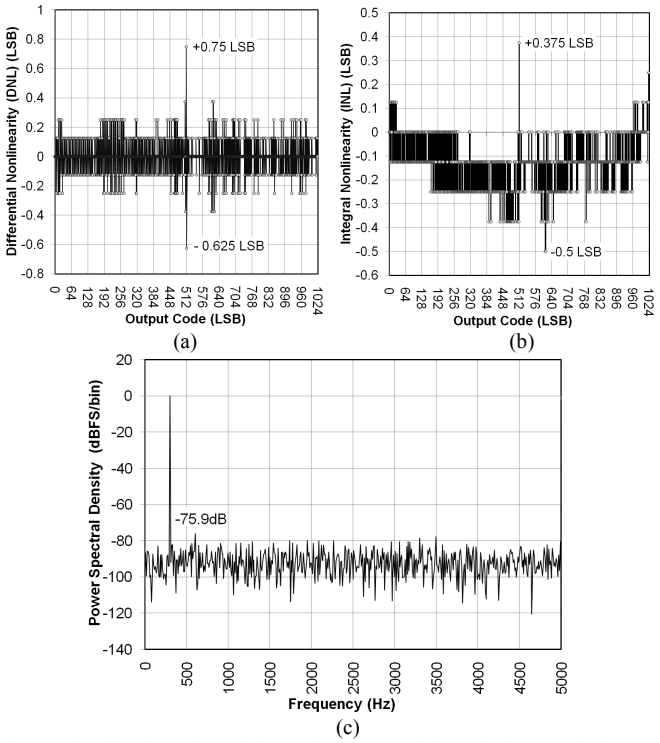


Fig. 8. Simulated static and dynamic characteristics of the supply boosted SAR ADC. a) differential nonlinearity (DNL), b) integral nonlinearity (INL), c) 1000pt FFT spectrum with 302Hz input tone. ($V_{AA}$=1.2V, 10KS/s, SNDR=61.3dB, SFDR=76dB, THD=73dB, ENOB=9.88).

buffers (BBF), and CMOS switches (CSW). Each SARL contains a DSR for implementing successive approximation analog-to-digital conversion algorithm using signals from second DSR and SBC. Binary weighted poly capacitors were used in the design. No offset compensation technique was utilized in the architecture since SB comparator was designed to have high gain and low offset in the range of few LSBs. Two reference signals were used for setting input low level ($V_{LOW}$) and full scale input range ($V_{FS}$). Clock boosting was used for sample and hold switch. Clock signal is alternated between DSR and SARL using RST input as shown on Fig.6. Conversion takes place when RST is low in (n+1) clock cycles. Digital bits are available when RST is high from SARL blocks. Detailed circuit diagram of the SARL, DSR, and BBF is shown in Fig.7. Each block was optimized for low voltage operation.

Static and dynamic characteristics of the supply boosted SAR ADC simulated using HSpice are shown in Fig.8. 40fF unit capacitance ($C_U$) and 1.2V power supply were used in ADC design. Full scale voltage ($V_{FS}$) was 0.75V while low reference level ($V_{LOW}$) was set to 50mV. 1024 quantization levels were scanned and differential and integral nonlinearities were determined. Simulated DNL and INL are shown in Fig.8. Dynamic characteristics were also simulated by applying a 302Hz single tone sinusoidal input. 1000 point FFT was used to determine power spectral density of the output [14]. FFT result is shown in Fig.8(c). Dynamic characteristics at 10KS/sec and 1.2V power supply are summarized in Table I.

Since clock frequency was fairly low, static power consumed in SBC was dominant. Total power consumption was 2.23µW. Using figure-of-merit (FOM) definition from [15], a FOM of 0.24pJ/conv.-step was achieved in proposed SB SAR ADC.

Simulation at different supply voltages was also performed. It was confirmed that the SBC and SB SAR ADC work at sub-1V supply voltages down to 0.85V. It was also observed that overall input common mode range is improved by supply boosting. Input range was around 60-70% of the supply voltage which is significantly larger than that of a standard design. Proposed SB SAR ADC is submitted for fabrication in a standard 0.5µm 2P3M CMOS process.

## V. CONCLUSION

A low-voltage design technique called supply boosting technique (SBT) is proposed to design very-low voltage analog/mixed-signal CMOS circuits in standard CMOS processes in where only high-$V_T$ devices in the order of supply voltage exist. One such process was chosen to implement supply boosted circuits to realize 10-bit SAR ADC. Other low voltage design techniques such as clock boosting were also used. A unique supply and clock booster was designed as integral part of new supply boosted comparator. Input common mode range of SB comparator was extended by using supply boosted level shifter circuits. Designed SB comparator is integrated in a standard SAR ADC architecture. SAR algorithm is implemented by a unique low-voltage optimized logic working in tandem with the SB comparator. It was observed from simulations that supply boosting does not degrade energy efficiency of the circuits as long as very low currents are drained from the boosted supply.

Despite none of the circuits were optimized for speed or power efficiency, very low energy FOM was attained when using supply boosting technique in a standard SAR ADC topology.

TABLE I
SIMULATED CHARACTERISTICS OF THE SUPPLY BOOSTED SAR ADC

| | |
|---|---|
| Resolution | 10-bit |
| Technology | 0.5µm, 2P3M, CMOS |
| Supply Voltage | 1.2 Volt |
| Conversion Speed | 10 KS/sec. |
| Differential Nonlinearity (DNL) | +0.75 LSB / -0.625 LSB |
| Integral Nonlinearity (INL) | +0.375 LSB / -0.5 LSB |
| ENOB* | 9.88 bits |
| THD* | 73.0 dB |
| SNDR* | 61.3 dB |
| SFDR* | 75.9 dB |
| Power Consumption | 2.23 µW |
| FOM | 0.24 pJ/conv.step |

*302Hz input tone and 1.2V supply

## REFERENCES


[1] L. Chang, et. al," Practical strategies for power-efficient computing technologies," Proc. IEEE, vol. 98, no.2, pp. 215-236, Feb. 2010

[2] K. Bult, "Analog design in deep sub-micron CMOS," IEEE European Solid-State Circuits Conference, pp. 126 – 132, 19-21 Sept. 2000.

[3] K. Bernstain, M. Bhushan, N. Rohrer, "On the selection of the Optimal Threshold Voltages for Deep Submicron CMOS Technologies," IBM Microelectronics, 1st Quarter, pp.29-31, 2001.

[4] Y. Matsuya, and J. Yamada, "1 V power supply, 384 kS/s 10b A/D and D/A converters with swing-suppression noise shaping," in 1994 IEEE ISSCC Dig. Tech. Papers, pp. 192–193, Feb. 1994.

[5] A. Abo, and P. Gray, "A 1.5-V, 10-bit, 14-MS/s CMOS pipeline analog-to-digital converter," IEEE JSSC, 34, pp.599–606, May 1999.

[6] T. A. F. Duisters, and E. C. Dijkmans, "A -90-dB THD rail-to-rail input opamp using a new local charge pump in CMOS," IEEE J. Solid-StateCircuits, vol. 33, pp. 947–955, July 1998.

[7] R.S.Pierre, "Low-power BiCMOS op amp with integrated current mode charge pump", IEEE J. Solid State Circuits, 35(7), pp1046-1050, 2000

[8] Lotfi, R.; et al "A 1-V MOSFET-only fully-differential dynamic comparator for use in low-voltage pipelined A/D converters," Int. Symp. on Signals Circuits and Systems, 2, pp.377- 380, July 2003.

[9] A. Baschirotto, and R. Castello, "A 1-V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing," IEEE J. Solid-State Circuits, vol. 32, pp. 1979–1986, Dec. 1997.

[10] Y. Berg, D. T. Wisland, and T. S. Lande, "Ultra low-voltage/low-power digital floating-gate circuits," IEEE Trans. Circuits and Systems-II, vol. 46, pp. 930–936, May 1999.

[11] B. Blalock, et al, "Designing 1-V opamps using standard digital CMOS technology," IEEE Tran. CAS-II, vol.45, pp.769–780, July 1998.

[12] Y.-C. Hung, and B.-D. Liu, "A low-voltage wide-input CMOS comparator for sensor application using back-gate technique", Biosensors and Bioelectronics, Vol. 20, no.1, pp.53-59, 30 July 2004.

[13] P. E. Allen, and D. R. Holberg, CMOS Analog Circuit Design, 2nd Ed., Oxford University Press, 2002.

[14] IEEE-SA Standards Board, " IEEE Standard for Terminology and Test Methods for A/D Converters," *IEEE std 1241-2000, 2001*J.

[15] J. Craninckx and G. van der Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS," ISSCC Dig. Tech. Papers, pp. 246-247, Feb. 2007.