INVITED PAPER

Supporting and Enabling Circuits for Antenna Arrays in Wireless Communications

This paper gives an overview of the four popular beamforming architectures for wireless antenna arrays with emphasis on silicon-based solutions for low power consumption and low-cost integration.

By Ada S. Y. Poon, *Senior Member IEEE*, and Mazhareddin Taghivand, *Student Member IEEE*

ABSTRACT | Antenna arrays have been demonstrated as a very promising technique for high-speed wireless networks, and are anticipated to be indispensable components in future wireless communication systems. This review paper presents an overview of the circuit techniques on combining signals from different receive array elements as well as splitting signals to different transmit array elements with emphasis on silicon-based solutions. It also reviews circuit techniques to control the phase and the amplitude of signals from/to each array element such that signals from those array elements can be combined and split in a desired manner for achieving high data rate communications as well as interference management.

KEYWORDS | Antenna array; baseband beamforming; Cartesian vector modulator; digital beamforming; load-line phase shifter; local oscillator (LO) beamforming; LO-path phase shifter; millimeter-wave communication; phase-oversampling vector modulator; reflective-type phase shifter; radio-frequency (RF) beamforming; switched-delay phase shifter; wireless local area network (WLAN); 60-GHz communication

Manuscript received August 6, 2011; revised January 10, 2012; accepted January 25, 2012. Date of publication March 16, 2012; date of current version June 14, 2012.
The authors are with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA (e-mail: adapoon@stanford.edu; mtaghiv@stanford.edu).

Digital Object Identifier: 10.1109/JPROC.2012.2186949

I. INTRODUCTION

Wireless communications beyond line-of-sight began in 1901, when Marconi received the first radio signal across the Atlantic Ocean. The signal was following the curvature of the earth as the ionosphere provided a reflecting surface for the signal to travel along the earth. In the mid-1950s, scattering from particles in the troposphere was used for long-distance communication in the very high-frequency (VHF) band. During the last three decades, diffraction around mountains and high-rise buildings has helped reduce the number of base stations deployed in cellular/personal communication service (PCS) systems in the ultrahigh-frequency (UHF) band. The scattering nature of physical environment was further exploited by antenna arrays to increase the data rate as demonstrated by the Vertical-Bell Laboratories Layered Space-Time (V-BLAST) system [1], [2] in the 1990s. A prototyping multiple-antenna system built by Bell Laboratories demonstrated an impressive increase in capacity from scattering sources such as walls and furniture. The success of V-BLAST yields the proliferation of multiple-input–multiple output (MIMO) systems using the super high-frequency (SHF) band. In the 2000s, it was included in the wireless local area network (WLAN) standard, as an integral component to achieve data rate of a few 100 Mb/s. Leading fabless semiconductor companies for wireless communications including Broadcom [3] and Qualcomm Atheros [4], [5] have developed products that include highly integrated silicon solutions.

Today, we are used to walking around with our laptops and enjoying the convenience of the Internet access via WiFi, and checking e-mail with our cell phones on the road. However, there is still a considerable gap in speed and security level between the wired and wireless connections.

Taking advantage of the scaling of silicon technologies, the f_t and f_{max} of advanced complementary metal–oxide–semiconductor (CMOS) and SiGe heterojunction bipolar transistor (HBT) processes well exceed 200 GHz. This enables low-cost transceivers in the millimeter-wave band. Higher carrier frequency allows the use of wider frequency spectrum. For example, there is 7 GHz of unlicensed spectrum available in the 60-GHz band in the United States. The multigigahertz spectrum allows multigigabit of data rate with ease. This is in contrast to current practice of cramming many bits per hertz of spectrum in the WLAN and cellular systems. Multigigabit data rate enables seamless integration of wireless and backbone wired Internet access, which can potentially revolutionize the future Internet. Startups and established companies including SiBeam [6], MediaTek, and IBM [7], [8] are developing highly integrated silicon solutions. Spatial power combining using active antenna arrays is used to extend the coverage from a few meters in line-of-sight condition to 10 m in non-line-of-sight condition.

As antenna arrays are indispensable components in high data rate wireless communication systems, this paper reviews circuits that enable and support antenna array beamforming with emphasis on silicon-based solutions.

II. BEAMFORMING ARRAY ARCHITECTURES

Beamforming can be performed at the radio-frequency (RF) path, local oscillator (LO) path, baseband, and digital domain. Fig. 1 contrasts the complexity of these architectures which will be detailed in the following.

A. RF-Path Beamforming

Referring to Fig. 1(a), the phase shifting in RF beamforming happens in the signal path in both Rx and Tx. As the component count of RF beamforming is the lowest, it is popularly used in millimeter and submillimeter wave systems as reflected from Table 1 which summarizes recent implementation of the various array architectures in silicon. Additionally, at high frequencies, for example, 24 GHz and above, RF phase shifting becomes increasingly more popular as the wavelength of electromagnetic waves on silicon is small enough for low-cost integration. This is

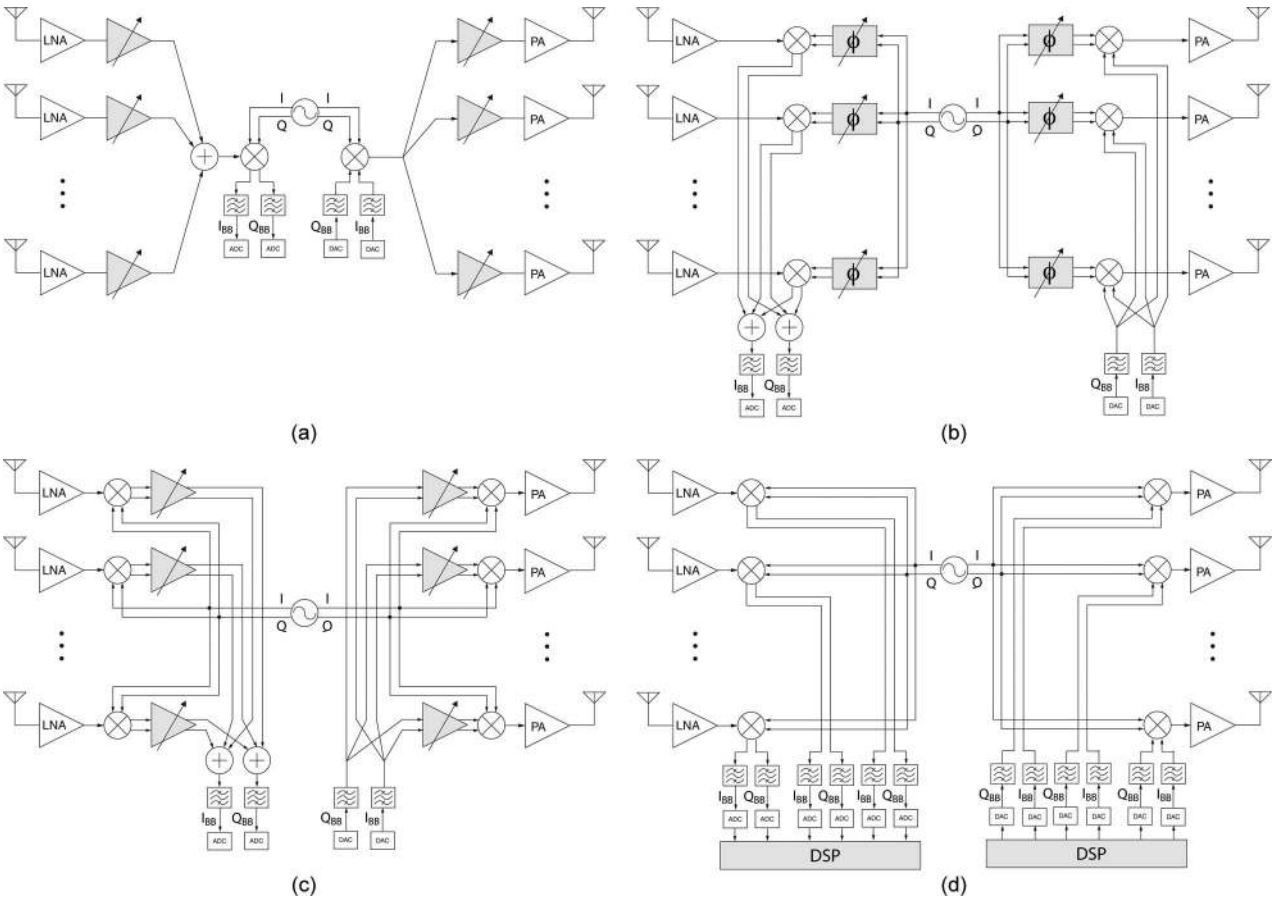

Fig. 1. *Block diagram of (a) RF-path beamforming, (b) LO-path beamforming, (c) baseband beamforming, and (d) digital beamforming. The shaded blocks highlight where phase shifting is performed.*

Table 1 Recent Silicon Implementation of the Four Beamforming Array Architectures

Architecture	Reference	Frequency (GHz)	# of Antennas	Area (mm^2)	Process
RF	[9]	1 – 15	4 RX	9.92	0.13μm CMOS
	[10]	3.1 – 10.6	2 TX	1.17	0.13μm CMOS
			2 RX	1	
	[11]	4	4 RX	1.92	0.13μm CMOS
	[12]	5	4 RX	4.11	90nm CMOS
	[13]	15	2 RX	10.32 (RF only)	0.18μSiGe BiCMOS
	[14]	24	4 RX	3.02 (RF only)	0.13μm CMOS
	[15]	25	4 RX	1.43 (RF only)	0.13μm CMOS
	[16]	39	4 TX/RX	4.04 (RF only)	0.13μSiGe BiCMOS
	[17]	45	16 TX	8.32 (RF only)	0.18μm SiGe BiCMOS
	[18]	60	2 Rx	1.6 (RF only)	65nm CMOS
	[19]	60	4 RX	3.4 (RF only)	65nm CMOS
	[20]	60	4 TX/RX	1.6 (RF and IF)	90nm CMOS
	[8]	60	16 RX	37.70	0.12μm SiGe BiCMOS
	[7]	60	16 TX	43.88	0.12μm SiGe BiCMOS
	[6]	60	32 TX, 4RX	72.67	65nm CMOS
			8 TX, 32 RX	77.16	
LO	[21]	3.1 – 4.8	2 TX, 2 RX	15.96 (RF and IF)	0.18μm CMOS
	[22]	6 – 18	4 RX	62.4	0.13μm CMOS
	[23]	24	4 TX	14.28	0.18μm CMOS
	[24]	24	4 TX/RX	5.05	0.13μm CMOS
	[25]	24	8 RX	11.55	0.18μm SiGe BiCMOS
	[26]	52	2 RX	1.4	90nm CMOS
	[27]	77	4 TX	17 (RF and IF)	0.13μm SiGe BiCMOS
	[28]	77	4 TX, 4 RX	25.84	0.13μm SiGe BiCMOS
Baseband	[29]	60	4 RX	1.93 (Baseband only)	40nm CMOS
	[30]	60	4 TX, 4 RX	8.75	65nm CMOS
Digital	[4]	2.4, 5	2 TX, 2 RX	11	0.13μm CMOS
	[3]	2.4, 5	2 TX, 2 RX	18	0.18μm CMOS
	[5]	2.4, 5	3 TX, 3 RX	10.4	65nm CMOS
	[31]	2.5, 5	2 TX, 2 RX	29.16	0.5μm SiGe BiCMOS
	[32]	5	2 RX	2.32	0.18μm CMOS
	[33]	5	2 RX	2.47	0.18μm CMOS
	[34]	8 – 20	2 RX	5.72	0.18μm SiGe CMOS

also a major advantage of RF beamforming, especially for large array systems.

At lower frequencies, such as between 700 MHz and 5 GHz, it is difficult to design true time delay or phase-shifting elements as the wavelength is in the order of centimeters, implying that their physical size would be prohibitively large. Active phase shifters are available at low gigahertz frequencies, but they could introduce noise and nonlinearity in the RF signal path.

Since the received signals are added in the RF path and before the mixer, hence still real signals that are not decomposed into I (in phase) and Q (quadrature phase), there is a much less risk of I/Q phase and amplitude imbalance. Multipath and other unwanted interferences will be spatially filtered in the RF receiver path after combining and before reaching the mixer. Simplicity in the LO generation and routing is another major advantage of beamforming at RF. Also the number of mixers is minimal.

There are some disadvantages in beamforming at RF. Noise figure (NF) can be degraded due to phase shifting at the RF signal path, which is always lossy. Also, RF phase shifters usually do not attain high resolution which potentially limits the performance.

B. LO-Path Beamforming

Referring to Fig. 1(b), the phase shifting in LO beamforming happens in the LO distribution network. The RF signal path at both the Rx and the Tx can be made very compact, which can improve the NF of the Rx and potentially save power in the Tx. Phase shifting at LO has minimal impact on system signal-to-noise ratio (SNR) and gain in both Rx and Tx as the noise and linearity requirements on LO are easier to meet than their counterparts in the signal path. Using the quadrature voltage-controlled oscillator (QVCO) [26] or ring oscillators [24], [25], accurate phase shift over a wide band can be achieved, which makes this architecture suitable at lower gigahertz frequencies [21], [22].

A major problem with LO beamforming is the large LO routing network, which can become very challenging and power hungry as the array size increases. Also I/Q imbalance from the LO signals and the mixers have to be calibrated. In order to calibrate the I/Q imbalance in both

Table 2 Advantages and Disadvantages of the Four Beamforming Architectures for an $N \times N$ Array System

Architecture	Frequency Low GHz	Frequency High GHz	Wideband Beamforming	Receiver SNR	LO Complexity	Mixer Complexity	Phase Shifter Resolution	Number of ADC	Number of DAC	Modem Calibration Complexity
RF	–	+	+	–	+	2	+/–	2	2	+
LO	+	+/–	–	+	–	$2N$	–	2	2	–
Baseband	+	+	–	+	–	$2N$	+	2	2	–
Digital	+	–	–	+	–	$2N$	+	$2N$	$2N$	–

phase and amplitude, a feedback loop from the Tx to the Rx is needed. This further complicates routings in the silicon, especially for large array systems.

C. Baseband Beamforming

Referring to Fig. 1(c), the phase shifting in baseband beamforming is done after downconversion and is in the baseband circuitry. Unlike RF beamforming where the phase shift for each array element can be accomplished by two variable gain amplifiers (VGAs), the phase shift in baseband beamforming is controlled by four VGAs. Baseband beamforming requires a mixer pair for each element, a large LO distribution network [30], and the implementation of the phase rotation and gain control after downconversion. I/Q mismatch can potentially be a critical problem, hence careful I/Q calibration is needed.

The advantage of this architecture is that fine phase resolution can be achieved with less power penalty, as the phase rotation is done at low frequency in the baseband. Therefore, baseband beamforming can be a very good candidate when a fine phase resolution is needed. It is also a good candidate to be used at lower gigahertz frequencies, as the phase shifting does not require passive elements.

D. Digital Beamforming

Referring to Fig. 1(d), the phase shifting in digital beamforming is performed in the digital domain inside the digital signal processing (DSP) unit. This architecture is most suitable for low gigahertz phase array systems [3]–[5], [31], where phase shifters are not easy to design and very expensive for integration. The advantage of this architecture is that the phase rotation is done in the digital domain. Hence, it simplifies the RF circuit design of the transceiver.

The major disadvantage is that two analog-to-digital converters (ADCs) and two digital-to-analog converters (DACs) are needed for each array element. Also the I/Q imbalance could be a major issue in digital beamforming. In addition to the same I/Q imbalance issues as the baseband beamforming, this architecture can potentially suffer from the issue of different group delays at the I-path and the Q-path of the baseband chains as they go through independent low-pass filters. This architecture has not yet been implemented at high gigahertz frequencies because low power, high resolution, and fast ADCs are very challenging to materialize. It might change in the future as CMOS gets faster and ADC designs can make digital beamforming competitive with other beamforming architectures.

Finally, there are other types of beamforming architecture such as switched-beam techniques using Butler matrix [35]. The beam patterns are predefined, and hence, it is less flexible than the four beamforming architectures described above. In summary, the choice of which beamforming architecture to use mainly depends on the operating frequency, the silicon technology node used, and the number of array elements. Table 2 summarizes the advantages and disadvantages of the four beamforming architectures.

III. PHASE AND AMPLITUDE CONTROL CIRCUITS

Phase shifters are integral components in an antenna array. They can be implemented using passive or active devices, and using lumped or distributed elements. The tradeoffs are die area, insertion loss, loss variation over range of phase shift, direct current (dc) power consumption, bandwidth, and signal linearity. In the following, we will explain six basic types of phase shifters, and their advantages and disadvantages. Similar to the beamforming architecture, there are many different variations from these six phase shifters and there are multiple ways to combine them to achieve phase shifting.

A. Reflective-Type Phase Shifter

A reflective-type phase shifter (RTPS) consists of a coupler with two of its ports connecting to identical reflective loads, as illustrated in Fig. 2. Variable phase shift

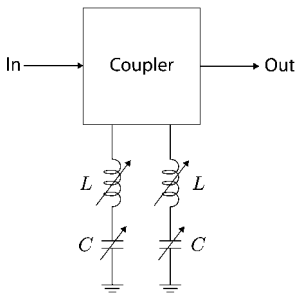

Fig. 2. *Reflective-type phase shifter.*

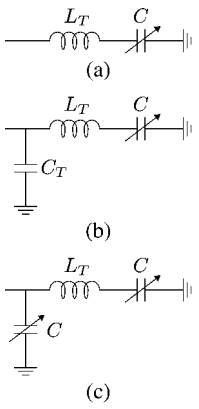

Fig. 3. *Types of reflective load in RTPS: (a) resonant load (RL), (b) resonant load with impedance transformation (RLT), and (c) π-type resonant load (π-RL).*

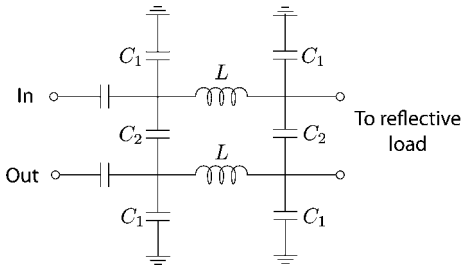

Fig. 4. *A branch-line coupler used in RTPS.*

is realized by tuning the reflective loads, L and/or C. Suppose the characteristic impedance of the coupler is Z_0. For a specific reflective load

$$Z_L = jwL + \frac{1}{jwC}. \tag{1}$$

The phase shift is determined by the phase of the reflection coefficient

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2}$$

and is given by

$$\phi = \angle\Gamma = \pm\pi - 2\tan^{-1}\left(\frac{\omega L - \frac{1}{\omega C}}{Z_0}\right). \tag{3}$$

Hence, tuning either C or L introduces phase shift. The range of phase shift depends on the tuning range of C and L. Both the coupler and the reflective loads can be implemented by passive or active devices. RTPS supports bidirectional phase shifting.

As tunable inductors are not available in most silicon processes, varactors are usually used in the reflective load. But varactors in silicon have limited tuning range on the capacitance. Usually, the varactor's capacitance can vary by a factor of around 2 or less. This limits the range of phase shift. Inductors are therefore added to increase the phase-shift range by resonating the capacitance of the varactor, as illustrated in Fig. 3(a). The loss of the resonant load (RL) can be reduced by adding a capacitor C_T to form an L-match impedance transformation network, as illustrated in Fig. 3(b).

Zarei *et al.* [36], [40] implement the resonant load with impedance transformation network (RLT) in both SiGe bipolar CMOS (BiCMOS) and CMOS. In the CMOS implementation, an active inductor is used to realize L_T to achieve low loss. Furthermore, a 3-dB 90° codirectional coupler is implemented using lumped LC networks, as shown in Fig. 4. That is, the RTPS is realized by passive coupler and active load at 2.4 GHz.

Zheng *et al.* [37], on the other hand, use active coupler and active load. The coupler is realized by a compact three-transistor active circulator. Resonant load with active inductor is used. The first two rows of Table 3 compare their performances. The architecture based on active coupler and active load achieves wider range of phase shift, incurs less loss, and occupies less die area. The architecture based on the passive coupler and active load, however, consumes much less power.

Moving up to millimeter-wave frequencies, Wu *et al.* [38] implement a passive-coupler and passive-load RTPS at 24 GHz. The coupler is a transformer-based quadrature hybrid coupler and is realized by multiple metal layers in CMOS. The load is a π-type resonant load, as illustrated in Fig. 3(c). Compared with the active RTPS in [37] and the hybrid active–passive RTPS in [36] and [40], the passive

Table 3 Summary of Recent Developments in Reflective-Type Phase Shifter

Reference	Frequency (GHz)	Coupler	Reflective Load	Phase Range	Area (mm^2)	Power (mW)	Gain (dB)	IP1dB (dBm)	Process
[36]	2.4	Lumped LC	RLT, active inductor	105°	1.08	1.8	−11	> 10	0.18μm CMOS
[37]	2.4	Active circulator	RL, active inductor	120°	0.357	111	−5	6	0.18μm CMOS
[38]	24	Transformer-based	π-RL	360°	0.33	0	−12.5	–	0.18μm CMOS
[39]	60	Coupled lines	π-RL	180°	0.28	0	−7.5	–	0.13μm SiGe BiCMOS

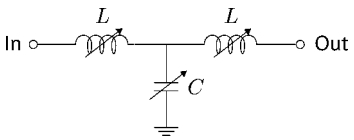

Fig. 5. *Loaded-line phase shifter.*

RTPS incurs more loss. But since the implementation is at 24 GHz, the passive RTPS occupies about the same area as the active RTPS at 2.4 GHz.

Tsai *et al.* [39] realize the coupler by coupled lines in the thick top metal layer and use π-type resonant load. The 60-GHz transceiver developed by IBM and MediaTek [7], [8] is based on this architecture. As there is loss variation across the phase-shift setting, a phase-inverting VGA is used in [7] and [8] to achieve both full 360° and fine variable gain to compensate for the RTPS loss. Table 3 summarizes recent developments in RTPS and their performances.

B. Loaded-Line Phase Shifter

Loaded-line phase shifter consists of tunable series and shunt elements, as illustrated in Fig. 5. It can be shown that for a given phase shift ϕ, the values of the inductance and capacitance are given by [42]

$$L = \frac{Z_0}{\omega}\tan\frac{\phi}{2} \qquad C = \frac{1}{\omega Z_0}\sin\phi. \tag{4}$$

As tunable inductors are not available, Hancock and Rebeiz [42] approximate the tunable inductor by a fixed inductor in series with a varactor. The range of phase shift will be determined by the tuning range of the MOS varactor which is limited. To increase the phase-shift range, multiple of varactor-tuned LC networks are connected in series. Amplifiers are sometimes inserted in between the varactor-tuned LC networks to compensate the insertion loss [41]. At high frequencies, for example, 60 GHz, the series elements can be realized by transmission lines [43]. Table 4 summarizes recent developments in loaded-line phase shifter and their performances.

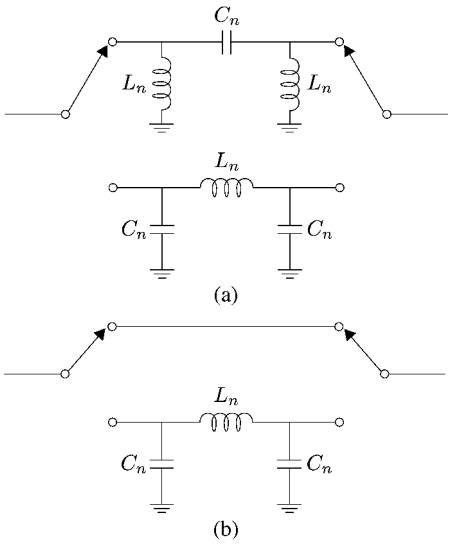

Fig. 7. *Types of unit cell in switched-delay phase shifter: (a) high-pass/low-pass and (b) bipass/low-pass.*

C. Switched-Delay Phase Shifter

Switched-delay phase shifter is made of a cascade of unit cells, as illustrated in Fig. 6. Each cell introduces two options on the phase shift: t_{dn} and t'_{dn}. The total phase shift is the sum of the phase shift introduced by each cell. It is inherently a digital phase shifter. Implementations in the

Table 4 Summary of Recent Developments in Loaded-Line Phase Shifter

Reference	Frequency (GHz)	Topology	Phase Range	Area (mm^2)	Power (mW)	Gain (dB)	IP1dB (dBm)	Process
[41]	2.4, 5.8	3 stages of LC π network	180°, 360°	2.76	n.a.	5.4, 2.1	–	0.18μm CMOS
[42]	12	4 stages of LC T network	180°	0.51	53.5	3.7	−27.3	SiGe
[43]	60	5 stages of LC T network	45°	0.10	66	–	–	0.12μm SiGe BiCMOS

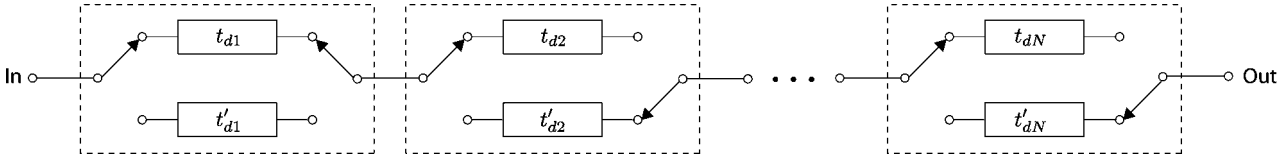

Fig. 6. *An N-stage switched-delay phase shifter.*

Table 5 Summary of Recent Developments in Switched-Delay Phase Shifter

Reference	Frequency (GHz)	Topology	Phase Resolution	Area (mm^2)	Power (mW)	Gain (dB)	IP1dB (dBm)	Process
[44]	1–14	Tapped delay trombone line	3 bit	0.28	22	–	–	0.18μm SiGe BiCMOS
[45]	7–11	High-pass/low-pass	6 bit	14.44	45	>-10	–	0.5μm SiGe BiCMOS
[46]	10.5	High-pass/low-pass	5 bit	9.84	248	–	4.4	0.13μm SiGe BiCMOS
[47]	12	1 bit high-pass/low-pass 3 bit by-pass/low-pass	4 bit	1.62	26.64	3.5	–	0.18μm CMOS
[48]	35	By-pass/low-pass	4 bit	0.1	0	-10	–	0.12μm SiGe BiCMOS
[16]	35	4 bit by-pass/low-pass 1 bit LC π network	5 bit	0.27	–	–	–	0.12μm SiGe BiCMOS
[20]	60	High-pass/low-pass	2 bit	0.03	–	-7	10	90nm CMOS

literature differ by the topologies used to realize the delay elements and the switches.

LC network is usually used to realize the delay elements in each unit cell. The high-pass/low-pass and bypass/low-pass LC networks are popular configurations. In the high-pass/low-pass configuration shown in Fig. 7(a), the difference between the phase from the high-pass filter path and the low-pass filter path yields the phase shift of the nth bit. The high-pass filter path can be replaced by a bypass filter path, as shown in Fig. 7(b). The high-pass/low-pass configuration supports a broader bandwidth than its bypass counterpart. Metal–insulator–metal (MIM) and metal-over-metal (MOM) capacitors in conjunction with spiral inductors are usually used to realize the LC networks. The solid-state switch is typically realized by a p-i-n diode or a transistor.

The unit cells need not be identical. Nonidentical cells are used in [16], [20], [45], [46], and [48]. Usually, the nth cell introduces a phase shift of $180^\circ/2^{n-1}$. The number of cells equals the number of bits in the phase resolution. Identical cells are used in [44] and [47]. The resolution becomes $\log_2 N$ instead of N where N is the number of cells. Table 5 summarizes recent developments in switched-delay phase shifter and their performances.

D. Cartesian Vector Modulator

The reflective-type, loaded-line, and switched-delay phase shifters only control the phase of the signal. These phase shifters are usually lossy and occupy large die area due to the use of many passive devices. The signal amplitude varies with the phase shift. VGAs are usually used to compensate for this variation. Occasionally, these VGAs are used to control the magnitude of the signal. That is, the LC-based phase shifter controls the phase while the VGA controls the magnitude. Alternatively, the phase and magnitude controls can be achieved by the summation of two weighted orthogonal vectors as contrasted in Fig. 8. This is the Cartesian vector modulator (VM) and can be realized by two VGAs. Mathematically, $a_R = a\cos\phi$ and $a_I = a\sin\phi$. The VGAs in Fig. 8(b) can change polarity, for example, by swapping the positive and negative paths in a differential topology, in order to support full 360° phase-shift range. But its implementation is very straightforward. Table 6 summarizes recent developments in Cartesian vector modulator and their performances.

E. LO-Path Phase Shifter

Passive implementation of phase shifters incurs large loss and active implementation causes nonlinearity problem. Both will degrade the overall sensitivity of a transceiver if phase shifters are introduced in the signal path of the transceiver. In addition, the signal amplitude varies with the amount of phase shift. Active amplifiers are sometimes inserted to compensate for this variation, and consume dc power. An alternative approach is to introduce phase shift in the signal from the LO that is used to downconvert the received signal to a lower intermediate frequency (IF), as illustrated in Fig. 9. As the phase shifting is introduced in the LO path, loss and nonlinearity from the phase shifter do not directly impact the transceiver sensitivity.

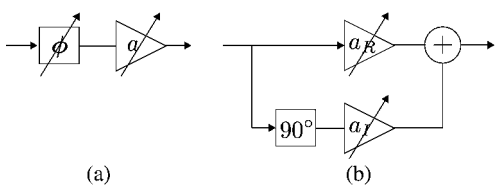

Fig. 8. *(a) Phase shifter followed by VGA and (b) Cartesian vector modulator.*

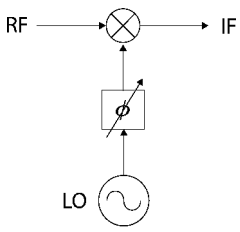

Fig. 9. *LO-path phase shifter.*

Table 6 Summary of Recent Developments in Cartesian Vector Modulator

Reference	Frequency (GHz)	Phase Resolution	Power[1] (mW)	Gain[1] (dB)	IP_{1dB}[1] (dBm)	Process
[12]	5	–	35	–	–	90nm CMOS
[49]	12	4 bit	8.7	1.2	−5.4	0.13μm CMOS
	24	4 bit	11.7	−3	−0.8	0.13μm CMOS
[14]	24	4 bit	28.8	–	−23	0.13μm CMOS
[18]	60	4 bit	78	12	−16	65nm CMOS

[1]The power consumption, gain, and IP_{1dB} in [12], [14], and [18] are per channel of the RF receiver which includes LNA, vector modulator, and combining circuits.

There are two main techniques to realize the phase shifter in Fig. 9. In the first technique, signal from the local oscillator is fed to a multiphase generation block which outputs a set of LO signals with different phases. Copies of these LO signals are distributing to individual front-end where a phase selector chooses the appropriate phase of the LO to the corresponding RF mixer. The multiphase generation block can be realized by a resistor-capacitor (RC) bridge [51], [52], a ring voltage-controlled oscillator (VCO) [25], [54], a divider-by-two circuits following the VCO [21], and a delay-locked loop (DLL) with or without phase interpolator [50]. With reference to Fig. 10, coherent distribution of the multiphase LO signals across the chip to multiple front-ends is challenging. This is the major bottleneck for its application at high frequencies.

In the second technique, phase shift is performed adjacent to the RF mixer of each front-end. The phase shifter in Fig. 11 can be realized by any phase-shifting technique discussed in previous subsections. Among them, the Cartesian vector modulator is the most commonly used due to its compact size [22], [53], [55], [56]. Finally, Table 7 summarizes recent developments in LO-path phase shifter.

F. Phase-Oversampling Vector Modulator

Every complex number can be represented by $u = a_R + ja_I$, which can be rewritten as

$$u = a_R e^{j0} + a_I e^{j\frac{\pi}{2}}. \tag{5}$$

The real and imaginary parts are uniquely defined by the following inner products:

$$a_R = \mathrm{Re}\langle u, e^{j0}\rangle \qquad a_I = \mathrm{Re}\langle u, e^{j\frac{\pi}{2}}\rangle \tag{6}$$

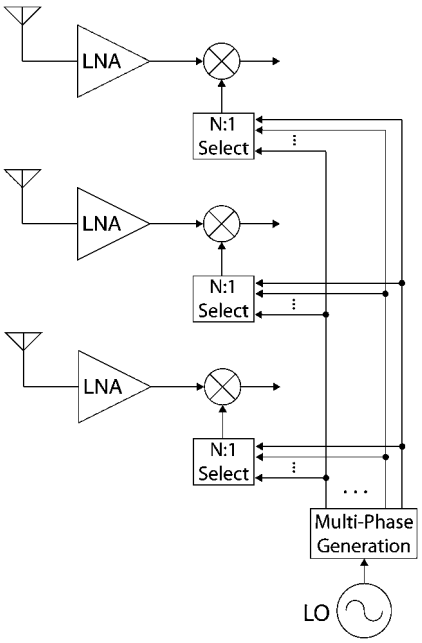

Fig. 10. *LO-path phase shifter: discrete phases are generated adjacent to the LO and are distributed to multiple front-ends.*

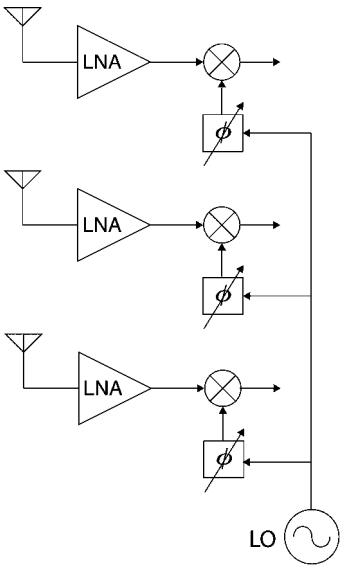

Fig. 11. *LO-path phase shifter: phase shift is generated adjacent to the mixer of each front-end.*

Table 7 Summary of Recent Developments in LO-Path Phase Shifter

Reference	Frequency (GHz)	Topology	Process
[50]	0.9, 2.4	DLL multi-phase generation	0.13μm CMOS
[51], [52]	2	RC-bridge multi-phase generation	Silicon
[21]	3.1 – 4.8	divider-by-two after VCO multi-phase generation	0.18μm CMOS
[53]	5.2	Cartesian VM phase shifter	0.25μm CMOS
[22]	6 – 18	Cartesian VM phase shifter	0.13μm CMOS
[25], [54]	24	Ring VCO multi-phase generation	0.18μm SiGe BiCMOS
[55]	24	Cartesian VM phase shifter	0.13μm CMOS
[56]	44	Cartesian VM phase shifter	0.18μm SiGe BiCMOS

where $\mathrm{Re}\, x$ denotes the real part of x. The basis $\{e^{j0}, e^{j(\pi/2)}\}$ is orthogonal and contains the minimum number of basis elements to represent any complex number. Now, let us consider another basis

$$\left\{e^{j\frac{n\pi}{M}} : n = 0, 1, \ldots, M-1\right\} \tag{7}$$

for $M \geq 3$. For any complex number u, it can be written as

$$u = u_0 e^{j0} + u_1 e^{j\frac{\pi}{M}} + \cdots + u_{M-1} e^{j\frac{(M-1)\pi}{M}}. \tag{8}$$

The coefficients u_n are no longer unique. As the basis in (7) is a unit-norm tight frame, one possible set of coefficients is [57]

$$u_n = \frac{2}{M}\mathrm{Re}\left\langle u, e^{j\frac{n\pi}{M}}\right\rangle. \tag{9}$$

In the Cartesian vector modulator, the real and imaginary parts a_R and a_I are quantized. For example, if each VGA in Fig. 8(b) has a 2-b resolution, the Cartesian vector modulator will synthesize the following complex gain:

$$u = \begin{Bmatrix} +1 \\ +\frac{1}{3} \\ -\frac{1}{3} \\ -1 \end{Bmatrix} e^{j0} + \begin{Bmatrix} +1 \\ +\frac{1}{3} \\ -\frac{1}{3} \\ -1 \end{Bmatrix} e^{j\frac{\pi}{2}}. \tag{10}$$

In the phase-oversampling vector modulator proposed in [11], [19], and [58], the u_n's in (8) are quantized. For example, if $M = 4$, the phase-oversampling vector modulator will synthesize the following complex gain:

$$u = \begin{Bmatrix} +\frac{1}{2} \\ -\frac{1}{2} \end{Bmatrix} e^{j0} + \begin{Bmatrix} +\frac{1}{2} \\ -\frac{1}{2} \end{Bmatrix} e^{j\frac{\pi}{4}} + \begin{Bmatrix} +\frac{1}{2} \\ -\frac{1}{2} \end{Bmatrix} e^{j\frac{\pi}{2}} + \begin{Bmatrix} +\frac{1}{2} \\ -\frac{1}{2} \end{Bmatrix} e^{j\frac{3\pi}{4}}. \tag{11}$$

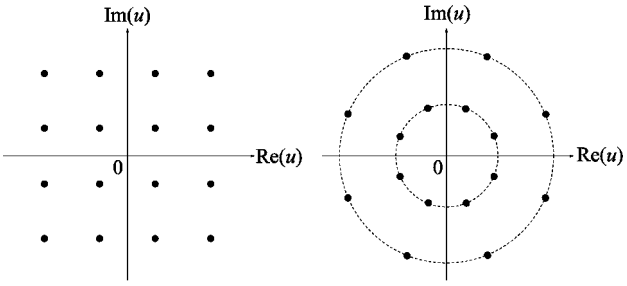

Fig. 12. *Synthesized complex gains from (left) Cartesian and (right) phase-oversampling vector modulators.*

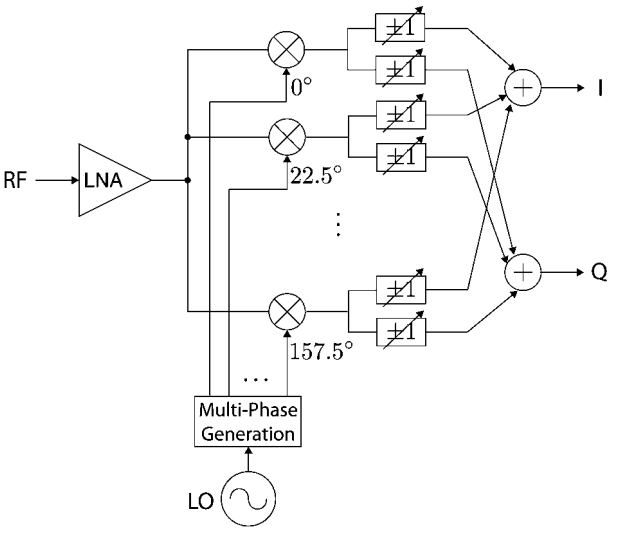

Fig. 13. *Phase-oversampling vector modulator implemented in [11] and [58]: oversampling phases are generated in the LO and distributed to the front-ends.*

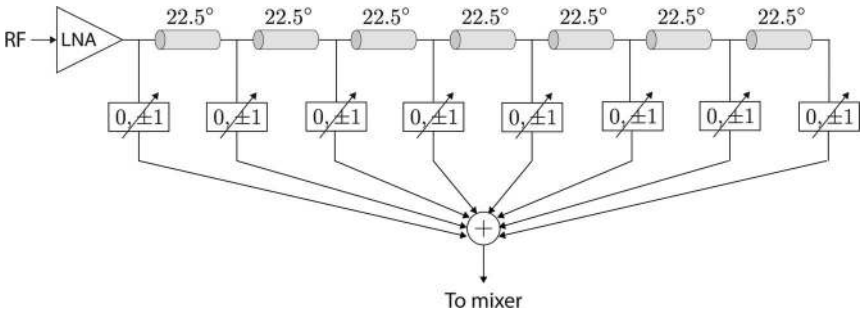

Fig. 14. ***Phase-oversampling vector modulator implemented in [19]: oversamplling phases are generated locally to each front-end using microstrip lines.***

Fig. 12 contrasts the two sets of complex gains. They both cover the same space and require the same number of bits to represent them. In the phase-oversampling vector modulator, however, the corresponding VGAs become ± 1 switches, which can substantially relax circuit requirements. It can potentially solve the bottlenecks of Cartesian vector modulator, especially at high frequencies.

In [11] and [58], Tseng *et al.* propose to generate the oversampling phases at the LO and distribute them to the multiple front-ends, as illustrated in Fig. 13. This architecture is suitable for low gigahertz frequencies. In [19], Lin *et al.* propose to generate the oversampling phases locally at each front-end using microstrip lines, as illustrated in Fig. 14. This is more suitable for millimeter-wave frequencies. The beamforming receiver in [19] achieves a phase resolution of 3.5°, which corresponds to about 7 b, and consumes 44.5 mW per channel at 60 GHz.

IV. CONCLUSION

This paper reviews the four popular beamforming architectures: RF path, LO path, baseband, and digital beamforming. It also reviews the six basic phase shifters: reflective type, loaded line, switched delay, Cartesian vector modulator, LO-path phase shifter, and phase-oversampling vector modulator. They are necessary for the circuit realization of antenna arrays used in both low gigahertz (WiFi and WiMax bands) and high gigahertz (millimeter-wave bands) wireless communications. We emphasize on silicon-based solutions for low-cost integration and low power consumption. Any antenna array system can be the result of a combination of the four beamforming architectures and the six phase-shifting circuit techniques. This review paper serves to help readers understand current implemented systems. More importantly, it is our hope that readers can find this article as an inspiration and a good starting point for their own designs. ■

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ABOUT THE AUTHORS

Ada S. Y. Poon (Senior Member, IEEE) was born in Hong Kong. She received the B.Eng. and M.Phil. degrees in electrical and electronic engineering from the University of Hong Kong, Hong Kong, in 1996 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering and computer sciences from the University of California at Berkeley, Berkeley, in 1999 and 2004, respectively.

In 2004, she was a Senior Research Scientist at Intel Corporation, Santa Clara, CA. In 2005, she was a Senior Technical Fellow at SiBeam, Inc., Fremont, CA. In 2006–2007, she was an Assistant Professor at the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana. Since 2008, she has been at the Department of Electrical Engineering, Stanford University, Stanford, CA, where she is currently an Assistant Professor. Her research focuses on applications of wireless communication and integrated circuit technologies to biomedicine.

Mazhareddin Taghivand (Student Member, IEEE) was born in Tehran, Iran. He received the B.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 2004 and the M.S. degree in electrical engineering from Harvard University, Cambridge, MA, in 2006. Currently, he is working towards the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA.

Since 2006, he has been with Qualcomm, San Diego, CA, designing local oscillator (LO) and synthesizer's building blocks for radio-frequency (RF) connectivity applications. His main research interests are in ultralow power, and high data rate communication at 60 GHz.