Suppression of GHz Range Power/Ground Inductive Impedance and Simultaneous Switching Noise Using Embedded Film Capacitors in Multilayer Packages and PCBs

Hyungsoo Kim, Byung Kook Sun, and Joungho Kim

***Abstract*—We measured and demonstrated the great advantages of embedded film capacitors in reducing power/ground inductive impedance and the suppression of SSN at frequencies up to 3 GHz for high-performance multilayer packages and PCBs. Eight-layer test PCBs were fabricated, and their inductive power/ground network impedances were measured as a function of film thickness, via distribution, and combined use with discrete decoupling capacitors, using a two-port self-impedance measurement method. This successfully demonstrated that the power/ground inductive impedance was reduced from 270 pH to 106 pH simply by using an embedded film capacitor instead of 16 discrete decoupling capacitors.**

***Index Terms*—Decoupling capacitor, embedded film capacitor, power integrity, power/ground impedance, simultaneous switching noise.**

I. Introduction

UNTIL recently, discrete decoupling capacitors have usually been used to stabilize the power supply voltage levels by providing low-inductive power supply current paths through the discrete decoupling capacitors [1]. However, the discrete decoupling capacitor is not effective above a few hundred MHz because of its large serial inductance, consisting of the equivalent series inductance (ESL) of the discrete decoupling capacitor itself, the decoupling capacitor-mounting pad, the necessary power/ground via, and power/ground traces [2]. There have been continuing efforts to reduce the parasitic ESL of the discrete decoupling capacitors. Low-ESL capacitors developed include the interdigitated capacitor (IDC), the low-inductance chip capacitor (LICC), and the low-inductance capacitor array (LICA). However, significant ESL still exists, caused by the mounting pad for the discrete decoupling capacitors, the power/ground trace, and the power/ground via on the multilayer power/ground decoupling network structure. These remaining persistent inductive parasitics of the power/ground network impedance eventually limit the decoupling behavior of the discrete decoupling capacitors at frequencies above the GHz range. Consequently, an embedded film capacitor (EFC) on a multilayer package or PCB is strongly suggested as a promising means of overcoming the limitations of discrete decoupling capacitors. The embedded film capacitor not only provides capacitance of low ESL, but also saves surface mounting area. Furthermore, it can eliminate the ESL of the power/ground network that is caused by the mounting pad and the power/ground traces for discrete decoupling capacitors. In addition, the ESL of the power/ground via can be significantly diminished by reducing the thickness of the capacitor film.

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H. Kim and J. Kim are with the Terahertz Interconnection and Package Laboratory, Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 305-701, Korea (e-mail: teralab@ee.kaist.ac.kr; http://tera.kaist.ac.kr).

B. K. Sun is with the Samsung Electro-Mechanics Co., Ltd., Chungcheongnam-Do, Korea 339-702 (e-mail: humchi.sun@samsung.com).

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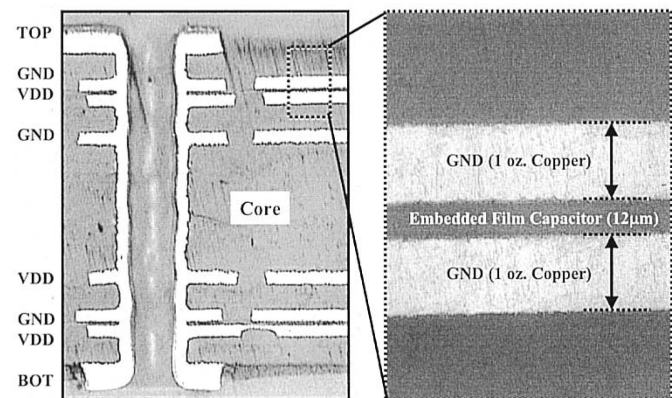

Fig. 1. SEM microphotograph of the cross section of the fabricated eight-layer PCB with the EFC (right: $500\times$ magnification; left: $50\times$ magnification).

We thoroughly investigated and demonstrated the great advantages of EFCs in reducing the power/ground inductive impedance and suppressing the SSN up to a frequency of 3 GHz. Eight-layer test PCBs were fabricated, and the inductive power/ground network impedances were measured as functions of the film thickness, the via distribution, and combined use with discrete decoupling capacitors, using a two-port self-impedance measurement [3]. This successfully demonstrated that the power/ground inductive impedance was significantly reduced from 270 pH to 106 pH simply by using an EFC rather than 16 discrete decoupling capacitors.

II. Fabricated Test PCB With EFCs

A scanning electron microscope (SEM) microphotograph of the fabricated test PCB is shown in Fig. 1. Two sets of EFCs are stacked in layers 2–3 and in layers 6–7. The film layers are placed near the top and bottom metal surface layers to minimize the ESL of the power/ground via to the device mounting pads

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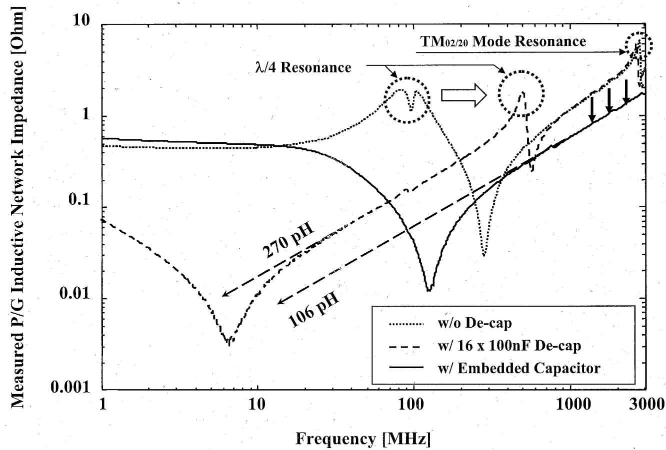

Fig. 2. Measured power/ground inductive impedance curves. The curves are: without any decoupling capacitor (dotted line); with only discrete capacitors (dashed line); and with only the EFC (solid line) inside the PCB.

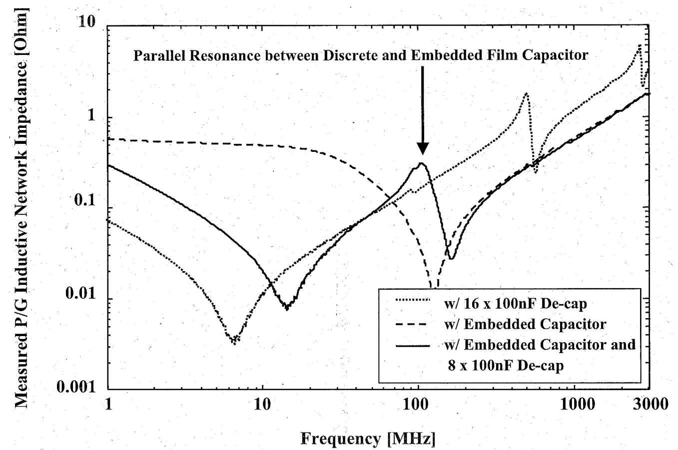

Fig. 3. Measured power/ground inductive impedance curves with respect to the different combinations of embedded film and discrete decoupling capacitors. The curves are: for discrete decoupling capacitors only (dotted line); for the EFC (dashed line); and for combined use of the embedded film and discrete decoupling capacitors (solid line).

on those layers. The vertical dimensions of the test PCBs are designed symmetrically to improve mechanical stability. The size of the test PCB was 5 cm by 5 cm with FR-4 as a dielectric material, and the dielectric permittivity of the embedded film was 4.1. Test PCBs with EFCs of different thicknesses (12 μm, 25 μm, and 50 μm) were used to investigate the effect of the embedded film thickness on the inductive power/ground impedance. Furthermore, to verify the via distribution effect on the power/ground impedance, test PCBs were designed and measured with three different via distributions (center-oriented, uniform, and hybrid) as shown in Fig. 6(a). The diameter of each power/ground via was 250 μm, and they had staggered connections to the power and ground planes. Eighteen pairs of the power/ground vias were placed on each test PCB for the center-oriented and uniform distributions, and 34 pairs for the hybrid distribution.

III. Measurement and Discussion

A two-port self-impedance measurement method was used for accurate and reliable measurement of the milliohm-scale impedance of the power/ground network of the test PCBs [3]. Graphs of the measured power/ground inductive network impedance curves are shown in Fig. 2, for the three different cases. As shown in the figure, the discrete capacitors exhibited a decoupling role at frequencies below 100 MHz compared to the bare test board without decoupling capacitors. The $\lambda/4$ resonance frequency was shifted upwards to approximately 500 MHz. This $\lambda/4$ parallel resonance occurs because of the parallel resonance between the dc power supply inductance and the power/ground plane capacitance. At higher frequencies, the $\lambda/4$ resonance can be precisely explained as a resonance when the $\lambda/4$ length is equal to the length between a short-circuit boundary, produced by the dc power supply, and the PCBs open-edge boundary. Although 16 discrete decoupling capacitors were used, the power/ground inductive impedance was 270 pH and the $\lambda/4$ resonance peak and TM02/20 mode resonances remained.

Conversely, by using the EFC, we demonstrated a significant reduction of the power/ground inductive impedance at frequencies up to 3 GHz, as shown in Fig. 2. The power/ground inductive impedance was reduced from 270 pH to 106 pH using the EFC. It is believed that the main cause of the reduction in the inductive impedance is the elimination of the ESL from the power/ground via, trace, and mounting pad. Furthermore, astonishingly, the $\lambda/4$ resonance and the TM02/20 mode resonance disappeared. Therefore, this proved that the EFC is the most effective method of suppressing the SSN at clock harmonic frequencies. Although we used EFCs of higher dielectric constant than the 4.1 of the current experiments, the inductive impedance of 106 pH was not reduced. However, the serial resonance that appears at approximately 100 MHz was shifted to a lower frequency range. The major source of the inductive impedance in the GHz frequency range is the inductive current path, and it is not related to the dielectric constant of the film.

On the other hand, for SSN caused by the output drivers of random data synchronized with a clock, the switching current spectrum extends far below the clock frequency, below 50 MHz. For this it is natural to use conventional discrete decoupling capacitors together with the EFC. The measured impedance graph for combined use of the EFC with the discrete capacitors is shown in Fig. 3. A significant high impedance peak was observed near 100 MHz. This peak was generated by a parallel resonance of the discrete decoupling capacitors' ESL and the capacitance of the EFC. Careful selection of the discrete capacitors is required to avoid this large SSN spectrum near the resonance frequency. If the major SSN concern is the harmonic frequency of the clock, the thin EFC alone is sufficient, without the use of the discrete decoupling capacitors.

The measured time-domain SSN waveforms excited by a high-current 50 MHz clock driver, and their frequency spectrums, are illustrated in Fig. 4. As shown in the graphs, the peak envelope of the SSN spectrum follows the measured impedance curve at the clock harmonic frequencies.

We also investigated experimentally the power/ground inductive impedance as a function of the thickness of the EFC, as shown in Fig. 5. In the high-frequency range above 1 GHz, we confirmed that a thinner film capacitor produces less inductance, aided by reduced via height and reduced plane inductance. By changing the film thickness, the effective inductance changes from 160 pH to 106 pH. Furthermore, we measured the power/ground impedance with variation of the power/ground

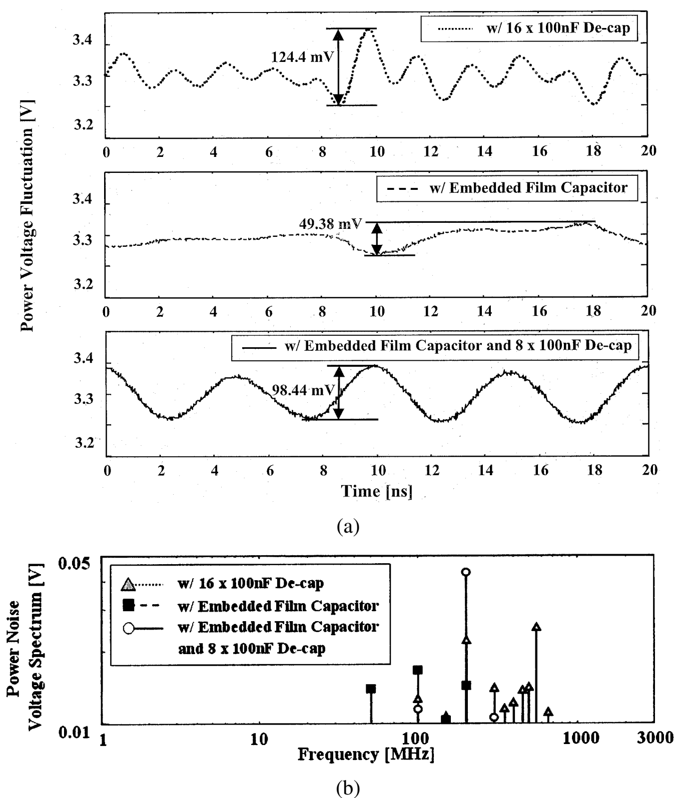

Fig. 4. Measured (a) SSN noise and (b) digital noise spectrum with a 50 MHz clock, with respect to the different combinations of embedded film and discrete decoupling capacitors in the multilayer PCB.

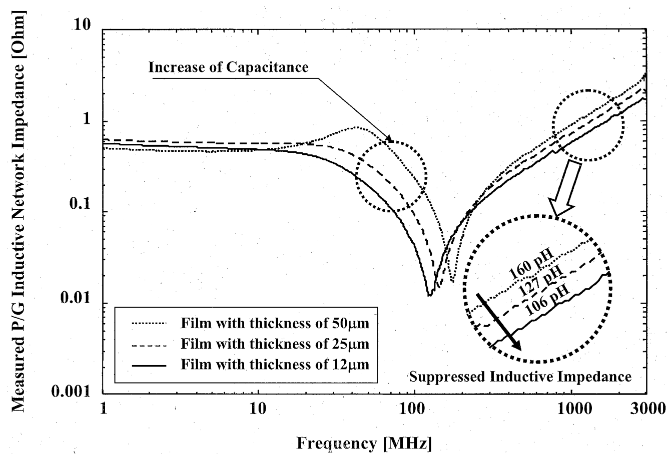

Fig. 5. Measured power/ground inductive impedance curves with respect to different capacitor film thicknesses inside the multilayer PCB (dotted line: 50 μm; dashed line: 25 μm; solid line: 12 μm).

via distribution as shown in Fig. 6. It was found that the hybrid via distribution has the lowest inductance. Little difference was observed between the hybrid and center-oriented via distributions. It was noted that the vias that made the greatest contribution to the low inductive current path were those adjacent to the center (the measurement probe point). This is because a via far from the center has additional inductance due to the current path through the power/ground plane. In the case of the uniform via distribution in Fig. 6(a), a small resonance peak was observed near 600 MHz. The parallel resonance is produced by the resonance between the ESL of the EFC in layers 6–7 and the capacitance of the EFC in layers 2–3.

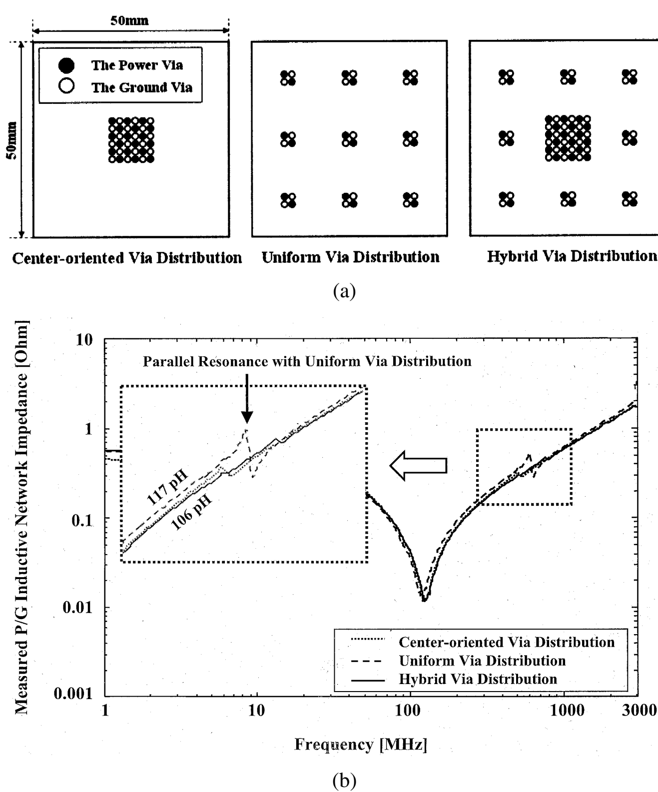

Fig. 6. (a) Three different via distributions on the multilayer PCB with the EFC for impedance and SSN measurements (left: center-oriented via distribution; center: uniform via distribution; right: hybrid via distribution). (b) The measured power/ground inductive impedance curves for the three different via distributions as depicted in (a).

IV. Conclusion

The use of an EFC is a promising method of suppressing power/ground inductive network impedance and simultaneous switching noise in multilayer packages and PCBs. This is mainly because the EFC provides a low inductance current path by removing the parasitic inductance from the discrete decoupling capacitors, the mounting pads, the power/ground traces, and the power/ground vias. This behavior becomes particularly effective at frequencies above the GHz range, where the discrete decoupling capacitor is no longer effective. Although the EFC requires additional power/ground layers inside the package and the PCB, thus increasing the cost, it is a uniquely effective solution to the problem of reducing the power/ground network impedance and the SSN in the GHz range. Otherwise, a large number of discrete decoupling capacitors need to be located near the chip in a circle of a limited radius, which is impractical and occupies considerable board area.

References

[1] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, “Power distribution system design methodology and capacitor selection for modern CMOS technology,” *IEEE Trans. Adv. Packag.*, vol. 22, Aug. 1999.

[2] M. Xu, T. H. Hubing, J. Chen, T. P. Van Doren, J. L. Drewnial, and R. E. DuBroff, “Power-bus decoupling with embedded capacitance in printed circuit board design,” *IEEE Trans. Electromag. Compat.*, vol. 45, pp. 22–30, Feb. 2003.

[3] I. Novak, “Measuring milliohms and picohenrys in power-distribution networks,” in *2000 High-Performance System Design Conf.*, Santa Clara, CA, 2000.