

Suppression of Line Voltage Related Distortion in Current Controlled Grid Connected Inverters

Tusitha Abeyasekera, C. Mark Johnson, *Member, IEEE*, David J. Atkinson, and Matthew Armstrong

Abstract—The influence of selected control strategies on the level of low-order current harmonic distortion generated by an inverter connected to a distorted grid is investigated through a combination of theoretical and experimental studies. A detailed theoretical analysis, based on the concept of harmonic impedance, establishes the suitability of inductor current feedback versus output current feedback with respect to inverter power quality. Experimental results, obtained from a purpose-built 500-W, three-level, half-bridge inverter with an L - C - L output filter, verify the efficacy of inductor current as the feedback variable, yielding an output current total harmonic distortion (THD) some 29% lower than that achieved using output current feedback. A feed-forward grid voltage disturbance rejection scheme is proposed as a means to further reduce the level of low-order current harmonic distortion. Results obtained from an inverter with inductor current feedback and optimized feed-forward disturbance rejection show a THD of just 3% at full-load, representing an improvement of some 53% on the same inverter with output current feedback and no feed-forward compensation. Significant improvements in THD were also achieved across the entire load range. It is concluded that the use of inductor current feedback and feed-forward voltage disturbance rejection represent cost-effect mechanisms for achieving improved output current quality.

Index Terms—Feed-forward voltage disturbance rejection, total harmonic distortion (THD).

NOMENCLATURE

V_{in}	Inverter output voltage.
V_{grid}	Grid voltage.
V_c	Filter capacitor voltage.
$V_{L/R}$	Inductor voltage drop.
I_{ind}	Inductor current.
I_{out}	Output current.
$C1, C2$	DC link capacitors.
L, L'	Filter inductance.
R, R'	Filter internal resistance.
K	Loop gain.
K_I	Integral constant.
K_P	Proportional constant.
Z_{in}	Harmonic impedance.

ω_s	Grid frequency.
N	Harmonic number.
GCI	Grid connected inverter.
THD	Total harmonic distortion.
DPLL	Digital phase locked loop.
FPGA	Field-programmable gate array.

I. INTRODUCTION

IN RECENT years, there has been a marked increase in the number of embedded power sources connected to the power grid. These include variable speed wind turbines, gas-turbine powered generators, fuel-cell units, and photovoltaic arrays. All of these power sources require inverters, either to convert dc to ac power or for frequency conversion. In addition, the availability of high power switching devices has facilitated increases in the capacity of individual grid-connected, inverter-based power sources to levels of over 1 MVA [1]. Connection of the increasing numbers of higher power inverters to the grid has generated concerns regarding their effect on power quality and has stimulated research into the harmonic-related issues in power systems [2]–[5]. Standards such as IEEE 929-1988 [6] provide guidance on the levels of voltage and current harmonic distortion that may be introduced by the inverter itself but they assume an ideal sinusoidal source of specified source impedance. In many practical applications, particularly those with connections to weak or remote systems, the inverter is required to operate in the presence of a distorted grid voltage. Reference [5] presents a comprehensive study of frequently encountered problems such as interference, heating, device malfunctions, capacitor bank failure, and breakdown in cable insulation. However, it is only relatively recently that the effects of a distorted supply on the performance of current-controlled, grid-connected inverters (GCIs) have begun to be investigated [7], [8].

This paper investigates the influence of a distorted line voltage on the level of low-order harmonic distortion occurring in current-controlled, GCIs. Section II provides an overview of the sources and effects of harmonic distortion while Section III introduces a mathematical model for the GCI and the concept of harmonic impedance [8]. In Section IV, a detailed control system analysis of a current-controlled GCI system is presented. The concept of harmonic impedance is extended to analyze the effect of the position of the feedback current sensor on the inverter power quality. An experimental verification of the theoretical analyses is presented in Section V, using results obtained from a purpose-built three-level prototype inverter system. Section VI describes a feed-forward disturbance-rejection controller which is shown to further reduce the level of

Manuscript received July 27, 2004; revised February 18, 2005. This work was supported by the U.K. Engineering and Physical Research Council (EPSRC), the Intelligent Power System Ltd (IPS), Gateshead, U.K., the Royal Academy of Engineering, and Rolls-Royce, plc. Recommended by Associate Editor V. Staudt.

T. Abeyasekera, D. J. Atkinson, and M. Armstrong are with the Power Electronics Drives and Machines Group, School of Electrical Electronic and Computer Engineering, University of Newcastle upon Tyne, Newcastle upon Tyne NE1 7RU, U.K.

C. M. Johnson is with the Department of Electronic and Electrical Engineering, University of Sheffield, Sheffield S1 3JD, UK (e-mail: c.m.johnson@sheffield.ac.uk).

Digital Object Identifier 10.1109/TPEL.2005.857557

low-order current harmonics. Final results confirm the accuracy of the models used and demonstrate that improved control systems can yield an overall reduction of up to 53% in the level of low-order harmonics without introducing additional system hardware.

II. SOURCES OF INVERTER HARMONIC DISTORTION

Inverter-related distortion can be divided into low-order and high-order harmonic regions of the frequency spectrum. High-order harmonic distortion is primarily associated with the inverter switching frequency harmonics. The widely used unipolar pulsewidth modulation (PWM), with its effective doubling of the switching frequency, pushes the lowest harmonics (in the idealized case) to sidebands grouped around twice the switching frequency [8]. Provided the switching frequency is high enough, the attenuation of these high-order harmonics occurs naturally as a consequence of the filtering effect of the predominantly inductive power grid. For other high-order harmonics, passive output filters are a cost-effective means of suppressing inverter-generated distortion, whether arising from grid voltage distortion or from control-loop deficiencies. In such cases, it is also possible to make effective use of the leakage inductance and winding capacitance of any isolating transformer. Low-order harmonics, on the other hand, are not attenuated by the natural filtering effect of the grid inductance and require bulky and costly output filters for their removal if a conventional passive filter is employed. It is thus common to rely on the inverter current control loop to reduce low-order harmonics to an acceptable level.

Although there are several potential schemes that can be adopted in the control of GCIs, a common strategy is to attempt to force a sinusoidal current into the grid regardless of the grid voltage waveform. Under these conditions, low-order harmonic distortion of the actual current can occur as a result of both intrinsic and extrinsic effects. Distortion generated intrinsically arises mainly from deficiencies in the inverter control loop, which result in an error between the sinusoidal reference and the actual inverter output. Some of the contributors to intrinsic low-order harmonic distortion are:

- 1) non-linear effects due to dead time, device volt drops [10], [11]current limit, and filter choke saturation;
- 2) limited PWM resolution;
- 3) finite loop time;
- 4) finite loop gain;
- 5) measurement inaccuracies;
- 6) lack of stiffness in the dc link resulting in excessive current ripple.

Extrinsic sources of low-order harmonic distortion include the effects of connection to a weak and distorted grid. Here, the distorted grid voltage acts as an external disturbance, impeding the control task and resulting in a distorted output current. Previous experimental investigations have shown that even small levels of grid voltage distortion can result in significant current distortion [7].

One method of improving the low-order harmonic rejection capability of the control loop would be to increase the bandwidth of the proportional integral (PI) controller, for example

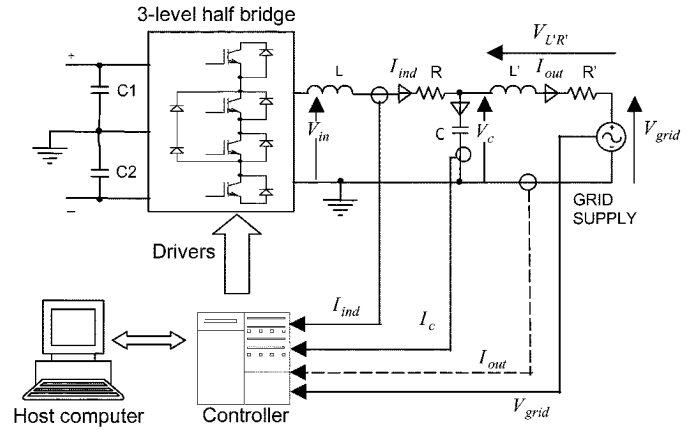


Fig. 1. GCI system with $L-C-L$ filter.

TABLE I
SYSTEM PARAMETERS

Utility voltage	50 V rms, 50 Hz
DC link voltage	$\pm 100V$
DC link capacitance C1, C2	2530 μF
Inductor L	1.2 mH
Inductor L'	0.5 mH
Filter capacitor C	20 μF
Resistance R, R'	0.5 Ω
Sample frequency, f_s	13.15 kHz
Effective switching frequency, f_{switch}	26.3 kHz

by increasing the proportional and/or integral gain. Twinning *et al.* [8] showed that although current distortion will decrease as the system bandwidth increases, system stability requirements will ultimately determine the upper bandwidth limit. Increased system bandwidth also decreases the noise immunity of the system. It is, therefore, worthwhile investigating alternative control system modifications which realize improved tracking and increased rejection of external voltage disturbances without additional hardware costs.

III. INVERTER SYSTEM MODEL

Fig. 1 shows a schematic diagram of the three-level half-bridge inverter system and $L-C-L$ output filter which together form the subject of this study. Salient parameters for the system are shown in Table I. A mathematical model describing the grid connected PWM inverter may be written in the following form:

$$V_{in} = V_c + L \frac{dI_{ind}}{dt} + RI_{ind} \quad (1)$$

$$V_c = V_{grid} + L' \frac{dI_{out}}{dt} + R'I_{out} \quad (2)$$

$$I_c = C \frac{dV_c}{dt} \quad (3)$$

$$I_c = I_{ind} - I_{out} \quad (4)$$

Assuming the switching frequency is high enough to neglect the inverter dynamics (the effective value is 26.3 kHz due to unipolar modulation), a block diagram of the equivalent circuit based on (1)–(4) may be constructed as shown in Fig. 2. Note

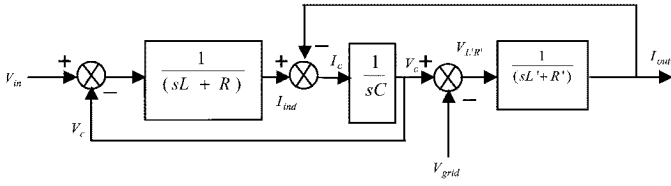
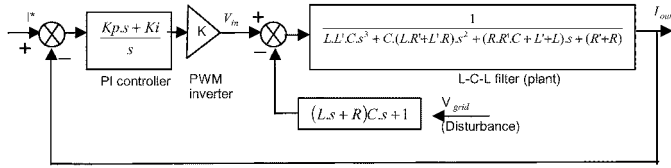

 Fig. 2. Control system block diagram of $L-C-L$ output filter (plant).


Fig. 3. Reduced-order system with PI output current control.

that the supply inductance is neglected, as it is much smaller than the filter inductance.

With some manipulation, the above system may be reduced to a third-order plant and an external disturbance with the output current, I_{out} , controlled by a PI controller, as shown in Fig. 3. For simplicity of analysis, PWM inverter is represented by a gain (K) which is reasonable for this case, where the switching frequency is relatively high.

A. Concept of Harmonic Impedance

Twinning *et al.* [8] showed that the sensitivity of an inverter control system to grid voltage harmonics can be investigated by calculating its “harmonic impedance” (Z_{in}), i.e., the relationship between an applied harmonic voltage disturbance and the resulting harmonic current. High harmonic impedance will result in a relatively small harmonic current in response to a harmonic voltage disturbance and it is thus a useful measure of the system’s disturbance rejection capability. The harmonic impedance of a GCI system with output current feedback is given by (5), shown at the bottom of the page.

IV. CHOICE OF FEEDBACK CURRENT: INDUCTOR CURRENT VERSUS OUTPUT CURRENT

Most commercially available GCIs use either the inductor current (I_{ind}) or the output current (I_{out}) as the controlled quantity, the choice normally being made on cost grounds. For example, some inverters use one current sensor to sense inductor current for both over current protection and current control. However, the authors have not found any definitive suggestion in the literature supporting the location of current measurement

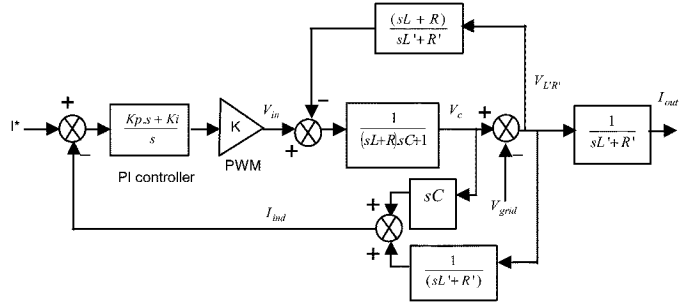
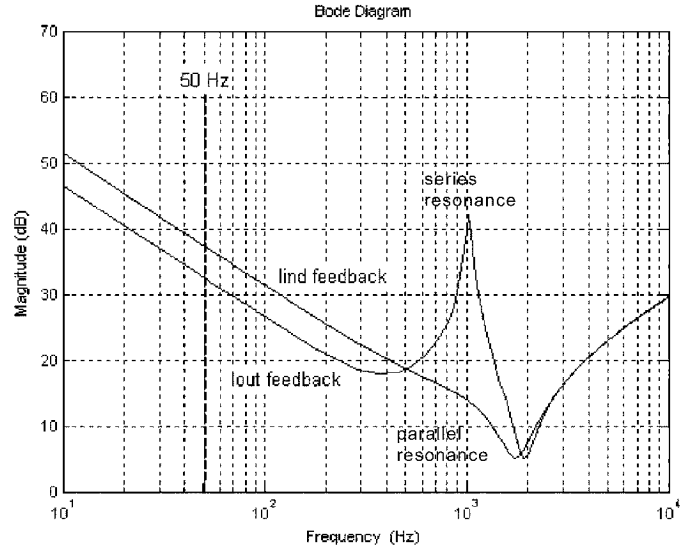


Fig. 4. Overall control diagram of the GCI with inductor current feedback.


 Fig. 5. Bode plot comparing the magnitude of the harmonic impedance, Z_{in} , with inductor current (I_{ind}) and output current (I_{out}) feedback.

with respect to the quality of power produced by the inverter. The following section is, therefore, dedicated to analyzing the inverter control system with inductor current (I_{ind}) as opposed to output current (I_{out}) as the controlled quantity, and explains why the former is better in terms of injected power quality.

The control system of Fig. 3 may be modified to use inductor current feedback, as shown in Fig. 4 and the corresponding harmonic impedance for the control system is then given by (6), shown at the bottom of the page. Fig. 5 shows a Bode plot comparing the harmonic impedance for both inductor current and output current feedback. The controller parameters, K_P and K_I , were chosen to minimize both the RMS error at the fundamental and the total harmonic distortion under steady state conditions, while maintaining stability. Values of $K_P = 0.076, 0.028 \text{ VA}^{-1}$ and $K_I = 215, 66.5 \text{ VA}^{-1}\text{s}^{-1}$ were used to tune the system for inductor current and output

$$Z_{in_{i_{out}}} = \frac{V_{grid}}{I_{out}} \Big|_{I_{out}} = - \left[\frac{L.L'.C.s^4 + C.(L.R' + L'.R).s^3 + (R.R'.C + L' + L).s^2 + (R' + R + K.K_P).s + K_I.K}{L.C.s^3 + R.C.s^2 + s} \right] \quad (5)$$

$$Z_{in_{ind}} = \frac{V_{grid}}{I_{ind}} \Big|_{I_{ind}} = - \left[\frac{L.L'.C.s^4 + C.(L.R' + L'.R + K_p.K.L')s^3 + (C.(R.R' + K_p.K.R' + K_I.K.L') + L' + L).s^2 + (R' + R + K.(C.K_I.R' + K_p))s + K_I.K}{L.C.s^3 + (R + K_p.K_I).C.s^2 + (1 + C.K_I.K)s} \right] \quad (6)$$

current feedback respectively. At low frequencies the harmonic impedances given by (5) and (6) are well approximated by a first-order system

$$Z_{in_{ind}} = \left. \frac{V_{grid}}{I_{out}} \right|_{I_{ind}} \approx \frac{KK_I}{s(1 + KK_I C)} \quad (7)$$

$$Z_{in_{i_{out}}} = \left. \frac{V_{grid}}{I_{out}} \right|_{I_{out}} \approx \frac{KK_I}{s}. \quad (8)$$

Thus, for both feedback schemes, the harmonic impedance is determined by the integral gain, K_I , of the controller. At higher frequencies, the behavior is determined by resonances associated with the LCL output filter. The denominators of (5) and (6) exhibit a pole-pair (series resonance), which in the absence of damping effects, has a resonant frequency $f_s = (1)/(\sqrt{LC})$. Its effect is particularly noticeable in the case of output current feedback, where there is little damping, and results in a sharp peak in the harmonic impedance at a frequency of just over 1 kHz. For inductor current feedback, the additional damping term resulting from the proportional feedback eliminates this peak. The numerators of (5) and (6) are dominated by a pair of zeros (parallel resonance) whose center frequency is well-approximated by $f_p = (\sqrt{L+L'})/(\sqrt{LL'C})$ resulting in a minimum in the harmonic impedance close to 1.7 kHz. This is clearly evident with both inductor and output current feedback (see Fig. 5).

The numerators of (5) and (6) are also the characteristic equations for the control system and may thus be examined to determine the stability limits for the two feedback schemes. Applying the Routh–Hurwitz stability criteria in the case of output current feedback yields the following inequalities, which determine the upper bounds for the proportional and integral gain (the proportional gain is assumed to be zero when determining the limit for integral gain):

$$(LR' + L'R)CRR' + L^2R + L^2R' - LL'KK_P > 0 \quad (9)$$

$$\begin{aligned} & ((LR' + L'R)CRR' + L^2R + L^2R')C(R + R') \\ & - C^2(LR' + L'R)^2KK_I > 0. \end{aligned} \quad (10)$$

In the case of inductor current feedback, the equivalent of (9) shows that the system is unconditionally stable to increases in proportional gain whatever the system parameters. The equivalent of (10) is:

$$\begin{aligned} & ((LR' + L'R)CRR' + L^2R + L^2R')C(R + R') \\ & + C^2RR'(2L^2 - 2LL' + CR'(LR' + L'R))KK_I \\ & + L^2RR'C^3(KK_I)^2 > 0. \end{aligned} \quad (11)$$

For the system parameters of Table I, (11) has no real roots and the system is therefore unconditionally stable for all values of integral gain. It is possible to reach a condition where the system is potentially unstable by increasing the capacitance, although in the case exemplified here this would require a capacitance value of 50 mF.

From the foregoing analysis, it is clear that the system with inductor current feedback is inherently more stable than that with output current feedback. It is therefore possible to operate the inductor current feedback scheme with a higher integral gain,



Fig. 6. Photograph of the experimental rig.

K_I , yielding a higher harmonic impedance. For example, at 50 Hz the harmonic impedances for the systems shown in Fig. 6 are 100 Ω and 52.9 Ω for inductor current and output current feedback, respectively. Consequently, the inverter output current (I_{out}) can be expected to display lower harmonic distortion when using inductor current feedback.

V. EXPERIMENTAL VERIFICATION

A 500-W, three-level, prototype inverter was constructed with the control functions being implemented in a TMS320C31-based digital signal processing (DSP) system with acquisition electronics. A dedicated field-programmable gate-array (FPGA) was used to generate the single-edged PWM signals whose carrier was synchronized with the interrupt service routine (ISR). A rectified three-phase supply, controlled through a variac, provided the split rail ± 100 VDC link while the laboratory supply (harmonic spectrum shown in Fig. 11) was used to represent the grid throughout the investigation. The harmonic content of the laboratory supply was observed over a number of weeks and was found to be stable with only small (typically less than the resolution of the spectrum analyzer) variations in individual harmonic levels being observed. Synchronization of the inverter current to the grid voltage was achieved by a digital phase locked loop (DPLL) designed and programmed for optimum dynamic performance. The dc-link voltage ripple was minimized by employing relatively large dc-link capacitors. A simple dead-time compensation scheme [9], based on device volt drops, was implemented in software to minimize output current nonlinear distortion. For both inductor and output current feedback, base values of control parameters were found through simulation using a RMS error criterion and then fine-tuned in real time for optimum performance.

Figs. 7 and 8 show, respectively, the measured inverter output currents with inductor current and output current feedback while Figs. 9 and 10 show the corresponding harmonic spectra with harmonic numbers shown. Odd harmonics from third, through 15th are seen to dominate both spectra although the higher-order odd harmonics are clearly attenuated when using inductor current feedback. The overall THD with inductor current feedback

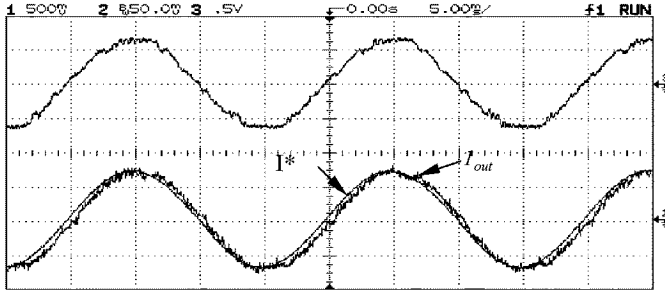


Fig. 7. Inverter output current I_{out} with output current I_{out} feedback. Time-base: 5 ms/div., trace2: inverter output current 5 A/div., trace3: Grid voltage 59 V/div.

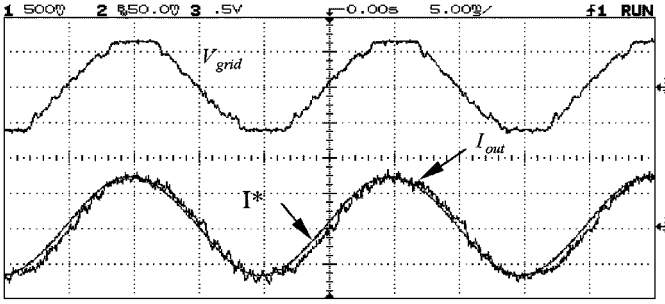


Fig. 8. Inverter output current I_{out} with inductor current I_{ind} feedback. Time base: 5 ms/div., trace2: inverter output current 5 A/div., trace3: Grid voltage 59 V/div.

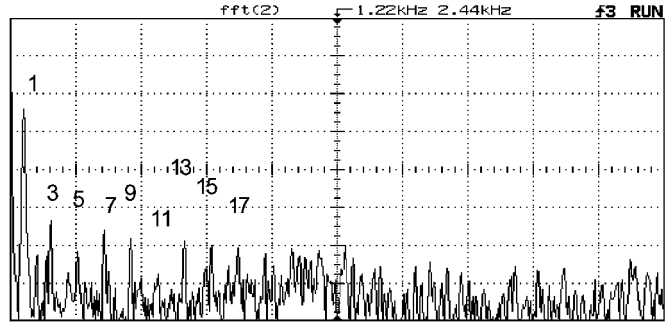


Fig. 9. FFT of inverter output current (I_{out}) with output current I_{out} feedback. THD = 6.4%. Frequency base: 244 Hz/div., vertical scale: 10 dB/div., sampled at 5 kHz.

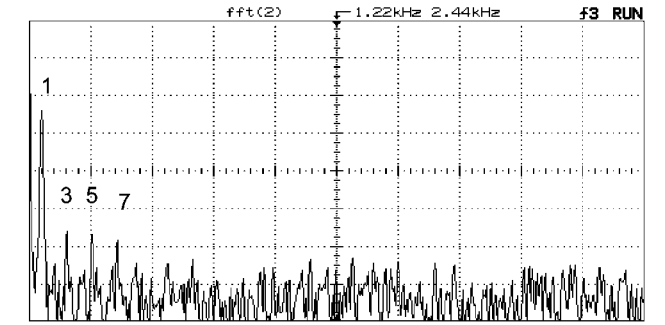


Fig. 10. Fast Fourier transform (FFT) of inverter output current (I_{out}) with inductor current I_{ind} feedback. THD = 4.5%. Frequency base: 244 Hz/div., vertical scale: 10 dB/div., sampled at 5 kHz.

is calculated to be 4.5% compared to 6.4% with output current feedback, representing a reduction of 29.6%. This result amply justifies the use of inductor current (I_{ind}) as the controlled quantity.

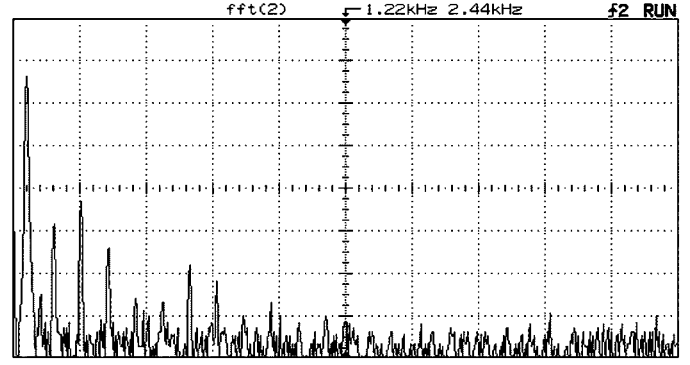


Fig. 11. Grid voltage harmonic spectrum. THD = 5.4%. Frequency base: 244 Hz/div., vertical scale: 10 dB/div., sampled at 5 kHz.

VI. IMPROVED DISTURBANCE REJECTION THROUGH FEED-FORWARD

In the previous section it was seen that although the harmonic content is reduced with the inductor feedback scheme, there is still an error between the fundamental frequency signals of the reference I^* and I_{out} (see Figs. 7 and 8). This is due in part to the distorted grid voltage but is also influenced by the finite loop delay inevitable in the digitally implemented control loops. A technique commonly used for improving the performance of the control loop is to introduce a feed-forward term which compensates for the effect of one or more system disturbance terms. In the case of a GCI, feed-forward compensation of the grid voltage, V_{grid} , is effective in reducing the control effort and thus can be expected to lead to further reductions in harmonic content. This section considers the introduction of suitable feed-forward term for a GCI with a $L-C-L$ output filter.

A. Feed-Forward Controller Design

A feed-forward method is proposed which uses the knowledge of the external disturbance, V_{grid} , to predict the control effort required to cancel it. Although this method is widely used in control applications, its application to GCIs with $L-C-L$ filtering is believed to be novel. In this implementation two methods are investigated for obtaining the feed-forward term: one based on the actual grid voltage V_{grid} and one based on the output filter capacitor current, I_c . In the latter case, I_c is used to provide an estimate for the time derivative of grid voltage.

Consider the system shown in Fig. 12 in which the block diagram symbols represent the following transfer functions:

$$A = \frac{1}{(sL + R)sC + 1} \quad D = \frac{sL + R}{sL' + R'}$$

$$B = \frac{1}{sL' + R'} \quad W = \frac{K_{PS} + K_I}{s}$$

$$C' = sC.$$

W_{ff} and α represent the transfer functions for grid voltage and capacitor current feed-forward.

Using the block diagram notation of Fig. 12 we can write

$$V_c = A(V_{in} - DV_{L'R'}) \quad (12)$$

$$V_c = V_{L'R'} + V_{grid} \quad (13)$$

$$I_{out} = B(V_c - V_{grid}) \quad (14)$$

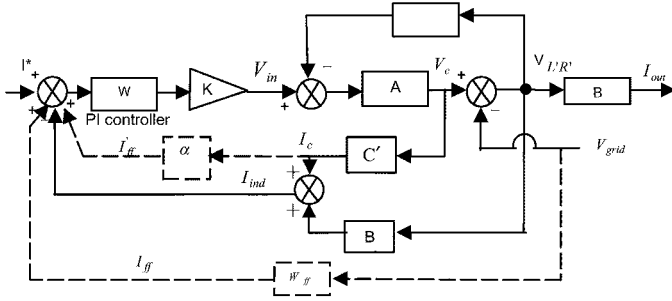


Fig. 12. Control system block diagram of the GCI with inductor current feedback showing options for disturbance feed-forward (marked using dashed lines).

$$V_i = WK(I^* - I_{ind} + I_{ff}) \quad (15)$$

$$I_{ind} = C'V_c + BV_{L/R'} \quad (16)$$

where the feed-forward term is.

After some manipulation, an expression for I_{out} can be found in terms of the current demand I^* , feed-forward term, and I_{ff} grid voltage (the disturbance) V_{grid}

$$I_{out} = B \frac{AWK(I^* + I_{ff}) - (AWKC' + 1)V_{grid}}{1 + A(B + C')WK + AD}. \quad (17)$$

The objective is to find W_{ff} such that V_{grid} is eliminated from I_{out} , a condition that is satisfied when

$$I_{ff} = \frac{AWKC' + 1}{AWK} V_{grid} = W_{ff} V_{grid}. \quad (18)$$

Substituting for the block diagram symbols

$$I_{ff} = \frac{sCWK + sC(sL + R) + 1}{WK} V_{grid} \quad (19)$$

and with feed-forward applied, the output current becomes

$$I_{out}|_{V_{grid}} = \frac{AWKI^*}{1 + A(B + C')WK + AD}. \quad (20)$$

Equation (20) shows that disturbance voltage V_{grid} is eliminated from the inverter output current I_{out} .

However multiple differentiation is needed (19) to synthesise the feed-forward term I_{ff} . In practice, this is difficult to implement, due to significant amplification of measurement noise inevitably present when acquiring the grid voltage, and an alternative method is therefore sought to reduce the influence of grid voltage on output current.

B. Feed-Forward Using Capacitor Current

For moderate frequencies and large values of WK , (19) can be approximated by

$$I_{ff} \approx sCV_{grid}. \quad (21)$$

It is thus reasonable to consider whether the capacitor current I_c can be used to provide a suitable approximation to the feed-forward term I_{ff} . Writing

$$I'_{ff} = \alpha I_c = \alpha C' V_c = \alpha C' (V_{L/R'} + V_{grid}) \quad (22)$$

and substituting into the block diagram of Fig. 12 gives, after some manipulation

$$I_{out}|_{I_x} = B \frac{AWKI^* - (AWKC'(1 - \alpha) + 1)V_{grid}}{1 + A(B + C'(1 - \alpha))WK + AD}. \quad (23)$$

An interesting observation is that when $\alpha = 1$ the situation is reduced to that obtained for output current feedback since the feed-forward term exactly cancels the contribution of I_c to I_{ind} (see Fig. 12)

$$I_{out}|_{I_c} = \frac{ABWKI^* - BV_{grid}}{1 + ABWK + AD}. \quad (24)$$

It is thus possible to vary the loop characteristic from that of output current feedback to inductor current feedback, with or without feed-forward simply by altering the value of α .

From a disturbance immunity perspective, the objective is to eliminate V_{grid} from I_{out} . The value of α which completely suppresses grid voltage effects can be determined from (23)

$$\alpha = 1 + \frac{1}{AWKC'} = 1 + \frac{sC(sL + R) + 1}{KC(sK_P + K_I)}. \quad (25)$$

Under these conditions the output current becomes

$$I_{out}|_{I_c} = \frac{BWKI^*}{BWK + D}. \quad (26)$$

It is clear from (25) that α is frequency dependant and thus full implementation of the feed-forward scheme would require a multiterm transfer function representation. However, for simplicity and convenience of implementation in a real-time environment, a simple gain was selected for α . It is clearly possible to define a number of values for α , depending on the user requirements to suppress low, moderate or high-frequency grid-voltage disturbance components from the output current. For frequencies below the corner frequency of the output filter the appropriate value of α is given by

$$\alpha \approx 1 + \frac{1}{CKK_I} \quad (27)$$

while for moderate frequencies

$$\alpha \approx 1 + \frac{R}{KK_P} \quad (28)$$

and for high frequencies

$$\alpha \approx 1 + \frac{sL}{KK_P}. \quad (29)$$

The inclusion of the time derivative term in (29) excludes its direct practical implementation and with it higher-order harmonic

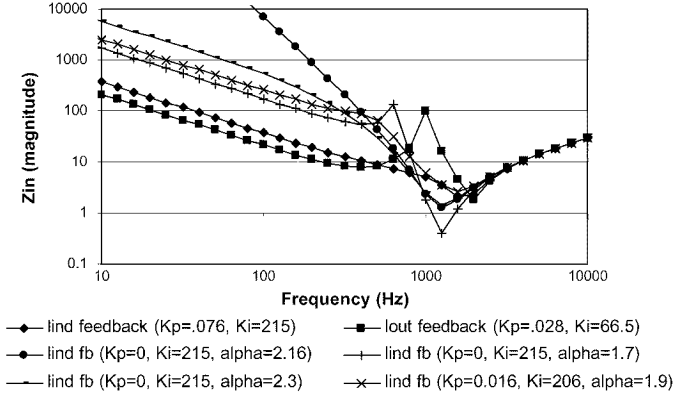


Fig. 13. Magnitude of harmonic impedance for various values of feed-forward parameter, α .

suppression. However, the output filter and line impedance is expected to provide adequate suppression of these higher-order harmonics.

C. Optimization of Feed-Forward Parameters

The theoretical harmonic impedance obtained for fixed-gain capacitor-current feed-forward is given by (30), shown at the bottom of the page. As was identified previously, the parameter α can be used to alter the loop characteristic from inductor current feedback ($\alpha = 0$) to output current feedback ($\alpha = 1$) and so (5) and (6) may be recognized as specific cases of (30) corresponding to $\alpha = 0$ and $\alpha = 1$, respectively.

Fig. 13 shows the calculated effect of varying the feed-forward parameter, α on the harmonic impedance of a system with an integral gain of 215 and zero proportional gain. The results presented in Fig. 5 for inductor current and output current feedback without feed-forward are shown on the same axes for reference purposes. It is immediately clear that much better low-frequency disturbance rejection can be achieved by setting α close to the optimum low frequency value given in (27), which is in this case 2.16. This feed-forward term has the added benefit of reducing the steady state phase error at the fundamental frequency, as shown in Fig. 14.

D. Experimental Verification

The final system, incorporating inductor current feedback and capacitor current feed-forward, was implemented and tested in real time on the three-level inverter described previously. The capacitor current I_c , a sample of which is shown in Fig. 15, was acquired using a current sensor with signal conditioning circuitry to reduce high frequency noise. Tuning of the feed-forward controller was accomplished by first increasing the integral gain K_I close to the limit of stability. The feed-forward term, α , was then increased until it was just less than the theoretical optimum given by (27) before finally adjusting the proportional gain, K_P , to fine-tune the dynamic response. The optimized values adopted in the practical controller were: $K_I = 206$, $\alpha =$

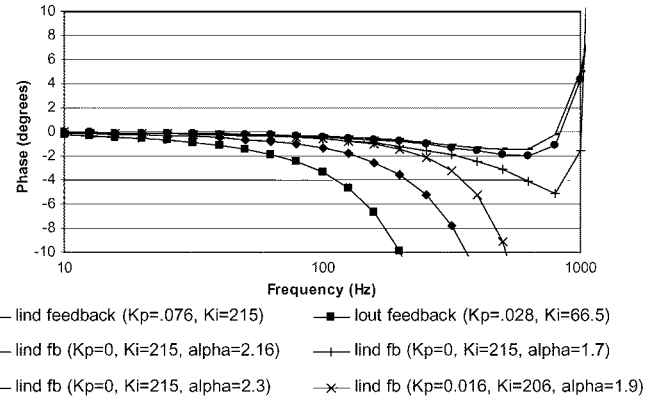


Fig. 14. Closed loop phase, as determined by (15), plotted for various values of feed-forward parameter α .

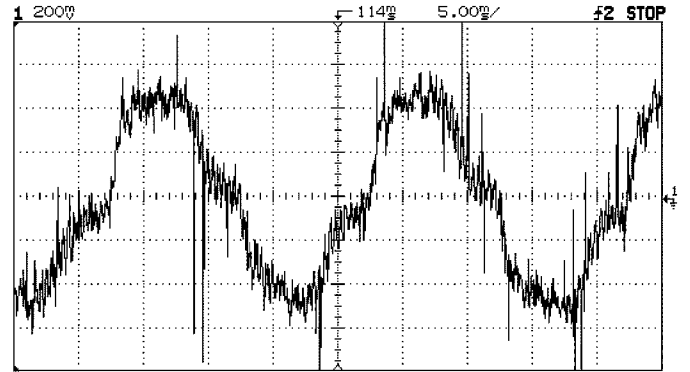


Fig. 15. Experimental feed-forward capacitor current.

1.9 and $K_P = 0.016$. Theoretical harmonic impedance and closed loop phase characteristics for the optimized controller are shown in Figs. 13 and 14, respectively.

Fig. 16 compares the measured current output with the simulation results before and after a step change in current demand and reveals a stable and rapid transient response. The close resemblance of the simulated and experimental waveforms demonstrates the accuracy of the adopted simulation model. Comparison of the results of Fig. 16 with those shown in Figs. 7 and 8 reveals a significant improvement in the controller's tracking ability (note the near zero phase-error between I^* and I_{out}). This is also reflected in the reduced low-order harmonic amplitudes in the harmonic spectrum which are evident by comparison of Fig. 17 with Figs. 9 and 10. The THD for the optimized feed-forward controller was calculated to be 3%, which is a reduction of 33.8% from the case without feed-forward (i.e., 4.5%). It is expected that using dc link compensation, which was avoided to minimize the number of transducers, the output current THD could be decreased further.

E. Effect of Feed-Forward Under Low Power Operation

A typical GCI is often required to operate at low demand, for example a PV inverter operating at partial insolation and

$$Z_{in}|_{I_c} = \frac{V_{grid}}{I_{out}} \Big|_{I_c} = - \left[\frac{L.L.C.s^4 + C.(L.R+L'.R+K_p.K.L'(1-\alpha)).s^3 + (C.(R.R'+(1-\alpha)(K_p.K.R+K_I.K.L))+L+L).s^2 + (R'+R+K.(1-\alpha)C.K_I.R+K_p)s + K_I.K}{L.C.s^3 + (R+K_p.K(1-\alpha)).C.s^2 + (1+C.K_I.K(1-\alpha))s} \right] \quad (30)$$

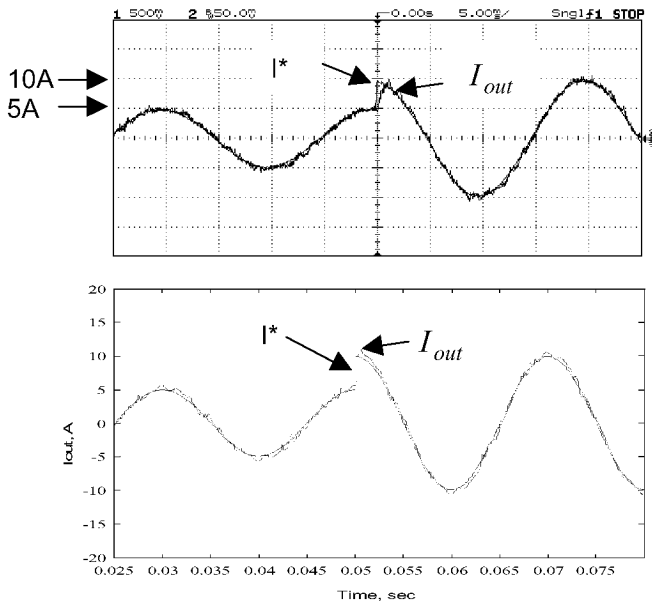


Fig. 16. Comparison of simulated (above) and experimentally obtained (below) inverter output current, I_{out} for a step change in demand (3.5–7 A RMS). Time base: 5 ms/div., trace1: inverter output current 5 A/div.

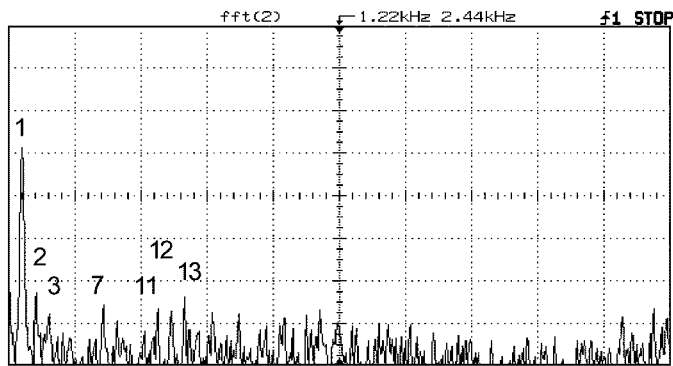


Fig. 17. Output current (I_{out}) harmonic spectrum for an output current of 5 A RMS (THD = 3%). Frequency base: 244 Hz/div., vertical scale: 10 dB/div., sampled at 5 kHz.

connected to the grid. Under these conditions the quality of the inverter output current waveform deteriorates, mainly due to finite PWM resolution. However, a component of distortion is also contributed by the presence of a distorted grid voltage. The results shown in Fig. 18 show the effect of feed-forward on the output current harmonic spectrum at lower current demand levels while Fig. 19 compares the THD as a function of output current. It is clear that the feed-forward compensation scheme is effective in reducing the levels of low-order harmonic distortion at low output current levels, as well as at a nominal full-load. It is therefore particularly well-suited to systems where operation at part-load can be expected as the norm.

VII. CONCLUSION

This paper has analyzed the influence of selected control strategies on the level of low-order harmonic distortion generated by an inverter connected to a weak and distorted grid. A detailed theoretical analysis, using a harmonic impedance concept, has been performed to establish the suitability of inductor

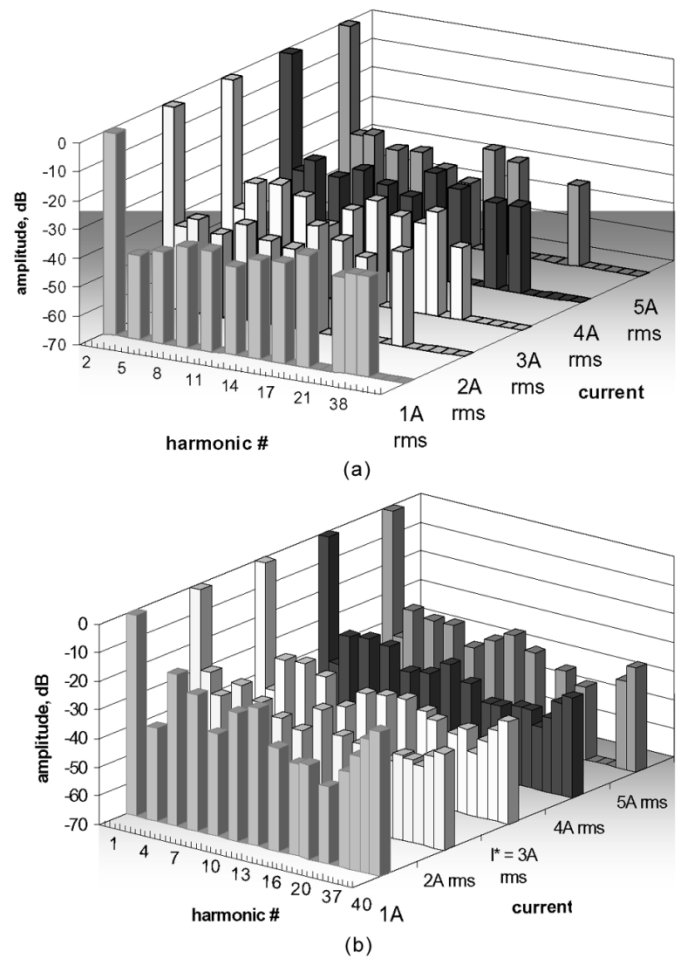


Fig. 18. Output current harmonic spectrum at various levels of current demand for feedback schemes (a) with and (b) without feed-forward compensation.

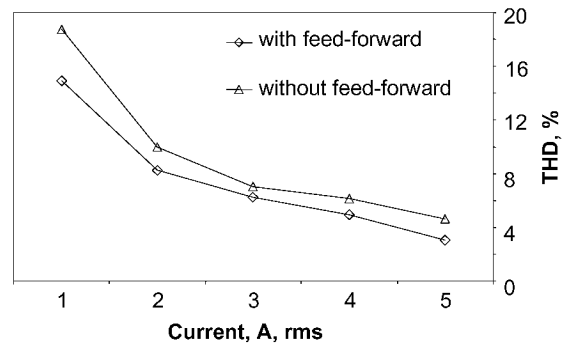


Fig. 19. Comparison of inverter output current THD as a function of output current with and without capacitor current feed-forward.

current versus output current feedback. Harmonic impedance functions for both cases have been derived and analyzed in the frequency domain, the results showing that inductor current feedback presented a much higher harmonic impedance and therefore greater capability for rejecting grid voltage harmonic distortion. Inductor current feedback also has the advantage of suppressing resonant peaks which are known to cause problems in inverters connected to weak grids. A 500-W three-level inverter system has been designed and constructed to verify the mathematical modeling and practical viability of the proposed

methods. The experimental results have shown that using optimized inductor current feedback yields an output current THD some 29% lower than that achieved using optimized output current feedback.

Further improvements to the inverter output current quality have been achieved through feed-forward disturbance rejection. A capacitor current feed-forward controller has been designed, simulated and implemented in real-time. Fine-tuning of an inverter with inductor feedback and capacitor current feed-forward disturbance rejection produced a very low THD, of just 3% at nominal full-load, representing an improvement of some 53% on the tuned converter with output current feedback and no feed-forward compensation. Significant improvements in THD were also achieved across the entire load range. The level of THD accomplished is well below the IEEE standard of 5% for grid interfaced inverters and is achieved with no substantial hardware costs (since it only requires one additional low cost current sensor for capacitor current measurement), thus justifying the commercial viability of the proposed methods.

REFERENCES

- [1] M. Prodanovič and T. C. Green, "Power quality improvement in grid connection of three-phase inverters," in *Proc. IEE Power Electronics, Machines Drives Conf. (PEMD)*, 2002, pp. 24–29.
- [2] R. Yakamini, "Power systems harmonics, part 3—Problems caused by distorted supplies," *Proc. Inst. Elect. Eng.*, pp. 223–238, 1995.
- [3] M. Armstrong, D. J. Atkinson, M. C. Johnson, and T. D. Abeyasekera, "Low order harmonic cancellation scheme for multiple PV grid-connected inverters," in *Proc. EPE'03 Conf.*, Toulouse, France, 2003, CD ROM.
- [4] T. D. Abeyasekera, C. M. Johnson, D. J. Atkinson, and M. Armstrong, "Elimination of subharmonics in direct look-up table (DLT) sine wave reference generators for low cost microprocessor-controlled inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1315–1321, Nov. 2003.
- [5] J. S. Subjak and J. S. Mcquillin, "Harmonics-causes, effects, measurements and analysis: An update," *IEEE Trans. Ind. Appl.*, vol. 26, no. 6, pp. 1034–1042, Nov./Dec. 1990.
- [6] *Recommended Practice for Utility Interface of Photovoltaic (PV) Systems*, IEEE Std. P929, Dec. 1998.
- [7] E. Twinning, "Modeling grid-connected voltage source inverter operation," in *Proc. AUPEC'01*, 2001, pp. 501–506.
- [8] E. Twinning and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power Electronics*, vol. 18, no. 3, pp. 888–895, May 2003.
- [9] N. Mohan, T. M. Underland, and W. P. Robbins, *Power Electronics, Converters, Applications, and Design*. New York: Wiley, 1989.
- [10] H.-S. Kim, K.-H. Kim, and M.-J. Youn, "On-line dead-time compensation method based on time delay control," *IEEE Trans. Contr. Syst. Technol.*, vol. 11, no. 2, pp. 279–285, May 2003.
- [11] J.-W. Choi and S.-K. Sul, "A new compensation strategy reducing voltage/current distortion in PWM VSI systems operating with low output voltages," *EEE Trans. Ind. Electron.*, vol. 31, no. 5, pp. 1001–1008, Oct. 1995.



Tusitha Abeyasekera received the M.Sc. degree (with honors) in electromechanical engineering from Kiev Polytechnic Institute, Kiev, Ukraine, in 1999 and the Ph.D. degree in power quality improvements for grid connected PV inverters from the School of Electrical Electronic and Computer Engineering, University of Newcastle Upon Tyne, Newcastle Upon Tyne, U.K., in 2005.

In Kiev, his work was focused on sliding mode control of induction motor drives. Since then he has been working with the Power Electronics, Drives and Machines Group, University of Newcastle Upon Tyne. He is currently involved in real time performance analysis of wind turbines under fault conditions. His main research interests are in inverter control for renewable energy and drive applications, power quality issues, nonlinear control, and multilevel inverters.



C. Mark Johnson (S'89–M'91) received the B.A. degree in engineering and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in 1986 and 1991, respectively.

From 1990 to 1992, he was a Research Associate at the University of Cambridge, investigating GTO thyristors for traction applications. In 1992, he was appointed Lecturer at the University of Newcastle upon Tyne, Newcastle Upon Tyne, U.K., where his research included the design, analysis, and characterization of power semiconductor devices, resonant power conversion, and instrumentation. From 1998 to 2001, he managed the UK national programme on silicon carbide electronics and in 2000 he became Reader of Power Electronics at the University of Newcastle Upon Tyne. In 2003, he was appointed as Research Professor of Power Electronic Systems in the Electrical Machines and Drives Research Group, University of Sheffield, Sheffield, U.K., where he leads research into power semiconductor devices, power device packaging, power module technologies, and power electronic applications. He is currently project manager for the UK Innovative Electronics Manufacturing Research Center Flagship Project in Power Electronics.



David J. Atkinson received the B.Sc. and Ph.D. degrees in electrical and electronic engineering from the University of Newcastle upon Tyne, Newcastle Upon Tyne, U.K., in 1978 and 1991, respectively.

He is currently a Senior Lecturer in the Drives, Power Electronics and Machines Group, Department of Electrical and Electronic Engineering, University of Newcastle upon Tyne. Prior to his university appointment Dr Atkinson had spent 17 years in the electronics industry including periods with NEI Electronics and British Gas Corporation. His research interests include electrical drive systems, real-time estimation and control, power electronics, wind, and solar energy.



Matthew Armstrong received the M.Eng. degree from the University of Newcastle upon Tyne, Newcastle Upon Tyne, U.K., in 1998.

Since then he has been a Research Associate with the School of Electrical, Electronic and Computer Engineering, University of Newcastle Upon Tyne. His main research has been focused upon the power quality improvement of grid connected photovoltaic systems.