Suppression of the Backgating Effect of Enhancement-Mode p-GaN HEMTs on 200-mm GaN-on-SOI for Monolithic Integration

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***Abstract*— The backgating effect on trench-isolated enhancement-mode p-GaN devices fabricated on 200-mm GaN-on-SOI was investigated. We show that to minimize the backgating effect in the monolithically integrated half-bridge, the sources of both the low side and high side need to be connected to their respective fully isolated Si(111) device layers to keep the substrates and the sources at equipotential.**

***Index Terms*— p-GaN, HEMT, backgating effect, GaN-on-SOI, half-bridge, monolithic integration.**

I. Introduction

MONOLITHIC integration of GaN-based half-bridges has recently attracted extensive attention because of the higher switching speed, better power conversion efficiency, and more compact chip volume [1], [2]. The monolithic integration of power devices on GaN-on-Si substrates is however challenging. A first issue is the crosstalk between devices, namely the high-voltage stress on one device can degrade another neighboring device by coupling through the common conductive Si substrate. Secondly, the substrate bias is still debated, and it is not clarified if the Si substrate should be floating, grounded, or connected to which device terminal. Indeed, crosstalk between two devices fabricated on the same GaN-on-Si substrate, and isolated with only implantation [3], or only mesa isolation [4], have been reported in literature. In addition, Chu *et al.* [5] and Tang *et al.* [6] have shown dynamic R_{ON} degradation for a floating Si(111) substrate which can store negative charges under stress, resulting in depletion of the two-dimensional electron gas (2DEG). We have recently reported [7] on the successful elimination of the crosstalk between the low side (LS) and high side (HS) high electron mobility transistors (HEMTs) in a half-bridge fabricated on GaN-on-SOI, by using deep trench isolation to fully isolate the common conductive Si(111) device layer between both devices (Fig. 1(b)). However, also in this case the substrate bias is not elaborated. For hybrid integrated half-bridge circuits, discrete power devices with separate substrate-source connections are mounted on a printed circuit board (PCB), resulting in full isolation between the Si substrates of the devices in the half-bridge. In contrast, for a monolithically integrated half-bridge on GaN-on-Si (Fig. 1(a)), because of the common conductive Si substrate B, the potential differences between the Si substrate and the separate device sources, V_{B-S1} and V_{B-S2}, cannot be zero simultaneously.

Furthermore, it was reported that both a positive and a negative substrate-source potential difference (V_{BS}) can induce

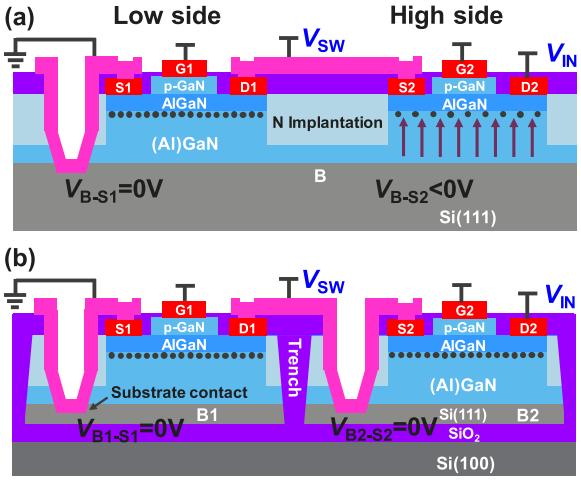

Fig. 1. Schematic cross-section of monolithically integrated half-bridge with e-mode (enhancement-mode) low side and high side devices fabricated on 200 mm (a) GaN-on-Si, and (b) GaN-on-SOI with trench isolation.

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trapping in the HEMTs [8], [9] and even jeopardize the switching performance of the half-bridge [2]. The static and dynamic characterization of a half-bridge on GaN-on-Si with different substrate bias has been discussed in [10]. Except the trapping, negatively biasing the substrate can also induce drain current collapse by electrostatic interaction [7], [11], a phenomenon that is commonly known as the "backgating" effect. Similarly, this backgating is also expected in a monolithically integrated half-bridge when the HS is in conduction ($V_{S2} \approx V_{IN}$), and the common Si(111) substrate B is grounded by connecting it with the source S1 of the LS through a "substrate contact" as shown in Fig. 1(a). This backgating effect on the HS transistor in a monolithically integrated half-bridge on GaN-on-Si has been reported to result in an increased power loss [10], but the solution was not yet clarified.

In this letter, we study the backgating effect of the HS in a monolithically integrated half-bridge on GaN-on-SOI. The source (S), gate (G) and D (drain) terminals were biased positively such as to imitate the real working state of the HS, and the output current was monitored while stressing the Si(111) device layer at different potentials.

II. Epitaxy, Fabrication, and Characterization

The GaN device stack was epitaxially grown on the 200 mm SOI wafer using metalorganic chemical vapor deposition (MOCVD). The SOI wafer used in this work includes a 1070 μm Si(100) handling wafer, a 1 μm SiO_2 buried layer, and a 3.5 μm p-Si(111) device layer with a resistivity of 1-10 $\Omega \cdot$cm. A GaN-on-Si reference wafer was also epitaxially grown for comparison, with a similar Si resistivity. Superlattice buffer stack was adopted in the epitaxy, and the superlattice thickness for GaN-on-Si is 1.4 μm while that for GaN-on-SOI is increased to 2.15 μm to keep the wafer warp well below 50 μm.

The e-mode p-GaN HEMTs were processed using Au-free process modules for the gate, ohmic contacts and metal interconnects. Nitrogen implantation was used for horizontal isolation. Both the LS and HS devices have a gate width W_G of 100 μm, a gate length L_G (namely the length of the p-GaN and gate metal) of 0.8 μm, a gate-source distance L_{GS} of 0.75 μm, and a gate-drain distance L_{GD} of 6 μm. For complete electrical isolation among neighboring devices, a 8-μm wide and oxide-filled trench was processed, surrounding the devices. This trench goes through the (Al)GaN/Si(111) layers, into the SiO_2 buried layer of the SOI substrate. The substrate contact was processed by etching through the oxide/(Al)GaN layers and stopping in the Si(111) layer, followed by Ti/Al sputtering to connect the Si(111) device layer with the source terminal. The device processing is then finalized with a thick Si_3N_4 scratch protect layer.

III. Results and Discussion

For both GaN-on-Si and GaN-on-SOI substrates, similar transfer characteristics with V_{TH} of ~2.5 V were obtained, as shown in Fig. 2 and in agreement with our previous observation described in [7].

To directly demonstrate the backgating effect, a substrate biasing experiment was executed as shown in Fig. 3. In this

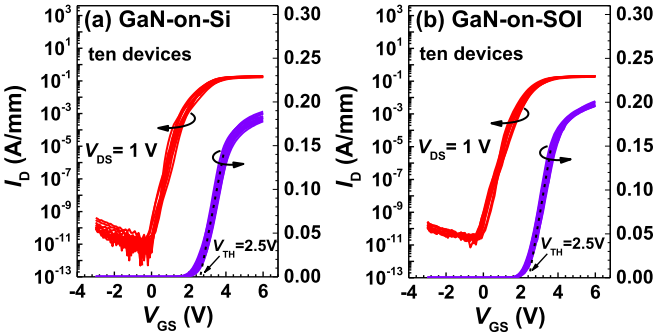

Fig. 2. Transfer characteristics of the e-mode p-GaN HEMTs on 200 mm (a) GaN-on-Si and (b) GaN-on-SOI at 25 °C, and ten devices were measured for each wafer.

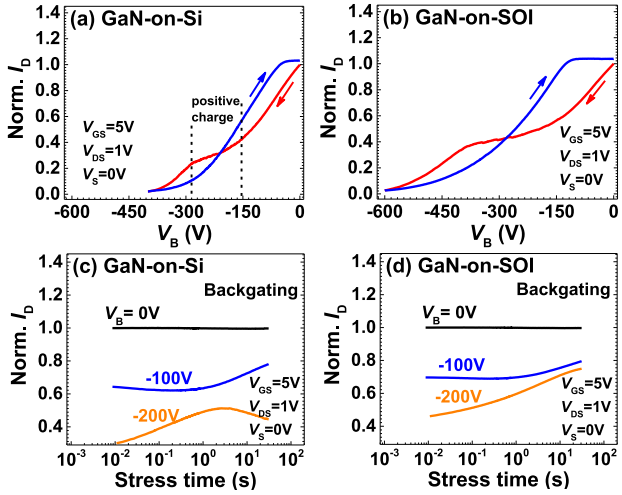

Fig. 3. Normalized drain current of HEMTs with the Si(111) substrate bias ramping from 0 V to a negative value and then back to 0 V on (a) GaN-on-Si and (b) GaN-on-SOI. Normalized drain current of HEMTs on (c) GaN-on-Si and (d) GaN-on-SOI while backgating the Si(111) substrates differently at 0, −100, and −200 V. V_S, V_{GS}, and V_{DS} are fixed at 0, 5, and 1 V, respectively. The devices have their Si(111) substrates disconnected from their respective sources.

measurement, both HEMTs on GaN-on-Si and GaN-on-SOI have their Si(111) substrates disconnected from their respective sources, in order to bias the Si(111) substrates freely, which is different from the setup in Fig. 1. In this case the bias V_S, V_{GS}, and V_{DS} are 0, 5, and 1 V, respectively. As shown in Fig. 3(a) for GaN-on-Si, the I_D varies with the Si(111) bias V_B that ramps down from 0 to −450 V and then back up to 0 V at a speed of 45 V/s. The strong electrostatic coupling between the substrate and the channel results in this backgating effect, during which the 2DEG density reduction ΔN_S has the relationship with the V_{BS} as [12]

$$q \cdot \Delta N_S = \frac{C_{epi} \cdot V_{BS}}{A} = \frac{\varepsilon \cdot V_{BS}}{t_{epi}}, \quad (1)$$

where q is the electron charge, A is the device area, C_{epi} is the buffer capacitance, ε is the buffer dielectric constant, and t_{epi} is the buffer thickness. The current plateau from −150 to −280 V is believed to be correlated with charge generation and storage in the buffer [13]. Fig. 3(b) demonstrates the same substrate bias ramping experiment conducted on GaN-on-SOI. The slightly different curves between the two substrates are due to

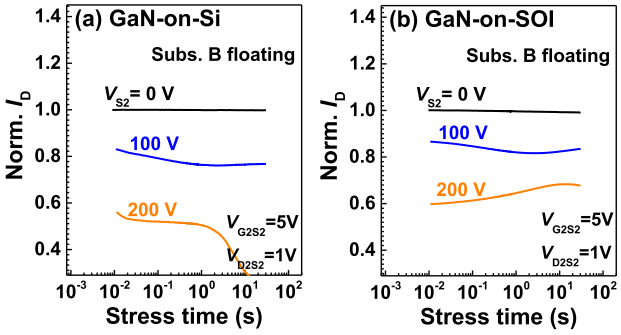

Fig. 4. Backgating effect of HEMTs on (a) GaN-on-Si and (b) GaN-on-SOI with the Si(111) substrates floating. V_{S2} is differently biased at 0, 100, and 200 V, and V_{G2S2} and V_{D2S2} are 5 V and 1 V, respectively.

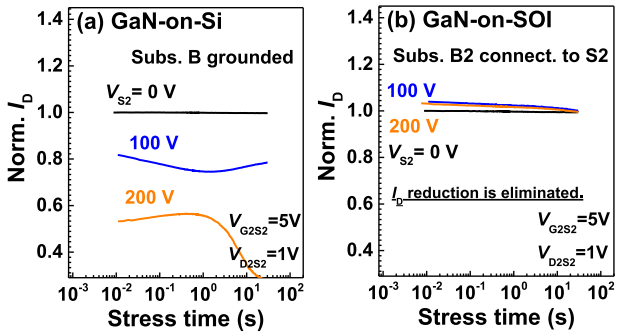

Fig. 5. Normalized drain current of (a) the HS device on GaN-on-Si with Si(111) substrate B grounded and (b) the HS device on GaN-on-SOI with Si(111) substrate B2 connected to its source S2. To mimic the real working state of the HS device, V_{S2} for the two devices is biased at 0, 100, and 200 V, and the $V_{G2\text{-}S2}$ and $V_{D2\text{-}S2}$ are kept at 5 and 1 V, respectively.

the different superlattice thickness on GaN-on-Si and GaN-on-SOI as explained by (1). The results of the direct backgating experiments are shown in Fig. 3(c) and (d) where the drain currents of the HEMTs are monitored while biasing the Si(111) substrate at different negative voltages. Both gradual increase and decrease of the drain current under stress are noticeable in Fig. 3(c) and (d), indicating the generation of both positive and negative charges in the buffer under stress as discussed in [14].

Further, to imitate the real working state of the HS whose S/G/D are all biased at high voltages ($\sim V_{IN}$) during conduction, V_{S2} in Fig. 4 is therefore sequentially fixed at 0, 100, and 200 V, and the V_{G2-S2} and V_{D2-S2} are respectively held at 5 and 1 V to keep the HS in ON state. During the measurement, the terminal biases were applied to the HS device and kept for 30 s, and meanwhile the drain current I_D was monitored to check whether the HS device can still operate normally as the reference condition of $V_{S2} = 0$ V. Different from the schematic in Fig. 1, the devices in this measurement have no substrate contact and the Si(111) is left floating, in order to check if the backgating effect can be eliminated by simply floating the Si(111). The data in Fig. 4(a) for GaN-on-Si, and in Fig. 4(b) for GaN-on-SOI, show however pronounced backgating effects for both cases. The backgating effect exists for floating the substrate because the substrate potential is still around 0 V even floating. Amano *et al.* [12] state that the buffer works as a capacitance of C_{epi}, therefore the substrate potential cannot follow the bias on the top surface swiftly, which results in the backgating effect in this case. Other strategy is therefore in need to figure out this problem.

Notice the backgating effect is induced by the negative V_{BS}, the Si(111) is therefore connected with its respective source terminal as shown in Fig. 1(b) for SOI, where the $V_{B1-S1} = 0$ and $V_{B2-S2} = 0$ V can be simultaneously achieved, thanks to the trench isolation. However, the common conductive Si(111) of GaN-on-Si can only be connected to the source of the LS that is grounded, and the V_{B-S2} will still be negative when HS is in conduction (Fig. 1(a)). On GaN-on-SOI, the I_D reduction for the HS is fully eliminated (Fig. 5(b)) because of $V_{B2-S2} = 0$ V. In contrast, Fig. 5(a) shows that the I_D decreases dramatically by 50% for $V_{S2} = 200$ V on GaN-on-Si. The significant contrast between Fig. 5(a) and (b) proves that keeping substrate and source at equipotential is key to suppressing the current reduction, i.e. backgating effect of the HS device. Moreover, the similar current curves in Fig. 5(a) and Fig. 3(c) verifies that the observed I_D reduction in Fig. 5(a) of the HS device on GaN-on-Si with a negative V_{B-S2} is indeed caused by the backgating effect.

For a monolithically integrated half-bridge on GaN-on-Si, simultaneous connections of S1 and S2 with the common conductive Si(111) substrate is evidently infeasible because of the crosstalk, and also because of the leakage path through the conductive Si(111) substrate between the terminals S1 and S2. Oppositely, benefiting from the full isolation of the two Si(111) substrates B1 and B2, GaN-on-SOI doesn't suffer from this issue. It's worth to mention this advantage is crucial for future monolithic integration of power circuits on GaN.

IV. Conclusion

We have compared the backgating effect in a monolithically integrated half-bridge fabricated on GaN-on-Si and GaN-on-SOI. For GaN-on-SOI the backgating effect can be adequately suppressed by connecting the sources of both the LS and HS transistors to their respective fully isolated Si(111) substrates. We conclude that GaN-on-SOI with trench isolation shows major advantages for monolithic integration of a GaN half-bridge by eliminating the backgating effect.

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