# Surface Chemistry and Electrical Properties of Germanium Nanowires

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***Abstract:*** Germanium nanowires (GeNWs) with p- and n-dopants were synthesized by chemical vapor deposition (CVD) and were used to construct complementary field-effect transistors (FETs). Electrical transport and X-ray photoelectron spectroscopy (XPS) data are correlated to glean the effects of Ge surface chemistry to the electrical characteristics of GeNWs. Large hysteresis due to water molecules strongly bound to $GeO_2$ on GeNWs is revealed. Different oxidation behavior and hysteresis characteristics and opposite band bending due to Fermi level pinning by interface states between Ge and surface oxides are observed for p- and n-type GeNWs. Vacuum annealing above 400 °C is used to remove surface oxides and eliminate hysteresis in GeNW FETs. High-$\kappa$ dielectric $HfO_2$ films grown on clean GeNW surfaces by atomic layer deposition (ALD) using an alkylamide precursor is effective in serving as the first layer of surface passivation. Lastly, the depletion length along the radial direction of nanowires is evaluated. The result suggests that surface effects could be dominant over the "bulk" properties of small diameter wires.

## Introduction

Currently, as electronic devices are scaled down to the sub-100 nm regime, Ge has gained renewed interest as a material of choice for future electronics due to its significantly higher electron and hole mobilities than Si.[1,2] It is well known that the water solubility of $GeO_2$ and the lack of a stable oxide have prevented Ge from being utilized as an electronic material in the past. This problem could now be solved, in principle, by using the recently advanced high dielectric-constant (high-$\kappa$) films as gate insulators. Indeed, promising results have already been reported for metal-oxide-semiconductor capacitors and field-effect transistors (FET) based on Ge with high-$\kappa$ films as dielectric materials.[3,4] Despite these progresses, the surface chemistry of Ge remains much less explored and understood than that of Si. Detailed understanding of how various species on Ge surfaces affect the electrical properties of Ge is lacking. Further, approaches to reliably passivate Ge surfaces still have to be fully established and require significant effort.

Chemically synthesized nanomaterials such as nanotubes and nanowires have attracted much attention lately as building blocks

for future electronics.[5–13] These bottom-up chemically derived materials may present advantages over top-down lithographically patterned materials in better intrinsic properties in the case of carbon nanotubes,[6,7] higher degrees of structural or surface perfection, lower costs than single crystalline wafer materials in the case of Ge, or high flexibility in the type of substrates that can be used for assembly of these materials. Ge nanowires are particularly appealing due to the high carrier mobility and the ease of synthesis. We have shown recently that single crystalline GeNWs can be readily synthesized by a simple chemical vapor deposition (CVD) method at a low temperature of 275 °C from Au nanoparticle seeds.[10] The growth condition for GeNWs is the mildest among all semiconducting wires and represents the lowest temperature under which single crystalline semiconductors are synthesized. The potential of the GeNWs as building blocks for electronic devices has also been demonstrated by successful fabrication of FETs based on p-type

† Stanford University.
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(1) Sze, S. M. *Physics of Semiconductor Devices*; Wiley: New York, 1981.
(2) Konig, U.; Schaffler, F. *IEEE Electron Device Lett.* **1993**, *14*, 205–207.
(3) Chui, C. O.; Baylor, S. R.; Triplett, B.; McIntyre, P. C.; Saraswat, K. C. *IEEE Electron Device Lett.* **2002**, *23*, 473–475.
(4) Wang, D. W.; Wang, Q.; Javey, A.; Tu, R.; Dai, H. J.; Kim, H.; McIntyre, P. C.; Krishnamohan, T.; Saraswat, K. C. *Appl. Phys. Lett.* **2003**, *83*, 2432–2434.

(5) Dai, H. *Surf. Sci.* **2002**, *500*, 218–241.
(6) Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom, M.; Dai, H. *Nat. Mater.* **2002**, *1*, 241–246.
(7) Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. J. *Nature* **2003**, *424*, 654–657.
(8) Wind, S.; Appenzeller, J.; Martel, R.; Derycke, V.; P, P. A. *Appl. Phys. Lett.* **2002**, *80*, 3817–3819.
(9) Yu, J.-Y.; Chung, S.-W.; Heath, J. R. *J. Phys. Chem. B* **2000**, *104*, 11864–11870.
(10) Wang, D.; Dai, H. *Angew. Chem., Int. Ed.* **2002**, *41*, 4783–4786.
(11) Lauhon, L. J.; Gudiksen, M. S.; Wang, D.; Lieber, C. M. *Nature* **2002**, *401*, 227–230.
(12) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 149–152.
(13) Zhang, D.; Li, C.; Han, S.; Liu, X.; Tang, T.; Jin, W.; Zhou, C. *Appl. Phys. Lett.* **2003**, *82*, 112–114.

GeNWs with a hole mobility on the order of 600 cm$^2$/(V s), approaching that of 1800 cm$^2$/(V s) for bulk Ge.[4]

The high surface areas of nanotubes and nanowires suggest that surface effects could play dominant roles in determining their physical properties. The electrical properties of nanotube and nanowire devices could be affected by various surface species including molecules adsorbed from the environment.[14] For example, hysteresis in the electrical characteristics of carbon nanotube FETs has been observed due to physisorbed water molecules on the nanotube surface and on the SiO$_2$ substrates around the nanotube.[15] Transistor prototypes based on several semiconducting nanowires including Si have been observed to exhibit hysteresis behavior.[16] The origin of hysteresis in nanowire FETs, however, remains largely elusive thus far. To our knowledge, no systematic effort has been taken to elucidate or eliminate the origin of the hysteresis. Uncontrolled hysteresis is highly problematic because it will make the operations of electronic devices highly unpredictable. Removal of the hysteresis will require detailed understanding of the surface chemistry involved in various nanowires. This is particularly important and challenging for GeNWs due to the well-known poor surface oxide properties of Ge.

In this Article, we present a systematic investigation of the electrical characteristics and surface chemical properties of p-type and n-type GeNWs. We first show that p- and n-type doping of GeNWs can be achieved by introducing desired doping gases during CVD growth of GeNWs. Detailed hysteresis behaviors of as-fabricated GeNW FETs are then described. A thermal annealing process is developed to eliminate or suppress such hysteresis. X-ray photoelectron spectroscopy is then used to elucidate the surface species for as-made and cleaned GeNWs. The spectroscopy results combined with electrical data lead to the conclusion that the hysteresis in GeNW FETs is caused by water molecules absorbed on GeNW surface oxides. Moreover, XPS measurements clearly reveal band bending in GeNWs due to Fermi level pinning of surface states. The importance of surface effects to nanowires is discussed especially for wires with sizes approaching the nanometer scale. We also present a preliminary surface passivation method based on atomic layer deposition of HfO$_2$ high-$\kappa$ dielectrics.

## Methods

**Materials.** Germane in helium (GeH$_4$, 10% in He), diborane in hydrogen (B$_2$H$_6$, 10 ppm in H$_2$), and phosphine in hydrogen (PH$_3$, 150 ppm in H$_2$) were purchased from Voltaix, Inc. (Branchburg, NJ). Gold nanoparticle colloid solutions were purchased from Sigma-Aldrich Co, and the diameters of the Au particles varied from 2 to 20 nm. Transmission electron microscopy grids with Ni frames and thin SiO$_x$ supporting film were obtained from Structure Probe, Inc. (West Chester, PA).

**CVD Growths of GeNWs. (1) Synthesis of Intrinsic GeNWs.** Growth was carried out at 275 °C with a GeH$_4$ flow of 10 sccm (standard cubic centimeter per minute) and an H$_2$ co-flow of 100 sccm in a 1 in. quartz tube furnace.[10] The typical growth time was 30−40 min. The catalyst was either Au nanoparticles (diameters = 2−20 nm) deposited on SiO$_2$ or Si substrates from an aqueous solution of Au colloids (by soaking the substrates in an (aminopropyl)triethoxysilane
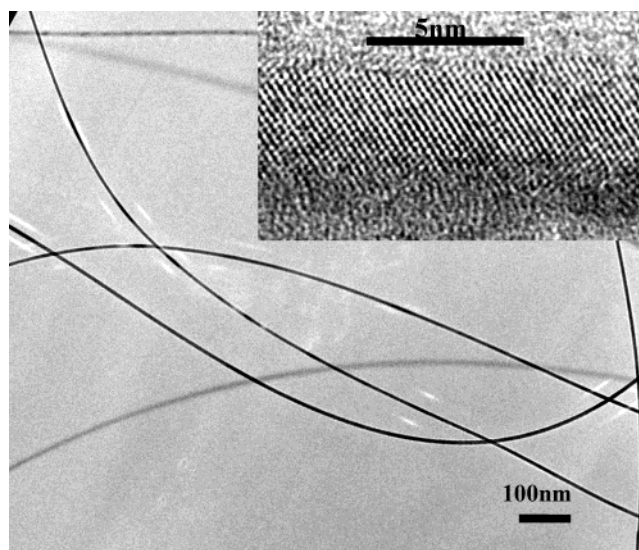


**Figure 1.** A TEM image of GeNWs grown from ∼5 nm Au nanoparticles. Inset: A high-resolution TEM image of a GeNW with a diameter of ∼4 nm.

APTES solution, and then in a Au colloid solution for 30 min) or a thin Au film (thickness ∼3 nm) evaporated from an electron-beam evaporator. **(2) Synthesis of Boron-Doped p-type GeNWs.** To grow p-type GeNWs, H$_2$ co-flow was replaced with a mixture of H$_2$/B$_2$H$_6$ (B$_2$H$_6$ concentration 10 ppm). All other growth parameters were kept the same as for the intrinsic wires. **(3) Synthesis of Phosphorus-Doped n-type GeNWs.** Pure H$_2$ and PH$_3$ in H$_2$ (PH$_3$ concentration 150 ppm) were used as co-flows (H$_2$ flow rate 80 sccm and H$_2$/PH$_3$ flow rate 20 sccm) of GeH$_4$ for n-type Ge nanowire growth. As shown later by transistor data, these growth conditions were effective in producing p- and n-doped GeNWs, respectively. Our low 275 °C CVD growth using germane was mild and highly reproducible. No significant reduction in the yield of GeNWs was observed due to the addition of B$_2$H$_6$ or PH$_3$. **(4) Synthesis of GeNWs on TEM Grids.** Au nanoparticles were deposited on a TEM grid with SiO$_2$ supporting film in the same manner as on a Si or SiO$_2$ substrate. The grid was subjected to CVD growth, and the resulting GeNWs were imaged by TEM directly after growth.[10]

**X-ray Photoelectron Spectroscopy (XPS).** XPS measurements were carried out on a PHI Quantum 2000 scanning microprobe equipped with an angle-resolved hemispherical electron energy analyzer and a base system pressure of 1 × 10$^{-9}$ Torr. All measurements were performed using the Al Kα line with a photon energy of 1486.6 eV. Charge compensation during acquisition was applied using the improved dual neutralization capability including an electron flood gun and an ion gun. C 1s (284.8 eV) on SiO$_2$ substrate were used to calibrate the process parameters and to ensure sufficient charge compensation. Ag and Cu standards were also employed to calibrate the system. The samples used for XPS studies were mats of p- or n-type GeNWs (random dense networks of GeNWs) grown on SiO$_2$ substrates with a thin Au film (3 nm) deposited on the substrates as catalyst.

**Transmission Electron Microscope (TEM) and Scanning Electron Microscope (SEM).** The transmission electron microscope used was a Philips CM20 with a working acceleration voltage of 200 keV. The scanning electron microscope used was a FEI Siron field emission instrument operated at relatively low acceleration voltages of 1−5 keV.

**GeNW FETs with Back-Gate and SiO$_2$-Gate Dielectrics.** SiO$_2$/Si (p$^{++}$) substrates were used for growth and integration of GeNWs into FET structures (Figure 2a). The thickness of SiO$_2$ formed by dry oxidation was 10 nm (verified by ellipsometry) in the source (S), drain (D), and NW channel regions. The SiO$_2$ thickness was 500 nm in regions under large electrical bonding pads to avoid potential damages to the SiO$_2$ during electrical probing or wire-bonding. Details of the

(14) Kong, J.; Franklin, N.; Zhou, C.; Chapline, M.; Peng, S.; Cho, K.; Dai, H. *Science* **2000**, *287*, 622−625.

(15) Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. *Nano Lett.* **2003**, *3*, 193.

(16) Duan, X. F.; Niu, C. M.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. L. *Nature* **2003**, *425*, 274−278.
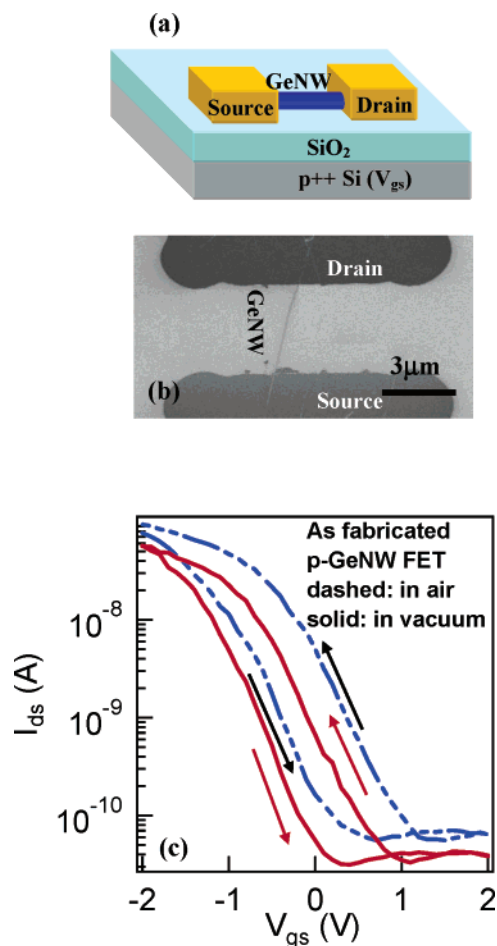
**Figure 2.** Back-gated p-type GeNW FETs. (a) A schematic view of the device structure. The $SiO_2$ thickness is $t_{ox} = 10$ nm. The doped Si substrate is used for the back-gate. (b) A SEM top-view image of an individual GeNW device recorded at an acceleration voltage of 5 keV. The electrodes and GeNW appear dark under this imaging condition because they conduct electrons better than the $SiO_2$ background. (c) A typical as-fabricated unpassivated GeNW FET exhibiting large hysteresis under back-and-forth gate sweeping (direction marked by arrows, $V_{ds} = 100$ mV) measured with the device placed in air and in a vacuum ($5 \times 10^{-7}$ Torr), respectively.

substrates design and preparation can be found in a previous work.[17] Au seeds (average particle size ~10 nm) were deposited on the $SiO_2$/Si surface in a patterned fashion[10,18] and were used for CVD growth to produce GeNWs (p-type or n-type) from the patterned catalyst sites. After growth, samples with p-type NWs were annealed at 400 °C for 2 h intended for dopant activation and then soaked in 0.1 M HCl for 30 s to remove native surface oxides on the GeNWs. No annealing or activation was carried out for n-type GeNWs prior to device fabrication. Photolithography or electron-beam lithography patterning of photoresist, metal evaporation (30 nm of Ti), and lift-off were then used to form S and D metal electrodes on top of the GeNWs. The length of the GeNW between the edges of the S and D electrode was typically $L = 3$ μm. FET operation was carried out by using the heavily doped Si as the back-gate electrode and the 10 nm $SiO_2$ as the gate dielectric (Figure 2a). Note that even though the GeNWs were treated in HCl (known to remove germanium oxides) prior to the fabrication steps, the GeNWs were exposed to the ambient environment for ~1−3 weeks through the device fabrication steps, which caused the formation of oxides on the GeNWs in the as-fabricated devices. Ti was used here for S and D electrodes to contact GeNWs because Ti−Ge contacts were found to
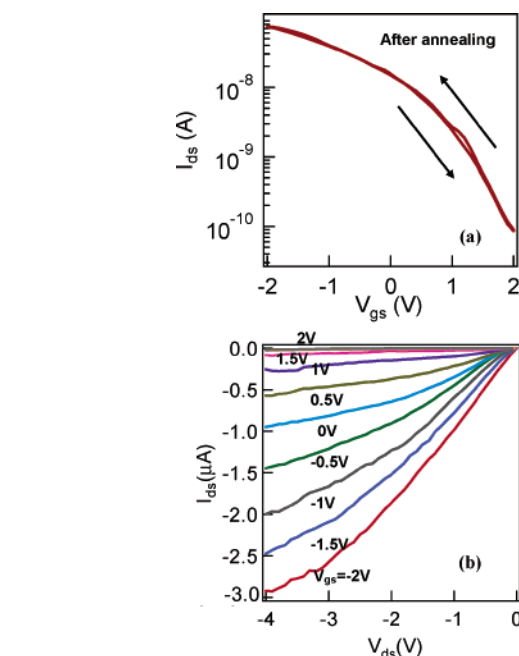


**Figure 3.** p-type GeNW FETs characteristics after removal of surface oxide by annealing in a vacuum at ~450 °C. (a) Current versus gate voltage ($I_{ds}$−$V_{gs}$) curves showing nearly eliminated hysteresis after annealing (measured in a vacuum) of the same device as in Figure 2. The bias voltage used to record this curve was $V_{ds} = 100$ mV. (b) Current versus voltage ($I_{ds}$−$V_{ds}$) curves under various gate voltages as labeled.

remain intact after high-temperature annealing up to 450 °C. This stability was useful for our annealing experiments carried out for GeNW FETs, as described below. Although optimization of contacts was not the main scope of the current work, we note that earlier, Pd was found to form more transparent contacts for GeNWs.[4] Pd was not used here because the quality of the contacts tended to degrade upon annealing to 450 °C. Also, as a side note, we did not observe significant improvement of the Ti contacts with GeNWs upon annealing to 450 °C.

**ALD of $HfO_2$ for Top-Gated GeNW FETs with High-$\kappa$ Dielectrics.** ALD of $HfO_2$ films on the back-gated p-type GeNW FETs described above was carried out to produce top-gated devices with high-$\kappa$ gate dielectrics (Figure 9a). The back-gated p-type GeNW FETs were first "cleaned" by annealing at 450 °C for ~0.5 h in a vacuum to remove surface oxides. The sample was then transferred to an ALD chamber for $HfO_2$ deposition after a brief and minimized exposure to air (<0.5 h). $HfO_2$ was deposited uniformly onto the sample (including GeNWs, S and D electrodes, and the substrate) by reacting deionized water with tetrakis(diethylamido)hafnium ($Hf[NEt_2]_4$) precursor in a layer-by-layer fashion.[19] Nitrogen was used as the carrier gas, and the deposition temperature was 90 °C. Each ALD reaction cycle involved alternating $H_2O$ and $Hf[NEt_2]_4$ doses, and the purge times were 350 s after the DI $H_2O$ dose and 150 s after the $Hf[NEt_2]_4$ dose. The sample was exposed to ~80 cycles of ALD to deposit an $HfO_2$ film with a nominal thickness of ~8 nm. After the dielectric deposition, a lithography step was carried out to pattern top-gate metal electrodes on top of the GeNW channels with $HfO_2$ sandwiched between, forming top-gated GeNW FETs. Note that there was an underlap between the gate and S/D electrodes (Figure 9a,b) with the top-gate switching only the GeNW section directly underneath the top-gate. The Si back-gate was used to control the NW sections aside of the top-gate and was fixed at a constant voltage. Detailed operation of this type of transistor can be found in a previous pubication.[20]

(17) Javey, A.; Wang, Q.; Kim, W.; Dai, H. IEEE: Piscataway, NJ, 2003.
(18) Kong, J.; Soh, H.; Cassell, A.; Quate, C. F.; Dai, H. *Nature* **1998**, *395*, 878.
(19) Hausmann, D. M.; Kim, E.; Becker, J.; Gordon, R. G. *Chem. Mater.* **2003**, *14*, 4350−4358.
(20) Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Wang, D. W.; Gordon, R. G.; Lundstrom, M.; Dai, H. *J. Nano Lett.* **2004**, *4*, 447−450.
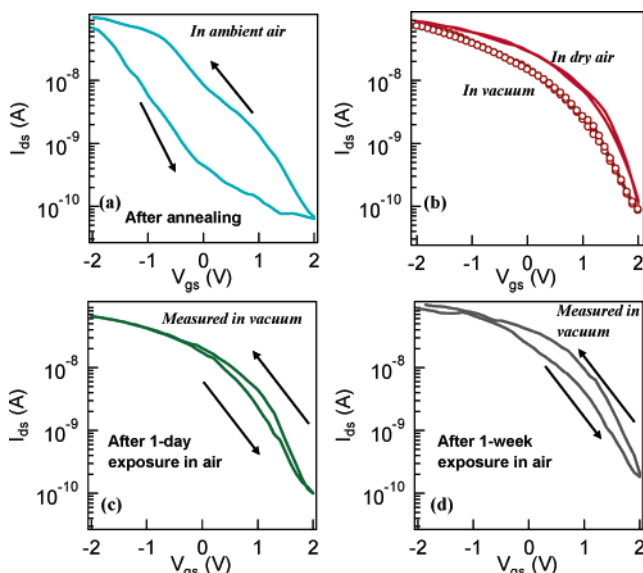
**Figure 4.** p-type GeNW FET hysteresis versus various environment. $V_{ds}$ = 100 mV for all measurements. (a) Large hysteresis in the $I_{ds}$–$V_{gs}$ characteristics of the device in Figure 3 observed during a brief exposure to ambient air after annealing and surface oxide removal. (b) Hysteresis diminished when the device was placed in a vacuum (symbols) and dry air (solid line). (c) After 24 h of exposure of the device to ambient air, the device exhibited hysteresis that persisted when measured in a vacuum. (d) After 1 week of exposure of the device to air, the device exhibited larger hysteresis than in (c) when placed back into a vacuum.

**Annealing of GeNWs in a Vacuum for Oxide Removal.** Annealing was performed for both mats of GeNWs grown on $SiO_2$ substrates and GeNW FETs in a vacuum chamber with a base pressure of $5 \times 10^{-8}$ Torr. The sample was placed on a metal stage equipped with a thermal heater and a thermal couple for temperature monitoring. Annealing was typically performed at 450 °C for 30 min, which was found to be efficient in volatilizing germanium oxides on GeNWs. After annealing, the GeNW FETs (p-type or n-type) were quickly transferred into a vacuum chamber ($5 \times 10^{-7}$ Torr) for ex-situ electrical measurements, and the transfer process exposed GeNWs in the devices to ambient air for ~10−20 min. For XPS measurements, the GeNW mats were transferred into the XPS vacuum chamber after exposure to ambient air for a specified amount of time ranging from minutes to $^1/_2$ h or to days.

## Results and Discussion

**Growth.** A high yield of single crystalline GeNWs can be grown by our simple CVD method at 275 °C with various Au seeds ranging from discrete Au colloidal nanoparticles to vapor-phase deposited thin Au films. The growth mechanism for the GeNWs involves the vapor−liquid−solid (VLS) process, as described previously.[10] Shown in Figure 1 is a low magnification TEM image of as-grown GeNWs from nominally 5 nm Au nanoparticles deposited on a TEM grid. The inset in Figure 1 shows a lattice resolved high-resolution TEM image of a ~4 nm diameter GeNW. We found that GeNW size was highly controllable by tuning catalyst sizes. The smallest wires we successfully and reproducibly grew were ~3 nm from ~2−3 nm Au nanoparticles. On 3 nm thick Au films, CVD growth led to the formation of a dense mat of GeNWs with diameters of 10−30 nm, suggesting that large Au particles were formed when the Au film was heated during CVD and these particles served as seeds for GeNWs growth.

**Characteristics of p-type GeNW FETs.** The back-gated FETs fabricated on B-doped GeNWs clearly exhibited p-type

transistor behavior with about 3 orders of magnitude conductance (G) decrease under positive gate voltages (Figure 2c), indicating successful incorporation of p-type B-dopants into GeNWs during the CVD synthesis process. An immediate phenomenon we observed during electrical characterization of the unpassivated GeNW FETs (with NWs exposed to ambient air) was the large hysteresis in the current versus gate voltage ($I_{ds}$−$V_{gs}$) curves. That is, the source−drain current is sensitive not only to gate voltage, but also to the gate voltage sweeping directions. The broken lines in Figure 2c are $I_{ds}$−$V_{gs}$ curves recorded with a p-type GeNW FET under gate sweeping from $V_{gs} = -2$ to 2 V and then back to $-2$ V at a sweep rate of $\Delta V_{gs}/\Delta t = 0.3$ V/s. A ~1 V difference in the threshold voltages was clearly present between the $I_{ds}$−$V_{gs}$ curves recorded under the two sweeping directions. The amount of hysteresis typically increased (i.e., larger differences in threshold voltages or larger hysteresis loops) under a decreased gate sweeping rate $\Delta V_{gs}/\Delta t$ and was observed with all of the as-fabricated GeNW FETs (nearly 100 devices characterized) without exception. The hysteresis was nearly unchanged when the GeNW FETs were placed and measured in a vacuum ($5 \times 10^{-7}$ Torr, Figure 2c), even under vacuum pumping for extended periods of time up to several days. At a first glance, the hysteresis behavior appeared to be a result of slow charging and discharging of states or chemical species on the GeNWs during gate sweeps.

**Elimination of Hysteresis for p-type GeNW FET.** We carried out various treatments of the GeNWs aimed at eliminating and understanding the origin of the hysteresis. Our general strategy was to clean the GeNWs and thus eliminate the states or chemical species responsible for the hysteresis. After experimenting with various methods including solution-phase chemical etching of Ge oxides,[21−23] we found that the most efficient method of eliminating hysteresis in the GeNW FETs was simple annealing in a vacuum at ~450 °C. The GeNW FETs were typically annealed in a vacuum at ~450 °C for $^1/_2$ h and then transferred to another vacuum chamber for ex-situ electrical measurements. During the transfer, the devices were briefly exposed to ambient air for ~20 min. After the brief exposure and when placed back in a vacuum, the annealed p-type GeNW FETs exhibited almost no hysteresis (<30 mV difference in threshold voltage) as shown in Figure 3a, and the result was independent of the gate voltage sweep rate in the range of $\Delta V_{gs}/\Delta t = 0.03-0.6$ V/s. These results illustrate that the thermal annealing step is effective in eliminating hysteresis for p-type GeNW FETs.

**Cause of Hysteresis.** The annealed GeNW FETs remained hysteresis free as long as they were kept in a vacuum. Upon exposure of the devices to air, large hysteresis was observed immediately (within 1 min) as shown in Figure 4a for a typical device. The hysteresis disappeared as soon as the sample was placed back into a vacuum (Figure 4b, red ○) after a short (~10 min) exposure to air. The reversible hysteresis removal and reappearance were observed for up to many vacuum/air-exposure cycles as long as the air exposure was brief (minutes). This result hinted that the hysteresis was caused by molecules

(21) Prabhakaran, K.; Maeda, F.; Watanabe, Y.; Ogino, T. *Thin Solid Films* **2000**, *369*, 289−292.
(22) Hovis, J. S.; Hamers, R. J.; Greenlief, C. M. *Surf. Sci.* **1999**, *440*, L815−L819.
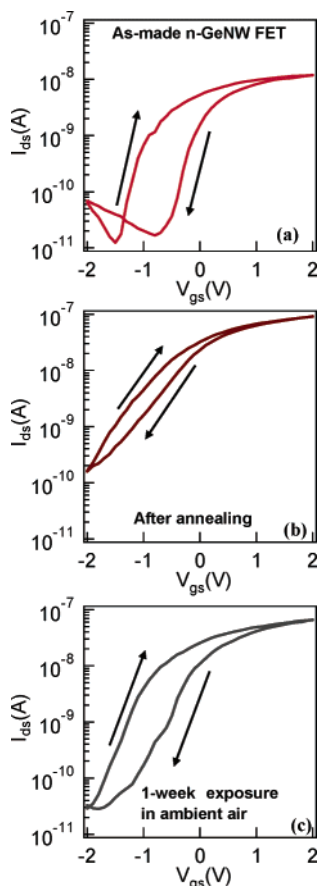(23) Bodlaki, D.; Yamamoto, H.; Waldeck, D. H.; Borguet, E. *Surf. Sci.* **2003**, *543*, 63−74.

**Figure 5.** Hysteresis of n-type GeNW FETs. (a) An as-fabricated n-type GeNW FET exhibited large hysteresis with the device placed in a vacuum. (b) The device exhibited significantly reduced hysteresis after 450 °C annealing in a vacuum, a brief exposure to air, and being placed back in a vacuum. (c) After 1 week of exposure to ambient air, large hysteresis recovered to the device. $V_{ds} = 100$ mV for all measurements shown here.

adsorbed on the GeNW surfaces from the ambient air and that, for p-type GeNWs with surface oxides removed by 450 °C annealing (see, for example, ref 21 and later sections for evidence of oxide removal), the molecules causing the hysteresis can be readily desorbed by pumping in a vacuum.

In a control experiment, we exposed an annealed GeNW FET to dry air and observed no hysteresis at all in the device characteristics (Figure 4b, solid line). This hints that $H_2O$ molecules adsorbed on the GeNW surfaces are responsible for the hysteresis behavior of the GeNW FETs.

Long exposures of p-type GeNWs (after high-temperature annealing/cleaning) to ambient air were found to cause hysteresis that was irreversible by vacuum pumping. For example, after 1 day exposure of annealed p-GeNW FETs to ambient air, a hysteresis of ~200 mV was observed (Figure 4c) when measured with the device placed back in a vacuum. After the sample was exposed to air for 1 week, the measured hysteresis in a vacuum increased to ~500 mV (Figure 4d). This result was consistent with that the as-made p-type GeNW FETs (with the GeNWs exposed to air for typically >1 week during device fabrication) exhibited large hysteresis that persisted in a vacuum. As shown later, long air exposure of p-type Ge leads to the formation of a surface $GeO_2$ layer that strongly adsorbs $H_2O$ molecules. The water molecules do not desorb from the $GeO_2$ layer on the GeNW in a vacuum and are responsible for the irreversible hysteresis behavior of the transistors.

**Characteristic of n-type GeNW FETs and Different Hysteresis Behaviors from p-type FETs.** The n-type GeNW FETs were successfully fabricated with phosphorus-doped n-type GeNWs, as shown by the orders of magnitude conductance increase (vs decrease for p-FET) under positive gate voltages (Figure 5a). This suggested successful incorporation of P-atoms into the GeNWs during CVD growth in the presence of $PH_3$. The as-fabricated n-type GeNW FETs (exposed to ambient air for ~1 week after growth) also exhibited large hysteresis (~1 V) under back-and-forth gate voltage sweeps (Figure 5a). Vacuum annealing experiments at 450 °C were conducted on n-type GeNW FETs, followed by transferring of the devices to another vacuum chamber for electrical characterization, during which the devices were exposed to ambient air briefly (20 min). This treatment led to clear reduction of hysteresis, but, unlike the p-type GeNW FETs, small hysteresis persisted for the n-type FETs (Figure 5b). This result, as shown later by XPS data, is due to rapid $GeO_2$ formation on n-type Ge (which differs from p-type Ge) during the brief air-exposure sample-transfer step, causing strong water adsorption on the $GeO_2$ on the nanowires and therefore the irreversible hysteresis. After annealing of the n-type GeNW FETs, exposure of the devices to air for ~1 week led to large hysteresis similar to that of as-fabricated n-FETs (Figure 5c).

**XPS of p-type and n-type GeNWs with Native Oxides.** XPS experiments were performed on mats of GeNWs to investigate the species on the nanowire surfaces and then correlate the results with electrical properties of the GeNW transistors. Ge is known to oxidize in various environments and form GeO and/or $GeO_2$ depending on the environmental conditions.[24,25] The freshly grown GeNWs contained large numbers of surface atoms and are therefore highly reactive. Once synthesized, the GeNWs were retrieved from the CVD growth chamber and exposed to the ambient air. For both p- and n-type GeNWs exposed to air for >~1 day after CVD synthesis, XPS revealed the presence of "native" GeO and $GeO_2$ on the GeNW surfaces, as shown in the Ge 3d and Ge 2p spectra in Figure 6. The zerovalent $Ge^0$ states are peaked in the 3d spectra around 29.8–29.95 eV (Figure 6a and b), and the germanium oxides are around 32.7–33 eV. Curve fittings (Figure 6a and b) reveal that the oxide peaks correspond to combinations of $Ge^{2+}$ (GeO) and $Ge^{4+}$ ($GeO_2$). The peak positions of $Ge^0$ and $Ge^{2+}$ and $Ge^{4+}$ are consistent with literature values reported for Ge wafers, with ~0.75 eV shift per oxidization state.[22,25,26] The presence of surface native oxides can also be clearly seen from Ge 2p spectra in Figure 6c and d for p and n-type GeNWs, respectively.

**XPS of p-type and n-type GeNWs after Annealing at 450 °C.** It is known that both GeO and $GeO_2$ can be removed from Ge surfaces by thermal annealing in a vacuum. GeO starts to vaporize above ~400 °C. $GeO_2$ by itself is stable up to higher temperatures,[27] but when in contact with Ge, $GeO_2$ reacts with Ge at >~400 °C, converts to GeO, and then sublimes.[21] Therefore, relatively clean and oxide-free surfaces are expected for GeNWs after heating above 400 °C. Our XPS data recorded with both p- and n-type GeNWs after being annealed to 450

(24) Tabet, N.; Al-Sadah, J.; Salim, M. *Surf. Rev. Lett.* **1999**, *6*, 1053–1060.
(25) Prabhakaran, K.; Ogino, T. *Surf. Sci.* **1995**, *325*, 263–271.
(26) Zhang, X. J.; Xue, G.; Agarwal, A.; Tsu, R.; Hasan, M. A.; Greene, J. E.; Rockett, A. *J. Vac. Sci. Technol.* **1993**, *11*, 2553–2561.
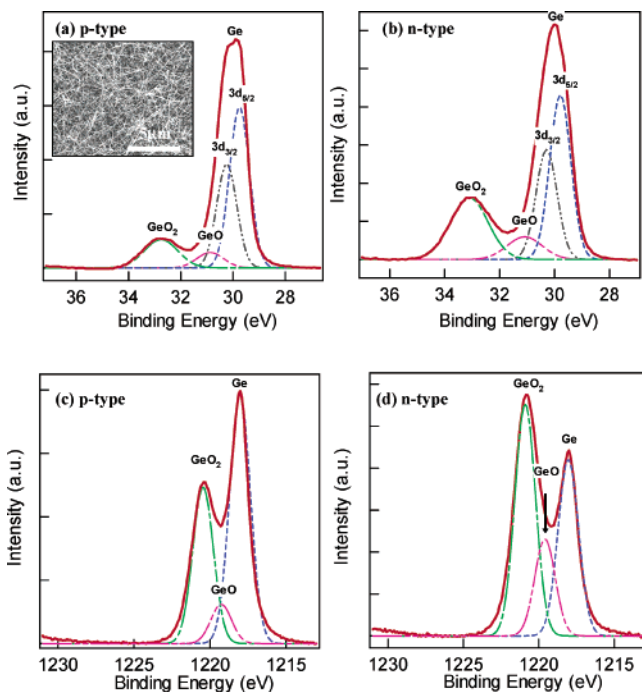(27) *CRC Handbook of Chemistry and Physics*; CRC Press: Boca Raton, FL, 1996.

**Figure 6.** XPS spectra of p-type and n-type GeNWs with native oxides. (a) and (c) correspond to p-type GeNWs for Ge 3d and 2p spectra, respectively. The inset in (a) shows an SEM image of the GeNW mat sample used for XPS experiments. The labeled peaks are curve-fitting results for the experimental data, showing various surface chemical compositions. (b) and (d) are for n-type GeNWs.

°C indeed revealed the removal of the oxides signaled by the significantly reduced peaks corresponding to the oxides (Figure 7a and b).

**Different Oxidation Behaviors of p- and n-type GeNWs.** The XPS data of p- and n-GeNWs after annealing shown in Figure 7a and b still display weak signals in the region corresponding to Ge oxides due to sample transfer and exposure to air for ~2 min after the annealing. We have systematically varied the air-exposure time and recorded XPS spectra to investigate the oxide formation processes on p- and n-type GeNWs. For p-type GeNWs, after annealing and 2 min of air exposure, a shoulder-like feature can be seen near the $Ge^0$ peak in the Ge 3d spectra, and peak fitting reveals that the shoulder mainly corresponds to GeO. Longer air exposures ($^1/_2$ h to 1 day) cause the shoulder to grow and shift toward higher binding energies (Figure 7c), and the spectrum recorded after 1 day of exposure shows a clear peak corresponding to $GeO_2$ (Figure 7c). Curve fitting also shows GeO in coexistence with $GeO_2$. These results suggest that upon exposure of "clean" p-type GeNWs to air, oxide quickly forms on the Ge surfaces and the oxide species is predominantly GeO. Longer air exposure causes the growth of oxides on the surfaces, and the formation of an appreciable amount of $GeO_2$ on p-type GeNWs is relatively slow and takes a relatively long time (hours).

The n-type GeNWs exhibit an oxidation behavior different than that of the p-type wires. After annealing and a brief 2 min of air exposure, an appreciable amount of $GeO_2$ is already detected on the nanowire surfaces (Figure 7b). Longer exposures ($^1/_2$ h to 1day) of the n-GeNWs to air cause the intensity of the oxide peak to grow, but unlike the p-type GeNWs, no significant shift in the peak position is observed (Figure 7d). These results suggest that $GeO_2$ formation is rapid on n-type GeNW surfaces,
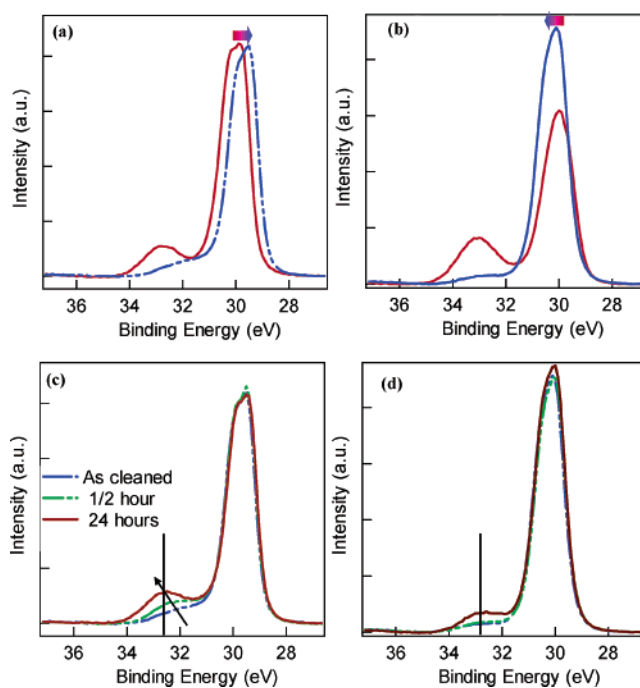


**Figure 7.** XPS spectra of p-type and n-type GeNWs before and after 450 °C annealing in a vacuum. (a) p-type GeNWs 3d spectra before (red) and after (blue) annealing. A brief exposure to air was involved during sample transfer to XPS chamber. (b) Similar data to (a) for n-type GeNWs. (c) Evolution of XPS spectrum for p-type GeNWs after vacuum annealing and exposure to air for various periods of times as indicated. Note that the Ge 3d peak exhibited only slight shifts after exposure to air for up to 1 day. The degree of band bending was smaller than the sample in (a) that had been exposed in air for >1 week due to less oxidation. (d) Data similar to (c) for n-type GeNWs.

within minutes of exposure to air. Longer exposure times in air lead to thicker $GeO_2$ films.

It is to our knowledge the first time that dopant-dependent reactivity is reported for Ge. The p-type GeNW oxidation behavior, that is, rapid GeO formation followed by slow $GeO_2$ growth, is similar to previous reports for p-type Ge wafers.[24] No systematic investigation on n-type Ge wafer oxidation has been reported previously. Note that dopant-dependent chemical reactivity is known for semiconductors including Si. An example is the drastically different etching rates for p- and n-type Si wafers in $XeF_2$ etching gases.[28] Nevertheless, a detailed understanding of the different oxidation behaviors of n- and p-type semiconductors is currently lacking, and we leave it for future investigations.

**Band Bending in Oxidized GeNWs Due to Interface States.** In addition to the oxide species on GeNWs, our XPS results also revealed band bending caused by Ge−$GeO_x$ interface states on GeNWs with surface oxides. For p-type GeNWs, the removal of the native oxides by annealing at 450 °C leads to a −0.3 eV shift of the $Ge^0$ 3d peak from 29.8 to 29.5 eV (Figure 7a). For n-type GeNWs, an opposite +0.1 eV shift from 29.95 to 30.05 eV is observed after oxide removal (Figure 7b). These results suggest the existence of Ge/$GeO_x$ interface states residing within the band gap of Ge, giving rise to Fermi level pinning at the interface and band bending away from the interface with a characteristic screening length $d$ (Figure 8). The band bending causes an increase (for p-type, Figure 8a) or decrease (for n-type,

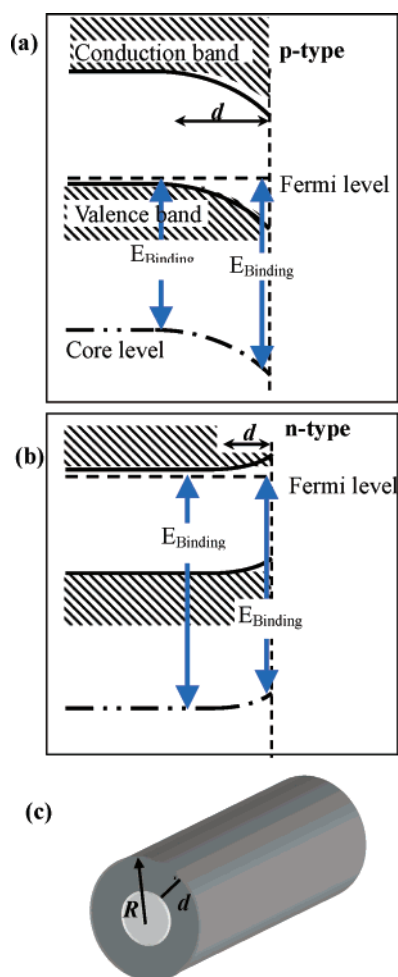(28) Winters, H. F.; Haarer, D. *Phys. Rev. B* **1987**, *36*, 6613−6623.

**Figure 8.** Schematic illustration of opposite band bending for (a) p- and (b) n-type GeNWs, respectively, due to Fermi level pinning of surface states. (c) shows the depletion layer (thickness = *d*) of a GeNW due to band bending caused by Fermi level pinning at the surface.

Figure 8b) in the distance between the Ge 3d core-level to the Fermi level, and thus increases or decreases the binding energy of the Ge 3d level relative to bulk Ge for p- and n-type GeNWs, respectively. Oxide removal at the surface eliminates the interface states and band bending, thus shifting the Ge peaks toward that of bulk Ge. The band-bending behaviors reported here for p- and n-type GeNWs are similar to those previously observed with p- and n-type Ge wafers.[22,29] Band bending due to surface interface states has also been reported for other semiconductors including Si and GaAs.[30−32] Note that for oxide-free p- and n- type GeNWs, the $Ge^0$ 3d peaks are at 29.5 and 30.05 eV, respectively (Figure 7a and b), and the 0.55 eV difference approximately matches the Ge band gap of 0.6 eV. The $Ge^0$ 3d peak shift for n-GeNW is relatively small after oxide removal as compared to the p-type, suggesting the interface states are close to the conduction band in n-type GeNWs with native oxides.

(29) Tabet, N.; Faiz, M.; Hamdan, N. M.; Hussain, Z. *Surf. Sci.* **2003**, *523*, 68−72.
(30) Himpsel, F. J.; Mcfeely, F. R.; Talebibrahimi, A.; Yarmoff, J. A.; Hollinger, G. *Phys. Rev. B* **1988**, *38*, 6084−6096.
(31) Grant, R. W.; Waldrop, J. R.; Kowalczyk, S. P.; Kraut, E. A. *J. Vac. Sci. Technol.* **1981**, *19*, 477−480.
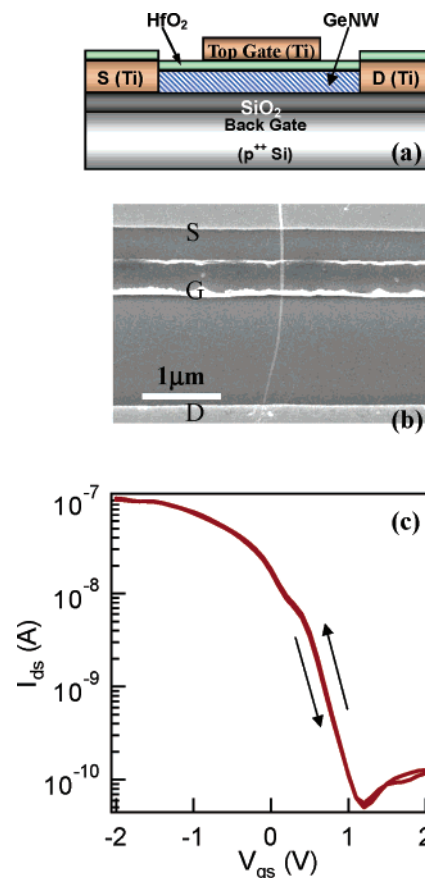(32) Kraut, E. A.; Grant, R. W.; Waldrop, J. R.; Kowalczyk, S. P. *Phys. Rev. B* **1983**, *28*, 1965−1977.

**Figure 9.** Top-gated p-type GeNW FETs with high-$\kappa$ HfO$_2$ dielectrics. (a) A schematic side view of the device. (b) A top-view SEM image of the device. SEM acceleration voltage = 5 keV. (c) $I_{ds}$−$V_{gs}$ characteristics of a typical device exhibiting little hysteresis ($V_{ds}$ = 100 mV).

**Correlating Hysteresis of GeNW FETs with Surface XPS Data.** Correlating our electrical and XPS data suggests that surface bound water is responsible for hysteresis in GeNW FETs. We can also infer that water association with GeO$_2$ on GeNW surfaces is strong and does not desorb by simple vacuum pumping, while the opposite appears to be true for water−GeO interaction. These are consistent with that as-fabricated p- and n-type GeNW FETs exhibit hysteresis that cannot be removed by placing the devices in a vacuum. For p-type GeNW FETs, hysteresis is diminished after annealing in a vacuum even with a brief reexposure to air. This is consistent with XPS data of GeO$_2$ removal by vacuum annealing and predominantly GeO formation (rather than GeO$_2$) during the brief air reexposure. For n-type GeNW FETs, hysteresis persisted after oxide removal followed by brief air exposure due to rapid formation of GeO$_2$ and strong association with water molecules. It is therefore rather difficult to eliminate surface-bound water and related hysteresis in n-type Ge devices if any short air exposure of clean n-type Ge surfaces cannot be avoided.

The interface states due to Ge surface oxides could also act as charge traps and caused hysteresis behavior to the electrical characteristics of FETs. However, for our p-GeNW FETs exposed to pure oxygen or dry air after vacuum annealing, no significant hysteresis was observed (Figure 4b) even after extended (2 h) exposure to pure oxygen, while XPS data revealed the formation of GeO and GeO$_2$ on p-type Ge during such exposure.[24] Hysteresis was observed immediately once the

devices were taken out of the pure oxygen and exposed to ambient air (Figure 4a). These results confirm $H_2O$ molecules on the oxide surface rather than the $Ge/GeO_x$ interface states as the main cause to the type of hysteresis concerned in the current work. The hysteresis is large (on the order of ~1 V), slow, and dependent on gate sweep rate (in the range of $\Delta V_{gs}/\Delta t = 0.03-0.6$ V/s). It is possible that $GeO_x/Ge$ interface states also give rise to hysteresis behavior, but at a different time scale than the one probed here by DC electrical measurements.

**Water on Ge Oxide Surfaces.** XPS data clearly revealed that GeNWs exposed to air contain native oxides on surfaces. The suggested strong interaction/association between $H_2O$ from the ambient air and surface $GeO_2$ is reasonable because $GeO_2$ is known to be soluble in $H_2O$. The surface chemistry of $SiO_2$ and Si is much better studied than for the Ge system. The existence of physisorbed water layers on native $SiO_2$ on Si is well known, and, in fact, approximately one monolayer of $H_2O$ is hydrogen bonded to the hydroxyl groups on $SiO_2$. As a result of the strong binding, desorption of the final surface water layer on $SiO_2$ only occurs above ~250 °C.[33] While systematic spectroscopy work is needed to elucidate detailed $H_2O$ interactions with $GeO_x/Ge$, we note that several previous infrared spectroscopy works on $GeO_x/Ge$ surfaces have indeed identified adsorbed water species.[34,35] A temperature-programmed desorption (TPD) experiment revealed the existence of water and related species on Ge surfaces at high temperatures up to 250–300 °C before desorption during heating.[36]

**Water in Various Bottom-Up Electronic Devices Including Nanotubes, Nanowires, and Organic FETs.** For modern Si electronics, much is known about the causes and elimination of hysteresis in metal-oxide semiconductor (MOS) FETs. Slow states and hysteresis related to water have been reported for MOSFETs without proper encapsulation/passivation, as well as for MOS capacitances and tunnel diodes with hydrated $SiO_2$ gate insulators.[37-39] Recently, we have reported hysteresis in single-walled carbon nanotube FETs formed on $SiO_2$ substrates due to water molecules physisorbed on nanotube surfaces and on $SiO_2$ surrounding the nanotube.[15] The current GeNW results represent another example of hysteresis phenomena in nanomaterials-based devices due to surface water. The water effect appears to be general in various unpassivated FETs based on materials derived by bottom-up chemical methods. There are several reports of large hysteresis observed in other types of nanowire FETs and in various organic transistors built on $SiO_2$ substrates.[40,41] We believe that water is a likely cause of hysteresis in these systems as well. The removal of surface-bound water will be dependent on the specific systems and surface chemistry involved. For instance, in the case of carbon

nanotube FETs, coating the nanotubes with a polymer, polymethylmathacrylate (PMMA), followed by baking can remove water adsorbed on the nanotube and on $SiO_2$ surfaces.[15] Hydrogen bonding of PMMA with the latter is responsible for removing the water layer on $SiO_2$.[42] In the case of GeNWs, a similar PMMA passivation method was unsuccessful in removing the hysteresis, suggesting that $H_2O$ association with surface $GeO_2$ is strong and cannot be removed by the PMMA treatment. Note that it is possible that $H_2O$-derived surface species such as $-OH$ groups may contribute to hysteresis. Systematic infrared spectroscopy work is indeed needed to clearly identify the species on Ge surfaces treated under various conditions and to correlate with the electrical properties of Ge devices.

**Mechanism of Hysteresis Due to Water.** The detailed mechanism of surface water causing hysteresis behavior in unpassivated electronic devices is not fully understood and requires further investigation. We suggest that a possible mechanism is due to the large electric dipole of water molecules. In an electric field on the order of ~1 V/nm generated by the gate voltage, water molecules will respond to the field and be oriented. The water molecule orienting and relaxation processes under sweeping gate voltages and electric fields could exert varying dipole fields to the channel of the FETs, giving rise to an additional gating mechanism to the transistors and therefore hysteresis. Other mechanisms are certainly possible, including the relaxation of mobile impurities and ions on the surface of the transistor materials in the presence of water.

**Doping Levels and Radial Screening Lengths in NWs.** The doping level ($n$) in GeNWs can be estimated on[43] the basis of the resistivity ($\rho$) of the nearly hysteresis-free GeNW FETs (Figures 3 and 5b for p- and n-type, respectively) at zero gate-voltage

$$n = \frac{1}{e\mu\rho} \qquad (1)$$

where $\mu$ is the carrier mobility estimated from the FET characteristics (e.g., Figure 3b)

$$\mu = \frac{dI_{ds}}{dV_{gs}} \times \frac{L^2}{C_{ox}} \times \frac{1}{V_{ds}} \qquad (2)$$

The gate-capacitance $C_{ox} = 3.8 \times 10^{-16}$ F is estimated from

$$C_{ox} = \frac{2\pi\epsilon_0\epsilon L}{\cosh^{-1}\left(\dfrac{R + t_{ox}}{R}\right)} \qquad (3)$$

where $t_{ox} = 10$ nm is the $SiO_2$ gate oxide ($\epsilon \approx 4$) thickness, $L \approx 3$ $\mu$m is the length of the GeNW between the source and drain electrodes, and $R \approx 5$ nm is the NW diameter. The resistivity $\rho$ of GeNW under zero gate voltage is determined from

$$\rho = \frac{dV_{ds}}{dI_{ds}} \times \frac{A}{L} \qquad (4)$$

where $A$ is the NW cross-sectional area. Through this analysis, we obtained a B-doping level of $n = 3 \times 10^{18}/cm^3$ for p-type

(33) Iler, R. K. *The Chemistry of Silica: Solubility, Polymerization, Colloid and Surface Properties, and Biochemistry*; Wiley: New York, 1979.
(34) Metcalfe, A.; Shankar, S. U. *J. Chem. Soc., Faraday Trans. 1* **1979**, *75*, 962–970.
(35) Thiel, P. A.; Madey, T. E. *Surf. Sci. Rep.* **1987**, *7*, 211–385.
(36) Cohen, S. M.; Yang, Y. L.; Rouchouze, E.; Jin, T.; D'Evelyn, M. D. *J. Vac. Sci. Technol., A* **1992**, *10*, 2166–2171.
(37) Andersson, M. O.; Farmer, K. R.; Engstrom, O. *J. Appl. Phys.* **1992**, *71*, 1846–1852.
(38) Zhang, J. F.; Eccleston, B. *IEEE Trans. Electron Devices* **1994**, *41*, 740–744.
(39) Chou, J. S.; Lee, S. C. *IEEE Trans. Electron Devices* **1996**, *43*, 599–604.
(40) Wang, G. M.; Moses, D.; Heeger, A. J.; Zhang, H. M.; Narasimhan, M.; Demaray, R. E. *J. Appl. Phys.* **2004**, *95*, 316–322.
(41) Komoda, T.; Kita, K.; Kyuno, K.; Toriumi, A. *Jpn. J. Appl. Phys.* **2003**, *42*, 3662.

(42) Jia, X. Q.; McCarthy, T. J. *Langmuir* **2002**, *18*, 683–687.
(43) Pierret, R. F. *Semiconductor Device Fundamentals*; Addison-Wesley: Reading, MA, 1996.

GeNWs and a P-doping level of $n = 6 \times 10^{18}$/cm³ for n-type GeNWs. Note that the ratio of B:Ge in the feeding gases for GeNW CVD growth was 1:500 and 1:300 for P:Ge, corresponding to maximum possible doping concentrations of $8 \times 10^{19}$ and $1.2 \times 10^{20}$ cm⁻³, respectively, for p- and n-type GeNWs.

The extent of band bending due to Fermi level pinning by surface states can be estimated for nanowires. For a planar surface with a surface Fermi level pinning potential of $\phi_0$, the screening length (or band bending length extending into the semiconductor with doping concentration of $n$) $d$ is given by[44]

$$d = \sqrt{\frac{4\pi\epsilon_0\epsilon\phi_0}{2\pi n}} \qquad (5)$$

where $\epsilon_0$ is the permittivity of the vacuum and $\epsilon$ is the dielectric constant of the semiconductor ($\epsilon \approx 16$ for Ge). For a nanowire with radius $R$, the depletion length $d$ (along the radial direction of the NW, Figure 8c) can be obtained after solving the Poisson's equation using cylindrical coordinates (for $d < R$),

$$-\frac{4\pi\epsilon_0\epsilon\phi_0}{2\pi n} = R^2\left(1 - \frac{d}{R}\right)^2 \times \left[1 - 2\ln\left(1 - \frac{d}{R}\right)\right] - R^2 \qquad (6)$$

For $d \ll R$, to the first-order of the NW curvature ($d/R$), the radial screening length $d$ in the NW is given by,

$$\frac{4\pi\epsilon_0\epsilon\phi_0}{2\pi n} = \left(1 - \frac{d}{3R}\right)d^2 \qquad (7)$$

which suggests that the screening length in a nanowire is longer than that in the planar surface case. This is a reasonable result because screening becomes less effective when approaching the core of a NW due to the reduced radial dimension. Note that eqs 6 and 7 are valid only for $d < R$. For $d \geq R$, the whole nanowire along the radius will be depleted, and it is no longer meaningful to calculate $d$.

If we assume that the GeNWs are large in radius with $R \gg d$, then for our p-type GeNWs with $n = 3 \times 10^{18}$ cm⁻³ and Fermi level pinning of $\phi_0 = 0.3$ eV (Figure 7a), a screen length of $d \approx 13$ nm is estimated on the basis of eq 5. For n-type GeNWs with $n = 6 \times 10^{18}$ cm⁻³ and $\phi_0 = 0.1$ eV, $d \approx 6$ nm is obtained. These lengths represent the lower limit of the true screening lengths for the finite radius nanowires. The fact that they are similar to our GeNWs radii in the range of $R = 5$ to 15 nm suggests that for the GeNWs with native oxides, Fermi level pinning and band bending at the surface will affect a large part of the NW "bulk". Such a surface effect could significantly alter the electrical properties of the wires. For p-type NWs, for instance, removal of surface oxides leads to a shift of threshold voltage by $+2$ V in the transistor characteristics (Figure 2c vs Figure 3a), indicating that the NWs with surface oxides are unintentionally "n-doped" as a result of band bending extending deep inside the wires from the surface due to surface states Fermi level pinning (Figure 8a).

The analysis above points to the importance of surface to the bulk properties of semiconducting nanowires. Clearly, as the size of NW decreases, the dominance of the surface effect will increase. Surface passivation is particularly important to

GeNWs due to the high density of surface states ($>10^{14}$/cm²).[45] Surface effects could also become significant in nanowires of Si or other types of semiconductors with low surface-state densities ($\sim 10^{12}$/cm²),[45] especially if the diameters of the wires become very small. These issues will need to be systematically addressed by future research.

**Preliminary Result of Passivation of GeNW FETs by ALD of $HfO_2$.** We carried out preliminary experiments for passivating GeNW FETs. For p-type GeNW FETs, we first removed surface oxides on the GeNWs by vacuum annealing at 450 °C and then carried out ALD $HfO_2$ at 90 °C with minimum exposure of the devices to air after the annealing ($\sim 10$ min total). Top-gate GeNW FETs obtained this way exhibited negligible hysteresis under top-gating when measured in a vacuum or dry environments. These devices can be stored in ambient air for days without exhibiting large hysteresis when measured in a dry environment. This result suggests that the high-$\kappa$ films on p-type GeNW FETs can be used as the first layer of passivation while serving as the gate insulator. Further work will be needed to investigate the nature of the $HfO_2$/Ge interface and understand the passivation effect. It will also be necessary to devise further passivation layers on top of the high-$\kappa$ films to completely block water, oxygen, and other molecular species from the ambient air.

## Conclusions

Single crystalline germanium nanowires with p- and n-dopants were synthesized by chemical vapor deposition at 275 °C and were used to construct p- and n-type field-effect transistors, respectively. The growth condition is mild, and the size of the nanowires can be well controlled by the size of the Au nanoparticle seeds down to the 3−5 nm scale. Electrical transport and XPS measurements were carried out to understand the Ge surface chemistry and its role in the electrical characteristics of GeNWs. Large hysteresis observed in the electrical properties of nonpassivated GeNWs was found to be mainly due to water molecules strongly bound to $GeO_2$ on GeNWs. Water adsorption on GeO was found to be weaker than on $GeO_2$ and can be easily removed. The n-type GeNW FETs were more susceptible to hysteresis behavior due to more reactive surfaces toward rapid $GeO_2$ formation than p-type Ge. The p-type GeNWs, on the other hand, form GeO on the surfaces initially when exposed to air and then an appreciable amount of $GeO_2$ after long exposures (hours). This is the first time that different chemical reactivity and hysteresis characteristics are observed for p- and n-doped Ge.

Opposite band bending due to interface states between Ge and surface oxides was observed for p- and n-type GeNWs. An annealing method was devised to remove surface oxides on GeNWs and eliminate or suppress hysteresis for GeNW FETs. Further, it was found that thin high-$\kappa$ dielectric $HfO_2$ films grown on $GeO_2$-free GeNW surfaces by atomic layer deposition (ALD) were effective in serving as the first layer of surface passivation for GeNWs.

The current work reveals fundamental chemical and physical properties of Ge and may have important implications to Ge as a candidate material for future electronics. Further, the results should be of interest beyond Ge because surface water appears

(44) Yu, P. Y.; Cardona, M. *Fundamentals of Semiconductors: physics and materials properties*; Springer-Verlag: Berlin, 2001.

(45) Kingston, R. H., Ed. *Semiconductor Surface Physics*; University of Pennsylvania Press: Philadelphia, 1957.

to be a generic cause of hysteresis in electronic devices-based bottom-up chemically derived nanomaterials ranging from carbon nanotubes to various semiconductor nanowires or even organic transistors. Last, the depletion length or screening length along the radial direction of nanowires is evaluated. The result suggests that surface effects could be dominant over the "bulk" properties of small diameter wires.

JA047435X