Survey on Fault Operation on Multilevel Inverters

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***Abstract*—This paper is related to faults that can appear in multilevel (ML) inverters, which have a high number of components. This is a subject of increasing importance in high-power inverters. First, methods to identify a fault are classified and briefly described for each topology. In addition, a number of strategies and hardware modifications that allow for operation in faulty conditions are also presented. As a result of the analyzed works, it can be concluded that ML inverters can significantly increase their availability and are able to operate even with some faulty components.**

***Index Terms*—Fault diagnosis, fault tolerance, multilevel (ML) converters.**

I. Introduction

HIGH-POWER inverters are increasingly being accepted in industry as a way to reduce operational costs and increase production. At high-power levels (more than 1 MW), several topologies have been accepted in the market, of which the most important are as follows: 1) current source inverters and 2) voltage source inverters in the form of multilevel (ML) inverters. In addition, due to the high power of these equipment, a fault is a very serious problem, because it causes significant production loss [1].

ML inverters are an array of power semiconductors and capacitors that allow for the generation of a high-quality load voltage. Today, the three most popular and widely used families of ML inverters in industry are neutral point (NP) clamped (NPC), flying capacitor (FC), and CM [2], [3].

These ML inverters have a high number of power semiconductors, and consequently, the possibility of a failure is much higher. Hence, the identification of possible faults and the operation under faulty conditions are of paramount importance.

Due to the high number of components, the detection of a fault can be complicated in principle. However, the availability of powerful microprocessors made it possible to develop very intelligent methods for fault detection. Some examples of these advanced methods are techniques based on frequency analysis [4], [5], the use of neural networks (NNs) to search for some specific patterns [6], and the study of the time behavior in voltages and currents at the load [7]–[9].

To allow for operation under fault condition, some methods include additional hardware and modify the topology. They also modify the software, principally the modulation strategy. In NPC inverters, a number of investigations have studied a variety of solutions adding semiconductors and passive components [10]–[21].

On the other hand, the cascaded inverter uses its modularity advantageously to introduce the idea of redundancy of cells instead of using redundancy of components. This approach presents a drastic reduction in the need for additional hardware [22].

The presence of a high number of levels, typical in ML inverters, is associated with a high number of redundant states, which offer an important alternative for operation without significantly deteriorating the performance of the equipment [23]–[26].

This paper presents a review of the most important techniques used to detect faults and operate under faulty conditions in the main topologies of ML inverters used in industry.

II. Faults in NPC Inverters

This section is devoted to the analysis of different fault-tolerant solutions for NPC converters. Mainly, the different solutions found in the literature can be divided into two major groups. On one hand, there are some solutions based on three-legged topologies. The main advantage of these solutions is their simplicity. However, due to this simplicity, the converters' performance under faulty conditions is limited. On the other hand, there are some solutions based on topologies with four legs. Although the converter structures are more complex in those cases, they can continue working after a fault, offering a similar performance as in normal operation mode. In the following sections, the main topologies are reviewed.

Manuscript received March 13, 2009; revised June 21, 2009 and August 12, 2009; accepted August 14, 2009. Date of publication September 22, 2009; date of current version June 11, 2010. This work was supported in part by the Chilean Research Council (CONICYT) under Grant FONDECYT 1085111, by the Ministerio de Ciencia y Tecnologia of Spain under Projects ENE2007-67033-C03-01 and ENE2007-67033-C03-03, by the Department d'Universitats Recerca i Societat de la Informació of the Generalitat de Catalunya, the Basque Country Government, and by the Torres Quevedo Program.

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Digital Object Identifier 10.1109/TIE.2009.2032194

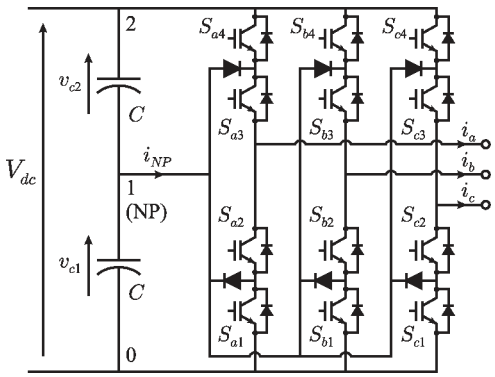

Fig. 1. NPC converter.

A. Fault Diagnosis

The diagnosis solutions found in the literature can be divided into two main groups.

1) Switch Measurements: Some authors propose solutions in which it is necessary to measure the voltage and/or current of each switch [12], [16]. This can be accomplished by means of the current and voltage sensors which are already integrated in the gate drivers. Therefore, it is not necessary to include additional hardware. In these solutions, it is possible to determine if one switch has failed in short or open circuit. For instance, regardless of the state of the gate signal, if the voltage across one switch is always zero, it means that the switch presents a short-circuit fault.

2) Output Waveform Analysis: On the other hand, there are other solutions based on the measurements of output phase voltages or currents [7], [8]. In these cases, after a fault, the measured phase voltage or current in the faulty leg is not the expected one. Therefore, an error signal is generated and processed in order to determine which insulated-gate bipolar transistor (IGBT) has failed. More details about this procedure will be given in Section IV-A1.

B. Hardware Solutions

1) Three-Legged Topologies:

Solution I: A very simple fault-tolerant solution for an NPC converter capable of coping with short-circuit faults is proposed in [10]. In this solution, there is no need to add extra power devices; therefore, the fault-tolerant converter has exactly the same structure as the usual one (Fig. 1). The fault-tolerant capacity is achieved due to the redundancy of voltage vectors present in NPC converters.

Some examples of fault conditions in this topology are explained here. For instance, if the switch S_{a4} fails in short circuit, phase a cannot provide level "1." Therefore, the remaining available voltage vectors are shown in Fig. 2(a). In this diagram, the voltage vectors that require S_{a4} to be open have been removed since they are no longer available. However, due to the redundancy of these voltage vectors, the converter is still able to continue working. Nevertheless, the switches have to withstand the total dc-link voltage. This fact should be taken into consideration during the design process of the converter.

On the other hand, if, for instance, switch S_{a3} fails in short circuit, for instance, phase a cannot provide level "0." The remaining voltage vectors are those shown in Fig. 2(b). In this case, there are some critical voltage vectors (those placed on the external limits of the vector diagram) which cannot be used. Taking into account that, in a steady-state condition, the reference vector describes a circumference on the plane, the maximum modulation index is now reduced to one half (it is assumed that the maximum modulation index under normal operation mode is equal to one).

A similar solution for a five-level converter is presented in [11].

Solution II: An attempt to provide open-circuit fault tolerance capabilities for the previous topology is shown in Fig. 3(a) [12]. In that case, three pairs of thyristors have been added to the basic structure of the NPC converter. The purpose of these new elements is to connect the faulty leg to the NP of the converter when any of its switches fail in open circuit.

Some other similar solutions have also been studied in [13]–[15]. In all those cases, the faulty leg can be connected to the NP of the converter under any fault condition, regardless of whether it is in open or short circuit. Consequently, it is not necessary to oversize the semiconductors because they do not have to withstand overvoltages. However, this also implies that the maximum modulation index is reduced to one half under any fault condition.

Different kinds of modulation strategies have been developed to control the converter when the faulty leg is connected to the NP. From the standpoint of the space-vector theory, Fig. 3(b) shows the available vectors when phase a is connected continuously to the NP. In order to generate sinusoidal three-phase voltages, only voltage vectors within the shadowed area can be generated.

Moreover, some strategies based on a carrier-based pulsewidth modulation (PWM) perspective have been developed. The main idea behind these strategies is to generate a set of voltages with a phase difference of 60°. For instance, if phase a fails, and it is hence connected continuously to the NP, the following set of reference voltages has to be generated:

$$\begin{aligned} v_{a0} &= 0 \\ v_{b0} &= A\sin\left(\omega t - \frac{5\pi}{6}\right) \\ v_{c0} &= A\sin\left(\omega t + \frac{5\pi}{6}\right). \end{aligned} \tag{1}$$

Under this assumption, a balanced set of line-to-line voltages is obtained as follows:

$$\begin{aligned} v_{ab} &= A\sin\left(\omega t + \frac{\pi}{6}\right) \\ v_{bc} &= A\sin\left(\omega t - \frac{\pi}{2}\right) \\ v_{ca} &= A\sin\left(\omega t + \frac{5\pi}{6}\right). \end{aligned} \tag{2}$$

Solution III: Another possible solution capable of coping with both short- and open-circuit faults is proposed in [16]

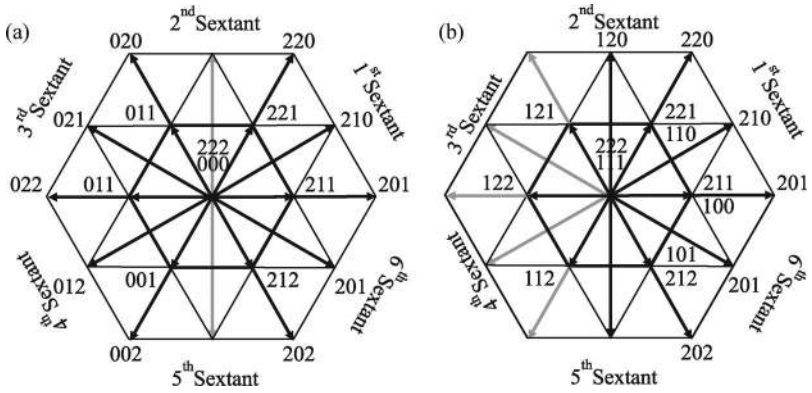

Fig. 2. Vector diagram when (a) S_{a4} fails and (b) S_{a3} fails.

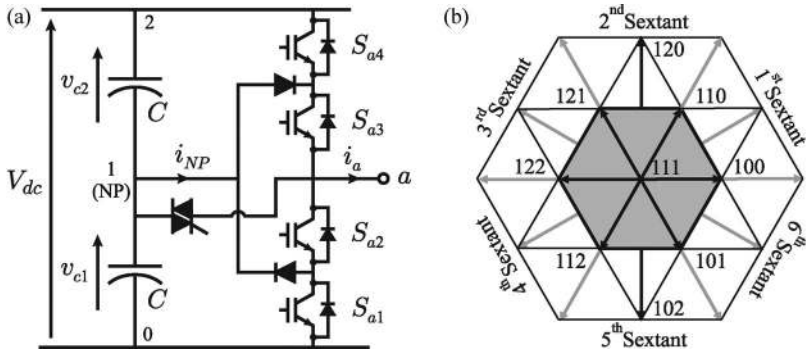

Fig. 3. (a) NPC fault-tolerant converter leg, solution II. (b) Vector diagram when phase a is connected to the NP.

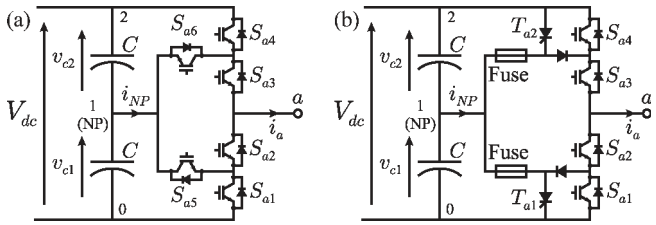

Fig. 4. NPC fault-tolerant converter leg. (a) Solution III. (b) Solution IV.

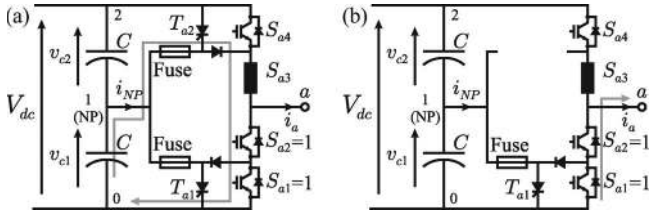

Fig. 5. (a) Transitory short-circuit when S_{a3} fails. (b) Reconfigured faulty leg.

[Fig. 4(a)]. This solution takes advantage of the additional IGBTs included in the topology and described in [17]. These additional switches introduce new redundant switching states which, during normal operating conditions, are used to balance power losses among devices. Therefore, a significant increase in the output power can be achieved.

Furthermore, it is also possible to take advantage of the additional switching states when any switch of one leg fails. In this case, the faulty phase is connected to the NP of the converter making use of the extra switches. Once the converter is reconfigured, the authors use a PWM modulation strategy with a set of modulation signals similar to those given by (1). Like in some of the former solutions, in this topology, it is not necessary to oversize the power semiconductors because they will not have to withstand overvoltages. However, the maximum modulation index under fault condition is reduced to one half.

Solution IV: In the previous solutions, the modulation index has to be reduced in fault operation mode. Due to this fact, those solutions are not well suited to working in grid-connected applications. In [18], an attempt to overcome this problem is made. Fig. 4(b) shows one of the solutions presented in this paper. Observe that some fast fuses and thyristors are added to the basic topology. The aim of these fuses is to avoid short circuits on the dc-bus capacitors due to the circulation path of the current established through the clamping diodes when a fault occurs. In addition, it is necessary to employ semiconductors which guarantee a short circuit in case of failure. These IGBTs are currently sold by various manufacturers (press-pack technology). Another possible alternative entails in connecting a pair of thyristors in parallel to each IGBT, which are activated to ensure a short circuit when there is a fault in the associated IGBT.

For example, if the switch S_{a3} fails in short circuit in this converter, a short circuit of the lower dc-bus capacitor takes place [Fig. 5(a)] at any time that a low voltage level is required at the output. To avoid this situation, it is necessary to activate the thyristor T_{a2}. This implies a transitory short circuit of the upper dc-bus capacitor, which blows the associated fuse. After that, the faulty leg is reconfigured, as shown in Fig. 5(b), and

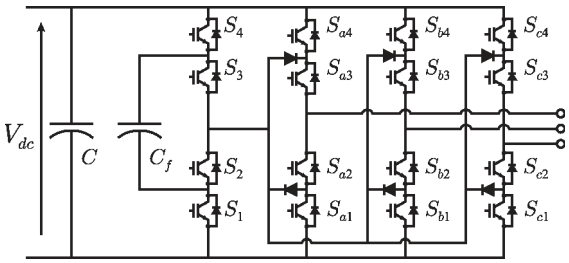

Fig. 6. Four-legged hybrid converter with FC.

it can switch between the upper and lower parts of the dc link. Therefore, the maximum modulation index is achieved.

Solution V: Another solution is presented in [18]. In this case, the topology is similar to the one proposed in [17] (Fig. 6) with the addition of six fast fuses in series with the clamping IGBTs. This solution has a behavior similar to the previous one. However, due to the additional switching states provided by the extra switches, the faulty leg is able to switch between the upper, medium, and lower voltage levels, even when a switch fails.

Another characteristic of the last two topologies is that they can withstand several faults per leg and even faults in two or three legs simultaneously. On the other hand, their main drawback is that the semiconductors have to be oversized in order to withstand the total dc-link voltage.

2) Four-Legged Topologies: The main advantage of the topologies introduced in the previous section is their simplicity. However, in all of them, after a fault, it is necessary to either reduce the working modulation index or oversize the semiconductors in order to withstand overvoltages, or both. This fact reduces the range of applications in which these solutions can be implemented.

There are other topologies in which, even after a fault, normal behavior of the converter can be guaranteed. These solutions are based on the addition of a fourth leg to the converter. The aim of this additional leg is to substitute the damaged phase after a fault. However, during normal operating conditions, this additional leg can also contribute to improving the behavior of the system. Some of these topologies are described as follows.

FC leg: Fig. 6 shows the basic structure of the solution presented in [19]. This solution is composed of three main legs (standard NPC structure), which are connected to the output phases, and a fourth leg with an FC structure. In normal operating mode, the aim of this additional leg is to provide a stiff NP voltage. To achieve this, the two switching states shown in Table I are used. Note that, by using these switching states, it is possible to control the voltage on the FC, which generates the NP voltage in this topology, regardless of the direction of the output current. This provides the converter with high flexibility because the modulation strategy of the three main legs no longer has to deal with the NP voltage balance issue. Therefore, it can focus on other aspects, such as decreasing the total harmonic distortion of the output voltages or minimizing the converter losses [20].

In order to endow this topology with fault-tolerant capability, it is necessary to add some extra switches (two IGBTs and three pairs of thyristors) and some fast fuses.

TABLE I
SWITCHING STATES, NP VOLTAGE, AND EFFECT OF THE NP CURRENT ON THE CAPACITOR VOLTAGE

S_1	S_2	S_3	S_4	V_{NP}	$i_{NP} > 0$	$i_{NP} < 0$
OFF	ON	OFF	ON	$V_{dc} - v_{Cf}$	$V_{Cf} \uparrow$	$V_{Cf} \downarrow$
ON	OFF	ON	OFF	v_{Cf}	$V_{Cf} \downarrow$	$V_{Cf} \uparrow$

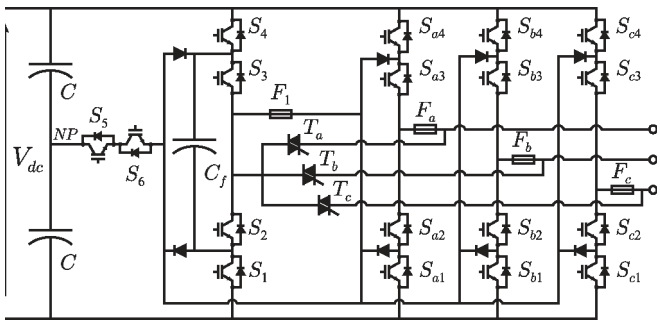

Fig. 7. Four-legged hybrid converter with FC. Fault-tolerant solution.

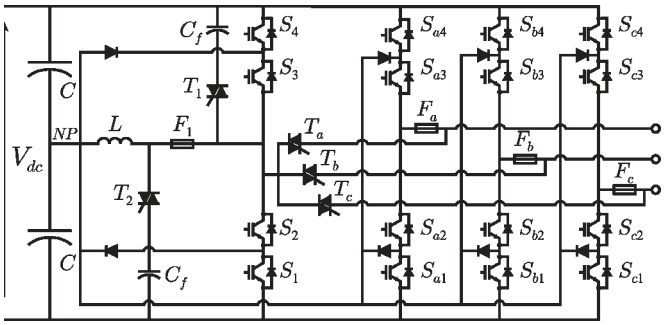

Fig. 8. Four-legged hybrid converter with inductance. Fault-tolerant solution.

Fig. 7 shows the complete solution. Once a failure in any of the switches of phase x (for $x = a, b, c$) has been detected, it is necessary to start the reconfiguration process of the converter. This implies blowing the fuses F_1 and F_x. In [19], this is accomplished using the switches of the converter. However, due to the difficulties on finding commercial fast fuses with an i^2t characteristic lower than the IGBTs, a more reliable solution could be obtained, introducing additional thyristors to blow the fast acting fuses (following a procedure similar to the one described in Solution IV). Once the fuses have been blown, it is necessary to activate S_5, S_6, and the pair of thyristors T_x. Subsequently, the faulty leg is substituted by the fourth leg, and the converter is reconfigured as a standard NPC converter.

Inductor-based fourth leg: Another four-legged solution is presented in [21] (Fig. 8). In this case, the fourth leg is connected to the NP of the converter through an inductance. As in the previous solution, under normal working conditions, this leg is used to provide a stiff NP voltage. This is achieved by controlling the current that is injected into and out of the NP through the inductance.

In the case of a failure of any IGBT, the faulty leg is substituted by the fourth leg, following a procedure similar to the one indicated for the preceding solution.

A slightly simpler solution can be derived by removing the inductance and the fast fuse F_1 in Fig. 8. In this case, the fourth

TABLE II
COMPARISON OF FAULT-TOLERANT TOPOLOGIES FOR NPC

	IGBT's rated at $V_{dc}/2$	IGBT's rated at V_{dc}	No. of Thyristors	No. of Fast Fuses	Price (p.u.)	Failures per year and 100,000 units	Output power (p.u.) after failure
Standard NPC	12	–	–	–	1	1,027	0
Solution I	6	6	–	–	1.3	5	0.5 or 1*
Solution II	12	–	6	–	1.1	7	0.5
Solution III	18	–	–	–	1.1	16	0.5
Solution IV	–	12	6	6	1.8	4	1
Solution V	6	12	6	6	1.9	5	1
4-leg with FC leg	18	–	6	4	1.7	17	1
4-leg with inductive leg	16	–	10	4	1.7	21	1

* Depending on the faulty switch.

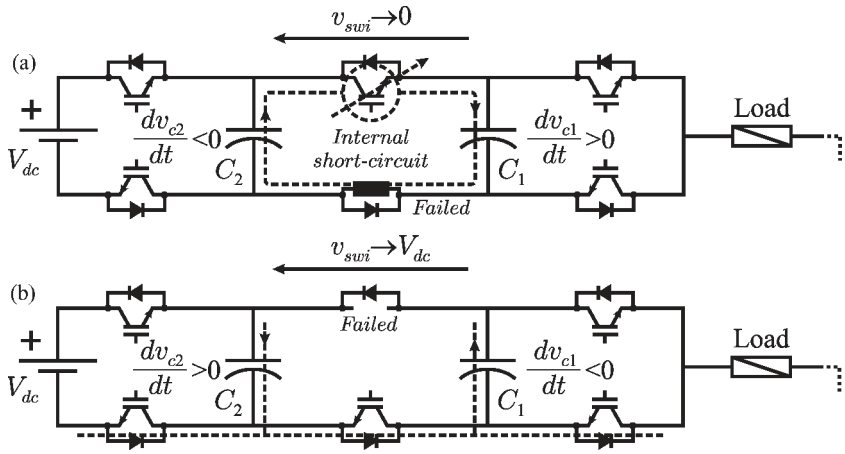

Fig. 9. Internal failure modes for a three-level FC inverter leg. (a) Short circuit. (b) Open circuit.

leg will be used only in the event of a fault. Therefore, this solution does not contribute to the NP voltage balance.

Finally, Table II shows the main features of the various NPC fault-tolerant topologies. In order to estimate the cost of the converters, only the prices of the semiconductor devices (IGBTs and thyristors) and the fast fuses have been considered. These prices are fully dependent on the system rated power and its voltage; therefore, the values shown in the table should be considered only as a rough reference. On the other hand, to estimate the reliability of the converters, a failure-in-time rate of 100 failures per billion hours has been considered for those IGBTs which have to withstand their rated voltage and 50 for those which have to withstand half of their rated voltage.

Notice that the price of the fault-tolerant topologies notably increases with respect to that of a standard NPC converter. However, even in the worst case, this price is still about 36% lower than the cost of adding a second converter to supply the system with fault-tolerant capabilities. In addition, the reliability of the system also increases drastically.

III. FAULTS IN FC INVERTERS

The FC converter is made of a series of imbricated cells, with an FC between them. Fig. 9 shows a typical three-cell (two FCs C_1 and C_2 on each output phase) inverter. Due to the series connection of switches, this topology allows the use of low voltage, fast, and robust IGBTs in high-voltage applications. Considering one leg, if quasi-identical duty cycles and regular phase shifts are applied to the control signals, an interleaved four-level output voltage is generated with an apparent switching frequency of three times the switching frequency of one cell [27]. Unlike the NPC inverter, two interesting properties should be noted. First, the topology offers a true capability of "online" series redundancy if the switch voltage rating is appropriate. Second, the current ripple through FCs is at the switching frequency which allows the use of low value and small size FCs.

A. Types of Fault

Only internal silicon failures, and the consequences resulting in stresses applied to the dies, or faulty control signals applied to switches will be analyzed. These failures induce high dynamics, and in general, these "critical" behaviors cannot be directly detected fast enough by the external sensors used by the control.

1) Internal Short-Circuit Failure Mode: In Fig. 9(a), the failure mode can result in a voltage breakdown, a thermal runaway of one die or an unwanted ON-state applied to the gate. Then, a short circuit appears inside the faulty cell. Depending on the faulty switch location, two different scenarios can occur.

1) Two FCs are connected in parallel through the faulty switch and its complementary switches. This is the case for a fault in the intermediate cell of Fig. 9(a).
2) One FC is forced to a fixed voltage value. This is the case for cell numbers 1 and 2, where C_2 is connected to $V_{\rm dc}$ or C_1 is connected to zero, respectively.

TABLE III
INTERNAL SHORT-CIRCUIT STRESS FOR A THREE-CELL FC CONVERTER

	Short-circuit on intermediate cell	Short-circuit on first or last cell
Energy stress	$CV_{swi}^2/4$	$CV_{swi}^2/2$
Transient over-voltage stress on non-faulty cells	50%	100%
Steady-state over-voltage stress on non-faulty cells including capacitors	50%	50%
Stresses numerical calculation V_{swi}= 600V - 20kHz C = 40μF	3.6J – 300V	7.2J – 600V

Then, a high short-circuit current flows through the capacitors, causing a rapid increase of the capacitor voltage at the output of the faulty cell and a decrease of the capacitor voltage at the input of the phase, until the voltage across the active switch reaches zero. The energy stress inside the faulty cell and the voltage dynamic stresses across the other switches are different, depending on the localization and the type of short-circuit failure. Table III summarizes the stresses based on numerical calculation.

In a fault, energy management is an important point, avoiding the permanent failure of the two switches inside the faulty cell, reducing the risk of bond-wire liftoff and the possible explosion of cases. Considering the basic waveforms of the converter, the maximum energy density to be considered for safe operation can be easily calculated, based on

$$\frac{V_{\rm dc}J}{2XF_{\rm sw}p^2} < 3\ \text{J/cm}^2 \tag{3}$$

where $V_{\rm dc}$ is the main dc-link voltage, J is the nominal current density through a die, X is the nominal and relative voltage ripple across a die, $F_{\rm sw}$ is the switching frequency of a cell, and p is the number of cells. A good practical value of the energy density capability of a 1.2-kV die is 3 J/cm^2.

Dynamic overvoltage management is another important point. It can be obtained by a *Transil* diode directly across switches or through a feedback connection anode gate, as an active clamping device [28]. Concerning the permanent overvoltage stress across switches and capacitors, overrating is given by the quantity $1/(p-1)$, p being the number of initial active cells. A sufficient number of cells are clearly required in series unless a reduced dc voltage is used at nominal operation. Here again, three cells are the minimal series connection number.

Fig. 10(a) shows the dynamic behavior under a short-circuit fault. A high current ripple and the imperfect balancing of the FC(s) are observed. Note, however, that the fundamental output component is unchanged with any current transient in the load. Even if the fail-safe management seems possible, the fault detection and the reconfiguration of the control signals are required to optimize the output voltage and to rebalance the voltage across the active switches.

It appears that very high power/voltage converters at low switching frequency could not respect (3), and in this case, the designer has to tolerate the destruction of one or two switches if

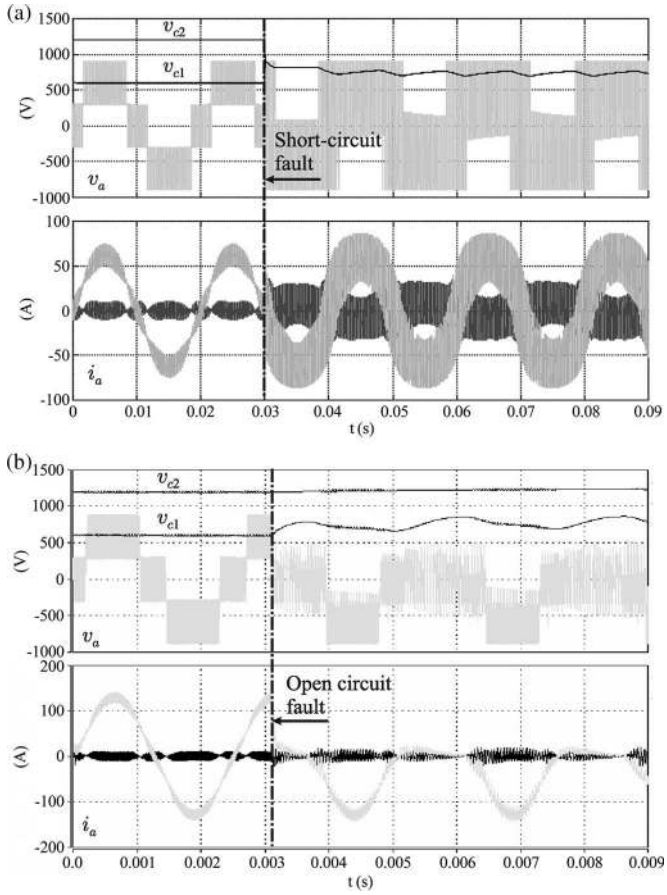

Fig. 10. Output voltage of a three-level FC inverter leg. (a) Short circuit. (b) Open circuit.

a short-circuit fault occurs. These failed dies will have to sustain a current probably through a small melting pit as a craterlike [29], and the designer could preferably choose a bondingless case such as bump-based or press-pack packaging [30].

2) Internal Open-Circuit Failure Mode: In Fig. 9(b), the open-circuit failure mode can result from a driver breakdown or the disconnection of digital control line. Unlike the short circuit, this fault causes a permanent and slow increase of the capacitor voltage at the input of the faulty cell. At the same time, it causes a permanent and slow decrease of the voltage capacitor at its output, until the voltage across the active switch reaches $V_{\rm dc}$, which is an excessive and probably destructive stress.

Fig. 10(b) shows the dynamic behavior under the open-circuit fault mode. Note that half of the current waveform is lost. Moreover, the voltage at C_2 can reach an unsafe value, which can lead to a larger fault. From this point of view, it is not very practical to continue the operation; thus, stopping all the control signals of the faulty leg seems mandatory. Then, postcontinuation could only be realized by a parallel active or passive redundancy.

B. Fault Diagnosis

Diagnosis and management are different according to the type of fault. For an open-circuit failure, the decrease of the output voltage and current can be easily detected by classical sensors, and a safe stop could be realized. On the other hand,

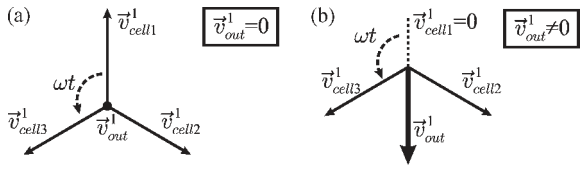

Fig. 11. Vector diagram of the voltage harmonics at the switching frequency. (a) Before failure. (b) After failure.

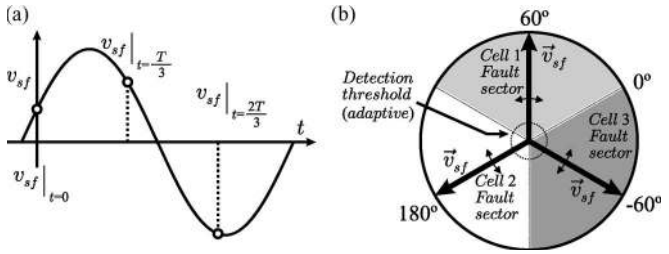

Fig. 12. Principle of the vector-based diagnosis. (a) Sampling of the switching component $v_{\rm sf}$. (b) Areas for faulty cell identification.

as shown in Section III-A1 for a short-circuit fault, the FC can keep operating after the fault, as shown in Fig. 10(a). However, for an optimum postfault operation, proper fault detection and localization must be achieved. An interesting idea, which seems general for all interleaved converters, is that a fault always induces a noncompensation of the output voltage harmonic (for a series connection) or the input current harmonic (for a parallel connection) at the cell switching frequency $f_{\rm sf}$. Then, the detection of a high magnitude of this harmonic appears to be a suitable approach for the series' ML FC converter fault detection algorithm, while its phase can be used to locate the faulty cell. Moreover, this approach requires only one voltage sensor per output phase.

Fig. 11(a) shows the normal behavior of the phasors at $f_{\rm sf}$, while Fig. 11(b) shows the noncompensated component for a short circuit in cell 1. Fig. 12 shows the principle of the diagnosis procedure: The output voltage is filtered through a bandpass filter tuned at $f_{\rm sf}$, three values spaced at 120° are sampled, and a $3\phi/2\phi$ transformation is applied to obtain a vector representation as defined by

$$\vec{v}_{\rm sf} = \frac{2}{3}\left(v_{\rm sf}\Big|_{t=0} + v_{\rm sf}\Big|_{t=\frac{T}{3}} e^{-j\frac{2\pi}{3}} + v_{\rm sf}\Big|_{t=\frac{2T}{3}} e^{j\frac{2\pi}{3}}\right). \quad (4)$$

An adaptive threshold on the three sectors is included to account for the influence of slightly different duty cycles on the harmonic magnitude and to safely detect and localize the faulty cell. A more detailed implementation is presented in [4]. For a greater number of cells (four, five, ...), the angle of the sectors is reduced, and localizing the fault can be difficult and unreliable with this method. In such a case, a direct diagnosis could be performed, owing to the $V_{\rm cesat}$ monitoring included in each gate driver.

C. Modulation and Control Technique

Following the diagnosis, the reconfiguration of the control signals consists of applying the suitable phase shift of the carriers to the remaining operative switches, in order to maintain

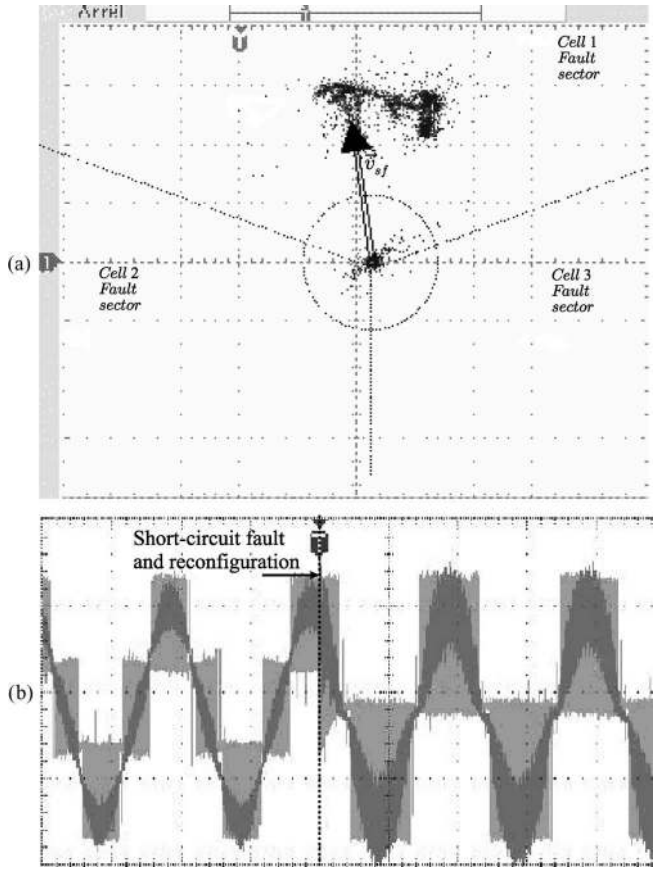

Fig. 13. (a) Practical diagnosis of a short-circuit fault applied over one cell to a three-cell/four-level inverter. (b) Three-cell → two-cell reconfiguration by means of the rephase shifting $2\pi/3 \rightarrow \pi/2$.

an optimal interleaved output voltage in postfault mode and to balance the voltage across all switches. For a three-cell converter, the optimum phase shift is $2\pi/3$ before the fault; it becomes $\pi/2$ after a short-circuit fault.

Finally, Fig. 13(a) shows the practical diagnosis of a short-circuit fault applied to one cell of a three-cell FC converter, with an effective switching frequency at a load of 3×16 kHz; following the three-cell → two-cell reconfiguration, the carrier phase shift is changed from $2\pi/3$ to $\pi/2$.

Unlike the NPC fault operation and the NP reconfiguration, the FC converter allows the use of a full modulation index at the cost of an overvoltage rating of all switches and capacitors, as detailed in Section III-A. Even if this condition is realized, the power level should be reduced in postfault operation at least for two reasons.

1) The overvoltage across the switches increases switching losses on the dies, and the load current should be reduced.
2) The spike voltage at turnoff can be higher that the voltage margin and, here again, the load current should be reduced to offer a fail-safe remedial operation.

IV. Faults in CM Inverters

A. Fault Diagnosis

1) Detection Based on Waveform Analysis: In fault operation, unexpected signal values are observed. In [9], the total

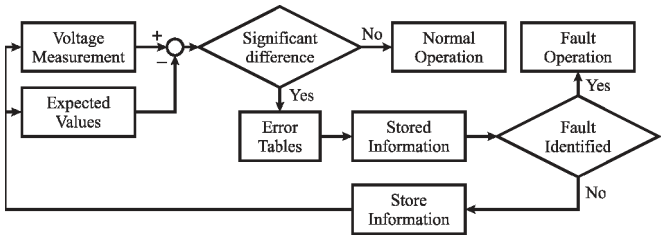

Fig. 14. General scheme for a fault detection system based on voltage waveform.

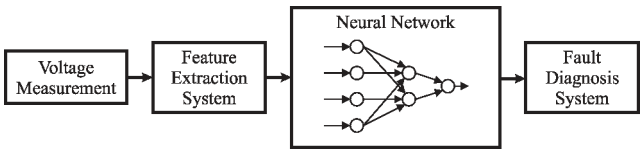

Fig. 15. General scheme for a fault detection system based on AI.

output phase voltage, e.g., v_{ao} in Fig. 17, is measured and compared with its expected value v_{ao}^{*}. In normal operation, both values are very similar; however, depending on the fault, large differences can be observed. These values can be tabulated to obtain information about the specific fault. Some faults produce similar effects on the voltage; thus, for proper fault identification, more than one step is required, and information from previous steps must be used, as shown in Fig. 14.

2) Use of AI Algorithms: In [6], the use of artificial intelligence (AI) algorithms, due to their ability to recognize patterns, is proposed to detect and identify faults in a CM inverter. The basic scheme is shown in Fig. 15. First, as in the previous method, the total output phase voltage is measured. Then, a series of mathematical algorithms like fast Fourier transform and correlations are applied to the measured data. This step is called feature extraction system (FES), and it allows the number of inputs and the size of the NN to be reduced, thereby simplifying the system and also reducing the NN training time.

Once the FES process has been completed, the NN analyzes the data and, if applicable, detects the fault. Note that the behavior of the NN will depend on the selection of the FES process, its own structure, and the training process. According to [6], the detection time is about 100 ms (six to ten times the fundamental period).

3) Detection Based on Spectral Analysis: Based on the same principle used in Section III-B, in [5], a detection method based on the spectral analysis of the total output phase voltage is used. In normal operation and using a phase-shift modulation strategy, the total output voltage on each phase will commutate at nf_s, where n is the number of series-connected cells and f_s is the switching frequency of each cell. Moreover, no significant component at f_s should be present in v_{ao}. In fault, however, a significant component at f_s appears in v_{ao}, indicating not only a fault in the phase but also the faulty cell. To do this, a discrete Fourier transform (DFT) focused on the f_s component is applied to v_{ao}, in order to calculate the magnitude and phase of its component at f_s. This value is compared with its expected value, which is estimated by a model based on the converter harmonic behavior plus a small offset signal to overcome unmodeled effects. If the measured magnitude is higher than the estimated value, the fault is detected, while the faulty cell is determined by calculating the angle of the measured f_s component though the DFT data, as shown in Fig. 16.

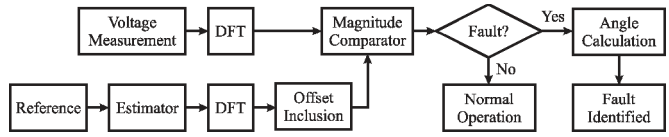

Fig. 16. General scheme for a fault detection system based on spectral analysis.

TABLE IV
FAULT DETECTION ALGORITHMS FOR CM COMPARISON

Method	Detection Speed	Computational Cost	Conceptual Complexity
Waveform Analysis	Normal	Low	Simple
AI Algorithms	Slow	High	Normal
Spectral Analysis	Fast	High	Hard

For internal short-circuit faults, a detection time about one sample time $(1/nf_s)$ is reached, while for open-circuit fault, the detection time will be between one sample time and a half fundamental period, depending on the fault instant.

Table IV summarizes the main characteristics of the fault detection algorithms described.

B. Hardware Solutions

1) Use of a Redundant Cell: The concept of redundant components has widespread use in power electronics. However, due to the high number of elements that an ML converter requires, in most of the cases, it is not an option. An alternative approach is presented in [22], where no redundant components but cells are used, as shown in Fig. 17. In this way, the number of extra components does not dramatically increase, while the reliability of the converter is not compromised. When a cell faults, it is isolated from the system by using the bypass switch T shown in Fig. 18, which changes from normal position n to fault position f. After that, the redundant cell becomes operative, reestablishing the normal operation.

According to [22], this solution allows the reliability to be almost the same with that using redundant power switches for each semiconductor but uses minimum additional hardware.

C. Modulation and Control Techniques

If the fault cannot be compensated by redundant hardware, control and modulation techniques can be applied to sustain the operation.

1) Bypass Operative Cells: When a fault occurs, the number of operative cells per phase is no longer the same; thus, unbalanced output voltages are applied to the load. A simple way to recover the balanced operation is to bypass as many cells as necessary, in order to operate with the same number of cells on each phase. Fig. 19 shows the fasorial diagram of an 11-level CM inverter operating in normal conditions [Fig. 19(a)] and

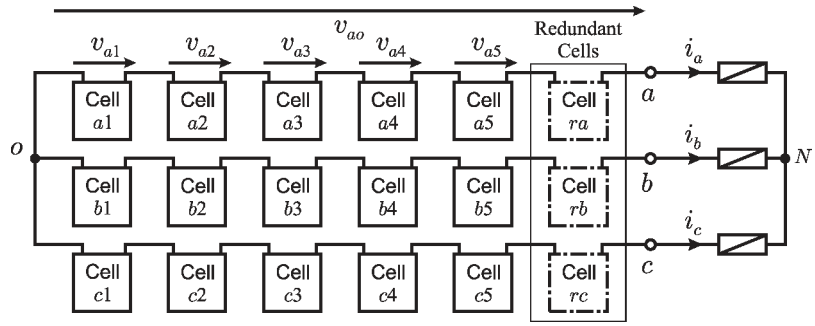

Fig. 17. CM inverter with redundant cells.

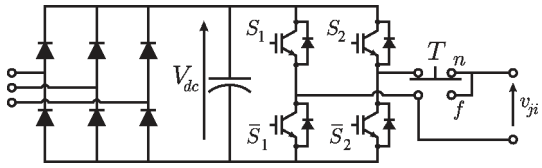

Fig. 18. CM cell with bypass switch T.

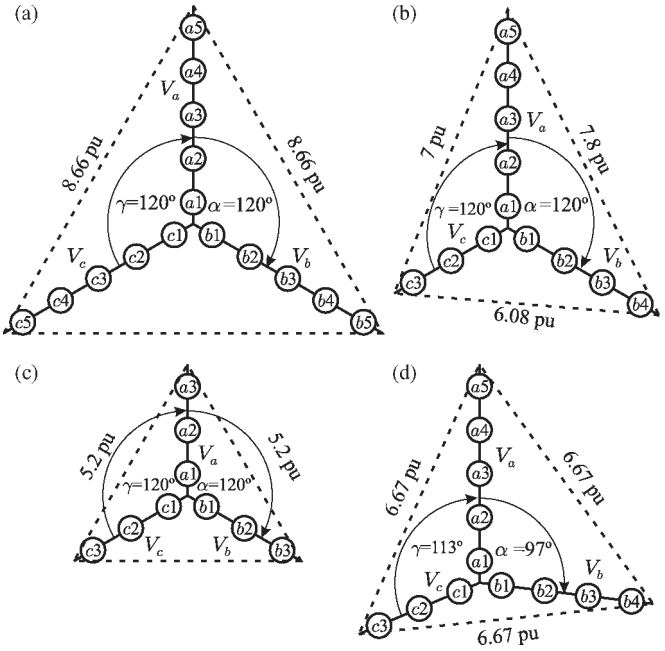

Fig. 19. FPSC in an 11-level CM converter. (a) Normal operation. (b) Unbalanced operation with one faulty cell in phase b and two cells in phase c. (c) Balanced operation by bypassing operative cells. (d) Balanced operation by using FPSC.

operating with three faulty cells, one in phase b and two in phase c [Fig. 19(b)]. Clearly, under a fault, nonbalanced line-to-line, and hence load, voltages are obtained. Then, to restore the balanced operation, three operative cells are bypassed: two in phase a and one in phase b, obtaining a 40% lower balanced voltage in the load, as shown in Fig. 19(c).

2) FPSC: In [31]–[33], the phase shift between the voltage references is modified to overcome the unbalanced voltage magnitude provided by the inverter phases, using all the operative cells. Using this concept, a larger balanced load voltage is obtained, as shown in Fig. 19(d), where the voltage under fault is only 23% lower than the full operative converter.

The optimum phase-shift angles for different faults can be obtained from

$$\hat{v}_a^2 + \hat{v}_b^2 - 2\hat{v}_a\,V_b\cos(\alpha) = \hat{v}_b^2 + \hat{v}_c^2 - 2\hat{v}_b\,\hat{v}_c\cos(\beta) \quad (5)$$

$$= \hat{v}_c^2 + \hat{v}_a^2 - 2\hat{v}_c\,\hat{v}_a\cos(\gamma) \quad (6)$$

$$\alpha + \beta + \gamma = 360^\circ \quad (7)$$

where $\hat{v}_a = \|V_a\|$, $\hat{v}_b = \|V_b\|$, $\hat{v}_c = \|V_c\|$, $\alpha = \angle(\vec{v}_a, \vec{v}_b)$, $\beta = \angle(\vec{v}_b, \vec{v}_c)$, and $\gamma = \angle(\vec{v}_c, \vec{v}_a)$.

As this system is nonlinear and the number of possible faults is limited, the use of a precalculated angle table is recommended. In [34], however, an online control structure that performs the balancing operation is proposed, based on common-mode signal injection concept. Finally, additional considerations and limitations of fundamental phase-shift compensation (FPSC) are detailed in [35], regarding large faults and the effect of output power factor (PF) in the behavior of the converter.

Fig. 20 shows the experimental results for an 11-level MC converter with five faulty cells, two in phase b and three in phase c. It can be clearly appreciated how the line-to-line voltages and load currents are highly unbalanced due to the fault and how they are rebalanced when the FPSC is applied, even with unbalanced converter voltages.

3) Use of Redundant States: A well-known characteristic of ML converters is that they have many redundant states. These states can be easily used to overcome fault operation, specially when vectorial approach, defined by

$$\vec{v} = \frac{2}{3}\left(v_a + v_b\,e^{-j\frac{2\pi}{3}} + v_c\,e^{-j\frac{4\pi}{3}}\right) \quad (8)$$

is used.

In [23]–[25], the space-vector modulation (SVM) algorithm is used. As usual, the three vectors nearest to the reference are located ($\vec{v}_x$, $\vec{v}_y$, and $\vec{v}_z$ in Fig. 21), and the proper times for those vectors are calculated. This information is sent to the modulator, which chooses, according to some prefixed criteria, a switch combination that generates the desired output voltage.

When a fault occurs, all the switching combinations that use the faulty cells are considered as invalid combinations, and they are not used by the modulator in the switch selector step, as shown in Fig. 21.

A similar approach is used in [26], where a space-vector control [36] modulation is used. In this case, the modulator uses the vector that is closer to the reference, $\vec{v}_y$ in Fig. 21(b), applying a valid combination along the whole sample period, reducing the commutation losses.

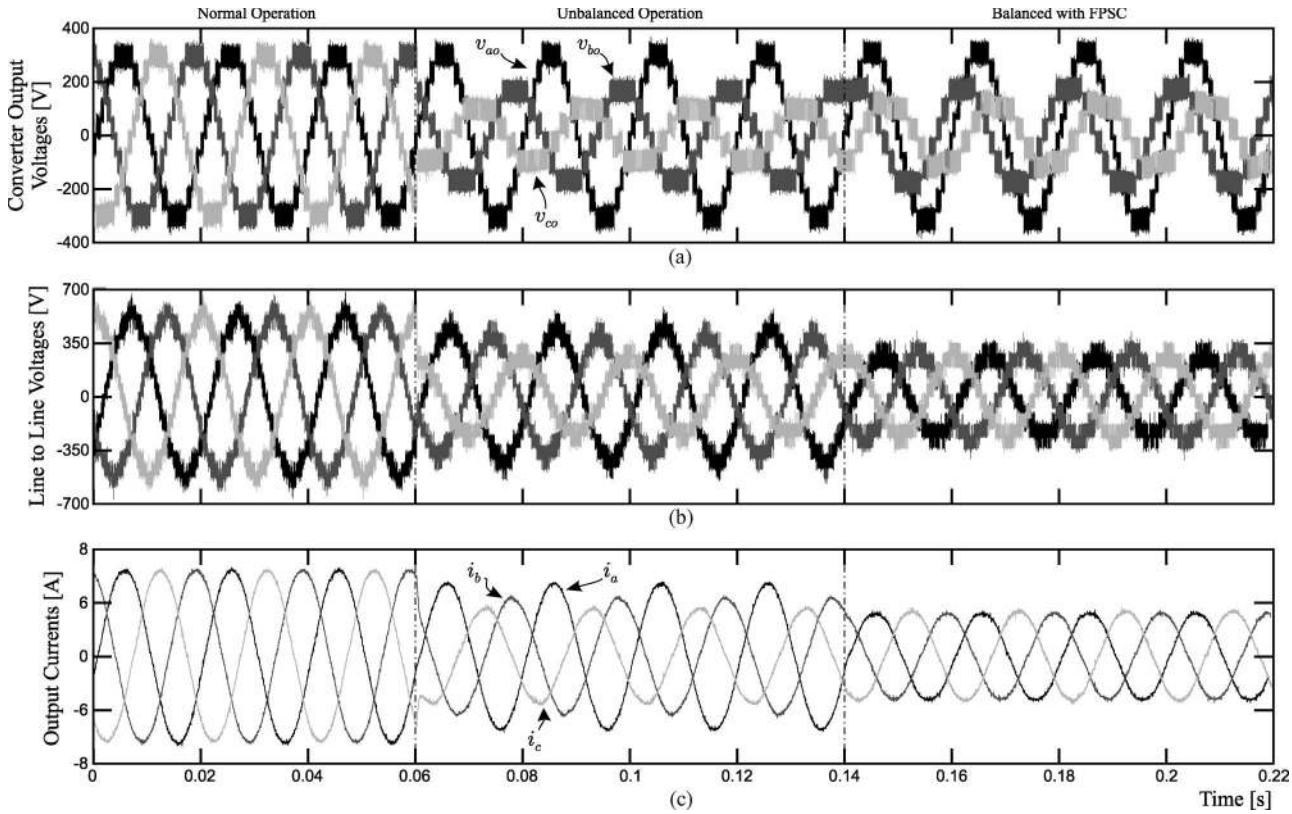

Fig. 20. Experimental results for an 11-level CM with five faulty cells, two in phase b and three in phase c. (a) Converter output voltages. (b) Line-to-line voltages. (c) Load currents.

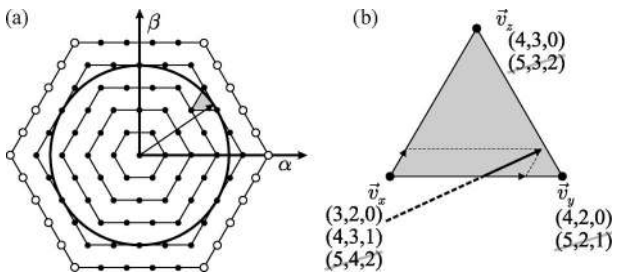

Fig. 21. Eleven-level CM inverter with a faulty cell in phase a. (a) Vectorial representation. (b) Redundant and forbidden states for an SVM with a faulty cell in phase a.

Note, however, that, using either of the previously presented solutions, the maximum output voltage vector that can be generated is lower than in normal operation, and its new maximum value will depend on the fault.

4) Control of the DC-Link Voltage: The CM inverter has been used as STATCOM in many works [37]–[39]; in such applications, H-bridge inverters are used as active rectifiers controlling the H-bridge current, to improve the PF of the overall system, and the dc-link voltage on each cell. This additional degree of freedom is used in [22]. When a fault is detected, the reference of the operative cells in the same phase is increased in such a way that the total phase voltage prior to and after the fault is the same. As a direct consequence of this, the dc-link voltage controller increases the active current reference i_a^*, as shown in Fig. 22. Both reactive and active currents (i_r and i_a, respectively) are controlled by an inner current control loop, which generates the gate signals for the converter. Note that, for

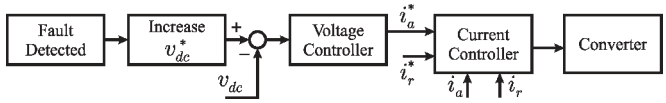

Fig. 22. General control scheme for operation under fault with controlled dc-link capability converters.

a proper operation, the converter components must be overrated in voltage and current to operate with the new dc-link voltage.

A similar concept is used in [40], where three-phase active rectifiers are used at the input of each cell, and then, control over the input currents and dc-link voltage of each cell is obtained. In this paper, the change in the dc-link reference is complemented with an FPSC strategy, allowing to share the dc-link voltage increase among all the converter operative cells, significantly reducing the overrate of the converter components.

V. Conclusion

This paper has shown that it is not necessary to measure the condition of each semiconductor to properly detect a fault in an ML converter. The availability of powerful microprocessors permitted the development of very intelligent strategies to identify faults quickly, using a reduced number of sensors, by measuring the converter output signals (voltage or current in the load).

This paper has established that reliability design is not sufficient for high-power converters with a great number of switches. Fault modes have to be safely managed by using the additional degrees of freedom for each topology. Fortunately, for ML converters, a large number of redundant states are

available, which can be exploited by using appropriate modulation and/or control, providing to the load high-quality signals and reasonable power even under fault operation.

All ML topologies are able to operate under fault conditions. For the NPC, many topology modifications have been proposed for operation in reduced, or even nominal, conditions. From the presented topologies, the FC is the only one that can operate at a nominal rate under fault without requiring additional hardware. However, its semiconductors and capacitors must be properly rated to deal with the dynamic and static overvoltage due to the fault. Finally, the CM expands the traditional concept of hardware redundancy, by using redundant cells instead of individual semiconductors and/or capacitors, which dramatically reduces the complexity of the design and the number of components.

Fault detection and operation are in continuous development. Among the unresolved problems are the stability of the short-circuit failure of a die according to stress after a fault in an FC, fault in NPC converters of five levels (or greater), fault in asymmetrical CM converters, and the dynamics along the transition from normal to faulty operation. Notice that additional tests, under full power operation in industrial installations, should be done in order to fully validate the strategies presented in this paper. However, the results presented based on laboratory prototypes give important information about the expected performance.

REFERENCES

[1] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] L. G. Franquelo, J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[4] F. Richardeau, P. Baudesson, and T. A. Meynard, "Failures-tolerance and remedial strategies of a PWM multicell inverter," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 905–912, Nov. 2002.

[5] P. Lezana, R. Aguilera, and J. Rodríguez, "Fault detection on multicell converter based on output voltage frequency analysis," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2275–2283, Jun. 2009.

[6] S. Khomfoi and L. M. Tolbert, "Fault diagnosis and reconfiguration for multilevel inverter drive using AI-based techniques," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2954–2968, Dec. 2007.

[7] H.-I. Son, T.-J. Kim, D.-W. Kang, and D.-S. Hyun, "Fault diagnosis and neutral point voltage control when the 3-level inverter faults occur," in *Proc. 35th IEEE Annu. Power Electron. Spec. Conf.*, Jun. 2004, vol. 6, pp. 4558–4563.

[8] E. R. da Silva, W. S. Lima, A. S. de Oliveira, C. B. Jacobina, and H. Razik, "Detection and compensation of switch faults in a three level inverter," in *Proc. 37th IEEE Annu. Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–7.

[9] G. Brando, A. Dannier, A. Del Pizzo, and R. Rizzo, "Quick identification technique of fault conditions in cascaded H-bridge multilevel converters," in *Proc. ACEMP*, Sep. 2007, pp. 491–497.

[10] S. Li and L. Xu, "Fault-tolerant operation of a 150 kW 3-level neutral-point clamped PWM inverter in a flywheel energy storage system," in *Conf. Rec. 36th IEEE IAS Annu. Meeting*, Sep./Oct. 2001, vol. 1, pp. 585–588.

[11] G. Sinha, C. Hochgraf, R. H. Lasseter, D. M. Divan, and T. A. Lipo, "Fault protection in a multilevel inverter implementation of a static condenser," in *Conf. Rec. 30th IEEE IAS Annu. Meeting*, Oct. 1995, vol. 3, pp. 2557–2564.

[12] S. Li and L. Xu, "Strategies of fault tolerant operation for three-level PWM inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 933–940, Jul. 2006.

[13] G.-T. Park, T.-J. Kim, D.-W. Kang, and D.-S. Hyun, "Control method of NPC inverter for continuous operation under one phase fault condition," in *Conf. Rec. 39th IEEE IAS Annu. Meeting*, Oct. 2004, vol. 4, pp. 2188–2193.

[14] J.-J. Park, T.-J. Kim, and D.-S. Hyun, "Study of neutral point potential variation for three-level NPC inverter under fault condition," in *Proc. 34th IEEE IECON*, Nov. 2008, pp. 983–988.

[15] J.-C. Lee, T.-J. Kim, D.-W. Kang, and D.-S. Hyun, "A control method for improvement of reliability in fault tolerant NPC inverter system," in *Proc. 37th IEEE Annu. Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–5.

[16] J. Li, S. Bhattacharya, and A. Q. Huang, "Three-level active neutral point clamped (ANPC) converter with fault tolerant ability," in *Proc. 24th Annu. IEEE Applied Power Electron. Conf.*, Feb. 2009, pp. 840–845.

[17] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, Jun. 2005.

[18] S. Ceballos, J. Pou, E. Robles, J. Zaragoza, and J. L. Martin, "Performance evaluation of fault tolerant neutral-point-clamped converters," *IEEE Trans. Ind. Electron.*, to be published. [Online]. Available: http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5166482&queryText%3D%28%28ceballos%29+AND+robles%29%26openedRefinements%3D*%26matchBoolean%3Dtrue%26searchField%3DSearch+All

[19] S. Ceballos, J. Pou, E. Robles, I. Gabiola, J. Zaragoza, J. L. Villate, and D. Boroyevich, "Three-level converter topologies with switch breakdown fault-tolerance capability," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 982–995, Mar. 2008.

[20] S. Ceballos, J. Pou, J. Zaragoza, J. L. Martin, E. Robles, I. Gabiola, and P. Ibanez, "Efficient modulation technique for a four-leg fault-tolerant neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1067–1074, Mar. 2008.

[21] S. Ceballos, J. Pou, J. Zaragoza, E. Robles, J. L. Villate, and J. L. Martin, "Soft-switching topology for a fault-tolerant neutral-point-clamped converter," in *Proc. IEEE ISIE*, Jun. 2007, pp. 3186–3191.

[22] W. Song and A. Q. Huang, "Control strategy for fault-tolerant cascaded multilevel converter based STATCOM," in *Proc. 22nd IEEE Applied Power Electron. Conf.*, Feb. 2007, pp. 1073–1076.

[23] S. Wei, B. Wu, F. Li, and X. Sun, "Control method for cascaded H-bridge multilevel inverter with faulty power cells," in *Proc. 18th IEEE Applied Power Electron. Conf.*, Feb. 2003, vol. 1, pp. 261–267.

[24] P. Correa, M. Pacas, and J. Rodríguez, "Modulation strategies for fault-tolerant operation of H-bridge multilevel inverters," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 2006, vol. 2, pp. 1589–1594.

[25] P. Correa and J. Rodríguez, "Control strategy reconfiguration for a multilevel inverter operating with bypassed cells," in *Proc. IEEE ISIE*, Jun. 2007, pp. 3162–3167.

[26] Y. Zang, X. Wang, B. Xu, and J. Liu, "Control method for cascaded H-bridge multilevel inverter failures," in *Proc. 6th WCICA*, Jun. 2006, vol. 2, pp. 8462–8466.

[27] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. 23rd IEEE Annu. Power Electron. Spec. Conf.*, Jun./Jul. 1992, pp. 397–403.

[28] P. Baudesson, "Sûreté de fonctionnement des convertisseurs multicellulaires série," Ph.D. dissertation, Enseeiht, INP Toulouse, Plasma Energy Convers. Lab., Toulouse, France, 2000.

[29] W. Wu, C. Fan, Y. Wang, Y. Wang, X. Cui, P. Jacob, and M. Held, "SEM investigation on IGBT latch-up failure," in *Proc. 6th Int. Conf. Solid-State Integr.-Circuit Technol.*, Oct. 2001, vol. 2, pp. 1040–1042.

[30] S. Gunturi and D. Schneider, "On the operation of a press pack IGBT module under short circuit conditions," *IEEE Trans. Adv. Packag.*, vol. 29, no. 3, pp. 433–440, Aug. 2006.

[31] P. W. Hammond, "Multiphase power supply with series connected power cells with failed cell bypass," U.S. Patent 6 222 284, Apr. 24, 2001.

[32] P. W. Hammond, "Enhancing the reliability of modular medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 948–954, Oct. 2002.

[33] J. Rodríguez, P. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. J. Escobar, "Operation of a medium-voltage drive under faulty conditions," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1080–1085, Aug. 2005.

[34] S. Wei, B. Wu, S. Rizzo, and N. Zargari, "Comparison of control schemes for multilevel inverter with faulty cells," in *Proc. 30th IEEE IECON*, Nov. 2004, vol. 2, pp. 1817–1822.

[35] P. Lezana and G. Ortiz, "Extended operation of cascade multicell converters under fault condition," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2697–2703, Jul. 2009.

[36] J. Rodríguez, L. Moran, P. Correa, and C. Silva, "A vector control technique for medium-voltage multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 882–888, Aug. 2002.

[37] C. K. Lee, J. S. K. Leung, S. Y. R. Hui, and H. S. H. Chung, "Circuit-level comparison of STATCOM technologies," *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 1084–1092, Jul. 2003.
[38] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1512–1521, Oct. 2006.
[39] S. Yonetani, Y. Kondo, H. Akagi, and H. Fujita, "A 6.6-kV transformerless STATCOM based on a five-level diode-clamped PWM converter: System design and experimentation of a 200-V 10-kVA laboratory model," *IEEE Trans. Ind. Appl.*, vol. 44, no. 2, pp. 672–680, Mar. 2008.
[40] P. Lezana, G. Ortiz, and J. Rodríguez, "Operation of regenerative cascade multicell converter under fault condition," in *Proc. 11th Workshop COMPEL*, Aug. 2008, pp. 1–6.

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