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Survey on Single Stage Amplifiers for Column Drivers in Active Matrix LCD Panels Leading to a Highly Linear Rail-to-Rail Robust Amplifier

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ABSTRACT This paper reviews single stage amplifiers identified in the literature as well as presents a new structure single stage highly linear rail-to-rail amplifier intended for column drivers in Active Matrix Liquid Crystal Display (AMLCD). The new proposed amplifier is based on applying current splitting technique on a rail-to-rail differential pair thus elevating the overall performance of the amplifier in terms of different performance parameters such as effective transconductance, output resistance, DC gain and unity gain frequency among others. One major advantage of the new proposed amplifier is its capability of providing a rail-to-rail stable operation without the need for compensation. The performance of the new proposed amplifier is tested on LTspice using 90nm CMOS technology under 1 Volts supply voltage and compared to other existing single stage amplifiers. Simulation results shows that the proposed amplifier provides a high DC gain, high effective transconductance and high output resistance while maintaining a stable operation with a phase margin of 80°. Obtained results also confirms that the amplifier exhibits rail-to-rail operation while maintaining a very low Total Harmonic Distortion (THD). The pulse response of the proposed amplifier indicates a fast response with a rise time and fall times almost twice as fast as the other examined topologies. Against Process, Voltage and Temperature (PVT) variations, the amplifier exhibits a robust performance as the DC gain variation range was within 20% only which is much less than the other examined topologies.

INDEX TERMS Highly linear, rail-to-rail, stable, current splitting, PVT, robust.

I. INTRODUCTION

For decades, Cathode Ray Tube (CRT) displays were dominating the market and providing an attractive performance in terms of quality, speed and resolution [1]. However, in the mid 90's flat panel displays were introduced and dominated the market ever since [2]. The first successful flat panel was the plasma displays, which provided higher image quality when compared to CRT technology [3]. However, it was not successfully utilized in small portable applications. Finally, the development of Thin Film Transistor Active Matrix Liquid Crystal Displays (TFT AMLCD), which utilizes a transistor in each pixel to switch ''ON'' or ''OFF'' the pixel, was a high point in the displays industry as it was applicable to small, medium as well as large display applications [4].

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The rapid development in this area in the past years tightened the requirements and led to higher demand on low power, low cost, low area display panels that also maintain high performance and quality of display [5]. Several technologies were introduced recently such as LED TVs and then OLED TVs. LED TVs working principal is exactly the same as an LCD display, the only difference is that LEDs is used as a backlight unit placed either in the back of the panel or on the sides of the panel to emit light instead of Cool Compound Fluroscent Lamps (CCFL) [6], [7]. The use of LEDs reduces the power consumption of the light unit in the panel making it more energy efficient [7]. However, the remaining parts in LED displays are exactly the same as in a conventional LCD display, which is why an LED TV can also be referred to as an LCD TV [6].

On the other hand, OLED TVs work in a slightly different manner as each pixel is capable of emitting light by itself [8].

This eliminates the need to a backlight unit wither CCFL lamps of LEDs allowing the panel to be much thinner than LCD and LED displays [9]. This technology also uses active matrix addressing technique with the incorporation of TFTs in each pixel while also addressing each pixel through the use of a row and a column drivers [10]. Both the LED and OLED TV technologies are still a strong competitive in the market nowadays, each with its own pros and cons. However, the main focus of this paper is the LCD (also referred to as LED) TV technology mainly because it has a competitive edge in terms the variety of sizes it comes in, its price as well as its life span [11].

To meet the tight demands of the market, it is crucial to develop proper driving schemes to insure the highest display quality and lowest power consumption [12]. Considering that pixels are driven through the use of row and column drivers [13]. Where column drivers deliver image data to each pixel, thus column drivers are a crucial part of the driving system [12]. There are several architectures available for column drivers intended for AMLCD, however they all share the same main parts which includes: registers, latches, level shifters, digital to analog converters and channel buffers [12]–[15]. The performance of the channel buffers directly affect the performance of the entire driver therefore the quality of display [15].

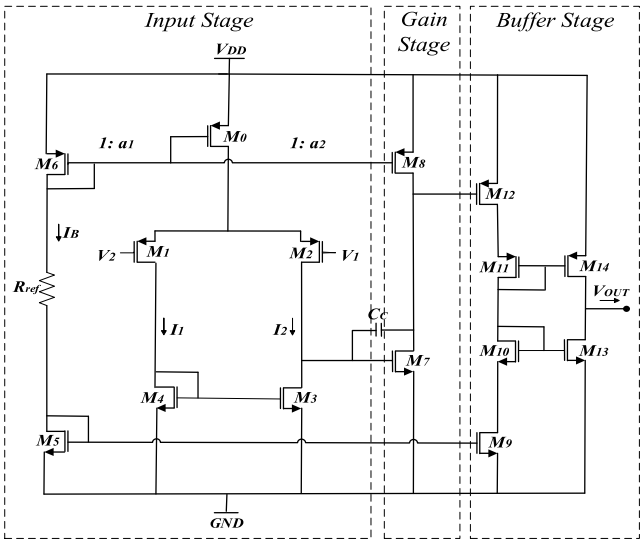

FIGURE 1. Miller compensated OPAMP.

Mostly, multi-stage amplifiers, seen in Fig. 1, that incorporate a differential input stage, gain stage and a buffer stage dominated display applications. This is mainly due to their key advantages of high DC gain and rail-to-rail output swing [16], [17]. The down side, however, is that they require frequency compensation which increases their design complexity, restricts their capacitive load drivability, as well as area and power efficiencies [18]. Thus, single stage amplifiers utilizing load compensation has recently emerged as an attractive alternative to optimize the area and power especially in applications that require a huge number of amplifiers similar to display applications [19]. The advantage of these single stage amplifiers, is that they can be almost unconditionally stable which naturally widens their capacitive load drivability. This feature allows these amplifiers to be used in small, medium as well as large display panels [20]. Conventional single stage amplifiers consist of a differential input stage and an output stage. However, this structure suffers from low DC gain (20 – 40 dB) and a low output resistance, not to mention their inability to provide a rail-to-rail output voltage swing [21]. It is worth to note that the use of the cascode structure to enhance the gain is not recommended for low voltage rail-to-rail operation.

In state of the art AMLCD, channel buffers must be capable of deriving a wide range of capacitive loads while still maintaining a phase margin $\geq 60°$, high DC gain ($\geq$66 dB for 10 bit resolution), rail-to rail output swing in order to accomplish higher gray levels as well as a low power consumption [22]. Naturally, several techniques have been presented over the years to improve the downfalls of a conventional single stage amplifier, some of which include current shunting from the differential input stage [23]–[25] and splitting the differential pair into N-sub pairs [22].

This paper reviews these identified single stage amplifiers, examines them theoretically in details as well as provide simulation results for each topology under open loop and closed loop conditions. This review leads to the development of a highly linear rail-to-rail robust single stage amplifier which is presented in this paper. The new amplifier is achieved by applying current splitting technique [22] on a rail-to-rail differential pair [27]. The paper illustrates that the new amplifier is capable of achieving the requirements of display application when configured as a buffer and thus replace conventional multistage amplifiers. The paper also showcase a comparison between the new enhanced amplifier and the other identified single stage amplifiers intended for the same application. All amplifier circuits were analyzed theoretically and then tested through simulations which were carried on LTspice using 90 nm CMOS technology.

II. EXSITING SINGLE STAGE AMPLIFIERS

In this section, the conventional single stage amplifier as well as four different enhanced single stage amplifier structures are presented. Each of the circuits are examined theoretically first then simulations were carried on LTspice software using 90 nm CMOS model, BSIM4 (level 54) version 4.3, which is an accurate model that takes into consideration many secondary effects. Simulations were carried under 1 volts supply voltage and all circuits were loaded with a 30 pF capacitor and biased with a 2μA bias current. All analysis and simulation results for all examined circuits are presented in the following subsections.

A. CONVENTIONAL SINGLE STAGE AMPLIFIER

This amplifier structure, shown in Fig. 2, is controlled by an external current, the amplifier bias current I_B. It consists

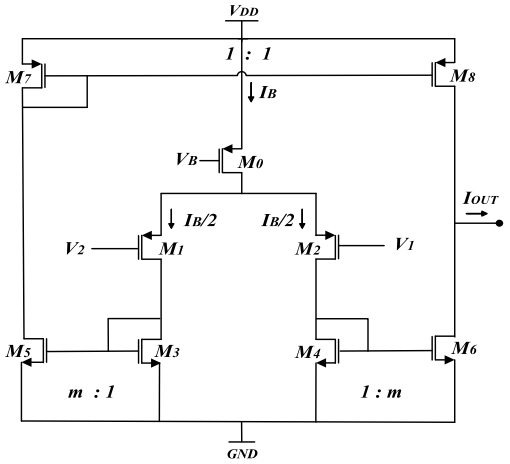

FIGURE 2. The conventional single stage amplifier.

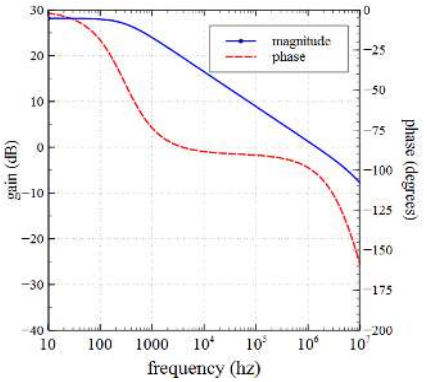

FIGURE 3. The magnitude and phase responses of the conventional single stage amplifier.

of a differential pair ($M_1 - M_2$) and current mirrors where the main bias current is provided by a current source transistor (M_0) biased by a constant amount of voltage V_B. The appeal of this configuration is the simplicity of design as well as the single dominant pole characteristics. However, even though this amplifier structure solves the stability issue, it still lacks in terms of gain and output resistance. Therefore some enhancement techniques must be incorporated.

Analyzing the circuit after obtaining the small signal model, the effective transconductance, output resistance and DC gain of the circuit can be derived as:

$$G_m = mg_{m_1} \tag{1}$$

$$R_{out} = \frac{1}{(\lambda_6 + \lambda_8)mI_B} \tag{2}$$

$$A_v = \frac{v_{out}}{v_{id}} = \frac{2g_{m_1}}{(\lambda_6 + \lambda_8)I_B} \tag{3}$$

where g_{m_i} is the transconductance of the input transistors, λ_i a process technology parameter inversely proportional to the channel length of each transistor and v_{id} the differential input voltage equal to $v_{gs2} - v_{gs1}$. As it can be seen, the current mirror gain m does not affect the value of the DC gain, which leaves it fall usually between values 20 - 40 dB. As for the slew rate and power dissipation of this amplifier, it can be driven as:

$$SR = \frac{I_B * m}{C_{load}} \tag{4}$$

$$P_{diss} = V_{DD}I_B\,(m + 1) \tag{5}$$

The equations listed above verifies that the structure lacks in terms of gain and output resistance. Thus, some enhancements to this structure must be incorporated to improve the overall performance of the amplifier.

In the carried simulations, the current gain factor m was set to 10. Open loop simulation results indicate that the circuit is capable of achieving a DC gain of 31 dB as seen in Fig. 3 with a phase margin of 91° and a unity gain frequency (UGF) of 1.16 MHz. Simulations also shows that the amplifier circuit has an output resistance of 0.19 MΩ and transcondactance of 217 μA/V. The overall power consumption of the circuit is of a very high value around 23 μWatt.

The closed loop simulations were carried to understand how this conventional amplifier structure performs when configured as a buffer. This is crucial since the application requires using the amplifier as a channel buffer in column drivers. Rail-to-rail operation of the amplifier was tested by plotting the output voltage versus an input ranging from value 0 to 1 and the output voltage corresponding to different input amplitudes ranging from 0.2 up to 1 Vp-p at 10kHz frequency. Linearity of the amplifier was tested by finding the THD values of the output corresponding to an input also ranging from 0.2 to 1 Vp-p. Finally the pulse response was found to also examine the rise and fall times of the amplifier.

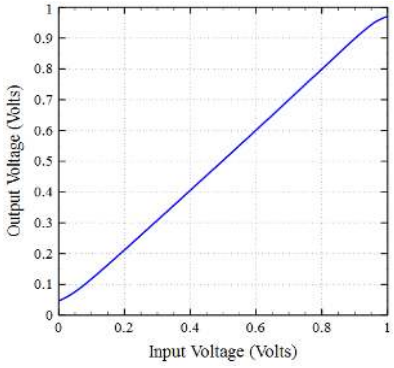

FIGURE 4. The output voltage versus the input voltage for the conventional single stage amplifier.

Simulation results indicate that this conventional single stage topology suffers from distortion. This can be seen in Fig. 4, Fig. 5 and Fig. 6 where the output is clearly incapable of reaching rail-to-rail and the total harmonic distortion goes from −54 dB corresponding to an input voltage of 0.2 to −16 dB corresponding to 1 volts. Regarding the pulse response seen in Fig. 7, it is clear that the output reaches steady state at a value much higher than zero and much lower than 1. The rise and fall times were found to be 1.64 μs

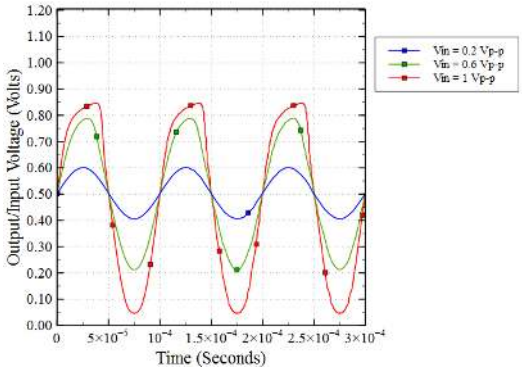

FIGURE 5. The output voltage corresponding to different input amplitudes of 0.2, 0.6 and 1 Vp-p at 10 kHz frequency in the conventional single stage amplifier based buffer.

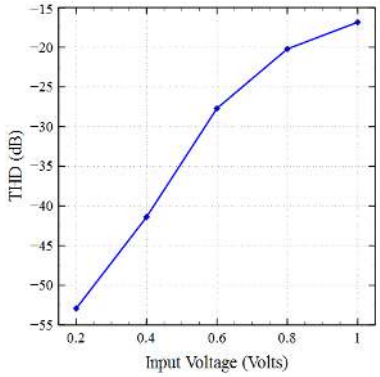

FIGURE 6. THD in dB of the output corresponding to different input amplitudes for conventional single stage amplifier based buffer.

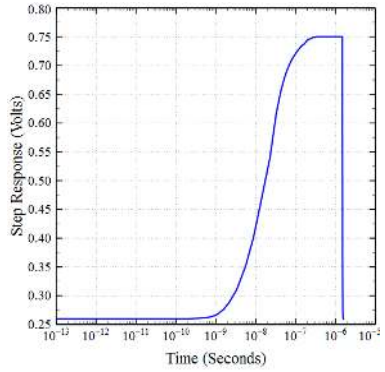

FIGURE 7. The pulse response of the conventional single stage amplifier based buffer.

and 0.476 μs respectively. It is clear, therefore, that this conventional topology lacks when operated as a buffer and thus is not suitable for the targeted application.

B. CONSTANT AMOUNT OF CURRENT SHUNT AMPLIFIER [23]

In this technique shown in Fig. 8 the diode-connected transistors M_3 and M_4 are shunt by a pair of fixed current sources implemented through the use of transistors M_9 and M_{10} and

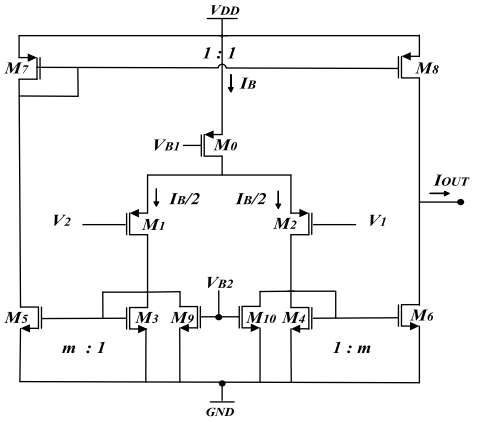

FIGURE 8. Constant amount of current shunt amplifier.

a bias voltage V_{B2}. The current mirror ratio can be sized similar to that of the conventional amplifier while still improving the effective transconductance, output resistance and DC gain. The compromise is the parasitic effect induced by the connection between M_3-M_9 and M_4-M_{10} which lowers the position of the non-dominant pole.

Analyzing the circuit after obtaining the small signal model, the effective transconductance, output resistance and DC gain of the circuit can be driven as:

$$G_m = mg_{m_1} \tag{6}$$

$$R_{out} = \frac{1}{(\lambda_6 + \lambda_8)m\left(\frac{I_B}{2} - I_{sh}\right)} \tag{7}$$

$$A_v = \frac{g_{m_1}}{(\lambda_6 + \lambda_8)\left(\frac{I_B}{2} - I_{sh}\right)} \tag{8}$$

where I_{sh} is the amount of current shunt from the differential pair by transistors M_9 and M_{10}. As it can be clearly seen, the term $\left(\frac{I_B}{2} - I_{sh}\right)$, which is present in the denominator of both the output resistance and DC gain equations, will boost their value. However, this configuration will not improve the effective transconductance of the circuit as seen in (6). The improvement is only seen in the large signal operation of the circuit not the small signal operation as DC voltage source V_{B2} will be shorted to the ground in the small signal operation, and thus no current is shunt through M_9 and M_{10} and the circuit operates similar to the conventional amplifier. Both the slew rate and power dissipation can be driven as:

$$SR = \frac{(I_B - I_{sh}) * m}{C_{load}} \tag{9}$$

$$P_{diss} = V_{DD}\left(2m\left(\frac{I_B}{2} - I_{sh}\right) + I_B\right) \tag{10}$$

Also noticed, the power dissipation is lowered by the presence of the shunt current term I_{sh}. However, one of the downfalls of this configuration is lowering the value of the slew rate as shown in (9).

In the carried simulations, the amount of shunt current was set to 90% of the current passing in the main differential

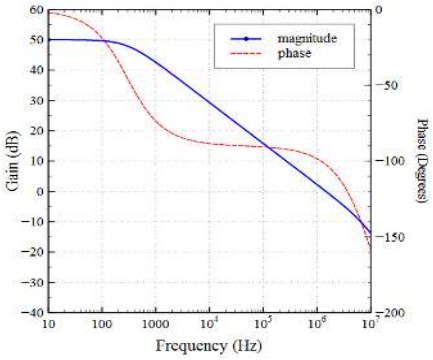

FIGURE 9. The magnitude and phase responses of the constant amount of current shunt amplifier.

pair and the current gain factor m was set to 10. Open loop simulation results indicate that the circuit is capable of achieving a DC gain of 50 dB as seen in Fig. 9 with a phase margin of 86° and a UGF of 1.245 MHz. Simulations also shows that the amplifier circuit has an output resistance of 1.38 MΩ and transcondactance of 233 μA/V. The overall power consumption of the circuit is around 4.4 μWatt.

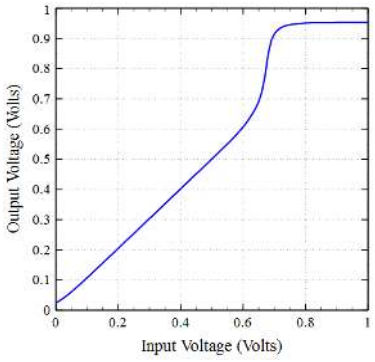

FIGURE 10. The output voltage versus the input voltage for constant amount of current shunt amplifier based buffer.

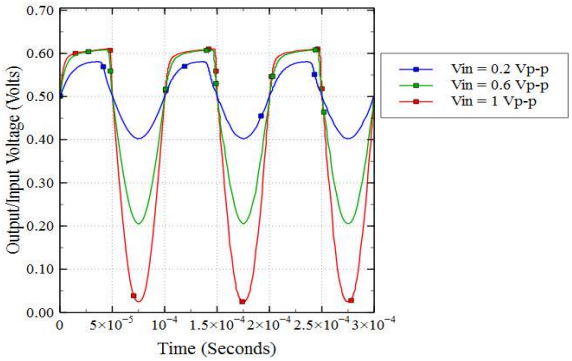

FIGURE 11. The output voltage corresponding to different input amplitudes of 0.2, 0.6 and 1 Vp-p at 10 kHz frequency in the constant amount of current shunt amplifier based buffer.

The closed loop simulations were carried to understand how the amplifier performs when configured as a buffer. Simulation results indicate that this topology suffers from a high amount of distortion. This is evident in Fig. 10, Fig. 11 and

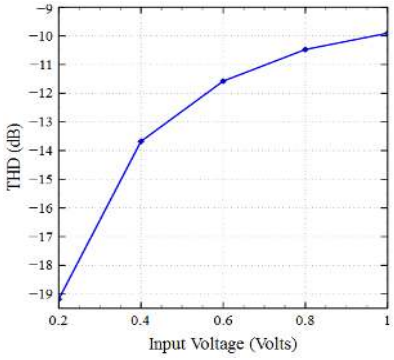

FIGURE 12. THD in dB of the output corresponding to different input amplitudes for constant amount of current shunt amplifier based buffer.

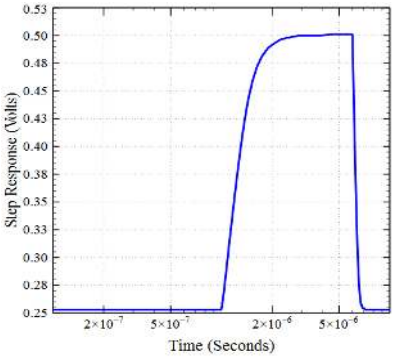

FIGURE 13. The pulse response of the constant amount of current shunt amplifier based buffer.

Fig. 12 where the output is incapable of reaching any of the two rails and thus the total harmonic distortion is of a high value going from −19 dB corresponding to an input voltage of 0.2 to −10 dB corresponding to 1 volts. Regarding the pulse response seen in Fig. 13, it is clear that the output reaches steady state at a value much higher than zero and much lower than 1. The rise and fall times were found to be 0.62 μs and 0.637 μs respectively. It is clear, therefore, that this topology lacks when operated as a buffer.

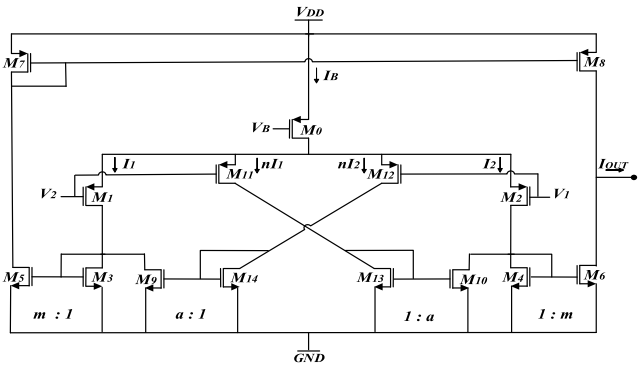

FIGURE 14. Adaptive amount of current shunt amplifier.

C. ADAPTIVE AMOUNT OF CURRENT SHUNT AMPLIFIER [24]

This technique presented in Fig. 14 utilizes a control circuit that consists of a second differential pair (M_{11} - M_{12}) that

senses the amount of input voltage and accordingly bias two transistors, M_9 and M_{10}, that shunt an adaptive amount of current from the main differential pair ($M_1 - M_2$). Thus, the amount of current shunt is not fixed as in the previous technique, it is adaptive and changes depending on the amount of input voltage. As it is shown in Fig. 14, the new addition are transistors M_9 through M_{14}. Both M_{11} and M_{12} are connected along with M_1 and M_2 to the differential input. Transistors M_{13} and M_{14} are controlling two voltage controlled current sources M_9 and M_{10}, which in return shunt current from transistors M_3 and M_4.

In order to reduce the output current in the quiescent state, a great portion of the drain current passing through M_2 passes through the voltage controlled current source M_{10}. Transistor M_{10} is controlled such that an increase in the current passing through transistor M_2 results in a decrease in the current passing through M_{10}. Based on that, the amount of current reduction in M_{10}, equals the amount of current incremented in M_4. Thus, the total current passing through transistor M_4 equals the sum of change in transistors M_2 and M_{10}. Factor n represents the strength of the second differential pair compared to the main pair and factors a and m represent current gain factors.

The effective transconductance, output resistance and DC gain can be driven as:

$$G_m = m\left[g_{m_1} + ag_{m_{11}}\right] \tag{11}$$

$$R_{out} = \frac{2}{(\lambda_6 + \lambda_8)m\frac{(1-an)}{(1+n)}I_B} \tag{12}$$

$$A_v = \frac{2\left[g_{m_1} + ag_{m_{12}}\right](1+n)}{(\lambda_6 + \lambda_8)(1-an)I_B} \tag{13}$$

The added enhancement affects not only the DC gain and the output resistance as in the case of the previous discussed amplifier circuit, but it also improves the effective transconductance as well. These equations indicate that the improvement added is seen in both the small and large signal operations. The effective transconductance is improved by an added term equal to $amg_{m_{11}}$. This term also is seen in the DC gain equation in addition to the factor $\frac{(1-an)}{(1+n)}$ seen in the denominator of both the DC gain and output resistance equations. As we increase the value of factor an, both the DC gain and output resistance increase given that the factor does not exceed the value 1. As for the slew rate and the power dissipation of the circuit, they can be driven as follows:

$$SR = \frac{\frac{I_B}{(1+n)} * m}{C_{load}} \tag{14}$$

$$P_{diss} = V_{DD}I_B\left(m\frac{(1-an)}{(1+n)} + 1\right) \tag{15}$$

These two equations are again controlled by factors a and n when compared to the previous two topologies. Increasing the value of an will reduce the power dissipation given that it does not go beyond 1. Increasing factor n reduces the value of slew rate, however, this reduction can be kept limited since factor n is also present in the term $(1 - an)$.

In the carried simulations, the amount of shunt current in the circuit was also set to 90% of the current passing in the main differential pair and the current gain factor m was set to 10. Factor n was set to value 1.2 and the current gain factor a was set to value 0.9. Open loop simulation results indicate that the circuit is capable of achieving a DC gain of 59 dB as seen in Fig. 15 which is higher than the previous topology with a phase margin of 84° and a UGF of 0.813 MHz. Simulations also show that the amplifier circuit has an output resistance of 7.4 MΩ and transcondactance of 150 μA/V. The overall power consumption of the circuit is lowered by the added shunting technique and is around 2.48 μWatt.

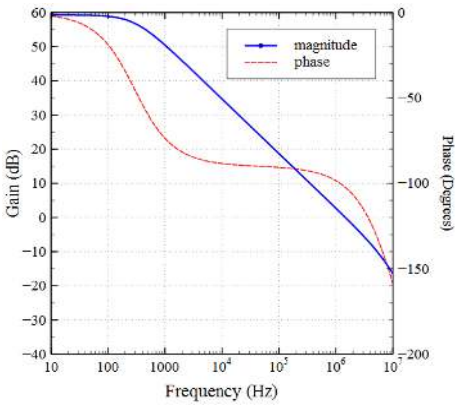

FIGURE 15. The magnitude and phase responses of the adaptive cross shunt amplifier.

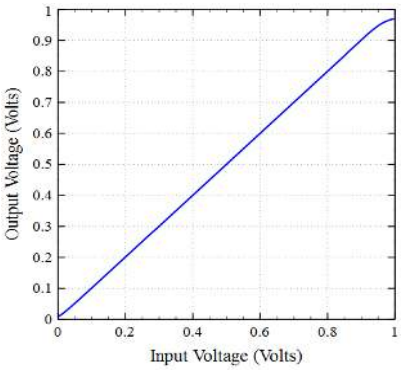

FIGURE 16. The output voltage versus the input voltage for the adaptive cross shunt amplifier based buffer.

Under closed loop simulation conditions, results indicate that the linearity of this amplifier is better that the constant amount of shunt amplifier. As can be seen in Fig. 16, the output input relationship is linear for most of the input range. However, it is also clear from Fig. 17 and Fig. 18 that at higher input amplitudes distortion increases and the circuit is also incapable of providing a rail-to-rail operation as the THD went from −55 to −16 dB corresponding to an input ranging from 0.2 to 1 Vp-p at 10 kHz frequency. Regarding the pulse response seen in Fig. 19, it is clear that the output reaches steady state at a value higher than zero and lower

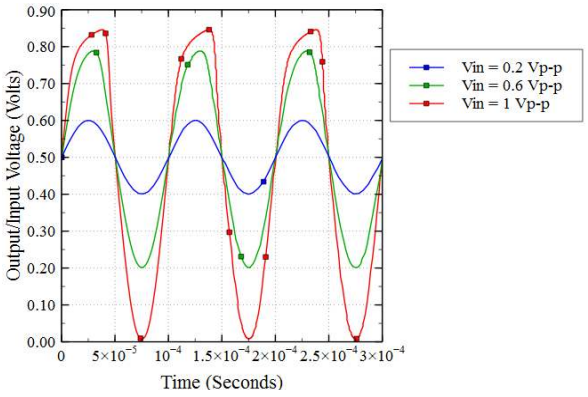

FIGURE 17. The output voltage corresponding to different input values of 0.2, 0.6 and 1 Vp-p at 10 kHz frequency in the adaptive cross shunt amplifier based buffer.

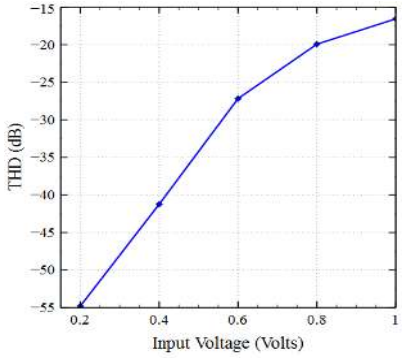

FIGURE 18. THD in dB of the output corresponding to different input amplitudes for the adaptive cross shunt amplifier based buffer.

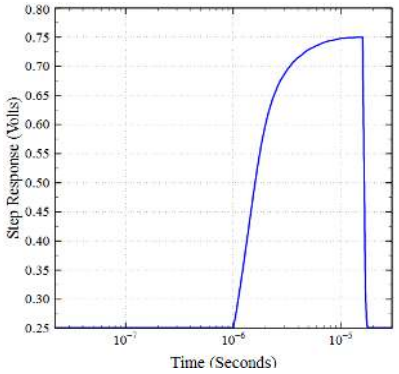

FIGURE 19. The pulse response for the adaptive cross shunt amplifier based buffer.

than 1. The rise and fall times were found to be 0.61 μs and 0.65 μs respectively which is almost similar to the previous topology since the same amount of current of 90% was shunt from the main differential pair. It is clear, therefore, that even though the results found for this amplifier are far better than the constant amount of current shunt amplifier, it still lacks when operated as a buffer and it does not satisfy the minimum requirements of open loop operating conditions.

D. HYBRID CURRENT SHUNT AMPLIFIER [25]

The circuit presented here employs two different techniques of shunting current from the main differential pair ($M_1 - M_2$), as seen in Fig. 20. The first technique is through shunting a fixed amount of current using fixed biased current source transistors M_{15} and M_{16} and the second is the adaptive cross shunt technique. Combing these two techniques is examined here. Similar to the previous amplifier, factor n represents the strength of the second differential pair compared to the main pair and factors a and m represent current gain factors.

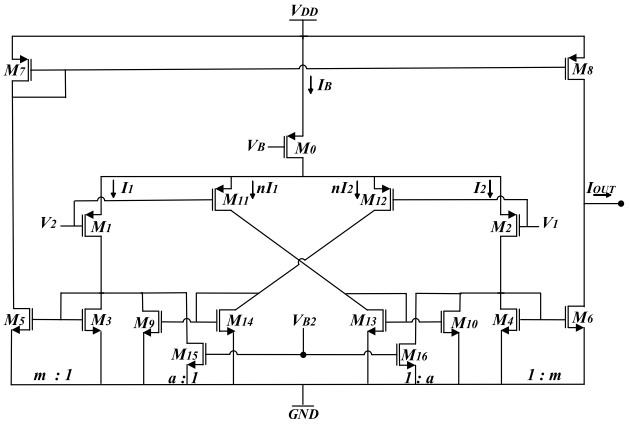

FIGURE 20. The hybrid amount of current shunt amplifier.

Analyzing the circuit, the effective transconductance, output resistance and DC gain can be derived as:

$$G_m = m\left[g_{m_1} + a g_{m_{11}}\right] \tag{16}$$

$$R_{out} = \frac{1}{(\lambda_6 + \lambda_8) m \left[\frac{I_B}{2}\frac{(1-an)}{(1+n)} - I_{sh}\right]} \tag{17}$$

$$A_v = \frac{\left[g_{m_1} + a g_{m_{12}}\right]}{(\lambda_6 + \lambda_8)\left[\frac{I_B}{2}\frac{(1-an)}{(1+n)} - I_{sh}\right]} \tag{18}$$

The effective transconductance is exactly similar to that of the adaptive cross shunt amplifier. This is due to the fact that in the small signal operation, voltage source V_{B2} which biases transistors M_{15} and M_{16} is shorted to the ground and thus these two transistors are not operational. Both the slew rate and power dissipation can be driven as:

$$SR = \frac{\left(\frac{I_B}{(1+n)} - I_{sh}\right) * m}{C_{load}} \tag{19}$$

$$P_{diss} = V_{DD}\left(2m\left[\frac{I_B}{2}\frac{(1-an)}{(1+n)} - I_{sh}\right] + I_B\right) \tag{20}$$

Again, it is noticed that the value of power is lowered along with the value of the slew rate.

For the carried simulations, the amount of shunt current in the circuit was set to 95% and the current gain factor m was set to 10. Since two techniques of shunting current are incorporated in this circuit, 80% of the current passing in the

main differential pair was shunt through the adaptive biased transistors M_9 and M_{10}, and the remaining 15% was shunt through the constant biased transistors M_{15} and M_{16}.

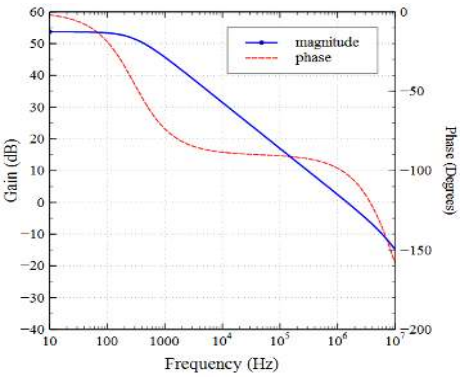

FIGURE 21. The magnitude and phase responses of the hybrid amount of current shunt amplifier.

Open loop simulation results indicate that the circuit can achieve a DC gain of 54 dB as seen in Fig. 21 with a phase margin of 85° and a UGF of 1.06 MHz. Simulations also shows that the amplifier circuit has an output resistance of 3.03 MΩ and transcondactance of 193 μA/V. The overall power consumption of the circuit was found to be around 3.24 μWatt.

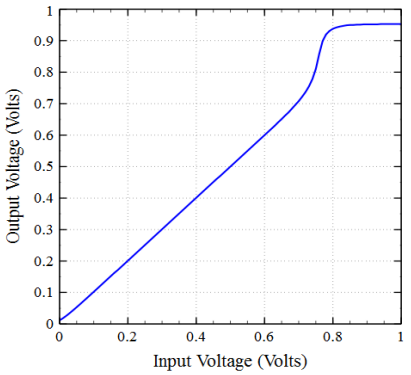

FIGURE 22. The output voltage versus the input voltage for the hybrid current shunt amplifier based buffer.

Under closed loop simulation conditions, results indicate a high level of distortion especially at higher input amplitudes. Due to incorporating a second bias voltage V_{B2}, as in the constant amount of current shunt amplifier, the output versus input seen in Fig. 22 indicates problematic performance at higher input amplitudes. This is also validated in Fig. 23 where rail-to-rail is clearly not achieved and in Fig. 24 where the THD went from −49 dB to −13 dB corresponding to an input ranging from 0.2 to 1 Vp-p at 10kHz frequency. Regarding the pulse response seen in Fig. 25, again it is noticed that the output reaches steady state at a value higher than zero and lower than 1. The rise and fall times were found to be 0.6 μs and 0.64 μs respectively. It is clear that incorporating the two current shunting techniques together

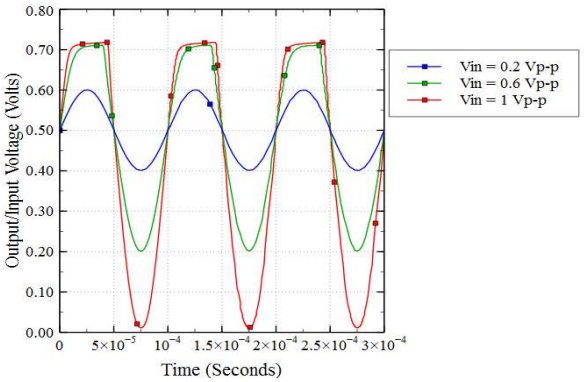

FIGURE 23. The output voltage corresponding to different input amplitudes of 0.2, 0.6 and 1 Vp-p at 10 kHz frequency in the hybrid current shunt amplifier based buffer.

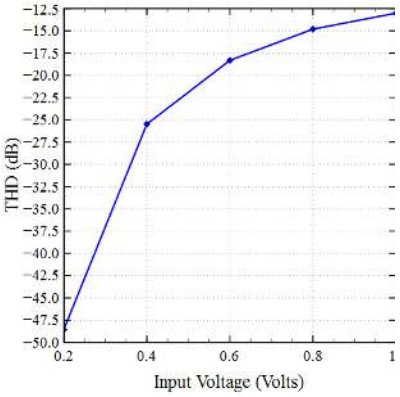

FIGURE 24. THD in dB of the output corresponding to different input amplitudes for the hybrid current shunt amplifier based buffer.

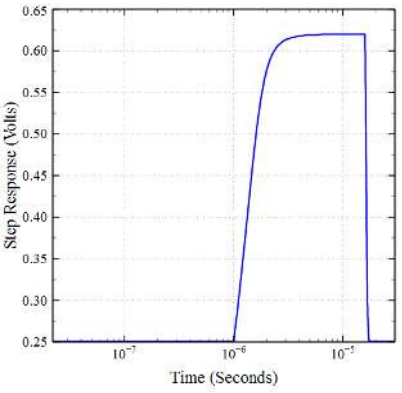

FIGURE 25. The pulse response of the hybrid current shunt amplifier based buffer.

adds no value to the circuit, and thus the adaptive current shunting insures better linearity and less distortion.

E. NESTED CURRENT MIRROR AMPLIFIER [22]

This technique, seen in Fig. 26, provides a solution to the strict performance tradeoffs found in single stage amplifier topologies that utilize the standard differential pair similar to

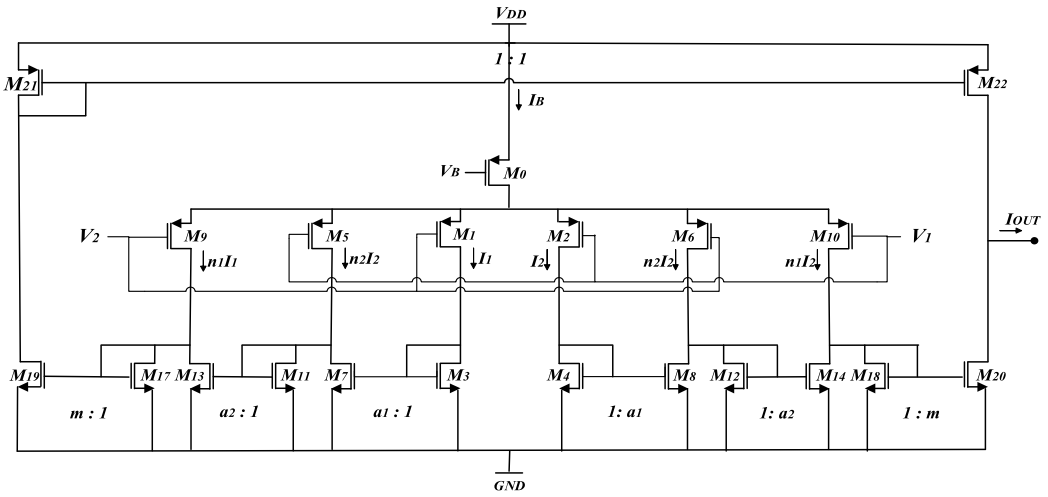

FIGURE 26. The 3-step nested current mirror amplifier.

the examined circuits previously. The Nested Current Mirror (NCM) technique is applied through two main steps: the first is splitting the main differential pair transistors M_1 and M_2 into N-sub transistors M_1 - M_N and connecting the two inputs V_1 and V_2 alternatively to the inputs of these sub-transistors. The second step is combining the outputs of transistors M_1 - M_N in sequence by the use of subdivided current mirrors with different ratios. By sharing the current of the N divided DP transistors, then their combined outputs are added through the nested current mirrors. Alternating V_1 and V_2 will insure that the outputs are in phase. The use of nested current mirrors also helps enhance the output resistance of the circuit, and therefore enhance the DC gain and UGF. In case further enhancements are required the number of current mirror stages should be increased, however it would be on the expense of more area and power consumption. The amplifier circuit shown in Fig. 26 is an example of employing three sub differential pairs and three nested current mirrors, thus it is a 3-step NCM amplifier. These sub pair transistors are assigned different strength factors denoted as n_1 and n_2. The outputs of each sub transistor are summed through the use of three nested current mirrors located in the path of each signal each assigned a different gain factor denoted as a_1, a_2 and m.

Analyzing the circuit, the effective transconductance, output resistance and DC gain can be driven as:

$$G_m = m[a_1 a_2 g_{m_1} + n_2 a_2 g_{m_5} + n_1 g_9] \tag{21}$$

$$R_{out} = \frac{2(1+n_1+n_2)}{(\lambda_6+\lambda_8)m[n_1 - a_2(n_2-a_1)](I_B/2)} \tag{22}$$

$$A_v = \frac{2(1+n_1+n_2)[a_1 a_2 g_{m_1} + n_2 a_2 g_{m_5} + n_1 g_9]}{(\lambda_6+\lambda_8)[n_1 - a_2(n_2-a_1)](I_B/2)} \tag{23}$$

As it can be clearly seen, All the tranconductance located in the signal path $(M_1 - M_N)$ contributed and thus elevated the overall transconductance of the circuit. Also, the term $\frac{(1+n_1+n_2)}{[n_1-a_2(n_2-a_1)]}$ which is present in both the output resistance and DC gain equations will boost their value. Thus, it is very evident that this topology elevates the performance of the circuit in both the small and large signal operations. The slew rate and power dissipation can be driven as:

$$SR = \frac{[I_B/(1+n_1+n_2)] * m}{C_{load}} \tag{24}$$

$$P_{diss} = V_{DD} I_B \left(1 + \frac{m[n_1 - a_2(n_2-a_1)]}{(1+n_1+n_2)}\right) \tag{25}$$

As it can be clearly also noticed, the power dissipation is lowered by the presence of the term $\frac{m[n_1-a_2(n_2-a_1)]}{(1+n_1+n_2)}$. And as been mentioned earlier, in order to enhance the slew rate a higher gain value can be assigned to the current gain factor m to overcome the effect of term $(1+n_1+n_2)$.

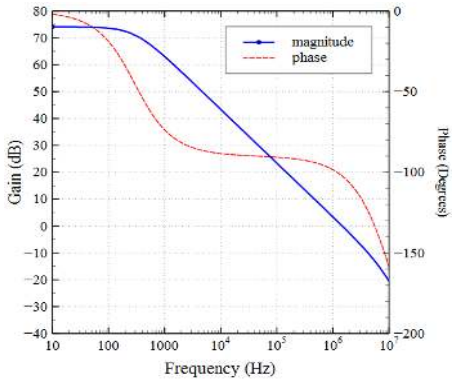

FIGURE 27. The magnitude and phase responses of the 3-step NCM amplifier.

In the carried simulations, both n_1 and n_2 factors, were set at value 2. Current mirror gain factors a_1, a_2 and m were set at values 1.5, 2.5 and 10 respectively. Open loop simulation results indicate that the circuit can achieve a DC gain of 74 dB as seen in Fig. 27 which is the highest among all tested circuits so far with a phase margin of 78° and a UGF

of 1.4 MHz. This also indicates that this topology achieved the open loop requirements for the application as the DC gain achieved is >66 dB. Simulations also shows a very high enhancement in the output resistance as it reached 24 MΩ with also a high transcondactance value of 270 μA/V. The overall power consumption of the circuit is also the lowest among all examined circuit with a value of 2.4 μWatt.

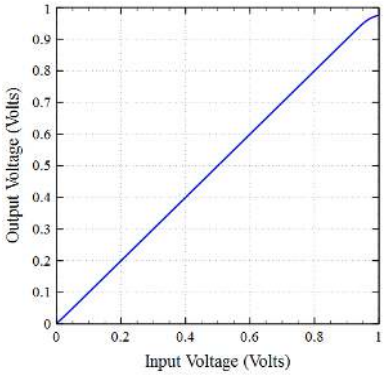

FIGURE 28. The output voltage versus the input voltage of 3-step NCM amplifier based buffer.

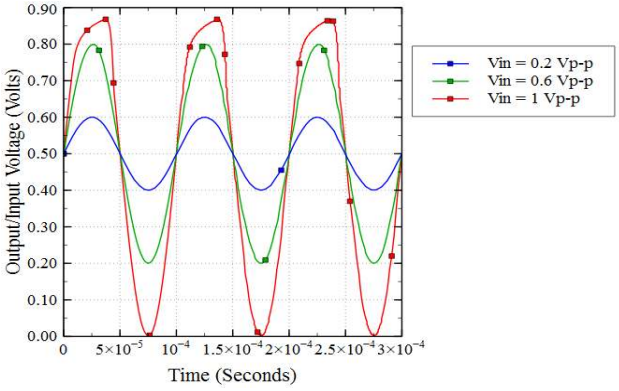

FIGURE 29. The output voltage corresponding to different input values of 0.2, 0.6 and 1 Vp-p at 10 kHz frequency in the 3-step NCM amplifier based buffer.

The results obtained for the closed loop simulations of the 3-step NCM amplifier shows a much improved performance in terms of linearity of the output versus input voltage as seen in Fig. 28. The output voltage swing goes from zero up to 0.85 volts, which is an improvement when compared to the topologies examined previously. However, at input amplitudes higher that 0.85 volts, the output is distorted and that is validated by the values of THD that keeps on increasing reaching up to −16 dB corresponding to 1 volts input voltage as seen in Fig. 30. The results indicate an improvement in linearity compared to the other examined topologies, however rail-to-rail operation is also not achieved. Regarding the pulse response seen Fig. 31, it is noticed that the output reaches steady state at a value slightly lower than 1 with a rise and fall times of 0.67 μs and 0.54 μs respectively. Overall, it is found that this topology achieves the open loop requirements

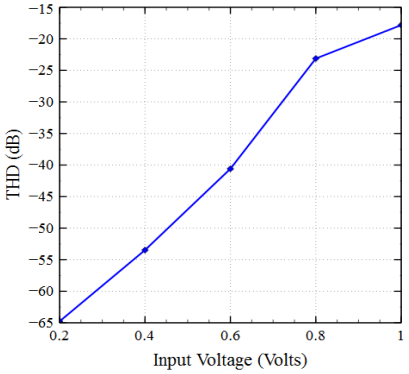

FIGURE 30. THD in dB of the output corresponding to different input amplitudes of 3 – step NCM amplifier based buffer.

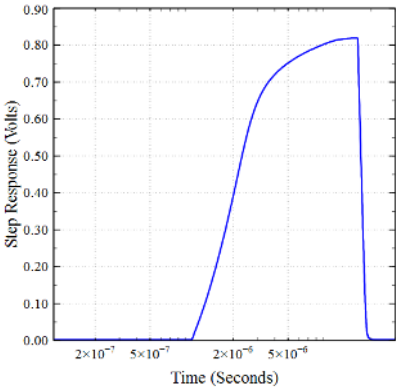

FIGURE 31. The pulse response of the 3-step NCM amplifier based buffer.

of LCD display applications, which is not the case for the other examined topologies. However, rail-to-rail operation, which is a crucial requirement for the application in hand is not achieved and thus some improvements can be added to this topology to enhance the closed loop simulation results.

III. HIGHLY LINEAR RAIL-TO-RAIL ENHANCED NESTED CURRENT MIRROR AMPLIFIER [26]

The amplifier presented here is an enhanced version of the 3-step NCM amplifier and is shown in Fig. 32. This amplifier is achieved by utilizing the three step current splitting technique on a rail - to - rail dual differential pair.

Current splitting is achieved by dividing the main differential pair into three sub pairs and alternating the input voltage connected to each transistors to insure that the outputs are in phase [22]. The outputs of each of the three sub pairs are combined using nested current mirrors located along the path of the signal with different gain factors. Rail-to-rail is achieved by replacing all sub differential pairs by rail-to-rail complementary pairs. Analyzing the circuit, the effective transconductance, output resistance and DC gain can be driven in (26)–(28), as shown at the bottom of the next page.

In this new amplifier, current summation of each complementary pair is achieved by mirroring the current in the NMOS pairs to the corresponding PMOS sub pairs [27].

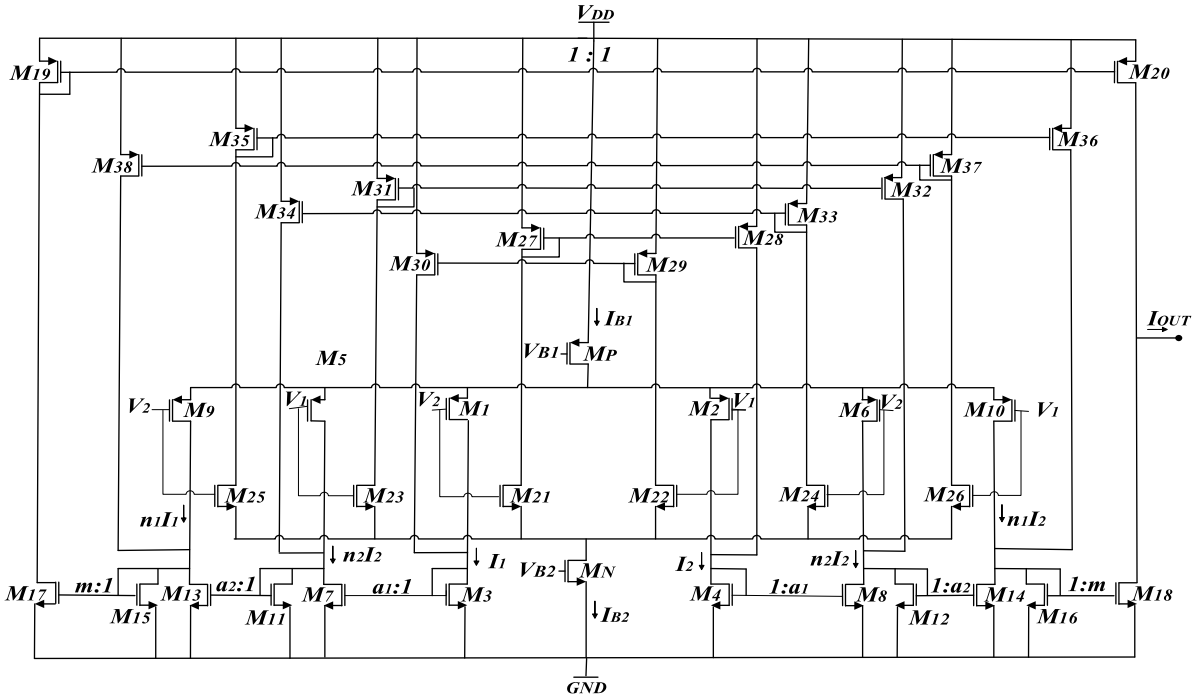

FIGURE 32. The CMOS realization of the new proposed highly linear rail-to-rail nested current mirror amplifier circuit.

Factors n_1 and n_2 represent the strength of each sub differential pair, while a_1 and a_2 and m represent the current mirror gains assigned to each nested current mirror. Similar to previous examined amplifiers, load compensation is used to compensate the operation of the circuit.

As can be noticed in equations (26) and (27), an increment in the value of the effective transconductance also corresponds to an equivalent decrement in the value of the output resistance. However, the major contribution this circuit adds, as mentioned earlier, is its rail-to-rail operation capability, which is highly important in display applications to insure higher grey level color scale. As for the slew rate and power dissipation, they can be driven as:

$$SR = \frac{[(I_{B1} + I_{B2})/(1 + n_1 + n_2)] * m}{C_{load}} \tag{29}$$

$$P_{diss} = V_{DD}(I_{B1} + I_{B2})\left(1 + \frac{m[n_1 - a_2(n_2 - a_1)]}{(1 + n_1 + n_2)}\right) \tag{30}$$

As ca be deduced from (29), the new amplifier circuit improves the slew rate with the additional amount of bias current. However, this improvement will increase slightly the power consumption of the circuit.

Similar to the 3-step NCM amplifier, both n_1 and n_2 factors were set at value 2 and current mirror gain factors a_1, a_2 and m were set at values 1.5, 2.5 and 10 respectively. Open loop simulation results indicate that the circuit can achieve a DC gain of 75.5 dB as seen in Fig. 33 which is the highest among all tested circuits with a phase margin of 80° and a UGF of 1.85 MHz. This also indicates that this topology achieved the open loop requirements for the application as the DC gain achieved is $>$ 66 dB. Simulations also shows that the circuit achieves high output resistance of 22.2 MΩ and very high transcondactance value of 350 μA/V, which is due to the addition of the second bias current. The overall power consumption of the circuit was found to be around 4.7 μWatt, which is slightly higher because of the additional bias current in the circuit.

As for the closed loop simulations, results indicate a huge improvement specially when compared to the typical 3-step NCM amplifier. The output is capable of reaching both rails which is evident in both Fig. 34 and Fig. 35. The amplifier is also highly linear as the THD values varied from −66 dB to −53 dB only corresponding to an input ranging from 0.2 to 1 Vp-p as seen in Fig. 36. The slew rate of the amplifier

$$G_m = m\left[a_1a_2(g_{m_1} + g_{m21}) + n_2a_2(g_{m_5} + g_{m22}) + n_1(g_{m9} + g_{m25})\right] \tag{26}$$

$$R_{out} = \frac{2(1 + n_1 + n_2)}{(\lambda_6 + \lambda_8)m[n_1 - a_2(n_2 - a_1)](I_{B1} + I_{B2})} \tag{27}$$

$$A_v = \frac{2\,(1 + n_1 + n_2)\left[a_1a_2(g_{m_1} + g_{m21}) + n_2a_2(g_{m_5} + g_{m22}) + n_1(g_{m9} + g_{m25})\right]}{(\lambda_6 + \lambda_8)[n_1 - a_2(n_2 - a_1)](I_{B1} + I_{B2})} \tag{28}$$

TABLE 1. The performance parameters of the proposed amplifier compared to four different amplifier topologies.

Parameter	[23]	[24]	[25]	[22]	Proposed
Gm (μA/V)	233	150	193	270	350
Rout (MΩ)	1.38	7.4	3.03	24	22.2
DC Gain (dB)	50	59	54.1	74	75.5
UGF (MHz)	1.245	0.813	1.06	1.4	1.85
PM (°)	86	84	85	78	80
T_r (μs)	0.62	0.61	0.6	0.67	0.32
T_f (μs)	0.637	0.65	0.64	0.54	0.411
Power (μWatt)	4.4	2.48	3.24	2.4	4.7
IRN (μV/√Hz)	0.232 @10k	0.076 @10k	0.076@10k	0.062 @10k	0.066 @10k
THD (dB)	-20 to -10	-55 to -16	-45 to -12	-65 to -17	-66 to -53
PVT	1.8% to 41%	+5.6% to -18.6%	+8.6% to -18.1%	+1.8% to -41%	+0.9% to -19%
Rail-to-Rail	Not obtained	Not obtained	Not obtained	Not obtained	Obtained

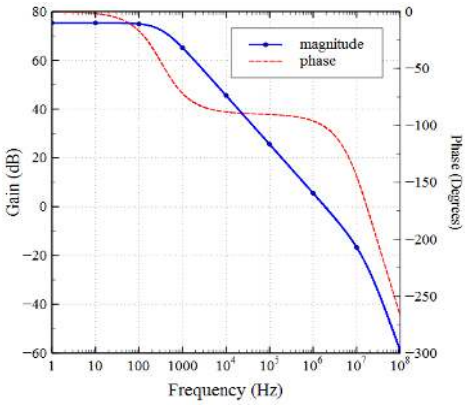

FIGURE 33. The magnitude and phase responses of the new highly linear rail-to-rail nested current mirror amplifier.

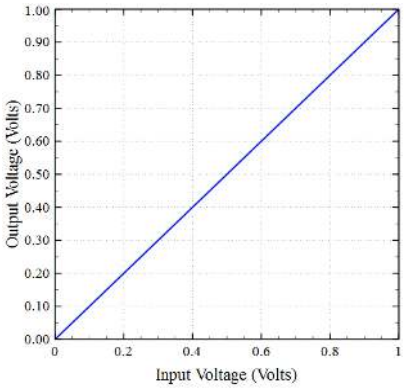

FIGURE 34. The output voltage versus the input voltage of the new highly linear rail-to-rail nested current mirror amplifier based buffer.

also improved giving a faster response as the rise and fall times indicate a response nearly twice as fast as the other amplifiers with values of 0.32 μs and 0.411 μs respectively.

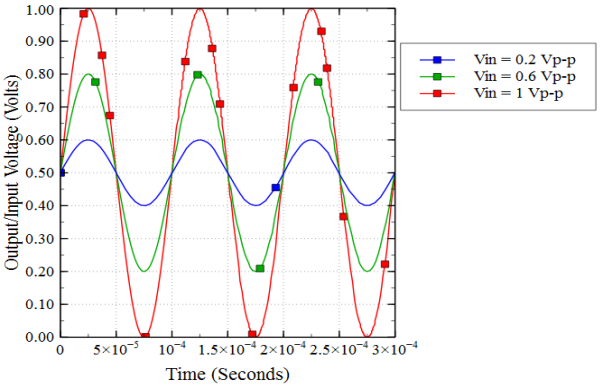

FIGURE 35. The output voltage corresponding to different input values of 0.2, 0.6 and 1 Vp-p at 10 kHz frequency of the new highly linear rail-to-rail nested current mirror amplifier based buffer.

IV. CROSS EXAMINATION OF THE DIFFERENT SINGLE STAGE AMPLIFIER TOPOLOGIES

In the previous sections, four different enhancements techniques on the conventional single stage amplifier topology were examined along with a new highly linear rail-to-rail amplifier. All circuits were tested under open loop and closed loop conditions to verify wither they satisfy the minimum requirements of channel buffers in column drivers of LCD panels. As the results found indicate, the nested current mirror amplifier was the only topology capable of achieving the open loop requirements of the application with a DC gain of 74 dB, phase margin of 78° and a UGF of 1.4 MHz. Thus the proposed amplifier was based on applying the complementary differential pair to the nested current mirror amplifier to insure its ability of matching both the open loop and closed loop requirements. Even though applying the

TABLE 2. PVT Simulation results for the constant amount of current shunt amplifier.

At VDD = 0.95 volts															
Temp. (°C)	10					27					40				
Corner	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF
DC Gain (dB)	40	40	39.7	40	39.3	12	11.2	12.4	10	20	23	21.2	24.6	14	50
UGF (kHz)	2	1.7	2.3	1.66	2.3	0.175	0.119	0.25	0.1	0.589	7.2	4.23	11	1.8	670
PM (°)	90	90	90	90	90	105	107	104	111	96	94	95	94	102	89.5
At VDD = 1 volts															
DC Gain (dB)	39.6	39.5	39.7	39.7	39.6	49.2	52	51.7	32.1	41.5	39.5	39.7	39.4	47	36
UGF (kHz)	3.6	3	4	3.1	4	1245	421	268	2.3	1200	8000	7100	9000	6000	8900
PM (°)	90	90	90	90	90	89	89	89.2	92	89	90	90	90	89	90
At VDD = 1.05 volts															
DC Gain (dB)	39.6	39.6	39.5	39.6	39.6	37.2	36.9	37.7	42.7	34.6	33.7	33.8	33.6	35	32.4
UGF (kHz)	5	4.5	5.4	4.3	5.4	1890	1600	2000	1600	2100	11000	10000	12000	10000	12800
PM (°)	90	90	90	90	90	90	90	90	89	90	91	91	90	90	91

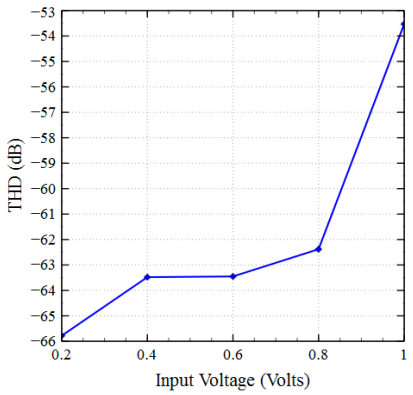

FIGURE 36. THD in dB of the output corresponding to different input amplitudes of the new highly linear rail-to-rail nested current mirror amplifier based buffer.

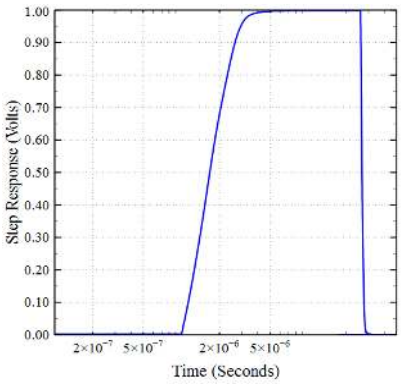

FIGURE 37. The pulse response of the new highly linear rail-to-rail nested current mirror amplifier based buffer.

complementary differential pair to the other topologies would improve their rail-to-rail operation capability, they would still be unsuitable for the application in hand as the open loop requirements are not met. Simulation results shows that the new amplifier exhibits a high DC gain of 75.5 dB and it operates under stable conditions with a phase margin of 80°

TABLE 3. PVT simulation results for the adaptive amount of current shunt amplifier.

At VDD = 0.95 volts															
Temp. (ºC)	10					27					40				
Corner	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF
DC Gain (dB)	35	34.3	35.6	34.6	35.2	57.3	57.5	57	56.9	57.6	56.7	57	56.5	56.4	57
UGF (kHz)	0.56	0.53	0.61	0.55	0.58	350	282	430	288	423	2790	2310	3250	2330	3280
PM (º)	84	83	85	84	84	86	86	86	86	86	86	86	86	87	86
At VDD = 1 volts															
DC Gain (dB)	35.8	35.4	36.6	36.2	35.5	58.9	59.2	58.6	58.6	59.2	58.4	58.7	58.1	58.2	58.5
UGF (kHz)	0.63	0.6	0.68	0.65	0.59	820	698	963	704	946	5800	5170	6830	5220	6530
PM (º)	86	86	87	86	87	85	85	85	85	85	86	86	86	86	85
At VDD = 1.05 volts															
DC Gain (dB)	36.4	35.3	37.8	36.7	36.4	59.6	59.9	59.3	59.4	59.8	59.1	59.5	58.8	59.1	59.2
UGF (kHz)	0.67	0.60	0.79	0.7	0.66	1400	1240	1618	1260	1630	9400	8460	10000	8620	10000
PM (º)	88	87	88	87	88	84	84	84	85	84	85	85	85	85	85

and UGF of 1.85 MHz. Due to the addition of the second bias current I_{B2}, the proposed amplifier exhibits the highest transconductance of 350 μA/V. However, this additional bias current increases the power consumption of the circuit as it reached 4.7 μWatt. It is important to note, however, that the proposed amplifier power consumption is much lower than the conventional single stage amplifier topology which was around 23 μWatt. Also, the power consumption can be lowered further by using a lower bias current values for I_{B1} and I_{B2}. This would lower the transconductance but will not affect the rail-to-rail operation of the proposed amplifier. As for the input referred noise (IRN) values, the proposed amplifier exhibits low values at different tested frequencies. Table 1 summarizes all the obtained simulation results.

When the circuits were configured as a buffer and tested under closed loop conditions, the new amplifier was the only topology capable of achieving rail-to-rail operation due to the incorporation of the complementary differential pair. This is apparent in the gain accuracy seen in Fig. 38, which was

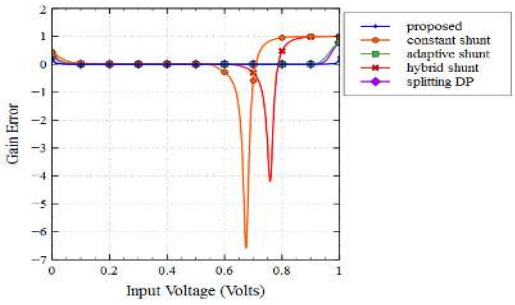

FIGURE 38. The gain accuracy of all tested buffers in comparison to the new amplifier.

computed by subtracting the actual gain of the buffers from 1 for the entire input range. As shown, the proposed amplifier has a value near zero corresponding to the entire input range. Obtained results of this test also shows that current shunting through constant biased transistors results in the worst gain accuracy as can be seen for the constant amount of current shunt amplifier and hybrid current shunt amplifier. Rail-to-

TABLE 4. PVT simulation results for the Hybrid current shunt amplifier.

At VDD = 0.95 volts															
Temp. (°C)	10					27					40				
Corner	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF
DC Gain (dB)	45.7	44.3	46.9	44.5	46.7	46.3	49.7	42.8	30.5	57.4	48.3	51.5	44.4	31.9	56.2
UGF (kHz)	2	1.8	2.5	1.8	2.5	16	21	12.2	1.6	341	222	303	156.7	18.1	2860
PM (°)	86	86	85	85	86	90	90	91	92	86	90	90	90	92	87
At VDD = 1 volts															
DC Gain (dB)	49.6	48.9	50.3	49	50.2	54.1	53.4	54.9	58.7	51.1	53.5	52.8	54.4	57.7	50.6
UGF (kHz)	4	3.5	4.7	3.5	4.5	1000	913	1180	515	1360	7880	7140	8310	4290	9680
PM (°)	86	86	86	86	86	86	86	86	86	86	86	87	86	86	87
At VDD = 1.05 volts															
DC Gain (dB)	51.3	50.8	51.6	50.9	51.6	50.3	50	50.6	52.5	49.1	49.8	49.5	50.2	52	48.4
UGF (kHz)	6	5.4	6.6	5.2	6.7	2110	1830	2370	1750	2420	14220	12780	15140	12220	15550
PM (°)	86	86	86	86	86	86	87	86	86	87	87	87	87	86	87

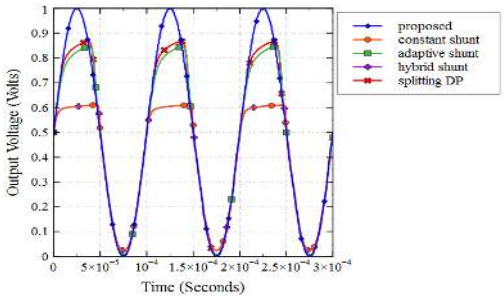

FIGURE 39. The output voltage of all tested buffers corresponding to 1 Vp-p at 10 kHz frequency.

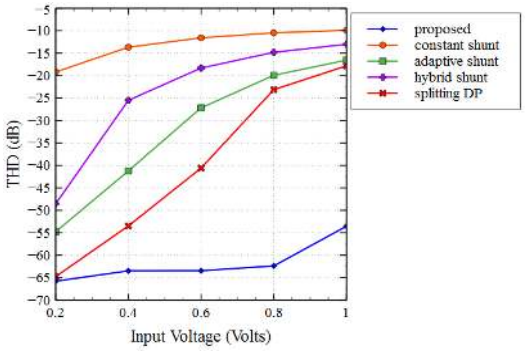

FIGURE 40. THD in dB of the output voltage for all tested buffers corresponding to different input amplitudes.

rail operation of the proposed amplifier was also proven by applying an input of 1 Vp-p at 10 kHz frequency to all five amplifiers. Obtained results in Fig. 39 highlights clearly the proposed amplifiers rail-to-rail operation capability. Testing for linearity shows that the proposed amplifier has very low distortion levels as the THD values obtained ranges from −66 dB to −53 dB in correspondence to an input voltage ranging from value 0.2 to 1 at 10kHz frequency

TABLE 5. PVT simulation results for the Nested Current Mirror amplifier.

At VDD = 0.95 volts															
Temp. (°C)	10					27					40				
Corner	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF
DC Gain (dB)	40	39.6	39.5	39.9	41	72	72.2	71.5	71.5	72.2	71	71.4	70.5	70.7	71.1
UGF (kHz)	0.68	0.83	0.58	0.86	0.52	611	534	712	534	693	4330	3924	4820	3995	4777
PM (°)	82	78	84	79	84	80	79	81	80	80	82	81	82	82	82
At VDD = 1 volts															
DC Gain (dB)	39	39.2	39.1	40	39.5	74	74.4	73.7	73.7	74.3	73.2	73.6	72.7	73.1	73.2
UGF (kHz)	0.66	0.86	0.53	0.94	0.44	1454	1317	1618	1314	1548	8936	8319	9097	8545	8856
PM (°)	85	82	87	83	86	78	77	79	78	78	81	80	82	81	81
At VDD = 1.05 volts															
DC Gain (dB)	40	41	39.5	39.2	40	75	75.5	74.9	75	75.4	74.3	74.8	73.7	74.4	74.2
UGF (kHz)	0.54	0.68	0.46	0.82	0.36	2531	2399	2695	2442	2624	13011	13128	13128	13485	12553
PM (°)	87	85	88	85	88	77	76	78	77	78	81	80	82	80	81

as seen in Fig. 40. Since rail-to-rail is not achieved in any of the other tested amplifiers, the value of THD increased as the value of input increased as seen in both Fig. 40 and Table 1. Regarding a pulse input, the output of the proposed amplifier shows a faster response in comparison to the other amplifier topologies with a rise time and a fall time of 0.32 μs and 0.411 μs respectively. The pulse response shown in Fig. 41 also confirms once again that the proposed amplifier exhibits rail-to-rail capability.

It is important to note that the different parameters identified in each of the examined circuits were varied in order to optimize the performance of the circuits under open loop conditions. The selected parameter values thus gives the best DC gain, output resistance and transconductance values in each circuit. However, even under different parametrization scenarios the proposed amplifier is the only topology capable of achieving rail-to-rail operation. Varying these parameters affects the performance of the circuits under open loop conditions, however under closed loop conditions rail-to-rail operation is only achieved in the proposed circuit even with different parameter values assigned.

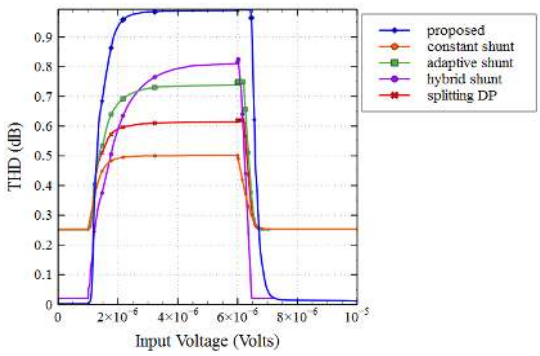

FIGURE 41. The pulse response of all tested buffers.

V. ROBUSTNESS OF TESTED AMPLIFIERS

Process, voltage and temperature (PVT) variation simulations were carried to test some of the non-idealities that may occur

TABLE 6. PVT simulation results for the Proposed amplifier.

At VDD = 0.95 volts															
Temp. (°C)	10					27					40				
Corner	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF	TT	SS	FF	FS	SF
DC Gain (dB)	60	62	60	61	61.1	74.1	74.4	73.8	74.2	73.9	71.9	72.4	71.3	72	71.8
UGF (kHz)	0.653	0.81	0.56	0.75	0.57	1102	935	1338	1159	1068	4753	4077	5374	4610	4902
PM (°)	82	79	85	81	83	81	81	82	82	81	85	84	85	85	84
At VDD = 1 volts															
DC Gain (dB)	62	63	61	60	60.2	75.5	75.6	74.9	75.3	75.3	73.7	74.2	73.2	73.3	73.7
UGF (kHz)	0.681	0.89	0.55	0.91	0.49	1840	1592	2119	1875	1914	8341	7765	8778	8006	8688
PM (°)	85	82	86	83	86	79	79	80	80	78	83	82	84	84	83
At VDD = 1.05 volts															
DC Gain (dB)	60	61.5	61.7	59.9	59.8	76	76.4	75.5	76	76.1	74.7	75.4	74	74.8	74.5
UGF (kHz)	0.595	0.76	0.5	0.86	0.42	2910	2654	3158	2881	2940	12426	11928	12426	12174	12299
PM (°)	87	85	87	85	87	77	76	78	77	77	82	81	83	82	82

internally or externally during the fabrication process of the five amplifier circuits [28]. Understanding how the circuit perform under different PVT variations in essential in order to insure that circuit is still operational under extreme conditions [28], [29]. Process corners are a representation of these extremes within which a circuit must operate correctly [30]. When operating at any of these corners, the circuit might run faster or slower than expected at lower or higher supply voltages and temperatures. However, if the circuit is not operational at any of the process corners then the design is considered inadequate [30].

In general, there are five different process corners that represent the extreme operating conditions of any integrated circuit. They are denoted by two letters, the first representing the speed of the NMOS transistors while the second the speed of the PMOS transistors. These corners are: slow-slow (SS), fast-fast (FF), typical-typical (TT), fast-slow (FS), and slow-fast (SF) [29]–[31]. All five corners were tested at different supply voltages (0.95 volts, 1 volts and 1.05 volts) and different temperatures (10 °C, 27 °C and 40 °C), which corresponds to the operating temperature of display screens [31]. In total, 45 different cases were examined for each amplifier circuit. The obtained PVT simulation results for each of the examined amplifier topologies are shown in Tables 2 to 6. Results indicate that the proposed amplifier circuit has a maximum and minimum variations in the value of DC gain by $+0.9\%$ and -19%. Simulation results also shows that phase margin is maintained $\geq 60°$ for all tested cases. The variation in the DC gain obtained for all tested cases for all amplifier circuits are presented in Fig. 42. The different dot colors incorporated indicates the temperature as RED corresponds to 40 °C, GREEN to 27 °C and BLUE to 10 °C. The worst performance was found for the constant amount of current shunt amplifier as the DC gain varied by a range of 40 dB. Whereas the lowest was obtained by the proposed amplifier with a variation of only 15 dB, making the least DC gain obtained around 60 dB. The proposed amplifier by far shows the best robustness against process, voltage and temperature variations as the DC gain varied within a 20% range around the nominal 75.5 dB value. Whereas the other

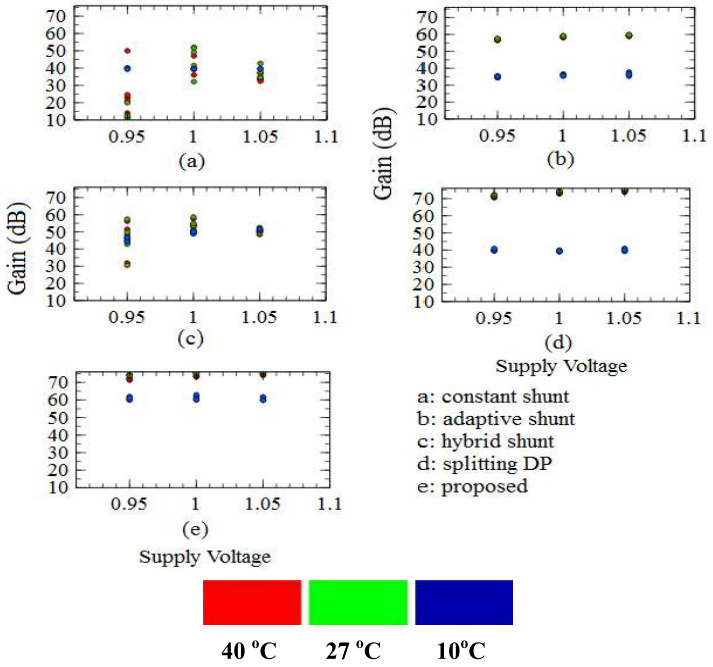

FIGURE 42. The PVT simulation results of the new proposed amplifier compared to the other four amplifier topologies.

topologies, as seen in Table 1, exhibit a much larger variation range making them less robust to PVT variations specially when compared to the proposed amplifier.

VI. CONCLUSION

The paper examined four different single stage amplifier topologies that were identified in the literature along with a new proposed highly linear rail-to-rail nested current mirror amplifier. All amplifiers were analyzed theoretically first then designed and optimized to insure the best performance. Simulations were carried using LTSPICE based on 90 nm CMOS model under both open and closed loop conditions. Achieved results indicate that the new proposed amplifier is capable of providing high performance in all tested conditions while maintaining stability with a phase margin of 80°. In addition, results shows that the new proposed amplifier is the only topology capable of providing rail-to-rail operation with a very low THD range values which is essential for column drivers of LCD panels. When tested for robustness against PVT variations the results indicate that the proposed amplifier exhibits a robust performance with only 20% variation in the DC gain. Overall, the amplifier shows good specifications that match and surpass the conventional OPAMP specifications without the need of compensation. It also shows a better performance in comparison to other state of the art single stage amplifier topologies under all tested conditions.

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