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Switch Bootstrapping for Precise Sampling Beyond Supply Voltage

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***Abstract*—Bootstrapped switches are used in a variety of applications including DC–DC converters, pipelined analog-to-digital converters and high voltage switches and drivers. Current work on highly integrated power management applications often requires the ability to measure voltage quantities that exceed the supply voltage in magnitude. This is primarily due to a basic need to maximize efficiency by running the power management IC on as low supply voltage as possible, while still maintaining the ability to sample and measure quantities from the surroundings that could well exceed the battery voltage. In this paper, a new bootstrapped switch is presented. The switch enables the precise sampling of input signals well greater than the chip supply voltage with no static power consumption, and without activating on-chip parasitic body diodes. The bootstrapped switch, presented here, is designed to sample an input signal with a 0–5.5-V range at a supply voltage of 2.75 V. Measurement data shows functionality for a 0–6-V input signal range with a supply voltage as low as 1.2 V.**

***Index Terms*—Analog-to-digital converters, bootstrap, power management, switch.**

I. Introduction

THE design of power management ICs (PICs) with high efficiency and wide load range requires the analog processing, including analog-to-digital conversion of large signals while using multiple supply sources and ensuring very low power consumption. Recent power management solutions [1] often integrate on the same chip multiple switched-mode regulators, multiple low-dropout regulators, voltage references, low-power low-speed analog-to-digital converters (ADCs), digital control cores, and serial interface units. The solutions should be able to share resources (voltage references, current references, etc.) among different sections of the chip thus obtaining optimum power efficiency. The ADC is one of the shared resources and is typically a very low power component used to supervise and monitor on-chip and off-chip voltages. The architecture employed is typically a multi-channel successive approximation register (SAR) ADC.

The supply voltage of an integrated circuit establishes the boundary of the signal to be processed as signals that go below the negative or above the positive supplies forward bias parasitic diodes of nMOS or pMOS transistors. Consequently, before processing signals that exceed the supply range it is normally necessary to attenuate the amplitude down to the IC supply limits worsening the system signal-to-noise ratio (SNR). Moreover, the attenuators have a limited accuracy and linearity, are a source of noise, and consume power. Finally, resistor-based attenuators often leads to inadequate input resistances.

An alternative approach to the use of attenuators consists of performing the first steps of the analog processing at the full input level while using a lower supply voltage. Bootstrapping beyond the supply voltage provides a means for achieving this goal.

Bootstrapping is a widely used technique in analog-to-digital converters and power management systems [2]–[5]. In ADCs, high-speed pipelines must sample the input signal within a very short time and must ensure an accurate charging of the sampling capacitor. The function is properly realized with bootstrapped switches that are used instead of transmission gates. The result obtains a faster operation with smaller transistors and better-controlled clock-feedthrough. In power management systems, DC–DC converters often employ bootstrapping techniques to drive the high-side (HSD) switch [6] to achieve the gate drive required for a low on resistance $r_{\mathrm{ds,on}}$ of the switch. Moreover, bootstrapped switches are highly effective in terms of power consumption and require no static current consumption to function. The power losses are only dynamic losses that occur during switching.

This paper presents a bootstrapped switch to be used for sampling input signals with a range exceeding the supply voltage [7]. The switch enables a precise input sampling without requiring extra power consumption. The proposed circuit is implemented using a conventional CMOS technology. The reliability and the lifetime of the proposed circuit are not affected by the high-voltage operating conditions.

This paper is divided into seven sections. After this introduction, Section II reviews the most commonly used bootstrap switch and discusses features and limitations when the bootstrap switch is used for voltages surpassing the supply. Section III describes the proposed solution. Section IV presents an analysis of reliability-related issues in the proposed switch. Section V is on simulation results and Section VI is on circuit implementation and experimental results. Finally, Section VII is on conclusions and discusses the possible uses of the obtained results.

II. Conventional Bootstrap Switch

The most widely used bootstrapped switch in ADC applications [2]–[4] is shown in Fig. 1. The transistor MN1 is the bootstrapped switch and the remaining part serves to generate a gate voltage that is shifted up by MN2, C3 and MP1 with respect to the input voltage. In short, the classical bootstrapped switch

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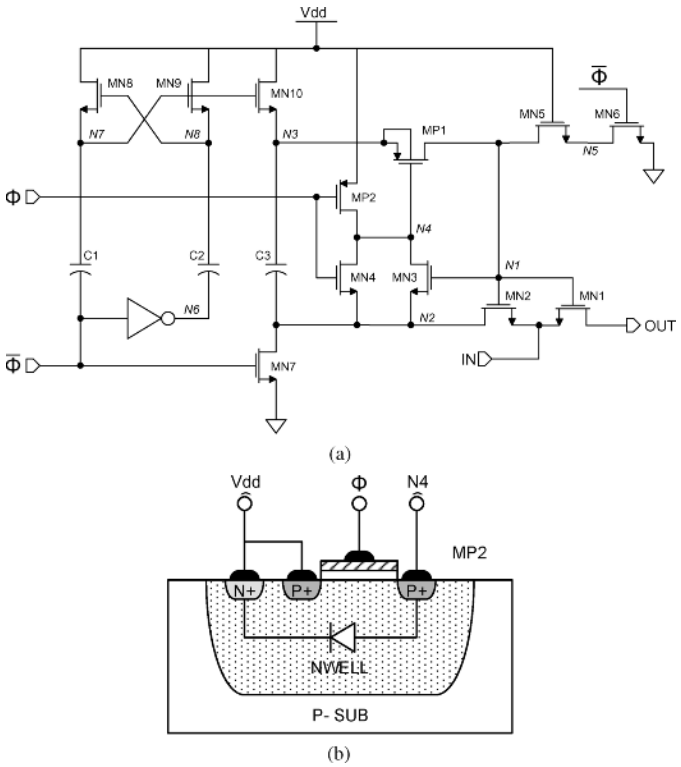

Fig. 1. Conventional bootstrap switch. (a) Circuit schematic. (b) Cross section of MP2 showing parasitic body diode.

charges C3 to $V_{\rm dd}$ using the charge pump circuit during the OFF phase $(\overline{\Phi})$ and connects it in between the gate and source terminals of the switch transistor MN1 during the ON phase (Φ).

The output of the boosted switch charges the sampling capacitor in ADCs. The voltage across C3 is equal to the supply voltage $V_{\rm dd}$ so that the driving voltage of the switch transistor is not larger than the supply. Thus, the stress of the gate oxide of MN1 is within the required limits.

In terms of reliability, there are two important techniques employed within the structure given in Fig. 1. First, the gate terminal of MP1 is driven to the input voltage during the ON state in order to bound the $V_{\rm gs}$ of MP1 to $V_{\rm dd}$ for all input conditions. Second, MN6 is cascoded with MN5 to reduce the stress on the oxide of MN6 for thin oxide CMOS implementations [3]. It should be noted that MN5 is not necessary for functionality and can be omitted for thick gate oxide or drain-extended (DEMOS) implementations of MN6. Further discussion of the reliability constraints of this switch along with the newly proposed switch can be found in Section IV.

Observe that the circuit in Fig. 1 works properly only with input voltages lower than the supply. In fact, in the ON state MN3 turns ON and transfers the input voltage to the drain of MP2 whose well is biased at $V_{\rm dd}$. If the input exceeds $V_{\rm dd}$, the well diode is forward biased, causing a large current to flow from input to $V_{\rm dd}$ through MN2, MN3 and the well diode of MP2. For input voltages higher than the well voltage, it would be necessary to automatically switch the well bias of MP2 to the higher voltage with a complication of the circuit and problems due to the bias switching transient [8]. In summary, this switch cannot operate if the input signal exceeds the supply voltage.

III. Improved Bootstrap Switch

Since, as already mentioned, PIC applications must foresee wide input swings with small supply voltages, the conventional bootstrapped switch given in Fig. 1 is not adequate. An input voltage that exceeds the supply can be switched on and off using the circuit shown in Fig. 2 [7]. The circuit, as in the scheme of Fig. 1, biases the gate of MN1 with a charged capacitance C3 connected across gate-to-source but avoids the forward biasing of substrate diodes with a more complicated but effective approach.

The bootstrapping scheme of Fig. 2 includes a charge pump realized by the transistors MN5 and MN6 with capacitors C1 and C2. The circuit requires only one clock cycle to reach the steady-state operation during which C1 and C2 are both charged to $V_{\rm dd}$. The voltage of node N5 is equal to $2V_{\rm dd}$ during $\overline{\Phi}$, thereby switching ON transistor MN12. Since MN9 is also ON during $\overline{\Phi}$, capacitor C3 is pre-charged to $V_{\rm dd}$. Observe that during $\overline{\Phi}$ the transistors MP3 and MN11 are also ON charging the capacitance C4 to $V_{\rm dd}$.

During the boost phase (Φ) the bottom plate of capacitor C3 is connected to $V_{\rm in}$ and the top plate to the gate of MN1 through MP4. The bottom plate switching is made possible by the action of the level shifter driven by Φ and $\overline{\Phi}$. The result is that node N8 swings from 0 to $V_{\rm in}$. If the input voltage is very low, the switching is ensured by the N-channel transistors MN7 and MN8.

The top plate of C3 is connected to N1 if the gate voltage of MP4 is lower than its source by more than the threshold voltage $V_{\rm tp}$. For high $V_{\rm in}$ values (i.e., $V_{\rm in} > V_{\rm dd} - V_{\rm tn}$ where $V_{\rm tn}$ is the threshold voltage of MN13), this is guaranteed by the voltage change on N3 during the transition to the boost phase (Φ) and a proper choice of the size of C4. For this case, the $V_{\rm gs}$ of MP4 immediately after the transition into the boost phase can be expressed as

$$V_{\rm gs,M_{P4}} = -\left(1 - \frac{C_{\rm gs,M_{P4}}}{C_4 + C_{\rm gs,M_{P4}}}\right) V_{\rm in} \qquad (1)$$

where $C_{\rm gs,M_{P4}}$ is the equivalent capacitance seen between the gate and source terminals of MP4 during the transition to the boost phase. For low $V_{\rm in}$ values (i.e., $V_{\rm in} < V_{\rm tp}$ where $V_{\rm tp}$ is the threshold voltage of MP4), MP4 is turned ON with the help of MN13.

Once MP4 is turned ON, nodes N1 and N3 are shorted and node N2 is driven to the input voltage $V_{\rm in}$ to protect MP4 with the help of the positive feedback provided by the action of MN14. It should be noted here that MN2 is included to enhance the turn on transient but is not necessary for the operation of this switch.

At the end of the boost phase (Φ), the voltage on node N1 is pushed to

$$V_{\rm N_1} = \frac{C_3}{C_3 + C_{\rm p,N_1}}(V_{\rm dd} + V_{\rm in}) \qquad (2)$$

where $C_{\rm p,N_1}$ is the parasitic capacitance loading N1. Table I summarizes the ideal node voltages seen during each phase of the clock.

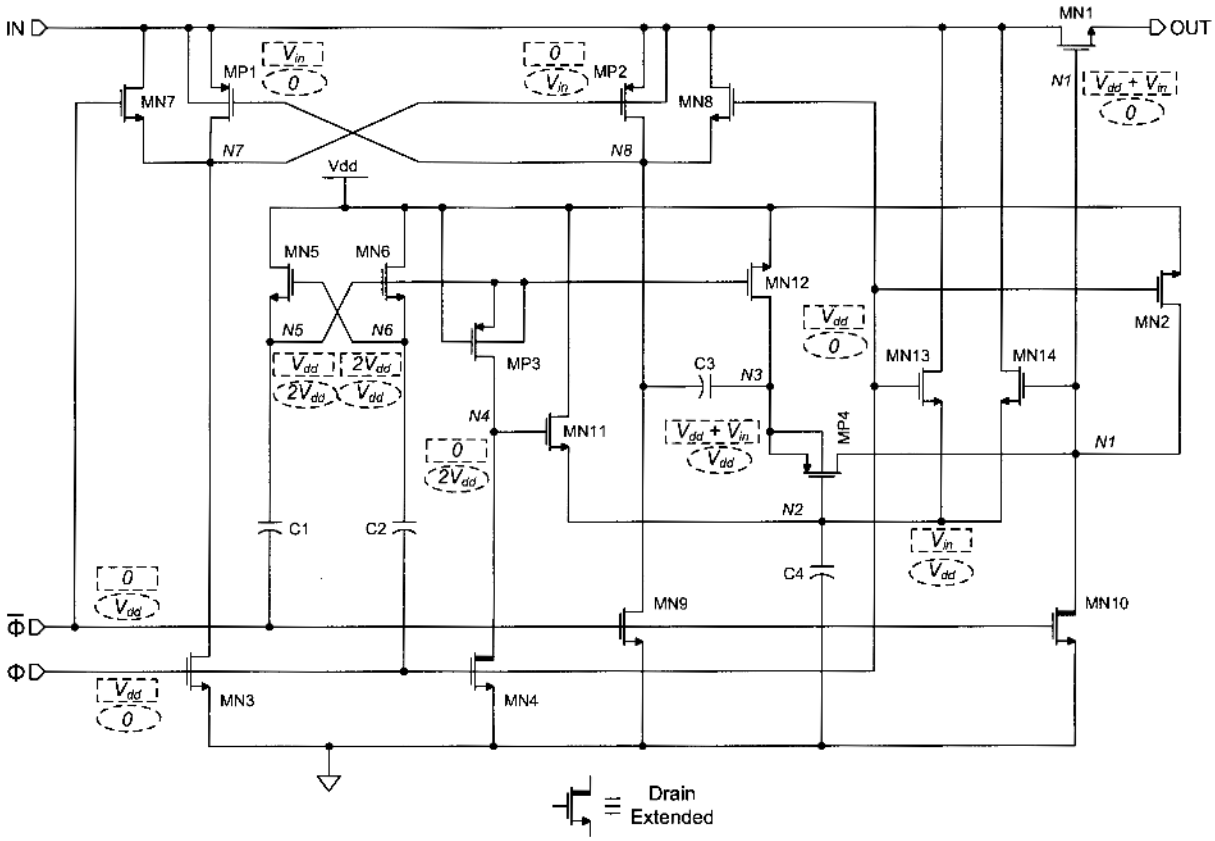

Fig. 2. Proposed bootstrapped switch with ideal node voltages (dashed rectangles denoting Φ, and dashed ovals denoting $\overline{\Phi}$).

TABLE I
STATE OF THE NODES AT $\Phi = 0$ AND $\Phi = 1$

Node	$\Phi = 0$	$\Phi = 1$
Φ	0	V_{dd}
N1	0	$V_{dd} + V_{in}$
N2	V_{dd}	V_{in}
N3	V_{dd}	$V_{dd} + V_{in}$
N4	$2V_{dd}$	0
N5	$2V_{dd}$	V_{dd}
N6	V_{dd}	$2V_{dd}$
N7	V_{in}	0
N8	0	V_{in}

IV. RELIABILITY DISCUSSION

A. Node Voltage Swing

An important requirement for reliability is to have swing of the internal nodes of the circuit such that the voltage across the gate oxide does not exceed the limits given by the technology. The utilized process makes available transistors with thicker gate oxide MOS together with drain-extended MOS (DEMOS), thus giving flexibility in the circuit design. Drain extended MOS transistor structures achieve high drain terminal breakdown $BV_{\rm dd}$ using drain diffusion engineering without any requirement for additional mask processing [9]. The above features, together with the design method illustrated earlier enables a proper operation of this circuit with input signals that are as large as 5.5 V. It is also possible to implement the proposed switch with good reliability using only 3.3-V thin oxide devices with cascoding techniques [2], [10]. This implementation is beyond the scope of this paper and interested readers can find more information on that in [11].

An important design step is the verification that the swing of the voltage on all the nodes in Fig. 2 does not exceed the process limits. By inspection, we obtain the node voltages given in Table I. It is clear from the table that all nodes exceed the supply voltage $V_{\rm dd}$, making it necessary to verify the following four conditions:

- The $V_{\rm ds}$ of all pMOS devices never reverses the biasing.
- The well of every pMOS devices is connected to its source.
- The $V_{\rm gs}$ of all devices never exceeds the reliability limit.
- Any transistor whose $V_{\rm ds} > BV_{\rm dd}$ uses drain extension.

In our implementation, transistors MP3 and MP4 do not use drain extension. The same holds for MN5 and MN6 as the maximum voltage swing across their terminals never exceeds $V_{\rm dd}$. Transistors MN10 and MN4 are realized with DEMOS transistors to comply with the aforementioned fourth condition.

B. Reliability and Device Lifetime

The reliability and the device/circuit lifetime depends on the possible occurrence of early breakdown of transistors undergoing high voltage stress. For the proposed switch, observe that at each time when a transistor is stressed, it happens when the transistor is in the off state with the higher voltage applied to its drain diffusion. This situation is depicted in Fig. 3. Under this operation condition, there exist three distinct breakdown currents: punchthrough current $I_{\rm DS(PT)}$, avalanche breakdown

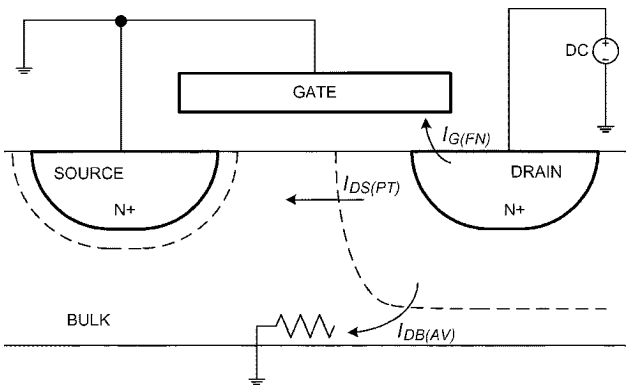

Fig. 3. Bootstrapped switch reliability.

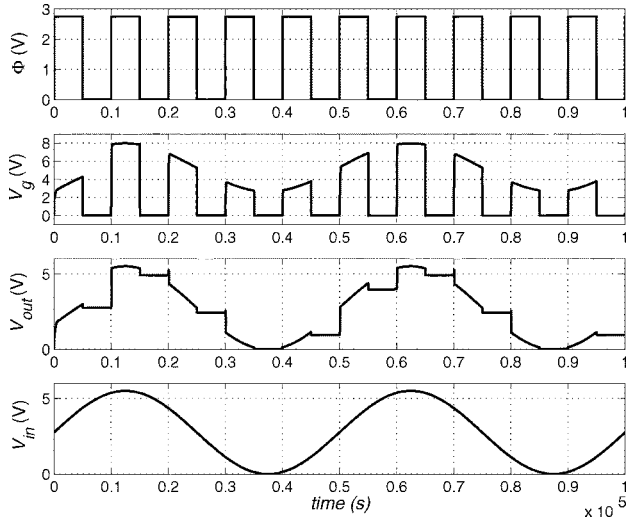

Fig. 4. Simulated switch behavior with a dynamically changing input signal.

current $I_{\mathrm{DB(AV)}}$, and Fowler–Nordheim gate leakage current $I_{\mathrm{G(FN)}}$. When occuring, the first two breakdown currents are nondestructive but degrade the performance of the switch by modulating the gate overdrive voltage (i.e., introducing a nonlinearity) and slightly loading the input terminal. The latter breakdown current does not affect the switch performance but ultimately determines the device/circuit lifetime.

A drain-to-source voltage exceeding a given limit causes punchthrough current (or subsurface drain-induced barrier lowering) and, at higher voltage, avalanche breakdown due to the impact ionization [12], [13]. Since the former effect occurs because of the merging of the source and drain depletion regions, this circuit uses four times larger lengths for the high voltage transistor than the allowed minimum. The impact ionization depends on the electric field across the drain–bulk depletion region. Once the electrical field reaches a critical level to create impact ionization current, increasing the drain potential further will result in the debiasing of the substrate, causing the parasitic lateral NPN structure to turn on. If V_{DB} exceeds snap-back voltage, thermal runaway might occur and completely destroy the device. The breakdown voltage of the drain–bulk junction can be increased with a DEMOS structure [9], thanks to the low doping profile resulting from the drain extension, or by exploiting lightly-doped drain (LDD) implants with careful device layouts [2]. For the used technology, the minimum junction breakdown voltage is 9 V and the snap-back voltage is well above 9 V.

Due to the circuit configuration used, the oxide breakdown ultimately occurs in transistors that do not carry current. This limit determines the maximum input voltage that can be applied to the switch. For the used technology, the oxide breakdown limit is 5 V.

Notice that the oxide breakdown voltage is higher than the process rating for the over-voltage stress condition shown in Fig. 3 [14]. When the electrical field across the drain–gate overlap region reaches a critical value, a gate leakage current flows due to the Fowler–Nordheim tunneling mechanism. Under this condition, highly energetic electrons, while accelarating towards the drain side, generate electron–hole pairs. Due to their relatively low mobility, some of the generated holes get trapped within the oxide, creating a localized positive charge, which in turn causes the tunneling current density to increase at these points. This positive feedback mechanism yields, in time, to higher trapped densities at these points and eventually the oxide breaks down.

In the current design, and assuming low operational duty cycle, we estimate that transistors MN1, MN8, and MN3 will determine the circuit's lifetime. The empirical model given in [13] estimates the oxide lifetime [or time-to-breakdown (tbd)]. The tbd depends strongly on the quality of the gate oxide, the operating temperature, the electrical field across the oxide, and the duty cycle or the duration of the over-voltage stress. Assuming C-Mode oxide failure and under worst case operating conditions, the estimated tbd is about 5 years, which is a satisfactory number for PIC applications.

V. Simulation Results

The proposed circuit has been simulated at the transistor level to verify the reliability conditions and the effectiveness of the bootstrapping method. Fig. 4 shows the simulated waveforms for an input sine wave with a swing of 0–5.5 V. The supply voltage is 2.75 V. The gate voltage during the on phase tracks the input signal and is shifted up by approximately 2.75 V.

Fig. 5 shows the gate drive voltage as a function of the input voltage. V_{dd} is equal to 2.75 V and the input range is swept from 0 to 5.5 V (i.e., $2V_{\mathrm{dd}}$). Observe that the driving voltage is slightly less than V_{dd} for low input signals and drops by about 200 mV when the input is twice the supply voltage. This small loss in gate overdrive is predicted by (2) and is due to the parasitic capacitors loading nodes N3 and N1. The loss can be reduced by increasing C3. However, it is necessary to find the best tradeoff between switching speed, power consumption, and driving effectiveness.

VI. Experimental Verification

The proposed bootstrapped switch was integrated in a 0.35-μm twin-well technology. The transistors which undergo the greatest oxide stress are implemented as drain-extended devices, made available by the used technology. However, the drain-extended option is not a limit to the general use of

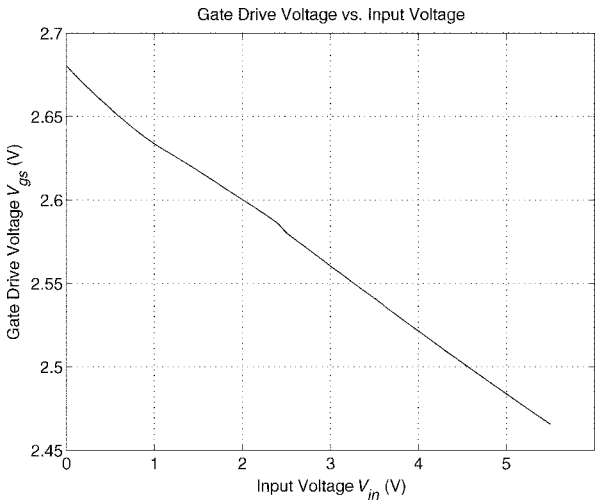

Fig. 5. Gate drive voltage $V_{\rm gs}$ versus input voltage $V_{\rm in}$.

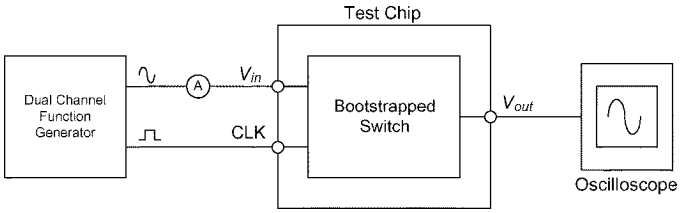

Fig. 6. Lab setup for characterizing bootstrapped switch.

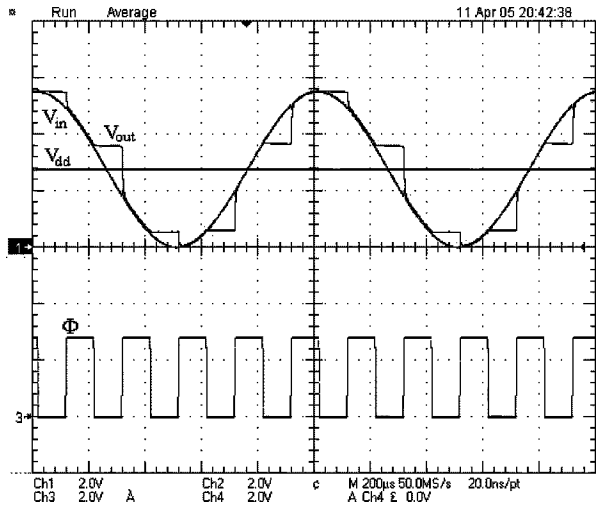

Fig. 7. Measured switch behavior with a dynamically changing input signal.

the proposed circuit. With digital CMOS technologies that do not have a drain-extended option, critical devices can each be replaced by a cascoded pair of normal transistors and obtain good reliability [2], [10], [11].

The performance of the bootstrapped switch was obtained by using it in a sub-ranging SAR ADC integrated on a system-on-chip (SoC) PIC. The ADC in our system was utilized to monitor low-frequency and DC signals exceeding supply voltage in a noisy environment. Moreover, a standalone version of the switch enabled us to verify functionality in the analog domain. Standard latch-up prevention techniques were employed in the

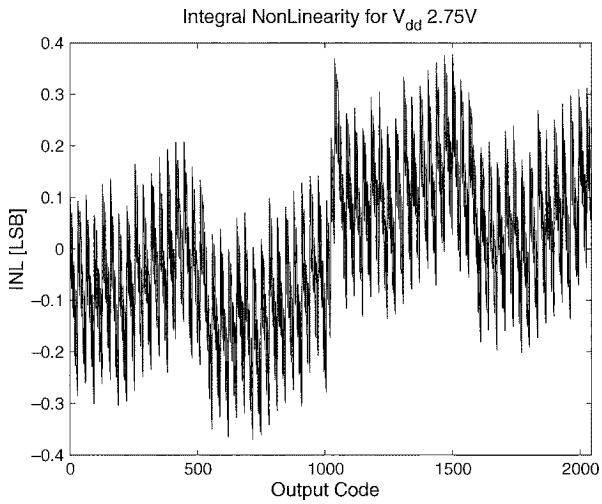

Fig. 8. Linearity performance of SAR ADC utilizing proposed bootstrapped switch.

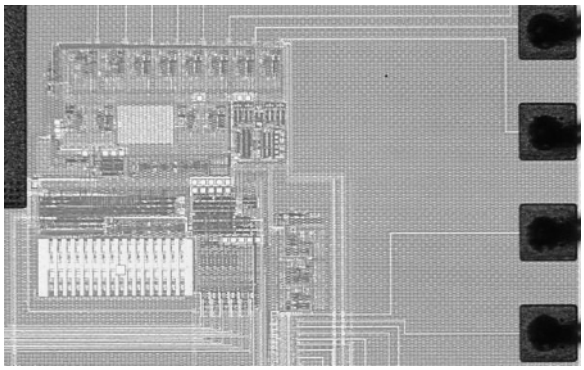

Fig. 9. Die photo of test chip containing proposed bootstrapped switch.

layout of the bootstrapped switch by separating all nMOS transistors from their pMOS counterparts with an N-well guard ring.

Fig. 6 shows the test setup used to characterize the standalone version of the switch. An ameter was included in the setup to verify that no parasitic diodes get forward biased when the signal exceeds the supply voltage. Fig. 7 shows the corresponding measured sampled signal. As expected, even when the input signal goes up to twice the supply voltage, the obtained output signal tracks the input signal very well. The input signal frequency used was 1 kHz and the sampling clock was running at 5 kHz. The nominal supply voltage was 2.75 V, while the input signal amplitude could rise up to 5.5 V.

The circuit can operate with a lower supply voltage. Simulation results show that the minimum allowed supply voltage is $2V_{\rm tn}$ and, indeed, measurement results indicate proper operation of the switch with supply voltage as low as 1.2 V. Using this supply voltage, the switch works properly with input signals up to 6 V, giving a maximum $V_{\rm in}/V_{\rm dd}$ ratio equal to 5. The current drained from the input signal generator is less than 1 μA. The current from the supply generator is also lower than 1 μA. Therefore, the load to the input is negligible, verifying also that there are no forward-biased diodes.

Fig. 8 shows the measured integral nonlinearity (INL) performance of a low-speed 11-bit SAR ADC where the bootstrapped

switch was employed to extend the input signal range beyond the supply voltage. The plot shows outstanding linearity performance for input signals above or below the supply voltage, further indicating proper functionality of the device.

Fig. 9 shows the microphotograph of the test chip. The active area required for the implementation of the switch was less than 0.008 mm^2.

VII. Conclusion

A new bootstrapped switch capable of operating with an input voltage much higher than the supply voltage has been presented. The operation is obtained thanks to a circuit solution that avoids forward biasing in the diffusion-well junctions. The switch is suitable for many applications, including various data-converter architectures. The switch is able to control the output transistor with a V_{gs} that is almost constant over a wide range of switched voltage. This ensures a low harmonic distortion. Finally, the voltage stress on the transistor gates is well controlled, leading to no degradation of the circuit reliability.

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Dr. Maloberti was the recipient of the XII Pedriali Prize for his technical and scientific contributions to national industrial production in 1992. He was co-recipient of the 1996 Institute of Electrical Engineers (U.K.) Fleming Premium. He was the President of the IEEE Sensor Council from 2002 to 2003 and Vice-President, Region 8, of the IEEE Circuits and Systems Society from 1995 to 1997 and an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART II. He received the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, and the 2000 IEEE Millennium Medal.