Switch-Induced Error Voltage on a Switched Capacitor

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Abstract—**A concise analytical expression for switch-induced error voltage on a switched capacitor is derived from the distributed MOSFET model. The result, however, can be interpreted in terms of a simple lumped equivalent circuit. With this expression we explore the dependence of the error voltage on process, switch turnoff rate, source resistance, and other circuit parameters. These results can be used to quickly predict the error voltage. The analytical expression is supported by the close agreement with computer simulations and experiments.**

LIST OF SYMBOLS

β	Conductance coefficient
C_L	Storage capacitance
C_{ol}	Gate-drain overlap capacitance
C_{ox}	Gate capacitance (excluding overlap capacitance)
C'_{ox}	Gate capacitance per unit area
G	Channel conductance
L	Effective channel length ($L_{drawn} - 2L_D$)
L_D	Lateral diffusion distance
N_{sub}	Substrate doping
R_S	Source resistance of the signal voltage source
t_{ox}	Gate-oxide thickness
U	Gate voltage falling rate
V_G	Gate voltage
V_H	High value of V_G
V_L	Low value of V_G
V_S	Signal voltage at the source
V_T	Threshold voltage with back-gate bias
V_{T0}	Zero-bias threshold voltage
$v_d(t)$	Error voltage at drain end at time t
v_{dn}	Error voltage at drain end after gate voltage reaches V_L
v_{dm}	Absolute value of v_{dn}
W	Channel width.

I. INTRODUCTION

THE error voltage induced by the turning off of an MOS switch is one of the fundamental factors that limit the accuracy of switched-capacitor circuits, such as A/D, D/A converters, and filters [1]. An MOS transistor holds mobile charges in its channel when it is on. When the transistor turns off, some portion of the mobile charges is transferred to the storage capacitor and causes an error in the sampled voltage (see Fig. 1). The clock voltage feedthrough through the gate–drain overlap capacitance also contributes to the error. The turnoff of an MOS switch consists of two distinct phases. During the first phase, the transistor is on and a conduction channel extends from the source to the drain of the transistor. As the gate voltage falls, mobile charges exit through both the source end and the drain end. When the gate voltage reaches the threshold voltage, the conduction channel disappears (subthreshold conduction is not included in our analytical analysis), and the transistor enters the second phase of turnoff. During this phase, only the clock feedthrough through the gate–drain overlap capacitance continues to increase the error voltage. The switch-induced error voltage on a switched capacitor can be reduced by turning off the switch very slowly to allow charges to return to the source end and by minimizing the part of gate voltage swing that is below the threshold voltage to minimize the effect of the gate–drain overlap capacitance. Compensation schemes [2], [3] have been used to reduce the switch-induced error voltage. However, little work has been done on the analysis of this phenomenon.

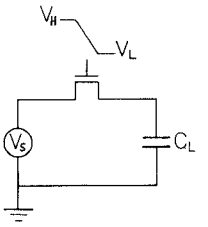

Fig. 1. Schematic of the switch circuit under study.

In this paper, we analyze the switching-off behavior of the MOS switch. An analytical expression for the switch-induced error voltage is derived. Using this expression we explore the dependence of the error voltage on process and gate voltage falling rate. These results can be used to quickly predict the error voltage. Finally, computer simulations and experiments are used to validate the analysis. The derivation of the lumped model from the distributed model is discussed in Appendix I.

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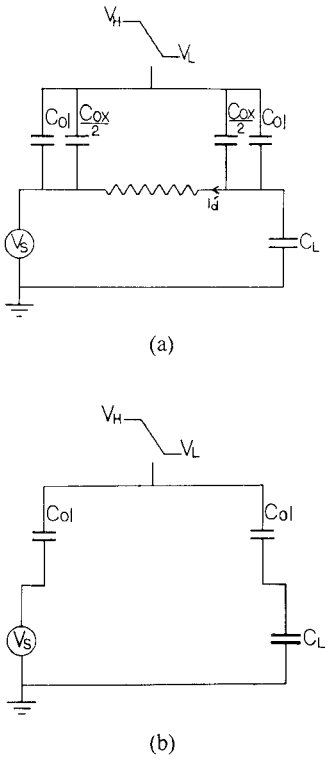

Fig. 2. Equivalent lumped models for the circuit shown in Fig. 1. (a) $V_H \geq V_G \geq V_S + V_T$. (b) $V_S + V_T > V_G \geq V_L$. This equivalent circuit is derived in Appendix I.

II. Analytical Model of Error Voltage

We assume that the charge pumping phenomenon [4] due to the capture of channel charges by the interface traps is not significant. In other words, when the transistor turns off, all the channel mobile charges exit through the source and drain ends. The circuit schematic to be analyzed is shown in Fig. 1 (NMOS switch is used for illustration). The source end of the switch is connected to a signal voltage source with value V_S, and the drain end is connected to a storage capacitor with capacitance C_L. The equivalent lumped models for the circuit during the first and second phases of turnoff are shown in Fig. 2. The configuration of the lumped model is not arbitrarily chosen but results from an exact analysis of the distributed MOSFET model as shown in the Appendix.

From the KCL law

$$C_L \frac{dv_d}{dt} = -i'_d + \left(C_{o1} + \frac{C_{ox}}{2}\right)\frac{d(V_G - v_d)}{dt}. \tag{1}$$

We assume that the gate voltage is a ramp function which begins to fall at time 0 from the high value V_H toward the low value V_L at a falling rate U:

$$V_G = V_H - Ut. \tag{2}$$

Under the condition $|dV_G/dt| \gg dv_d/dt|$[1], (1) simplifies to

$$C_L \frac{dv_d}{dt} = -i'_d - \left(C_{o1} + \frac{C_{ox}}{2}\right)U. \tag{3}$$

[1]This assumption is also needed in deriving the lumped model. See Appendix I.

When the transistor is operated in the strong inversion region ($V_H \geq V_G \geq V_S + V_T$),

$$i'_d = Gv_d \equiv \beta(V_{HT} - Ut)v_d \tag{4}$$

where

$$\beta = \mu C'_{ox}\frac{W}{L} \text{ and } V_{HT} = V_H - V_S - V_T.$$

Equation (3) becomes

$$C_L \frac{dv_d}{dt} = -\beta(V_{HT} - Ut)v_d - \left(C_{o1} + \frac{C_{ox}}{2}\right)U. \tag{5}$$

The solution of the differential equation is

$$v_d(t) = -\sqrt{\frac{\pi UC_L}{2\beta}}\left(\frac{C_{o1} + \frac{C_{ox}}{2}}{C_L}\right)\exp\left\{\frac{\beta U}{2C_L}\left(t - \frac{V_{HT}}{U}\right)^2\right\}$$
$$\cdot\left\{\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}V_{HT}\right] - \operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}(V_{HT} - U_t)\right]\right\}. \tag{6}$$

At $t' = V_{HT}/U$, the threshold condition is reached ($V_G = V_S + V_T$) and the first phase ends. After that only the gate–drain overlap capacitor continues to contribute to the error voltage. The error voltage at this time is

$$v_d(t') = -\sqrt{\frac{\pi UC_L}{2\beta}}\left(\frac{C_{o1} + \frac{C_{ox}}{2}}{C_L}\right)\operatorname{erf}\left(\sqrt{\frac{\beta}{2UC_L}}V_{HT}\right). \tag{7}$$

When the gate voltage reaches its final value V_L, the total amount of switch-induced error voltage on a switched capacitor is

$$v_{dn} \equiv -v_{dm} = -\sqrt{\frac{\pi UC_L}{2\beta}}\left(\frac{C_{o1} + \frac{C_{ox}}{2}}{C_L}\right)\operatorname{erf}\left(\sqrt{\frac{\beta}{2UC_L}}V_{HT}\right)$$
$$-\frac{C_{o1}}{C_L}(V_S + V_T - V_L). \tag{8}$$

It is well known that

$$\operatorname{erf}(x) \approx \begin{cases} 1 & \text{if } x \gg 1 \\ \frac{2x}{\sqrt{\pi}}\left(1 - \frac{x^2}{3}\right) & \text{if } x \ll 1 \end{cases}$$

therefore, (8) can be simplified under the two extreme cases:

for slow switching-off

$$\frac{\beta V_{HT}^2}{2C_L} \gg U$$

$$v_{dm} = \left(\frac{C_{o1} + \frac{C_{ox}}{2}}{C_L}\right)\sqrt{\frac{\pi UC_L}{2\beta}} + \frac{C_{o1}}{C_L}(V_S + V_T - V_L) \tag{9}$$

for fast switching-off

$$\frac{\beta V_{HT}^2}{2C_L} \ll U$$

$$v_{dm} = \left(\frac{C_{o1} + \frac{C_{ox}}{2}}{C_L}\right)\left(V_{HT} - \frac{\beta V_{HT}^3}{6UC_L}\right) + \frac{C_{o1}}{C_L}(V_S + V_T - V_L). \tag{10}$$

III. Dependence on Process and Electrical Parameters

The switch-induced error voltage on a switched capacitor is affected by many factors. The factors of the greatest interest are the gate voltage falling rate, signal voltage level, substrate doping, oxide thickness, transistor size, and source resistance of the signal voltage source. Common parameter values used in the following examples are: $W = 4$ μm, $L = 3.3$ μm, $L_D = 0.35$ μm, $C_L = 2$ pF, $t_{ox} = 70$ nm, $N_{sub} = 5.0 * 10^{14}$ cm^{-3}, $V_{T0} = 0.6$ V, $V_H = 5$ V, $V_L = 0$ V, $U = 1$ V·ns^{-1}, and $\mu_n C'_{ox} = 25 * 10^{-6}$ A·V^{-2}. These are typical values to be found in the state-of-the-art circuit designs. From (8) we notice that the switch-induced error voltage of an NMOS switch is negative. In the following discussion we will focus on the absolute value of this error voltage and denote it as v_{dm}.

A. Dependence on Gate Voltage Falling Rate

Error voltage v_{dm} is plotted against the gate voltage falling rate ranging from 10^4 V·s^{-1} to 10^{11} V·s^{-1} for four signal voltage levels, 0, 1, 2, and 3 V in Fig. 3. In the case of slow falling rate, most of the channel charges return to the source when the switch is on, and the error voltage is primarily due to the clock feedthrough of the gate–drain overlap capacitance after the switch is turned off. At a very slow falling rate, v_{dm} saturates at $(V_S + V_T - V_L)C_{o1}/C_L$, as can be seen from (9). In the case of fast falling rate, nearly one half of the channel charges are deposited in the storage capacitor and v_{dm} saturates at $V_{HT}(C_{o1} + C_{ox}/2)/C_L + (V_S + V_T - V_L)C_{o1}/C_L$ as can be seen from (10). From Fig. 3, it is obvious that the dependence of v_{dm} on V_S may be minimized by judiciously choosing the falling rate.

B. Dependence on Signal Voltage Level and Substrate Doping

Error voltage v_{dm} is plotted against signal voltage V_S for five substrate dopings in Fig. 4. As the substrate doping increases, body effect increases accordingly, which in turn causes the threshold voltage in (8) to become more sensitive to V_S. The argument of the error function in expression (8) is smaller for large V_S or heavier substratee doping. As long as the first term in (8) dominates, e.g., at fast falling rates, v_{dm} is a strong function of V_S and more so in the heavy-substrate-doping circuits.

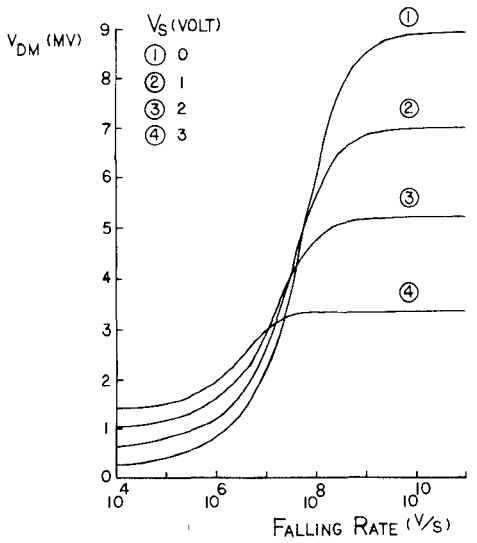

Fig. 3. The error voltage as a function of the gate voltage falling rate for four signal voltage levels.

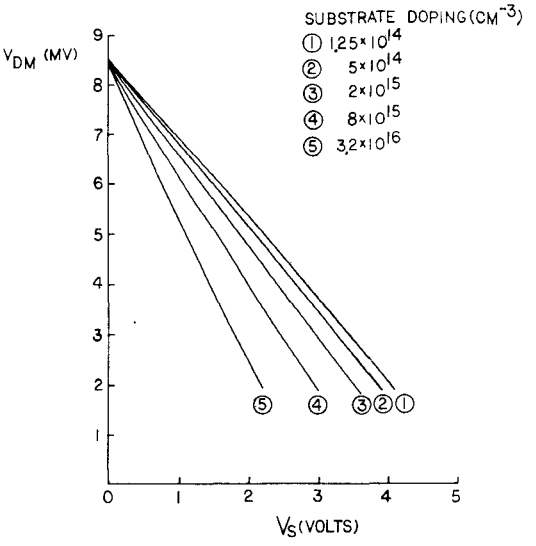

Fig. 4. The error voltage as a function of the signal voltage level for five substrate dopings.

C. Dependence on Oxide Thickness

Advances in silicon technologies continue to make smaller MOS device dimensions possible. As the device size shrinks, the oxide thickness reduces, too. If storage capacitor oxide and gate oxide are scaled by the same factor, $(C_{o1} + C_{ox}/2)/C_L$ remains constant. The effect of C_L increase due to oxide reduction is exactly balanced by the effect of β increase (assuming constant W/L) such that the square root term and the error function term in (8) are unaltered. Hence, error voltage v_{dm} is not affected.

D. Dependence on Channel Width and Length

Transistor size is one of the most important variables in circuit design. Designers have to choose the appropriate combination of transistor sizes in order to achieve optimum circuit performance. Error voltage v_{dm} is plotted

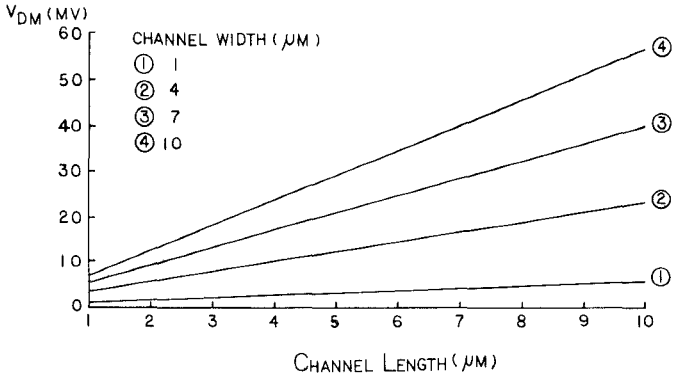

Fig. 5. The error voltage as a function of transistor channel length for four channel widths

against channel length ranging from 1 to 10 μm for four different channel widths, 1, 4, 7, and 10 μm in Fig. 5. It is clear that smaller transistor size introduces smaller error voltage with the set of typical circuit parameter values listed at the beginning of this section.

E. Effect of Source Impedance

Source impedance of the signal voltage affects the error voltage. The circuit schematic which includes a source resistance is shown in Fig. 6. Derivation of the analytical model including source resistance is quite similar to that without source resistance and is attached as Appendix II. Error voltage is plotted against source resistance in Fig. 7. As the source resistance increases, fewer channel charges return to the source end of the transistor and error voltage becomes larger.

IV. Comparison with Computer Simulation

To validate the model, computer simulations using the SPICE 2G [5], [6] circuit simulation program have been performed. The circuit configuration for computer simulations is the same as that of Fig. 1. One example of a SPICE input file is as follows:

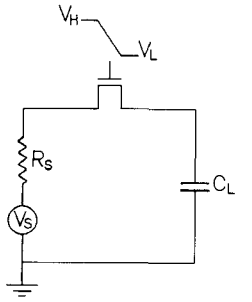

Fig. 6. Schematic of the switch circuit with source resistor.

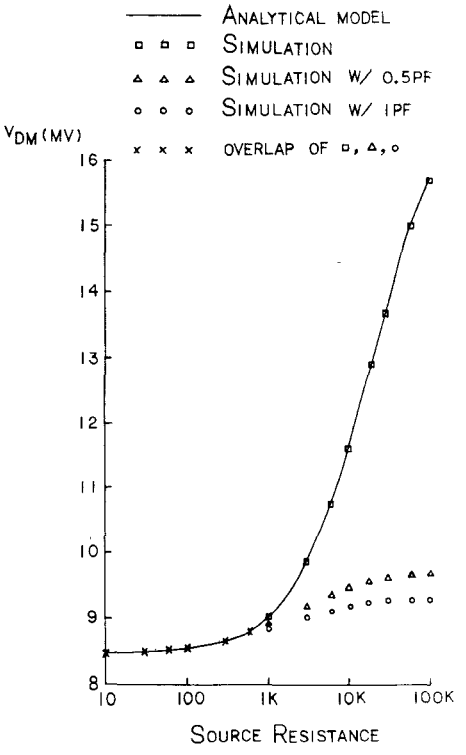

Fig. 7. Comparison of the analytic and computer simulated results of the error voltage as a function of source resistance. Computer simulated results with 0.5 pF/1 pF capacitance in parallel with R_S are also shown.

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SIMULATION OF SWITCH-INDUCED ERROR VOLTAGE ON A SWITCHED CAPACITOR
* XQC < 0.5 FOR CHARGE CONTROLLED MODEL
M1 2 1 3 0 MODN W = 4U L = 4U
CSTORAGE 2 0 2P
·MODEL MODN NMOS LEVEL = 2 TOX = 70N NSUB = 5E14 KP = 25U LD = 0.35U
+ VT0 = 0.6 VMAX = 5E4 CGS0 = 1.7255E-10 CGD0 = 1.7255E-10 XQC = 0.4999
VG 1 0 PWL (0 5 10N 5 60N 0)
VS 3 0 DC 0
.OPTIONS ABSTOL = 1E-14 CHGTOL = 1E-16 RELTOL = 1E-5
.TRAN 1N 65N
.PRINT TRAN V(2)V(1)
.END.
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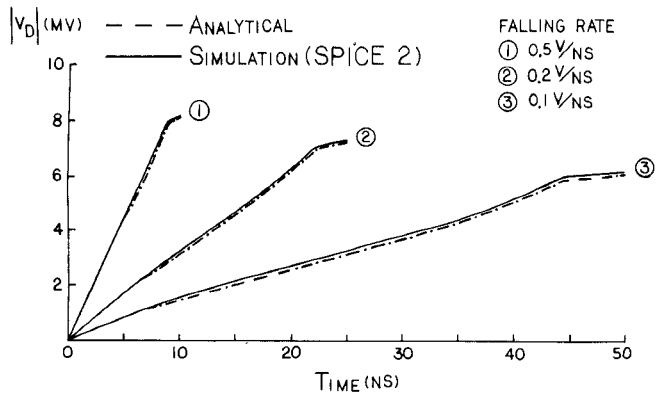

Fig. 8. Comparison of the analytic and computer simulated transient responses for three different gate voltage falling rates.

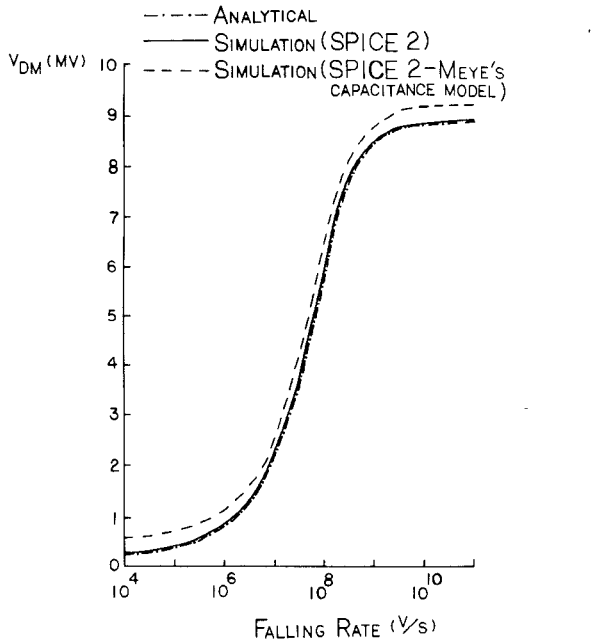

Fig. 9. Comparison of the analytic and computer simulated results of the error voltage as a function of the gate voltage falling rate.

The analytical transient response, (6), and computer simulated results for three different gate voltage falling rates 0.1 V/ns, 0.2 V/ns, and 0.5 V/ns are shown in Fig. 8. The close correspondence between the analytical analysis and the computer simulation is evident. The error voltage is plotted against the gate voltage falling rate for both the analytical and simulation results in Fig. 9. The agreement is excellent. Error voltages from both analytical and computer simulated results are shown in Fig. 7. Computer simulated result is shown in Fig. 7 together with the analytical result for the circuit schematic of Fig. 6. They match very well. Two other curves of simulated results in Fig. 7 correspond to the case where source capacitance exists in parallel with source resistance. The existence of the source capacitor compensates the effect of source resistance and inhibits the error voltage from increasing too much. The larger the capacitance is, the more the compensation effect will be.

A charge controlled model is used in the SPICE simulation by specifying the *XQC* parameter a value smaller than

TABLE I

NMOS Switch Parameters	
V_T (V_{SB} = 0.0 V)	0.70 V
V_T (V_{SB} = 0.2 V)	0.81 V
W_{drawn}	40 μm
L_{drawn}	6 μm
L_D	0.45 μm
β	295 $\mu A \cdot V^{-2}$
t_{ox}	85 nm

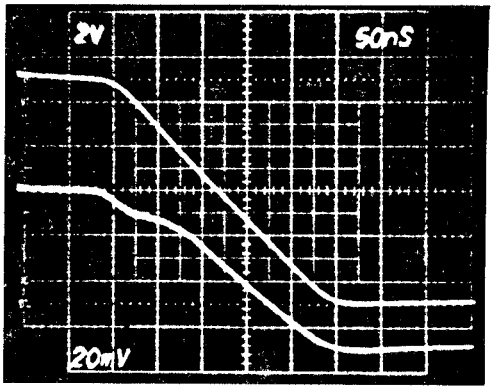

Fig. 10. Turnoff transient response of the switched-capacitor circuit shown in Fig. 1. The top curve is the waveform applied to the gate. The bottom curve is the error voltage waveform at the drain.

0.5 so that charge conservation is retained. If the *XQC* parameter is assigned a value greater than or equal to 0.5, Meyer's capacitance model is automatically employed and charge conservation is not guaranteed [7]. Meyer's capacitance model is implemented in a SPICE MOS level-2 model in such a manner as to improve the convergence of circuit simulation [8]. However, it might introduce a small error to those transient simulations which are very sensitive to the capacitive currents of the transistors. The error introduced is insignificant for most circuit simulations but may be quite serious in simulating switched-capacitor circuits. One curve corresponding to simulated results using SPICE MOS level-2 and Meyer's capacitance model is also shown in Fig. 9. The SPICE simulation with Meyer's capacitance model generates an error of a fraction of a millivolt. The analytical model presented in this paper has no hidden error to the extent that its underlying assumptions, which are easily identified, are valid.

V. Experimental Results

Experimental transistors for the MOS switch were designed and fabricated using a local oxidation polysilicon gate CMOS process. The transistor parameters are listed in Table I. The stray capacitance between the probes of a on-wafer testing station is quite large when the probes are close to each other. We put the transistors inside a 24-pin package to reduce such interprobe capacitance.

A precision capacitance meter is employed to determine the effective storage capacitance C_L existing at the drain end. The measured value was 24.5 pF. Fig. 10 shows a typical turnoff transient response of the switched capacitor

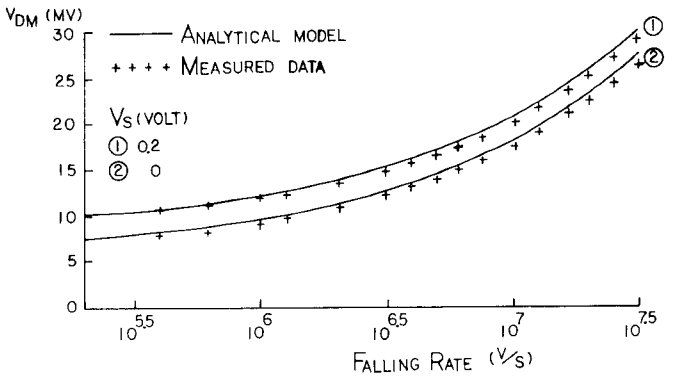

Fig. 11. Measured and calculated error voltages as functions of gate voltage falling rate for two signal voltage levels

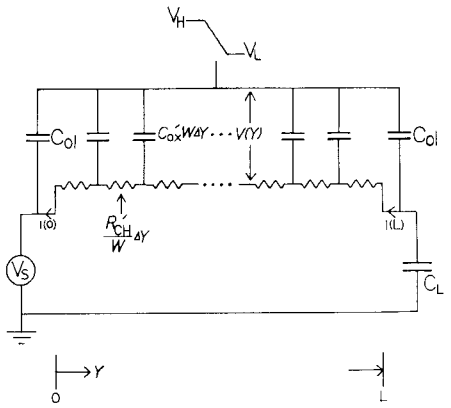

Fig. 12. Distributed model for the circuit shown in Fig 1.

circuit studied. The top curve is $V_G(t)$ and the bottom curve is $v_d(t)$. The lower linear part of the bottom curve, corresponding to the second phase of switch turnoff, was used to extract the total capacitance between the gate pin and the drain pin of the switch, including the true transistor gate-drain overlap and the parasitic probe capacitances. The obtained value was 195 fF. It was used as C_{o1} in (8). Switch-induced error voltage was measured against the gate voltage falling rate ranging from 4×10^5 V·s^{-1} to 3.3×10^7 V·s^{-1} for two different signal voltage levels, 0 and 0.2 V. Fig. 11 shows the measured data and calculated results from the analytical model (8). Good agreement is found in both cases.

VI. Conclusion

An analytical expression for the switch-induced error voltage on a switched capacitor is presented. The expression plainly predicts the dependence of the error voltage on gate voltage falling rate, signal voltage level, transistor size, and process changes. For example, the error voltage increases with increasing V_S at low gate voltage falling rates and decreases with increasing V_S at high gate voltage falling rates. Computer simulations and experiments affirm the validity of the analysis. The compact expression (8) should be convenient in the analysis of switched-capacitor circuits.

Appendix I
Derivation of the Lumped Model from the Distributed Model

Referring to Fig. 12,

$$\frac{di}{dy} = -C_{ox}'W\frac{d[V_G - V(y)]}{dt}$$

$$\approx -C_{ox}'W\frac{dV_G}{dt} \tag{A1}$$

$$i(y) = i(0) - C_{ox}'W\frac{dV_G}{dt}y \tag{A2}$$

$$i_d \equiv i(L) = i(0) - C_{ox}'WL\frac{dV_G}{dt}$$

$$= i(0) - C_{ox}\frac{dV_G}{dt} \tag{A3}$$

$$\frac{dv}{dy} = i(y)\frac{R_{ch}'}{W}$$

$$= i(0)\frac{R_{ch}'}{W} - C_{ox}'R_{ch}'\frac{dV_G}{dt}y$$

$$v(y) = i(0)\frac{R_{ch}'}{W}y - C_{ox}'R_{ch}'\frac{dV_G}{dt}\frac{y^2}{2} \tag{A4}$$

$$v_d \equiv v(L) = i(0)\frac{R_{ch}'}{W}L - C_{ox}'R_{ch}'\frac{dV_G}{dt}\frac{L^2}{2}$$

$$= \frac{i(0)}{G} - \frac{C_{ox}}{2G}\frac{dV_G}{dt}. \tag{A5}$$

Eliminate $i(0)$ from (A3) by using (A5)

$$i_d = v_dG - \frac{C_{ox}}{2}\frac{dV_G}{dt}. \tag{A6}$$

It is obvious that

$$C_L\frac{dv_d}{dt} = -i_d + C_{o1}\frac{dV_G}{dt}. \tag{A7}$$

Hence we obtain the desired expression

$$C_L\frac{dv_d}{dt} = -Gv_d + \left(C_{o1} + \frac{C_{ox}}{2}\right)\frac{dV_G}{dt}$$

$$= -i_d' + \left(C_{o1} + \frac{C_{ox}}{2}\right)\frac{dV_G}{dt}. \tag{A8}$$

Expression (A8) may be interpreted with a equivalent lumped circuit as shown in Fig. 2(a). It is trivial to show that Fig. 12 reduces to Fig. 2(b) for $V_G < V_S + V_T$.

Appendix II
Derivation of the Analytic Model Including Source Resistance

Referring to Fig. 6 and (A8), KCL law at node A and node B requires

$$C_L\frac{dv_d}{dt} = -i_d' + \left(C_{o1} + \frac{C_{ox}}{2}\right)\frac{d(V_G - v_d)}{dt} \tag{B1}$$

$$\frac{v_s}{R_S} = i_d' + \left(C_{o1} + \frac{C_{ox}}{2}\right)\frac{d(V_G - v_s)}{dt} \tag{B2}$$

With the same assumptions in Section II, when the transistor is on, (B1) and (B2) simplify to

$$C_L\frac{dv_d}{dt} = -\beta(V_{HT}-Ut)(v_d-v_s)-\left(C_{o1}+\frac{C_{ox}}{2}\right)U \quad \text{(B3)}$$

$$\frac{v_s}{R_S} = \beta(V_{HT}-Ut)(v_d-v_s)+\left(C_{o1}+\frac{C_{ox}}{2}\right)U. \quad \text{(B4)}$$

Using (B4) to eliminate v_s from (B3), we obtain a first-order differential equation,

$$C_L\frac{dv_d}{dt} = -\frac{\beta(V_{HT}-Ut)}{1+\beta R_S(V_{HT}-Ut)}v_d-\left(C_{o1}+\frac{C_{ox}}{2}\right)\cdot\left[2-\frac{1}{1+\beta R_S(V_{HT}-Ut)}\right]U. \quad \text{(B5)}$$

Solving this differential equation and including the clock feedthrough due to gate–drain overlap capacitance when the transistor is off, we get the complete solution,

$$v_{dm} = \frac{C_{o1}}{C_L}(V_S+V_T-V_L)+U\left(\frac{C_{o1}+\frac{C_{ox}}{2}}{C_L}\right)\cdot\exp\left[-\frac{V_{HT}}{UC_LR_S}\right]\cdot\int_0^{V_{HT}/U}(\beta R_S(V_{HT}-U\xi)+1)^{1/C_L\beta R_S^2U}\cdot\exp\left(\frac{\xi}{C_LR_S}\right)\left(2-\frac{1}{1+\beta R_S(V_{HT}-U\xi)}\right)d\xi. \quad \text{(B6)}$$

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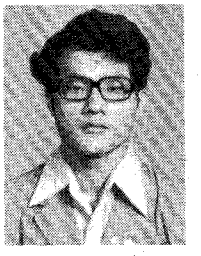
References

[1] P. R. Gray, D. A. Hodges, and R. W. Brodersen, Eds., *Analog MOS Integrated Circuits*. New York: IEEE Press, 1980.
[2] R. E. Suarez, P. R. Gray, and D. A. Hodges, "All-MOS charge redistribution analog-to-digital conversion techniques: Part II," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 379–385, Dec. 1975.
[3] R. C. Yen and P. R. Gray, "An MOS switched-capacitor instrumentation amplifier," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 1008–1013, Dec. 1982.
[4] D. Schmitt and G. Dorda, "Interface states in MOSFET's due to hot-electron injection determined by the charge pumping technique," *Electron. Lett.*, vol. 17, no. 20, Oct. 1981.
[5] L. W. nagel, "SPICE2: A computer program to simulate semiconductor circuits," Electron. Res. Lab., Univ. California, Berkeley, memo. ERL-M520, May 1975.
[6] A. Vladimirescu and S. Liu, "The simulation of MOS integrated circuits using SPICE2," Electron. Res. Lab., Univ. California, Berkeley, memo. ERL-M80/7, Oct. 1980.
[7] D. E. Ward and R. W. Dutton, "A charge-oriented model for MOS transistor capacitances," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 703–708, Oct. 1978.
[8] A. Vladimirescu, private communication.



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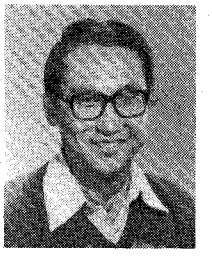

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