SWITCHED-CAPACITOR DC-DC CONVERTERS FOR LOW-POWER ON-CHIP APPLICATIONS

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***Abstract** – The paper describes switched-capacitor dc-dc converters (charge pumps) suitable for on-chip, low-power applications. The proposed configurations are based on connecting two identical but opposite-phase SC converters in parallel, thus eliminating the need for separate bootstrap gate drivers. We focus on emerging very low-power VLSI applications such as battery-powered or self-powered signal processors where high power conversion efficiency is important and where power levels are in the milliwatt range. Conduction and switching losses are considered to allow design optimization in terms of switching frequency and component sizes. Open-loop and closed-loop operation of an experimental, fully integrated, 10MHz voltage doubler is described. The doubler has 2V or 3V input and generates 3.3V or 5V output at up to 5mW load. The converter circuit fabricated in a standard 1.2μ CMOS technology takes 0.7mm^2 of the chip area.*

1 Introduction

Switched-capacitor (SC) dc-dc converters (also called "charge pumps") are power converters that consist of switches and energy-transfer capacitors in the power stage. The switches are periodically turned on and off so that the converter cycles through a number of switched networks. Possible low and medium-power applications of SC converters have been examined in a number of publications ([1]-[9], and others). In this paper, we focus on very low-power, on-chip applications [1, 2, 3], where there is a need to generate various DC voltage levels from a given external DC supply V_{DD}. Such applications include EEPROM and Flash memories, auxiliary supplies for analog portions of low-voltage, mixed-signal VLSI, and implementation of emerging adaptive voltage-scaling power management techniques [10] in energy-limited systems. The output power in these applications is often in the milliwatt range, but converter efficiency and area taken by the converter can be very important.

The purpose of this paper is to introduce design objectives and constraints in the relatively new and expanding power electronics area of on-chip power conversion. A general approach to construct SC converter configurations well suited for on-chip implementation in standard CMOS technologies is discussed in Section 2, together with analysis of conduction and switching losses. An experimental, fully
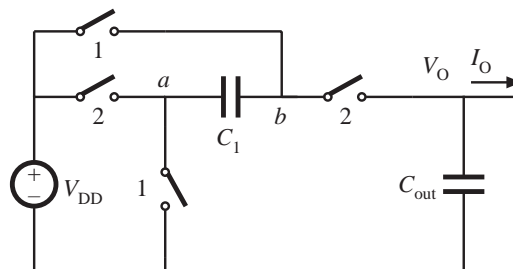
Figure 1: Ideal switched-capacitor voltage doubler. Switches "1" are on during one phase of the clock, switches "2" are on during the opposite phase.

integrated voltage doubler is described in Section 3.

2 On-Chip Implementation of SC Converters in Standard CMOS Technology

In two-phase SC converters, an example of which is shown in Fig. 1, the number of switched networks is two. When an ideal SC converter is unloaded, the DC voltage conversion ratio $M = V_O/V_{DD}$ assumes a value $M = M_i$, which is uniquely determined by the converter topology. For example, the basic voltage doubler shown in Fig. 1 has the ideal step-up conversion ratio $M_i = V_O/V_{DD} = 2$.

In this section we examine issues related to design and implementation of fully integrated switched-capacitor power converters in standard CMOS technology. First, it is of interest to compare some of the traditional discrete-component power converter design constraints to integrated-circuit (IC) realizations. In discrete-component realizations, minimizing the power-stage component count and circuit complexity are the usual cost constraints, whereas in IC realizations the required chip area is important. Much more flexibility is available to the designer in sizing components (switches and capacitors), but the component characteristics are subject to the technology limitations, some of which are pointed out in this section.

2.1 On-chip capacitors

In a standard CMOS process, there are a number of ways to construct capacitors. For example, Fig. 2 shows a capacitor constructed as a parallel-plate capacitor using two polysillicone layers in a double-poly CMOS process. The circuit model for the capacitor
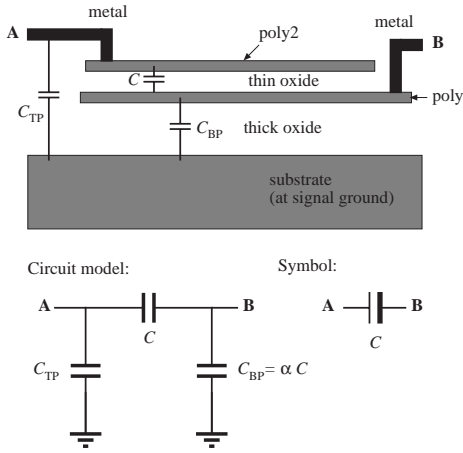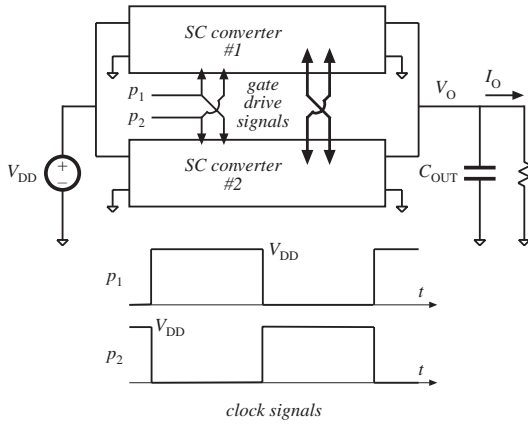
Figure 2: Double-poly capacitor.

Figure 3: A general implementation block diagram using two opposite-phase SC converters connected in parallel.

C also includes parasitic capacitances: C_{BP} from the bottom plate of C to substrate (ground), and C_{TP} from the top plate to substrate. The top-plate capacitance is due to the interconnect metal wires, and is usually very small compared to the capacitance C. However, the bottom-plate capacitor has area at least equal to the area of the capacitor C, and so it can have very significant value and effects on the circuit operation. The bottom-plate capacitance can be expressed as $C_{BP} = \alpha C$, where can be up to 10% for the double-poly capacitor.

2.2 Switched-capacitor circuit configurations

The switches in an on-chip SC converter can be realized using NMOS or PMOS device, or their parallel or series combinations. For step-up voltage-conversion applications, such as the basic voltage doubler shown in Fig. 1, appropriate gate-drive signals for the switches must include voltage levels above the available supply voltage V_{DD}.

One approach to constructing step-up SC configurations together with appropriate gate drive signals is illustrated in Fig. 3. The idea is to combine two identical SC converters in parallel and operate the converters with opposite-phase clock signals [1]. Fig. 3 shows the two-phase clock signals p_1, p_2, at constant switching frequency f, generated from the input V_{DD} supply. The two converters have the same but opposite-phase pulsating voltages at the internal nodes. The
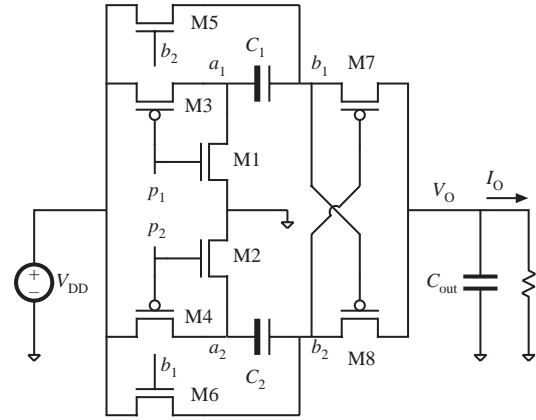

Figure 4: Realization of the voltage doubler based on the block diagram of Fig. 3.

pulsating voltages from one converter are used as gate-drive signals in the other converter.

Fig. 4 shows implementation of the basic voltage doubler of Fig. 1 based on the block diagram of Fig. 3 [2]. One SC converter consists of the switches M_1, M_3, M_5, M_7, and the capacitor C_1. The other SC converter consists of the switches M_2, M_4, M_6, M_8 and the capacitor C_2. The two converters share the same input voltage V_{DD}, and the same output filter capacitor C_{out}. The gates of M_5, M_6 and M_7, M_8 are cross-coupled. Operation of the cross-coupled converter can be described as follows: when p_1 clock is equal to $+V_{DD}$ (i.e. high) and p_2 clock is 0 (i.e. low), M_1 is on, and node a_1 is at approximately zero volts. Device M_4 is on so that node a_2 is at V_{DD}, bringing node b_2 up to approximately $2V_{DD}$ since C_2 was charged up to $+V_{DD}$ in the previous half cycle. As a result, the NMOS device M_5, with the gate tied to the node b_2, is turned on, node b_1 is at approximately V_{DD}, and the capacitor C_1 is charged to $+V_{DD}$ through M_5 and M_1. At the same time, since the node b_2 is at $+2V_{DD}$ and b_1 is at $+V_{DD}$, the PMOS device M_8 turns on and the output is charged to $+2V_{DD}$ through M_4 and M_8, while the device M_7 is off. In the opposite phase, C_2 is recharged to $+V_{DD}$ through M_6 and M_2, while the output is charged to $2V_{DD}$ through M_3, C_1, and M_7.

The parallel, opposite-phase, cross-coupled converter connection eliminates the need for separate bootstrap gate drivers. Also, the effective switching frequency for the output filter capacitor is $2f$, where f is the clock frequency. Each switch is driven with a gate-to-source on-voltage equal to at least V_{DD}, so that the on-voltage drop can be reduced to a small drop across the device on resistance. There are no constant (threshold) voltage drops as in some other low-efficiency implementations.

The cross-coupled converter connection can be used to construct other SC converter configurations. Fig. 5 shows two SC converters with ideal unloaded step-up conversion ratio $V_O/V_{DD} = 3$. Possible on-chip realizations of these two converters following the block diagram of Fig. 3 are shown in Fig. 6.

2.3 Losses and efficiency

Conduction losses originate from charging and discharging of energy-transfer capacitors. The power is dissipated on the switch on-resistances. A switched-capacitor converter model that can predict DC conversion ratio $M = V_O/V_{DD}$ and conduction losses consists of an ideal transformer with turns ratio $M_i = V_O/V_{DD}$ equal to the ideal, no-load conversion ratio of the SC converter, and a series output
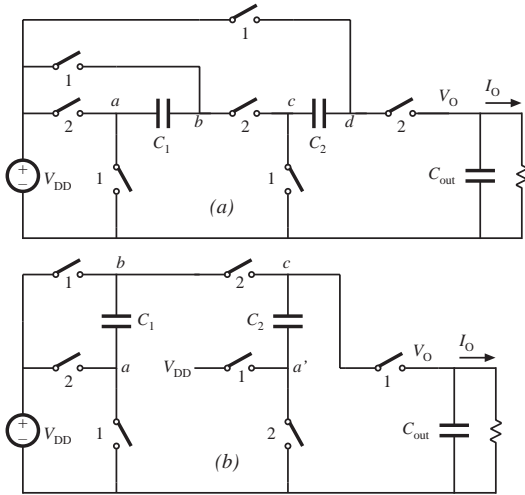
Figure 5: Two switched-capacitor voltage tripler examples.

resistance $R_o(f)$ which is a function of clock frequency f [8, 9].

In the low-frequency limit, the output resistance is inversely proportional to the energy-transfer capacitance values, and the clock frequency [8],

$$R_o(f) = \frac{K}{Cf} \qquad (1)$$

At high switching frequencies, the output resistance reaches a minimum value R_{omin}, which depends on the switch on resistances, and which can be found using state-space averaging. An analytical approximation for $R_o(f)$ over wide range of frequencies was proposed in [9]:

$$R_o(f) \approx R_{omin}\sqrt{1+(f_c/f_s)^2}\,, \qquad (2)$$

where the "corner" frequency f_c is the frequency where the low-frequency asymptote and the high frequency asymptote have the same value,

$$f_c = \frac{K}{CR_{omin}} \qquad (3)$$

For a given load current I_O, the conduction loss P_c can be found as

$$P_c = R_o(f)I_O^2\,. \qquad (4)$$

In an on-chip implementation, the switching losses can be estimated by finding the total parasitic capacitances at various nodes and the voltage swing across the capacitances. If the capacitance from node a to ground is C_a, and if the voltage at the node a is pulsating between $V_1 = m_1 V_{DD}$ and $V_2 = m_2 V_{DD}$, the switching power loss due to this capacitance is

$$P_a = C_a(V_2 - V_1)^2 f = (m_2 - m_1)^2 C_a V_{DD}^2 f \qquad (5)$$

The total switching loss is found by summation of switching losses over all nodes in the SC converter:

$$P_{sw} = \sum_{\text{nodes}} P_{\text{node}} \qquad (6)$$

For example, in the voltage tripler of Fig. 6(a), we get:

$$P_{sw}(a) \approx 2fV_{DD}^2\left(C_a + 2C_b + 4C_c + 6C_d\right)\,, \qquad (7)$$

where, C_a is the total parasitic capacitance from node a_1 (or a_2) to ground.
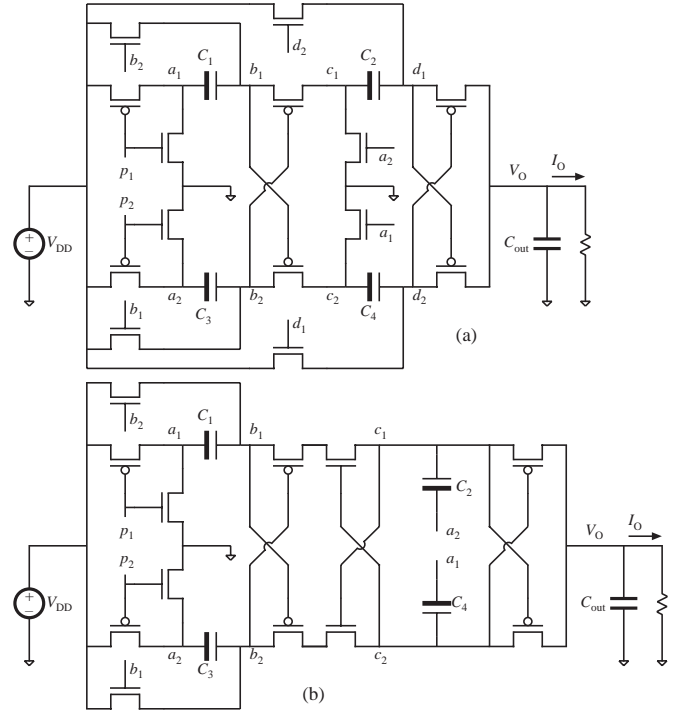

Figure 6: Implementation of the converter examples from Fig. 5 based on the block diagram of Fig. 3.

In the converter of Fig. 6(b), we get:

$$P_{sw}(b) \approx 2fV_{DD}^2\left(C_a + 2C_b + 3C_c\right)\,. \qquad (8)$$

From the results above, one can observe that the converter (b) has an advantage over the converter (a) because the internal voltage node swings are smaller, thus resulting in lower switching losses.

With on-chip capacitors, the bottom-plate parasitic capacitances dominate the nodal capacitances. In the converter (a), we have $C_a \approx C_{BP}$, and $C_c \approx C_{BP}$, so that this portion of the power loss becomes:

$$P_{BP}(a) \approx 10fV_{DD}^2C_{BP} = 10fV_{DD}^2\alpha C\,. \qquad (9)$$

In the converter (b), $C_a \approx 2C_{BP}$, so that:

$$P_{PB}(b) \approx 4fV_{DD}^2C_{BP} = 4fV_{DD}^2\alpha C\,. \qquad (10)$$

Notice that the power loss due to the bottom-plate capacitance in the converter (b) is about 2.5 times smaller than in the converter (a).

From the discussion above, the total switching loss in the converter can be written as

$$P_{sw} = C_{sw}V_{DD}^2 f\,, \qquad (11)$$

where C_{sw} is the equivalent switching-loss capacitance of the converter. For a given converter configuration, optimum clock frequency f can be found where the sum of conduction and switching losses $P_c + P_{sw}$ is minimum [9].

3 Voltage doubler implementation and experimental results

To illustrate on-chip SC converter design issues, we consider implementation of a voltage doubler based on the cross-coupled configu-
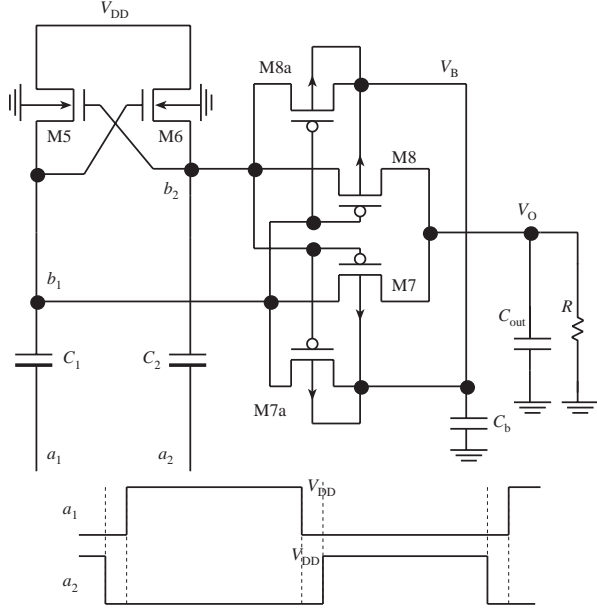
Figure 7: Detailed circuit diagram of the voltage doubler of Fig. 4. Drive transistors M_1, M_2, M_3, M_4 are not shown.

Figure 8: Circuit diagram of the experimental voltage doubler.

ration of Fig. 4. The technology used for fabrication is AMI 1.2μ double-poly n-well technology available through MOSIS [11].

Detailed circuit diagram of the basic voltage doubler is shown in Fig. 7. Substrate connections for all devices are indicated in the figure: NMOS device share the common substrate, which is connected to ground, while PMOS devices are constructed in a common n-well, which is biased at voltage V_B. Two opposite-phase clock signals (p_1 and p_2 shown in Fig. 3), are used to drive CMOS inverters M_1, M_3 and M_2, M_4 shown in Fig. 4, in order to produce two pump drive signals at nodes a_1 and a_2 as shown in Fig. 7. The drive signals at nodes a_1 and a_2 are shown as non-overlapping opposite-phase signals: there are short time intervals when both a_1 and a_2 are at zero volts. NMOS pump devices M_5, M_6 have cross-coupled gates (nodes b_1, b_2), that swing between V_{DD} and $2V_{DD}$. Since the drive signals at nodes a_1, a_2 are nonoverlapping, M_5 and M_6 are never on at the same time. The energy-transfer pump capacitors C_1, C_2 are charged through M_5, M_6 to $+V_{DD}$ in opposite phases of the clock signals. Series PMOS switches M_7, M_8 also have cross-coupled gates and are used to pass $2V_{DD}$ to the output filter capacitor C_{out}. In addition, auxiliary PMOS devices M_{7a}, M_{8a}, and capacitor C_b are used to bias the n-well of the PMOS devices at voltage $V_B \approx 2V_{DD}$ [2]. Since C_b is unloaded, V_B is always greater than or equal to V_{out}, which ensures that the source and drain to n-well junctions of the PMOS devices are always reverse biased. This is important because forward bias of these junctions may cause lossy discharge of the output or latch-up condition through the p-substrate of the chip [2].

A problem with the circuit shown in Fig. 7 is that during the intervals when both a_1 and a_2 are close to ground, both b_1 and b_2 are close to V_{DD}, and therefore *both* PMOS switches M_7, M_8 are turned on at the same time. As a result, undesirable lossy discharge of the output filter capacitor C_{out} occurs. One may attempt to reduce the time intervals when a_1 and a_2 are simultaneously low, or even to slightly overlap the two drive signals. However, this contradicts the desirable timing of the drive waveforms for the NMOS pump devices M_5 and
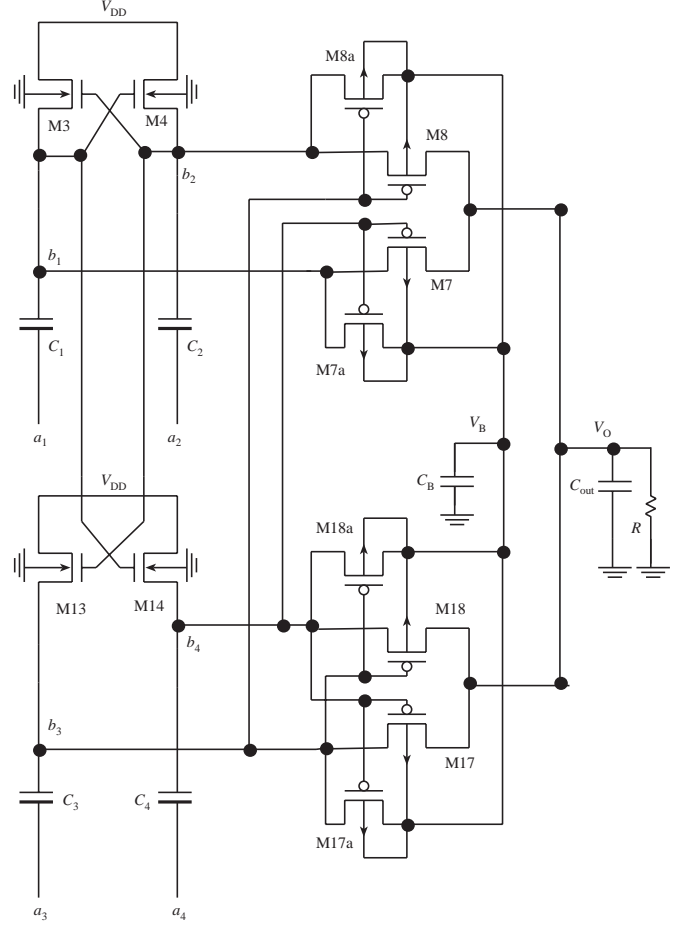
M_6, and may lead to the case when both M_5 and M_6 are turned on at the same time. This would result in lossy discharge of C_1, C_2 back to V_{DD}. The problem with exact timing of the drive signals a_1, a_2 is particularly important at high clock frequencies (in the MHz range and above), because the losses incurred due to the undesirable conduction of the cross-coupled device effectively increase the switching losses in the converter.

In order to alleviate the problem observed in the circuit of Fig. 7, we investigated the circuit shown in Fig. 8. Another cross-coupled pump is added. The second cross-coupled pump is driven by overlapping drive signals at nodes a_3, a_4. The two pumps are coupled so that NMOS devices in both pumps are driven by non-overlapping signals, while PMOS devices in both pumps are driven by overlapping signals as shown in Fig. 9. As a result of this arrangement, possible lossy simultaneous conduction of the pairs (M_3, M_4), (M_{13}, M_{14}), (M_7, M_8), and (M_{17}, M_{18}) are eliminated. However, it is still important that the transitions of a_1 and a_3, as well as of a_2 and a_4 occur at the same time, and that these transitions have short rise and fall times, in order to avoid parasitic discharge of the output filter capacitor C_{out} through one of the PMOS series switches.

The circuit of Fig. 8, together with an oscillator, and a clock generator to produce the waveforms shown in Fig. 9, have been fabricated in 1.2μ double-poly CMOS technology. All capacitors are double-poly capacitors described in Section 2.1. The device and capacitor
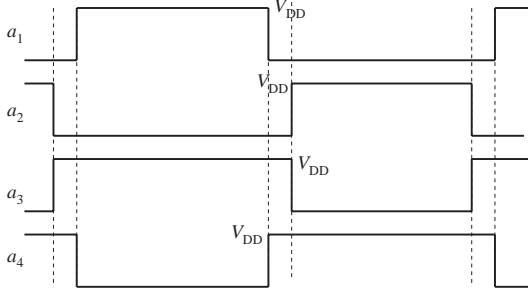
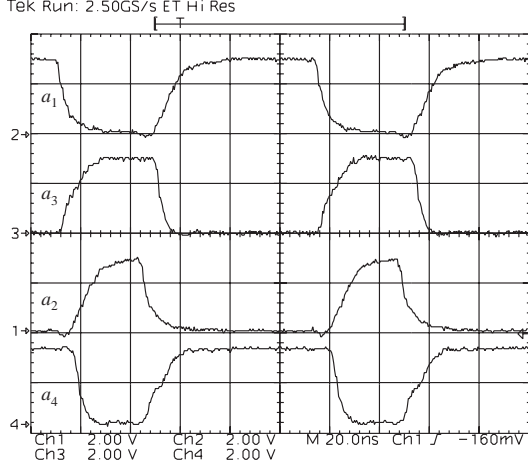Figure 9: Drive waveforms for the voltage doubler in Fig. 8.

Figure 10: Experimental drive waveforms in the doubler of Fig. 8 operating at $f = 10$MHz.
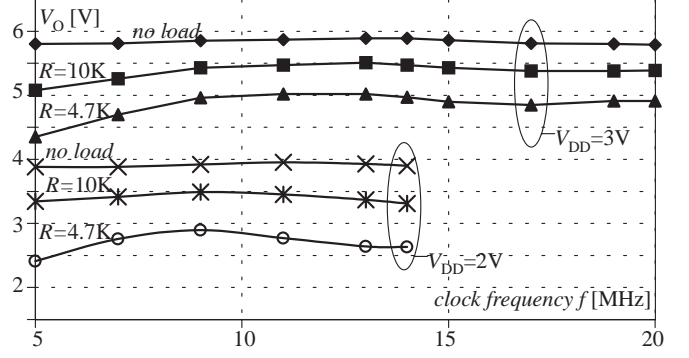

Figure 11: Output DC voltage V_O as a function of clock frequency f for various loads and input supply voltages.
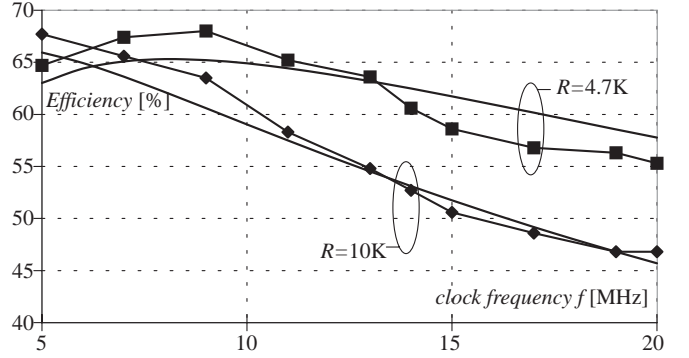

Figure 12: Measured (lines with points) and theoretical power efficiency of the voltage doubler of Fig. 8 as functions of clock frequency f for two different loads.

sizes were selected so that the voltage doubler can produce $V_O = 5$V output from $V_{DD} = 3$V input at the maximum output power of 5mW. The energy-transfer capacitors are 30pF each, the output filter capacitor is 60pF. The doubler occupies 0.7mm^2 of the chip area, not including i/o and supply/ground pads.

Experimental pump drive signals a_1, a_2, a_3, a_4 observed through four output pads are shown in Fig. 10 for $f = 10$MHz clock frequency.

The plot of output voltage as a function of frequency is shown in Fig. 11 for $V_{DD} = 2$V and $V_{DD} = 3$V for a frequency range of 5MHz to 20MHz at no load, $R = 10k\Omega$ and $R = 4.7k\Omega$ load. The fact that the no-load output voltage is slightly lower than the ideal $2V_{DD}$ indicates that the SC voltage doubler still has some undesirable discharge of the output filter capacitor through the PMOS switches.

The voltage doubler of Fig. 9 consists of four basic doublers connected in parallel. The low-frequency asymptote of the output resistance as a function of frequency is: $R_o(f) = \frac{1}{4Cf}$, while the high-frequency asymptote is: $R_{omin} = (R_{n1} + R_{n2} + R_{p1} + R_{p2})/2$, which depends on the on-resistance R_{n1} of the NMOS driver transistor M_1, R_{n2} of the NMOS pump transistor M_3, R_{p1} of the PMOS driver M_3, and R_{p2} of the PMOS switch M_7. For $V_{DD} = 3$V, and the selected device sizes, we have $R_{omin} = 196\Omega + 148\Omega + 279\Omega + 279\Omega = 450\Omega$. Each of the four energy-transfer, 30pF pump capacitors has $C_{BP} = 2.3$pF bottom-plate capacitance. If all other switching losses are neglected, the equivalent switching loss capacitance is $C_{sw} \approx 4C_{BP} = 9.2$pF. Experimental power-loss measurements at

no load for various V_{DD} and for a range of clock frequencies, indicate that the switching loss indeed follows the theoretical expression $P_{sw} = C_{sw}V_{DD}^2 f$, but the value of the equivalent switching-loss capacitance estimated from the measurement is $C_{sw} = 20$pF. Additional switching loss can be attributed to other nodal capacitances, losses in the waveform generator circuit, and parasitic discharge of the output through the PMOS switches.

Fig. 12 shows theoretical and measured power efficiency for $f = 10$MHz, $V_{DD} = 3$V, and two different loads, $R = 10k\Omega$ and $R = 4.7k\Omega$. For $R = 4.7k\Omega$, which is the maximum load the doubler was designed for, the efficiency peaks at about 68% for f around 10MHz. Good agreement between the theoretical and the measured results can be observed.

The voltage doubler can be operated as a closed-loop voltage regulator using a simple "bang-bang" feedback circuit shown in Fig. 13 [9]. The on-chip oscillator has a clock-enable input $\overline{CE}$. When $\overline{CE}$ is low, the oscillator is enabled and generates the clock signal for the voltage doubler. When $\overline{CE}$ is high, the oscillator is disabled and no clock signal is produced. A voltage comparator with hysteresis is used to generate the clock-enable signal. Closed-loop operation was tested for: $V_{DD} = 2$V, $V_{ref} = 3.3$V, and the hysteresis loop of ± 0.1V around the 3.3V reference, and for $V_{DD} = 3$V, $V_{ref} = 5$V, and ± 0.1V hysteresis loop around the 5V reference. Waveforms of Fig. 14 illustrate how the converter maintains the output voltage within the limits specified by the hysteresis loop when subject to a step change in load.
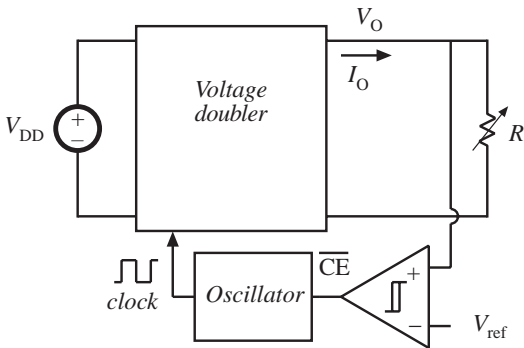
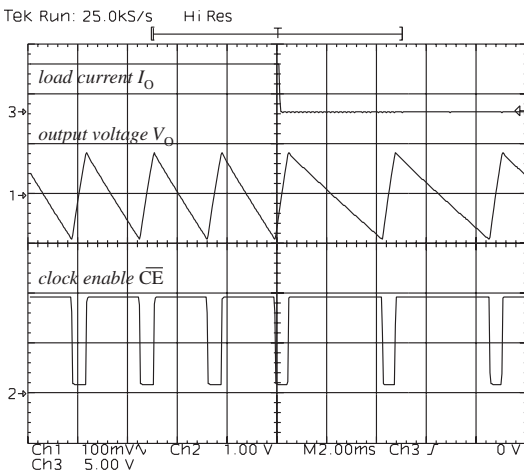Figure 13: Voltage doubler operated as a closed-loop voltage regulator.

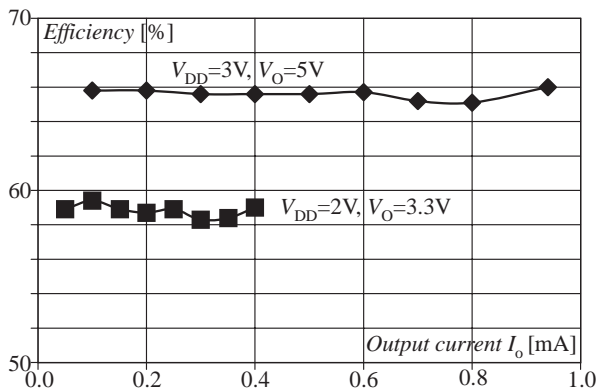Figure 14: Waveforms illustrating closed-loop operation of the voltage doubler.

Figure 15: Efficiency of the closed-loop doubler voltage regulator operating at $f = 10$MHz as a function of load current, for two different operating conditions: $V_{DD} = 2$V, $V_O = 3.3$V, and $V_{DD} = 3$V, $V_O = 5$V.

In addition to good output voltage regulation, another advantage of the closed-loop control scheme is that both switching and conduction losses scale with load. At no load, the oscillator is almost always turned off and no-load power losses are very small, 5μW for $V_{DD} = 3$V in our experimental circuit. Fig. 15 shows efficiency measured for fixed $f = 10$MHz frequency over a range of loads and the output

closed-loop regulated at 3.3V (with $V_{DD} = 2$V), and at 5V (with $V_{DD} = 3$V). It can be observed that almost constant efficiency is maintained for a wide range of loads.

4 Conclusions

The paper describes switched-capacitor dc-dc converters (charge pumps) suitable for on-chip, low-power applications. We focus on emerging energy-limited very low-power VLSI applications (such as battery-powered or self-powered signal processors) where high power conversion efficiency is important and where power levels are in the milliwatts range. In fully integrated realizations with on-chip capacitors, the design is not limited by the number of components or the circuit complexity. Also, compared to discrete-circuit designs, there is much more flexibility in sizing switches and capacitors. However, on-chip capacitors exhibit large parasitic (bottom-plate) capacitances that increase switching losses in the converter and ultimately limit the achievable power efficiency.

Converter configurations suitable for on-chip realization are described. The proposed configurations are based on connecting two (or more) identical but opposite-phase SC converters in parallel, thus eliminating the need for separate bootstrap gate drivers. Conduction and switching losses are considered to allow design optimization in terms of switching frequency and component sizes. Open-loop and closed-loop operation of an experimental, fully integrated, 10MHz voltage doubler is described. The doubler has 2V or 3V input and generates 3.3V or 5V output at up to 5mW load. The converter circuit fabricated in a standard 1.2μ CMOS technology takes 0.7mm^2 of the chip area.

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