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Switched Inductor Double Switch High Gain DC-DC Converter for Renewable Applications

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ABSTRACT High voltage gain DC-DC converter is a prime requirement for renewable applications, in particular for PV. Though numerous DC-DC converter is available for increasing the voltage gain, the passive elements requirement is higher which reduces the compactness, consequently, increases the cost of the system. To address this issue, a high gain DC-DC converter is reported recently. However, the number of passive elements is quite high which increases the size. To reduce the number of passive elements and maintain the same number of semiconductor devices, in this paper, a new switched inductor arrangement is proposed which is named as switched inductor double switch DC-DC converter (SL-DS-DC). Moreover, the proposed converter has a higher gain as compared to the recently reported converter. The proposed converter is analyzed in steady state and a comparative analysis is presented to prove the suitability. Finally, the proposed converter is validated experimentally.

INDEX TERMS High voltage gain, non isolated, DC-DC converter, switched inductor, CCM.

I. INTRODUCTION

Power generation using photovoltaic (PV) is an emerging technology that can provide a clean and sustainable solution. However, the voltage level is highly fluctuating and low [1]. In these applications, the DC-DC boost converter plays an integrating role to regulate the voltage level [2]. DC-DC converter's ability to operate in boost mode is dependent on the input inductor current. Based on the inductor current profile, the step-up DC-DC converter can operate in continuous current mode(CCM) and discontinuous current mode(DCM). The CCM is widely popular due to load independent voltage gain, lower current ripple, and better efficiency [3].

Several DC-DC converters can be used to step up the DC voltage. The classification of these converters is based upon the isolation property. Traditional boost, Sepic, Zeta [4] and Cuk [5] which can fulfill the demand of boosting the voltage level, however, fails to provide galvanic isolation and operates in larger duty cycle to achieve high gain [6]. Moreover, flyback, forward, push-pull, half-bridge and full-bridge converters are still popular and are employed for use at various voltage and power levels where galvanic isolation is required [7]–[9]. This structure makes the system complicated and bulky. Moreover, these topologies have a restricted range of boosting the voltage level along with higher voltage stress and therefore bigger in size. There are various voltage boosting techniques reported. Some of the popular techniques involved are multilevel topologies, interleaved topologies, cascaded topologies, voltage multiplier cells (VMC) topologies, combined with switched capacitors (SC) [10], [11] and/or switched inductors(SL) topologies [12], magnetically coupled topologies [13], [14]. Among them, in magnetically coupled topologies, root mean square(RMS) current of the switches, RMS current of the inductors and diode blocking voltages are increased [15]. Though the gain of the converter can be increased, they are prone to leakage inductance effect, therefore, producing voltage spikes and ringing which needs extra clamping to avoid switching spikes and to recover the leakage energy [16].

Nevertheless, various reported topologies can fulfill the demand for high voltage gain but most of them have wider duty cycle variation($0 < D < 1$). Therefore, there is a danger

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that converter may enter into inductor current saturation for duty cycle > 0.5 which dramatically deteriorates the performance of the converter. Recently, several DC-DC converters are proposed such as Z-source based [17]–[21], 3 Z network [22] and A high gain network [23], double switch based DC DC converter [24], switched capacitor based converter [25] etc. to reduce the duty cycle range. As the name suggests, 3-Z network DC-DC converter consists of 3-Z network connected in a series-parallel combination. To further improve the gain with the same number of the total component count, a high gain DC-DC converter is proposed. However, the efficiency is reduced in case of a high gain DC-DC converter. Similarly, a switched capacitor/switched inductor switched boost converter (SC/SL-SBC) is reported by Zhu et al [26] to improve the voltage gain. The SC/SL-SBC has similar gain to a high gain network [23] with reduced components count. Though the components are lower, the main drawback of the converter is lower efficiency.

In this paper, a new high gain DC-DC converter is proposed to address the aforementioned issues. The proposed converter utilizes a reduced number of components as compared to 3 Z network and a high gain network. Therefore, the compactness of the converter is increased with reduced order dynamics. Moreover, the proposed converter has better gain than the existing converters. The proposed converter is called as SL-DS-DC. The operating principle, steady-state analysis, design guidelines, and comparative analysis is presented in this paper for SL-DS-DC. At last, a SL-DS-DC is designed, developed and tested experimentally. The performance of developed hardware is reported for different operating conditions.

II. DESCRIPTION AND OPERATING MODES OF SL-DS-DC

The proposed converter (SL-DS-DC) is shown in Fig-1. The SL-DS-DC consists of two inductors, three capacitors, seven diodes, and two MOSFETs. The inductor is directly connected with the source all the time, therefore, the current drawn from the source will be continuous in nature. Both the inductors in the proposed converter are having same magnitude. This is particularly useful in reducing the current stress on the battery/source. The operation of the SL-DS-DC will be explained only in CCM due to better efficiency than DCM. The SL-DS-DC operates in two modes and the operating waveforms are shown in Fig-2. The blue lines in the Fig-3 and Fig-4 show the current flow path.

A. MODE 1

In mode 1, i.e. $(0 < t < t_1)$, both the switches S_1 and S_2 are turned ON. The diodes D_1, D_2 and D_0 are in forward condition due to polarity of inductors and voltage source, respectively. During this mode, the inductor L_1 and L_2 charges in parallel through S_2, C_2 and S_1, by sum of $V_g + V_{C1}$. Due to parallel operation of the inductors, the voltage across them is equal i.e. $V_{L1} = V_{L2}$. The load is also supplied by the sum of $V_g + V_{C1} + V_{C2}$ in this period. The steady state equations as per Fig-3 are as follows (Assumption: $L_1 = L_2 = L$)

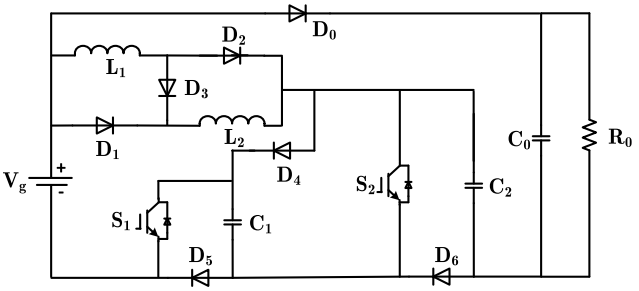


FIGURE 1. Proposed DC-DC converter(SL-DS-DC).

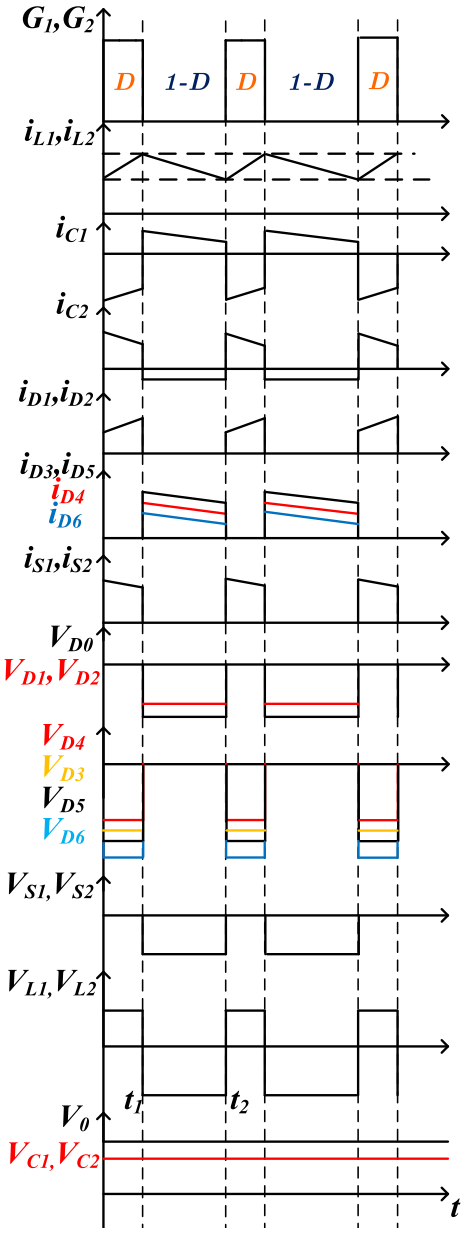


FIGURE 2. Operating waveform.

$$V_g - V_L + V_{C1} = 0 \tag{1}$$

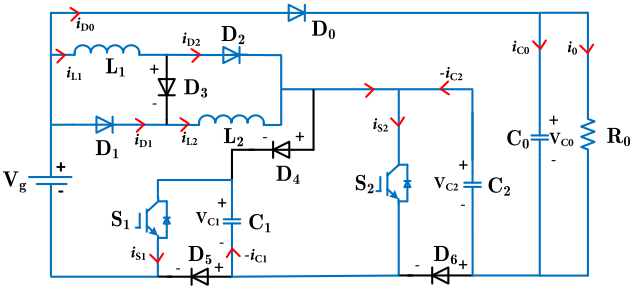


FIGURE 3. Operating mode 1.

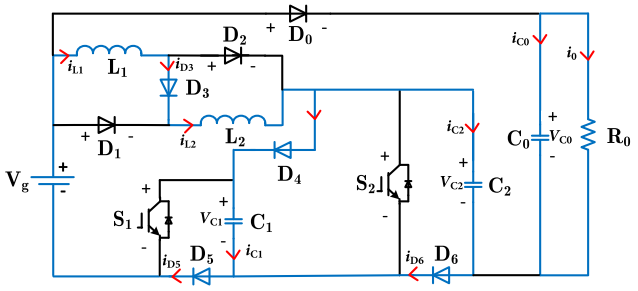


FIGURE 4. Operating mode 2.

$$-V_0 + V_{C2} + V_L = 0 \tag{2}$$

$$V_g - V_0 + V_{C2} + V_{C1} = 0 \tag{3}$$

and current equations related to this mode are

$$\begin{cases} i_{L1} + i_{L2} = i_{C1on} + i_{C2on} \\ i_{C2on} = -(i_{C0on} + i_0) \end{cases} \tag{4}$$

B. MODE 2

In mode 2, i.e. ($t_1 < t < t_2$), both the switches S_1 and S_2 are in OFF state. The diodes D_1, D_2 and D_0 becomes reverse biased. The diodes D_3, D_4, D_5 and D_6 are forward biased. Both the inductors come in series and dissipate their energy into the capacitor C_1 and C_2 equally. During this period, the load is supplied by the capacitor C_0. The steady state equations according to Fig-4 during this period are as follow

$$V_g - 2V_L - V_{C1} = 0 \tag{5}$$

$$V_{C1} = V_{C2} \tag{6}$$

The current equations in this mode are

$$\begin{cases} i_{L1} = i_{L2} = i_{inoff} \\ i_{L1} = i_{L2} = i_{C1off} + i_{C2off} \\ i_{C0off} = -i_0 \end{cases} \tag{7}$$

C. VOLTAGE GAIN DERIVATION

By taking average of voltage over a switching cycle across the inductor L,

$$\int_0^{DT_s} V_L dt + \int_{DT_s}^{T_s} V_L dt = 0 \tag{8}$$

Substituting the value of V_L from Equation-(58) and Equ-(5),

$$D\left(V_g + V_{C1}\right) + (1-D)\left(V_g - V_{C1}\right)/2 = 0 \tag{9}$$

Above equation results into the following

$$V_{C1} = \frac{1+D}{1-3D} V_g \tag{10}$$

As $V_{C1} = V_{C2}$, so

$$V_{C2} = \frac{1+D}{1-3D} V_g \tag{11}$$

Substituting the value V_{C1} and V_{C2} into Equation-(3), the output voltage is given by

$$V_0 = \frac{3-D}{1-3D} V_g \tag{12}$$

Therefore, the voltage gain for the SL-DS-DC is given as

$$G = \frac{3-D}{1-3D} \tag{13}$$

D. CURRENT STRESS CALCULATION

The current stress in the semiconductor devices occur only in On state or forward biased condition. In mode 1, the diodes D_0, D_1, D_2 are forward biased and switches S_1, S_2 are On. So, $i_{D0} = i_{C0on} + i_0$, $i_{D1} = i_{D2} = i_L$, $i_{S1} = i_{S2} = -i_{C1on}$. In mode 2, the diodes D_3, D_4, D_5, D_6 are forward biased. Hence, $i_{D3} = i_L$, $i_{D4} = i_{C1off}$, $i_{D5} = i_{in}$, $i_{D6} = i_{C2off}$.

Based on the above analysis, the diode average current is given as

$$\begin{cases} I_{D0A} = I_0 \\ I_{D1A} = I_{D2R} = DI_L \\ I_{D3A} = (1-D)I_L \\ I_{D4A} = (1-D)I_L - I_0 \\ I_{D5A} = (1-D)I_{in} \\ I_{D6A} = I_0 \end{cases} \tag{14}$$

and the rms value of the diode current is given as

$$\begin{cases} I_{D0R} = \dfrac{I_0}{\sqrt{D}} \\ I_{D1R} = I_{D2R} = I_L\sqrt{D} \\ I_{D3R} = I_L\sqrt{1-D} \\ I_{D4R} = \dfrac{(1-D)I_L - I_0}{\sqrt{1-D}} \\ I_{D5R} = I_{in}\sqrt{1-D} \\ I_{D6R} = \dfrac{I_0}{\sqrt{1-D}} \end{cases} \tag{15}$$

The peak value of the switches current is given as

$$I_{S1P} = I_{S2P} = \frac{(1-D)I_L - I_0}{D} \tag{16}$$

Based on the peak current, the rms value of current in the switches is given as

$$I_{S1R} = I_{S2R} = \frac{(1-D)I_L - I_0}{\sqrt{D}} \tag{17}$$

The rms value of the current in capacitors from equation-(4) and equation-(7) are given as

$$I_{C0R} = \sqrt{\frac{1}{D}} I_0$$
$$I_{C2R} = \sqrt{\frac{1}{D\,(1-D)}} I_0$$
$$I_{C3R} = \sqrt{\frac{1}{D\,(1-D)}} (I_L(1-D) - I_0) \quad (18)$$

III. DESIGN CONSIDERATION

The design of inductor and capacitors is based on the voltage across and current flowing through them, respectively. For that, it is necessary to calculate the average current in the inductors. The inductor current during charging period is given as

$$i_{in} = 2i_L - i_0 \quad (19)$$

while the inductor current during discharging period is given as

$$i_{in} = i_L \quad (20)$$

Based on the power balance theory, Equation-(19) and Equation-(20) can be combined as

$$DI_{in} + (1-D)I_{in} = D(2I_L - I_0) - (1-D)I_L \quad (21)$$

simplifying the above equation, the average inductor current in terms of input (I_{in}) and output current (I_0) is given as

$$(1+D)\,I_L = I_{in} - DI_0 \quad (22)$$

Substituting the value of I_{in} and I_0 in terms of voltage and resistance, average inductor current is written as

$$I_L = \frac{1}{1+D}\left(\frac{V_0^2}{V_g R_0} - \frac{DV_0}{R_0}\right) \quad (23)$$

A. INDUCTOR DESIGN

For inductor design, ripple current in the inductor is calculated first. From Equation-(58), the ripple current ΔI_L is written as

$$L\frac{\Delta I_L}{DT_s} = V_g + V_{C1} \quad (24)$$

Hence, the inductance is calculated as

$$L = \frac{V_g + V_{C1}}{\%r_i I_L} DT_s \quad (25)$$

where r_i is percent current ripple allowed.

To operate the converter in CCM, following equation must be valid:

$$I_L > \Delta I_L/2 \quad (26)$$

Solving the Equation-(23), Equation-(24) and Equation-(26), following inequality results

$$K > K_{crit} \quad (27)$$

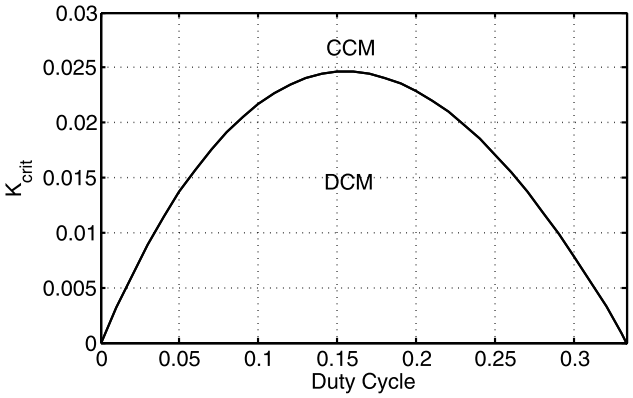


FIGURE 5. Boundary between CCM and DCM.

where $K = L/R_0T_s$ and $K_{crit} = D\left(1-D^2\right)(1-3D)\,/\,(3-D)\left(3-2D+3D^2\right)$.

To demarcate the boundary between CCM and DCM, K_{crit} iis plotted against the duty cycle as shown Fig-5. The area under the curve denotes the DCM region while outer region represents the CCM.

B. DERIVATION OF VOLTAGE GAIN IN DCM

To derive the voltage gain in DCM, applying the volt-sec principle across inductor L

$$\int_0^{DT_s} V_L dt + \int_0^{(1-D-D_x)T_s} V_L dt = 0 \quad (28)$$

where D_x is discharging duty cycle in DCM.

Substituting the values of V_L from ON and OFF state, above equation is modified as

$$D(V_g + V_{C1}) + D_x\frac{(V_g - V_{C1})}{2} = 0 \quad (29)$$

From above equation, D_x is written as

$$D_x = \frac{(V_g + V_{C1})}{(V_{C1} - V_g)} 2D \quad (30)$$

In DCM, the average inductor current is written as

$$I_L = \frac{1}{2T_S}\Delta I_L (D + D_x) T_S \quad (31)$$

substituting the value of ΔI_L, the average current is given as

$$I_L = \frac{V_i + V_{C1}}{2L}(D + D_x) DT_S \quad (32)$$

After substituting the value of I_L from Equation-(23), above equation is changed to

$$\frac{1}{1+D}\left(\frac{V_0^2}{V_g R_0} - \frac{DV_0}{R_0}\right) = \frac{(V_i + V_{C1})}{2L}(D + D_x) DT_S \quad (33)$$

Solving the above equation, following equation is achieved

$$G_d^2 - DG_d = \frac{(G_d + 1)(3G_d - 1)\lambda}{G_d - 3} \quad (34)$$

where $G_d = \frac{V_0}{V_g}$, $\lambda = \frac{D^2(1+D)}{4K}$

Therefore, the voltage gain polynomial in DCM is written as

$$G_d^3 - G_d^2(3 + D + 3\lambda) + G_d(3D - 2\lambda) + \lambda = 0 \quad (35)$$

where G_d is voltage gain in DCM.

C. CAPACITOR DESIGN

For capacitor design, the current flowing through the capacitor C_1 is $2I_L + I_0$ in DT_s, hence,

$$C_1 \frac{\Delta V_{C1}}{DT_s} = 2I_L + I_0 \quad (36)$$

which gives

$$C_1 = \frac{2I_L + I_0}{\%r_{v1} V_{C1}} DT_s \quad (37)$$

where r_{v1} is percent voltage ripple allowed in C_1.

Similarly, the current through capacitor C_2 is I_0 in DT_s. Hence

$$C_2 \frac{\Delta V_{C2}}{DT_s} = I_0 \quad (38)$$

$$C_2 = \frac{I_0}{\%r_{v2} V_{C2}} DT_s \quad (39)$$

where r_{v2} is percent voltage ripple allowed in C_2.

The capacitor C_0 is based on the load current which is being supplied by it during $(1 - D)T_s$. Hence,

$$C_0 \frac{\Delta V_{C0}}{(1 - D)\, T_s} = I_0 \quad (40)$$

which results in

$$C_0 = \frac{I_0}{\%r_{v0} V_{C0}} (1 - D)\, T_s \quad (41)$$

where r_{v0} is percent voltage ripple allowed in C_0.

IV. CALCULATION OF EFFICIENCY IN PROPOSED CONVERTER

The efficiency is dependent on the internal characteristics of all the elements and devices present in the converter. In the following sections, the power loss contributed by individual element/device is explained.

A. INDUCTOR LOSS

The inductor loss consists two losses: core loss and copper loss. The core loss of the inductor is calculated as

$$P_{core} = 71.93 B^{1.92} f_s^{1.47} Ve \quad (42)$$

where B is half of AC flux swing and V_e is core volume. The exponent term of B i.e. 1.92 and f_s i.e. 1.47 are empirically calculated values.

The copper loss for the inductor is largely dependent on the average current of the inductor. So, the power loss is given as

$$P_L = I_L^2 r_L \quad (43)$$

substituting the value of average inductor current, the power loss is

$$P_L = \left(\frac{1}{1 + D}\left(\frac{3 - D}{1 - 3D} - D\right)\right)^2 I_0^2 r_L \quad (44)$$

where r_L is internal resistance of the inductor.

B. CAPACITOR LOSS

The power loss in the capacitor is based on the RMS current flowing through it and effective series resistance of it. Based on the capacitors current in shoot through and non shoot through state, the RMS current flowing through the capacitors are given by equation-(18). The capacitors resistance for C_0 is r_{C0} while for C_1 and C_2 are equal to r_{C1}, the power loss in the capacitors is calculated as

$$P_C = I_{C0R}^2 r_{C0} + (I_{C1R}^2 + I_{C2R}^2) r_{C1} \quad (45)$$

after putting the values of capacitance current, the power loss in terms of duty cycle is given as

$$P_C = \frac{(I_L(1-D) - I_0)^2 + I_0^2}{D(1-D)} r_{C1} + \frac{I_0^2}{D} r_{C0} \quad (46)$$

C. DIODES LOSS

The diode loss is basically three types: loss due to forward voltage drop (V_F), conduction loss due to internal resistance (r_f) and reverse recovery loss due to trapped charge (Q_{rr}). However, loss due to trapped charge is negligible. The loss due to forward voltage drop is based on the average current and given as

$$P_{VF} = (I_{D0A} + I_{D1A} + I_{D2A} + I_{D3A} + I_{D4A} + I_{D5A} + I_{D6A}) V_F \quad (47)$$

substituting the values of average current, the power loss is given as

$$P_{VF} = \left[2I_L + I_0\left(1 + \frac{(1 - D)(3 - D)}{1 - 3D}\right)\right] V_f \quad (48)$$

The conduction loss is dependent on the RMS current of diodes. Therefore, power loss due to conduction is

$$P_{DCond} = (I_{D0R}^2 + I_{D1R}^2 + I_{D2R}^2 + I_{D3R}^2 + I_{D4R}^2 + I_{D5R}^2 + I_{D6R}^2) r_f \quad (49)$$

Therefore, the conduction loss in terms of duty cycle is

$$P_{DCond} = \frac{1}{D(1 - D) I_0^2} + (1 + D) I_L^2 + (1 - D) I_{in}^2 + \frac{((1 - D) I_L - I_0)^2}{1 - D} r_f \quad (50)$$

Therefore, total loss in diodes is

$$P_{Dtotal} = P_{DVF} + P_{DCond} \quad (51)$$

D. SWITCHES LOSS

The losses due to switches is divided into conduction and switching loss. The conduction loss for both the switches is given as

$$P_{Scond} = I_{S1R}^2 r_{S1} + I_{S2R}^2 r_{S2} \tag{52}$$

Above equation is written in terms of duty cycle as

$$P_{Scond} = 2\frac{((1-D)I_{L1} - I_0)^2}{D} I_0^2 r_S \tag{53}$$

The switching power loss is dependent on the switching frequency, turn on and turn off time, voltage across the switch and peak current. Therefore, the switching loss for the switches is

$$P_{Sswit} = \frac{t_{on} + t_{off}}{2} f_s V_{S1} I_{S1P} + \frac{t_{on} + t_{off}}{2} f_s V_{S2} I_{S2P} \tag{54}$$

where I_{S1P} and I_{S2P} are peak currents in S_1 and S_2, respectively. The switching loss in terms of duty cycle is

$$P_{Sswit} = \frac{t_{on} + t_{off}}{2} f_s \left[\frac{(1+D)}{(3+D)} \frac{((1-D)I_L - I_0)}{D}\right] 2V_0 I_0 \tag{55}$$

Total loss due to switches is

$$P_{Stotal} = P_{Scond} + P_{Sswit} \tag{56}$$

Therefore, the total power loss in the converter is given as

$$P_{loss} = P_L + P_C + P_{Dtotal} + P_{Stotal} \tag{57}$$

For calculating the efficiency, the parasitics used are $r_L = 0.15$, $r_{C0} = 0.12$, $r_{C1} = r_{C2} = 0.001$. Moreover, MOSFET on resistance-r_{dson} = 0.008 mΩ, Diode forward voltage V_f = 0.7 V, Diode on resistance r_f = 0.01 Ω, switching frequency=50 kHz, R = 200 Ω are used. Based on V_{in} = 25 V, D = 0.22 and 200 W output power, the power loss P_L, P_C, P_{Dtotal} and P_{Stotal} are equal to 13.32 W, 0.1125 W, 11.97 W and 1.43 W, respectively. Based on these details, the efficiency of proposed converter is equal to 88.6%. Furthermore at V_{in} = 40 V, D = 0.15 and 200 W output power, the power loss P_L, P_C, P_{Dtotal} and P_{Stotal} are equal to 6.16 W, 0.077 W, 8.34 W and 1.01 W, respectively. At this operating point, the efficiency is 93.2%.

V. COMPARATIVE ANALYSIS

To compare the proposed converter, SL-Boost, Z-source DC-DC, cascaded DC-DC, 3-Z network DC-DC, A high gain and SC/SL-SBC DC-DC converters are considered which is listed in Table-1. The boosting factor comparison is presented in Fig-6. It is evident that the SL-DS-DC has the highest gain at all the duty cycle. As far as the number of components is considered, Z-source and cascaded boost DC converter have the lower components count, but Z-source DC-DC has discontinuous input current and cascaded boost converter operates in larger duty cycle which may cause saturation problem in the inductor current or core. As compared to 3-Z network and a high gain network, the proposed converter has reduced number of passive elements and semiconductor devices.

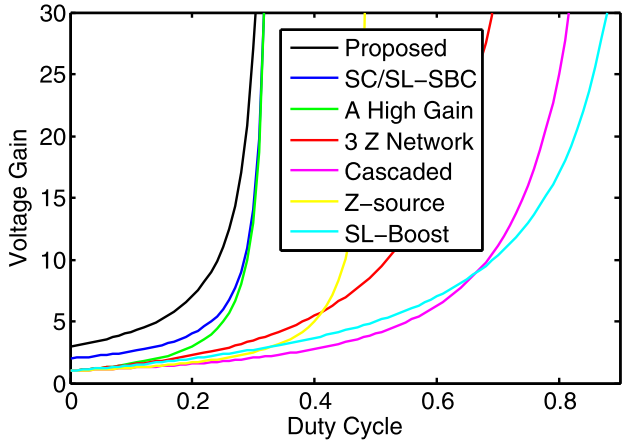


FIGURE 6. Voltage gain comparison.

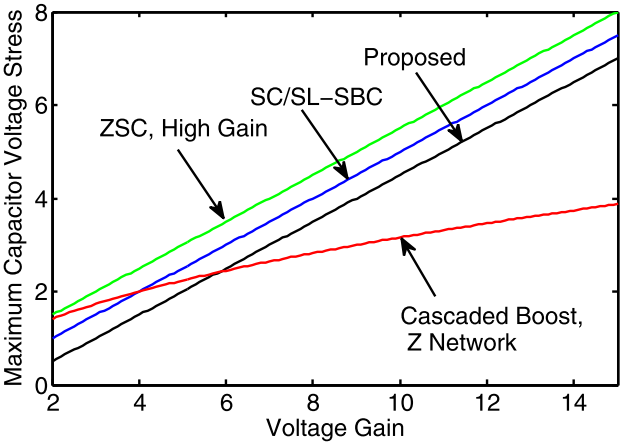


FIGURE 7. Capacitor stress comparison.

The maximum capacitor voltage stress in each converter is compared as shown in Fig-7. Unlike the 3 Z network and cascaded Boost converter, the proposed converter has higher stress. Nevertheless, the proposed converter has lower capacitor voltage stress as compared to ZSC, high gain network and SC/SL-SBC. The maximum switch voltage stress for each converter is also presented in Fig-8. The maximum switch voltage stress for the proposed converter is low as compared to ZSC, cascaded Boost, 3 Z network, SL-Boost, SC/SL-SBC and high gain converter. Furthermore, the output diode voltage stress is compared as shown in Fig-9. The diode voltage stress is lower in proposed topology except SC/SL-SBC. The efficiency of the proposed converter is comparable except cascaded Boost converter and SC/SL-SBC as shown in Fig-10. Though, the cascaded Boost converter has higher efficiency but higher gain can not be achieved due to parasitics. On the other hand, SC/SL-SBC has poor efficiency although it has similar components count as proposed converter. Theoretically, the power density of any converter is dependent on the number of semiconductor devices used and the volume of the passive elements. The volume of passive

TABLE 1. Comparison of proposed converter with existing converter.

	SL-Boost [12]	ZSC [17]	Cascaded Boost [27]	3 Z Network [22]	High Gain [23]	SC/SL-SBC [26]	SL-DS-DC
Gain	$\frac{1+3D}{1-D}$	$\frac{1}{1-2D}$	$\frac{1}{(1-D)^2}$	$\frac{(1+D)^2}{(1-D)^2}$	$\frac{1+D}{1-3D}$	$\frac{2-2D}{1-3D}$	$\frac{3-D}{1-3D}$
Inductor	4	2	2	4	4	2	2
Diodes	10	2	3	9	8	7	7
Capacitors	1	3	2	2	3	3	3
Switches	1	1	1	1	1	2	2
Boosting network Capacitor Voltage	NA	$V_C = \frac{V_0+V_g}{2}$	$V_C = \sqrt{V_o * V_g}$	$V_{C1} = \sqrt{V_o * V_g}$	$V_{C1} = -\frac{V_0-V_g}{2}$ $V_{C2} = \frac{V_0+V_g}{2}$	$\frac{V_0}{2}$	$V_{C1} = V_{C2} = \frac{V_0-V_g}{2}$
D_0 Voltage	V_0	V_0	V_0	V_0	V_0	$\frac{V_0}{2}$	$V_0 - V_g$
Switch Voltage	V_0	V_s=V_0	V_s=V_0	V_s=V_0	V_s=V_0	V_S=$\frac{V_0}{2}$	V_{S1}=V_{S2}=V_{C1}
Energy stored in inductor	8	60	20	7.2	27.18	48.7	10.5
Energy stored in capacitor	25	43	30	30	38	31.9	24

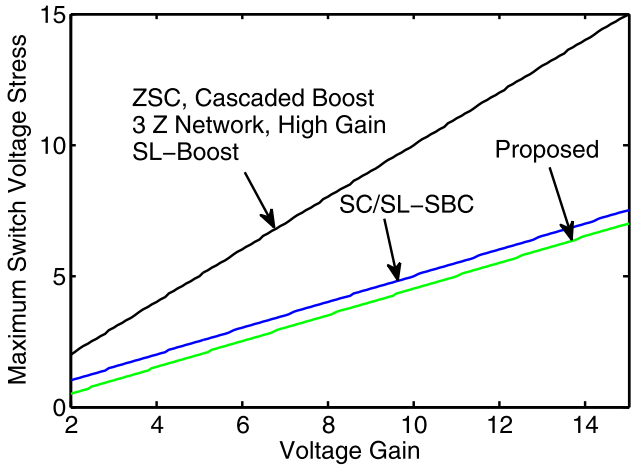


FIGURE 8. Switch stress comparison.

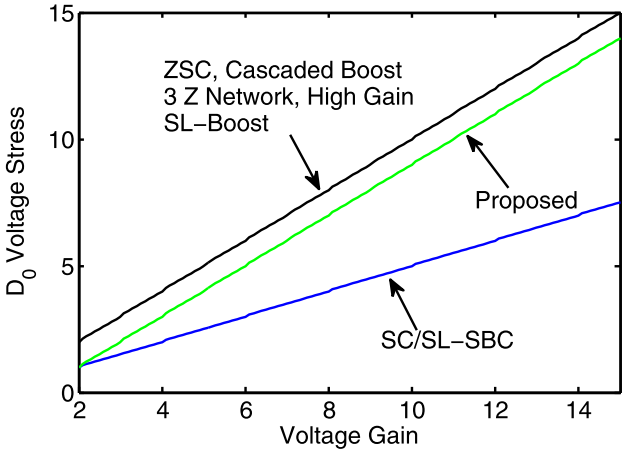


FIGURE 9. Diode stress comparison.

elements is proportional to the energy stored in them. Therefore, if the energy stored is calculated then the volume of the passive elements can be estimated. The total energy stored for the inductor is given as

$$E_L = \frac{1}{2} L I_{av}^2 \tag{58}$$

where I_{av} is average current through the inductor L. and the total energy stored for the capacitor is given as

$$E_C = \frac{1}{2} C V_C^2 \tag{59}$$

where V_C is voltage across capacitor C.

While calculating the energy stored in the inductor, it is assumed that the frequency and ripple current are the same for all the compared converters. Moreover, for energy stored in the capacitor is calculated for a similar value of capacitances. For voltage gain, $G = 5$, the total energy stored in the inductor and capacitor for all the topologies is listed in Table-1. It is evident that the total energy stored,i.e. volume required is lowest in the proposed converter (34.5) except for SL-Boost (33). The quantity mentioned in the table is made to be unitless. But SL-Boost has higher number of semiconductor devices and larger input current ripple as

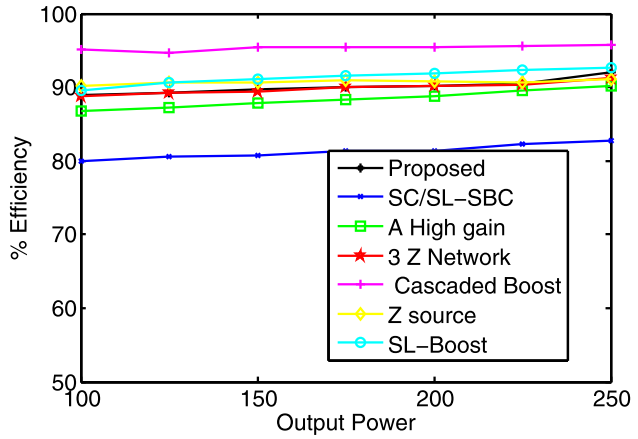


FIGURE 10. Efficiency comparison.

TABLE 2. Specification of converter.

Parameter	Rating
Switch	IRFP4668PbF-200 V, 130 A, 8 $m\Omega$
Diodes	STPS60SM200C-200 V, 2*30 A
Inductor	350 μH, EPCOS B64290L0632X830
Capacitor C_1, C_2	47 μF, 200 V, ECA2DHG470
Capacitor C_0	100 μF, 400 V, EEUEE2G101
Resistance	200 Ω
Input voltage	25-50 V
Frequency	50 kHz

compared to proposed converter. Based on these characteristics, the proposed converter has good potential.

VI. EXPERIMENTAL RESULTS

For validating the proposed converter, the converter is tested on the hardware platform as shown in Fig-11. The converter is evaluated for two distinct input voltage to prove its potential. For experimental analysis, a capacitor is connected to make the input voltage stiff. Following are the parameters those are common in both the cases $L_1 = L_2 = 350$ μH, $C_1 = 47$ μF, $C_2 = 47$ μF, $C_0 = 100$ μF, f_s =50 kHz. These are also listed in Table-2.

A. AT V_g= 40 V, R_0=200 Ω, D=0.15, P_0=200 W

In first operating condition, the parameters are: Input voltage $V_g = 40$ V, load resistance $R_0 = 200$ Ω, duty cycle $D = 0.15$. The profile of output voltage, the output current, input voltage, and the input current is shown in Fig-12a. The achieved output voltage is 200 V and the load current is 1 A which indicates that output power is 200 W.

At this rating, the inductor current and sum of inductors current are shown in Fig-12b. The inductor current i_L is continuous which shows that the converter is operating in CCM. The percent ripple in both the inductor is equal to 18%. The maximum amplitude of the sum of inductors current is 10 A which proves that it is in accordance with the analytical calculation.

The capacitors voltage C_1 and C_2 is also shown in Fig-12b. Both the voltage of the capacitor is equal and has an average

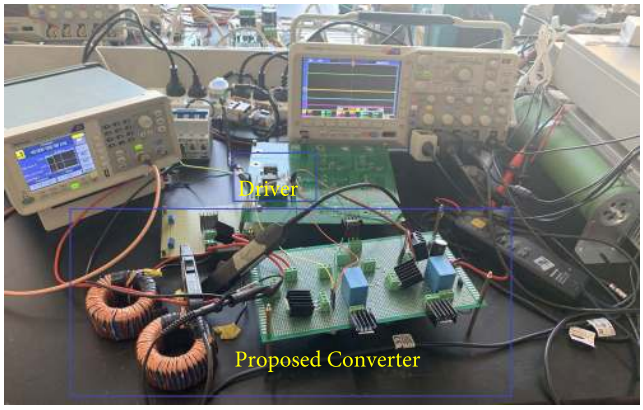
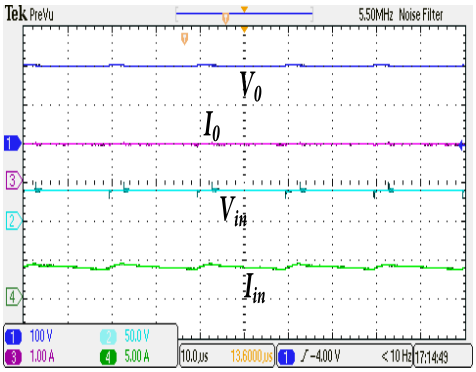
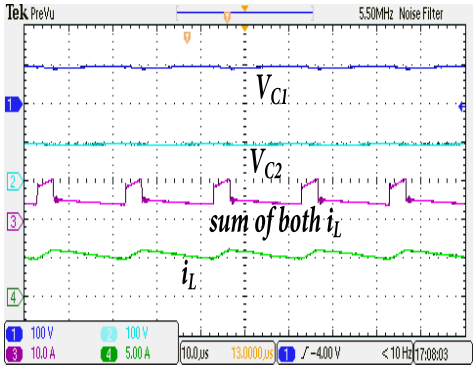


FIGURE 11. Experimental set up.



(a) Output and input voltage, current

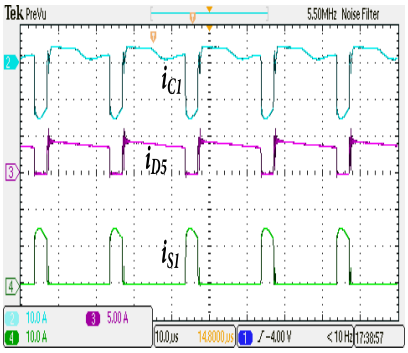


(b) Capacitors voltage, inductor currents

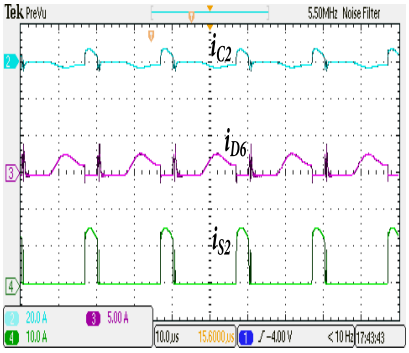
FIGURE 12. Voltage and current for d= 0.15 and V_{in}= 40.

value of 88 V which is in accordance as per the Equation-(10) and Equation-(11). The current for all the diodes, switches and capacitors is shown in Fig-13a, Fig-13b and Fig-13c. From the currents profile of capacitors, it is to note that the capacitors have large current during charging whereas small current during discharging. Moreover, the diodes and switches have currents in them only during on period as shown in Figures.

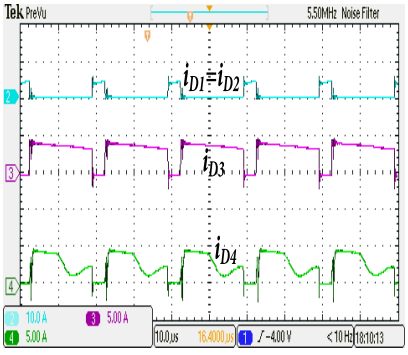
The diodes and switches voltage stress is shown in Fig-14a and Fig-14b. The diodes D_0, D_1 and D_2 are forward biased during charging while diodes D_3, D_4, D_5 and D_6 are forward biased during discharging. The diodes D_1 and D_2 voltage show ringing due to resonance of intrinsic inductance and



(a) Current in C_1, D_5, S_1



(b) Current in C_2, D_6, S_2



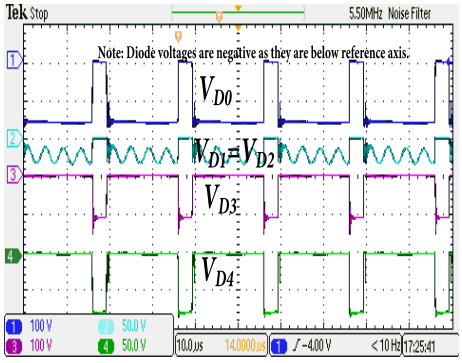
(c) Current in D_1, D_2, D_3, D_4

FIGURE 13. **Current stress for d= 0.15 and V_{in}= 40.**

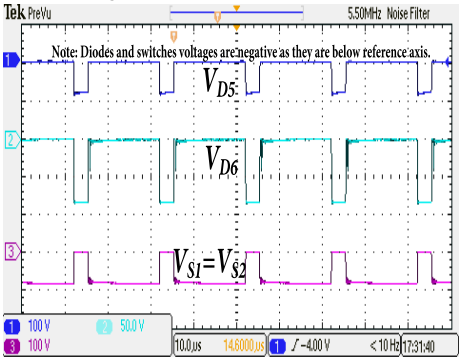
capacitance. The switches S_1 and S_2 are On during charging period.

B. AT V_g = 25 V, R_0 =200 Ω, D =0.24, P_0 =200 W

For second operating condition, following parameters are selected: input voltage-V_g = 25 V, load resistance R_0 = 200 Ω, duty cycle $D = 0.24$. At the output, 200 V is obtained due to which 1 A current flows through the load as shown in Fig-15a. Based on these values, the power output achieved is 200 W. The input current and input voltage are also shown in Fig-15a. The inductor current i_L is continuous, hence, the converter is still in CCM as shown in Fig-15b. The percent ripple in both the inductor is equal to 14%. The maximum amplitude of the sum of inductors current is 18 A which resembles the analytical calculation. The capacitor voltage C_1 and C_2 are similar and has equal magnitude i.e. 87 V as shown in Fig-15b. The current for all the diodes, switches

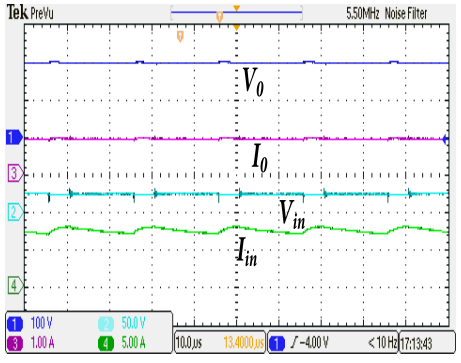


(a) Voltage across diode D_0, D_1, D_2, D_3, D_4

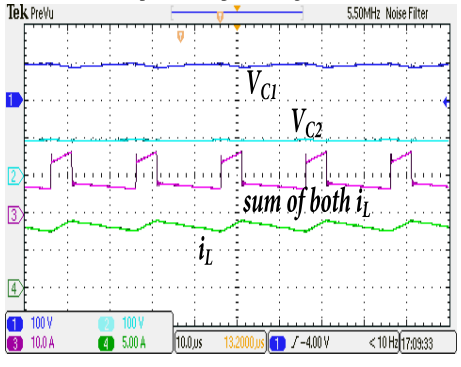


(b) Voltage across diode D_5, D_6, S_1, D_2

FIGURE 14. **Voltage stress for d = 0.15 and V_{in} = 40.**



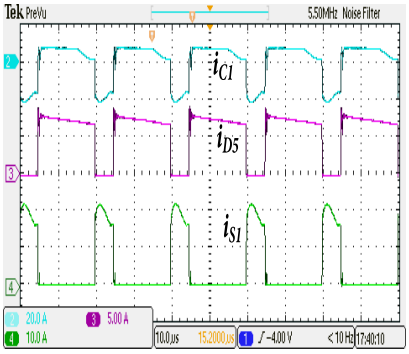
(a) Output and input voltage, current



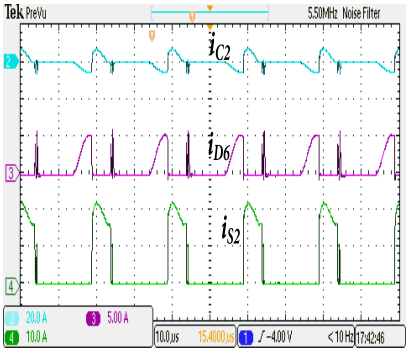
(b) Capacitors voltage, inductor currents

FIGURE 15. **Voltage and current for d = 0.24 and V_{in} = 25.**

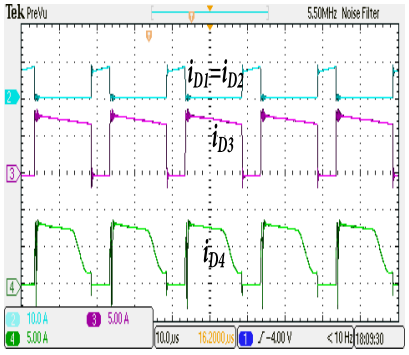
and capacitors is shown in Fig-16a, Fig-16b and Fig-16c. From the currents profile of capacitors, it is to note that the capacitors have large current during charging whereas small



(a) Current in C_1, D_5, S_1

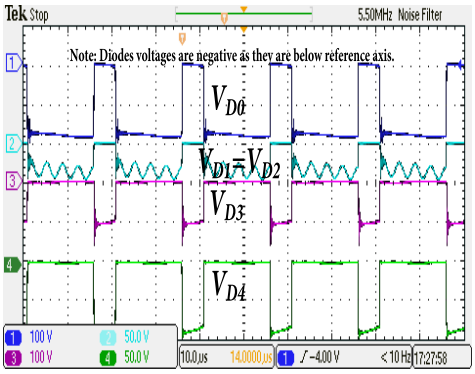


(b) Current in C_2, D_6, S_2

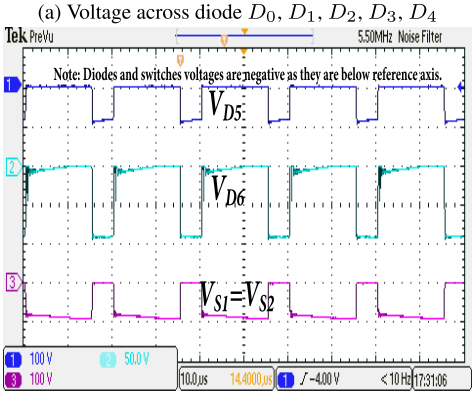


(c) Current in D_1, D_2, D_3, D_4

FIGURE 16. Current stress for $d = 0.24$ and $V_{in} = 25$.



(a) Voltage across diode D_0, D_1, D_2, D_3, D_4



(b) Voltage across diode D_5, D_6, S_1, D_2

FIGURE 17. Voltage stress for $d = 0.24$ and $V_{in} = 25$.

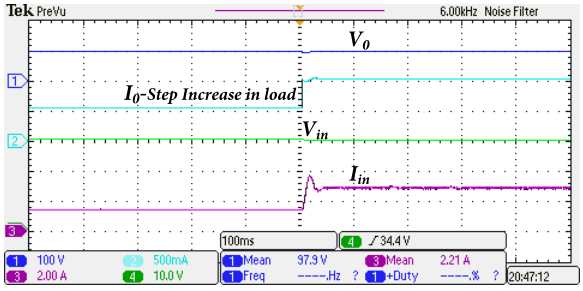


FIGURE 18. Response to step increase in load current.

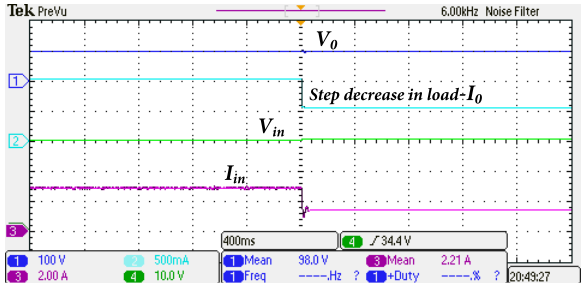


FIGURE 19. Response to step decrease in load current.

current during discharging. Moreover, the diodes and switches have currents in them only during on period as shown in Figures.

The diodes and switches voltage stress is shown in Fig-17a and Fig-17b. The diodes D_0, D_1 and D_2 are forward biased during charging while diodes D_3, D_4, D_5 and D_6 are forward biased during discharging. The switches S_1 and S_2 are On during charging period.

C. CLOSED LOOP PERFORMANCE

For closed loop control, a simple PI controller is implemented in the DSP-F28335. The parameters for the PI are $K_P = 0.0001$ and $K_I = 0.5$.

Primarily, the converter is tested for variation in load change. The response to the step increase in load is shown in Fig-18. The load current is increased from 0.5 A to 1 A. Contrary to this, a step decrease in load is also performed as shown in Fig-19. The load current is decreased from 1 A to 0.5 A. It is evident from both the figures the proposed converter is operating at constant output voltage and input voltage satisfactorily under load changes.

Secondly, the proposed converter is operated for the change in input voltage keeping the output power constant. The input voltage is increased/decreased by 5 V. It can be seen from the Fig-20 and Fig-21 that the output voltage and output current

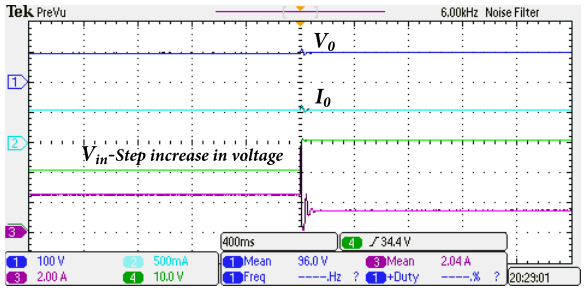


FIGURE 20. Response to step increase in input voltage.

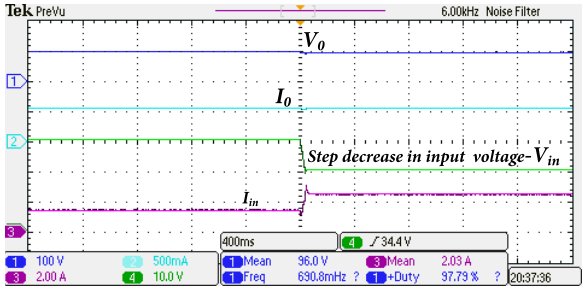


FIGURE 21. Response to step decrease in input voltage.

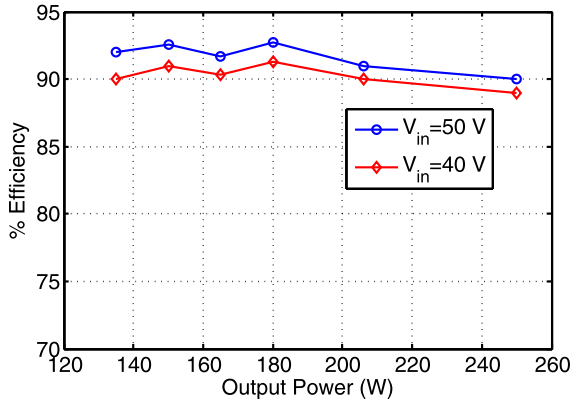


FIGURE 22. Efficiency of SL-DS-DC at two distinct input voltage.

is constant, therefore, output power is constant in both the cases. So the proposed converter is operating satisfactorily under the input change also.

D. EFFICIENCY

For performance evaluation in terms of efficiency, the converter is operated at different power rating for two fixed input voltage. At 50 V input voltage, maximum efficiency achieved is 93%. However, at 40 input voltage, the maximum efficiency is reduced to 91.2% as shown in Fig-22. At different power levels also, the efficiency in case of 40 V input voltage is lower as compared to 50 V input. This is due to the fact at lower input voltage, higher current is drawn to achieve the same power rating, hence, the conduction losses in the devices and intrinsic losses of inductor and capacitor are increased.

VII. CONCLUSION

In this paper, SL-DS-DC converter is proposed to achieve high voltage gain. The SL-DS-DC has better efficiency and lower energy stored. Moreover, the proposed converter has lower voltage stress as compared to various converter except few. The design guidelines along with comparative analysis are presented. The converter is tested for different power rating for efficiency analysis and maximum 93% efficiency is obtained. It is also observed that at lower input voltage, converter has lower efficiency as compared higher input voltage for similar power rating due to higher conduction losses.

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