Switched-Opamp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages

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Abstract—**The implementation of analog CMOS circuits that operate in the very low power supply voltage range (1 V to 2 V) becomes more important nowadays. Most accurate filter circuits are designed in the switched-capacitor technique. The existing design techniques require, however, the on-chip generation of a higher voltage by means of a voltage multiplier. In this paper, a novel technique, derived from the standard switched-capacitor technique, is presented. It is called switched-opamp because it is based on the replacement of the critical switches with opamps which are turned on and off. This technique results in a true, very low voltage operation without the need for voltage multipliers. As an example, a second order lowpass switched-capacitor filter is implemented in the switched-opamp technique. This filter operates with only a 1.5 V power supply. It is realized in a 2.4-μm CMOS process with $V_T = \pm 0.9$ V. It has a measured total harmonic distortion of -60 dB for a signal swing of 600 $\mathrm{mV_{ptp}}$ and a powerdrain of only 110 μW.**

I. Introduction

THE demand for circuits that can operate at very low power supply voltages (i.e., between 1 and 2 V) is very high. Most important are the battery-operated systems, but new submicron technologies also require the use of a decreased power supply voltage. When, at these very low power supply levels, an analog integrated circuit is needed, the choice is limited. For bipolar circuits there are some techniques available [1], but in CMOS the switched-capacitor technique is the only technique that can be used in practice to achieve good quality circuits. This paper deals with the design of a switched-capacitor filter for a very low power supply voltage in a standard CMOS process. A new technique for very low voltage switched-capacitor circuits, called switched-opamp, is introduced. The emphasis in this work is on the low operating voltages and the low power consumption that can be achieved in battery-operated systems with switched-opamp and on how this technique enables the use of switched-capacitors at very low voltages in technologies where this was impossible before.

The use of switched capacitor filters is very attractive because they achieve a high filter accuracy with a low distortion. Even at low power supply voltages, the quality of both parameters is fairly independent of the power supply. This is in contrast to e.g., g_m-C filters where the linearity of the OTA's is highly dependent on the available power supply voltage [2] and where the distortion increases rapidly when the power supply voltage is decreased to very low voltages. The distortion in switched-capacitor filters is mainly determined by the linearity of its capacitors when the amplification of the OTA is high enough. These capacitors are very linear and their linearity is not influenced by the power supply level. Consequently a THD of -70 dB is achievable down to a 2.5 V power supply for the full output swing of the OTA's, i.e., the output range in which they deliver a high amplification [3]. However, the performance reduces drastically at a very low power supply voltage, due to the reduction of the signal swing caused by the switches. Special techniques, different from the standard switched-capacitor design, have to be used to overcome this problem.

Until now switched-capacitor circuits at very low voltages could only be realized either in a special process with extra low V_T transistors or by using an on-chip voltage multiplier. In this paper, the switched-opamp technique is presented and its capabilities are demonstrated with a practical example. This technique can be used in a standard CMOS process and it has no need for voltages higher then the power supply. In the switched-opamp technique critical switches are eliminated and replaced by opamps which are switched on and off.

This paper deals in depth with the performance of switches at low and very low voltages. The existing techniques for switched-capacitors at very low voltages are discussed and their possibilities and disadvantages are pointed out. In the next part, the principles of the switched-opamp technique are fully discussed. The practical design of a switchable opamp is presented and finally, as an example of a switched-opamp circuit, the realization of a full switched-opamp filter is described. The realized filter is a lowpass biquad clocked at 115 kHz and it has a cut-off frequency of 1.5 kHz. The power supply voltage is 1.5 V. It is realized in a 2.4-μm n-well standard CMOS process with $V_T = \pm 0.9$ V. The filter shows a THD of -60 dB for a voltage swing of 600 $\mathrm{mV_{ptp}}$.

Manuscript received December 13, 1993; revised March 29, 1994.

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IEEE Log Number 9402466.

II. Switched-Capacitor At Very Low Voltages

A. Limitations

The following devices must be available for the realization of a switched-capacitor circuit: a capacitor, an OTA or an opamp and a switch. The operation of a poly-poly capacitor is always independent of the power supply level. Opamps and OTA's for switched-capacitors can be realized in a CMOS down to very low power supply voltages. Fig. 1 shows the most simple input and output stage for an amplifier. Normally

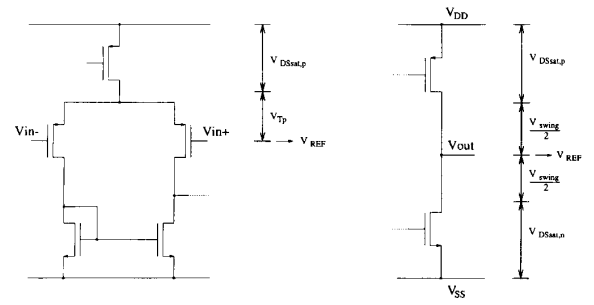

Fig. 1. Dc operating point requirements for the input and output stage of an OTA.

the input stage is the limiting factor for an OTA [2]. However, due to the virtual ground principle, used in switched-capacitor, no input swing is necessary and, as a result, a V_T is enough as V_{GS} for the input transistors when they are used in weak inversion. The minimum value for the reference level V_{REF} is therefore $V_T + V_{DSsat}$. Another boundary is set by the output stage. The output stage must be able to deliver an output signal V_{swing} centered around the reference level. The minimum power supply voltage is therefore $V_{REF} + \frac{V_{swing}}{2} + V_{DSsat}$. In (1), an approximate formula is given for an OTA with respectively an NMOS or PMOS input pair. In a low voltage design a V_{DSsat} will be between 0.1 and 0.15 V. The reference level is high enough to bias the input pair if $\frac{V_{swing}}{2} > V_T$. The minimal power supply voltage is then completely determined by the output voltage swing and rail-to-rail operation is possible. The minimal power supply is given in (2). The main problem in a very low voltage switched-capacitor are the switches. An NMOS transistor, for instance, needs at least a V_T on top of the highest possible signal that it has to switch. This is given in (3).

$$V_{DD,OTA,\min} \approx V_{DSsat,n} + V_{Tn} + \frac{V_{swing}}{2} + V_{DSsat,p} \quad \text{or } V_{DSsat,p} + |V_{Tp}| + \frac{V_{swing}}{2} + V_{DSsat,n} \quad (1)$$

$$V_{DD,OTA,r\text{-}to\text{-}r,\min} \approx V_{DSsat,n} + V_{swing} + V_{DSsat,p} \quad (2)$$

$$V_{DD,n\text{-}switch,\min} > V_{Tn} + V_{swing} + V_{DSsat,p} \quad (3)$$

A typical switched-capacitor switch consists of complementary driven NMOS and PMOS transistors of minimal size. The NMOS transistor conducts were the PMOS does not and vice versa and rail-to-rail operation is possible. (4) gives the conductivity of the transistors in function of the power supply voltage V_{DD} and the source voltage V_S which is equal to the signal that has to be switched. The conductivity of a minimum size complementary switch is given in Fig. 2 as a function of the voltage to switch. It is given for the 2.4 μm process in which the filter presented in this paper is realized. The power supply voltage is 5 V and the picture shows clearly that rail-to-rail operation is possible. In that case the maximal applicable swing is only limited by the output swing of the OTA given

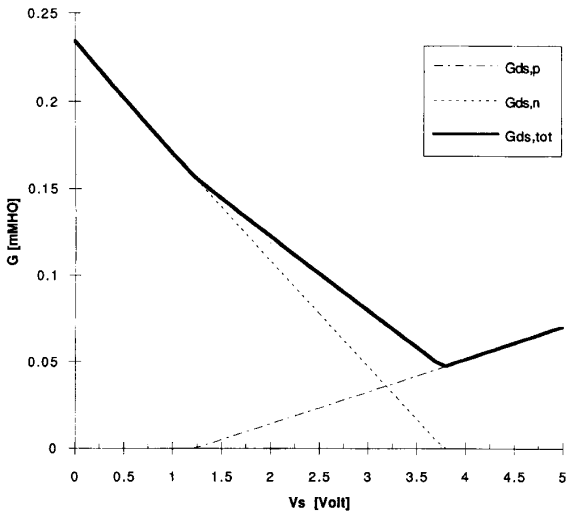

Fig. 2. Conductivity of a minimum size complementary switch for V_{DD} = 5 V.

by (2).

$$g_{DSn} = KP_n \frac{W}{L} \cdot \left[V_{DD} - V_S - V_{Tno} - \gamma_n\left(\sqrt{2\phi_f + V_S} - \sqrt{2\phi_f}\right)\right]$$
$$g_{DSp} = KP_p \frac{W}{L} \cdot \left[V_S - |V_{Tpo}| - \gamma_p\left(\sqrt{2\phi_f + V_{DD} - V_S} - \sqrt{2\phi_f}\right)\right]. \quad (4)$$

The maximal resistance of a switch must be high enough because it has, in combination with the switched capacitor, a big influence on the speed performance of the switched-capacitor circuit. A maximal resistivity of about 10 kΩ is accepted for most applications. Fig. 3 represents the maximal resistivity of a complementary switch as a function of the power supply voltage. The use of a switch which is not minimum size can compensate for the increased resistivity caused by a reduction of V_{DD}. First, the PMOS must be enlarged until both transistors have equal conductivity and from then on both transistors must be scaled up. Larger switches, however, give rise to a larger clock feedthrough, an often unwanted effect. This effect is unavoidable, but it is limited because the clock signal voltage has been lowered at the same time. When designing a low voltage switched-capacitor circuit, one must make a compromise between high speed and high clock feedthrough or low speed and low clock feedthrough, resulting in the use of big or small switch transistors, respectively. Making this tradeoff becomes harder and harder for lower power supplies because the resistivity increases faster than the power supply decreases. When the power supply reaches $V_{Tn} + |V_{Tp}|$, the resistivity becomes infinite and rail-to-rail operation is not possible anymore. The conclusion is that the standard switched-capacitor techniques can be used down to a power supply voltage which is equal to $V_{Tn} + |V_{Tp}| + 0.5$ V. For our technology this is 2.5 V. Hence,

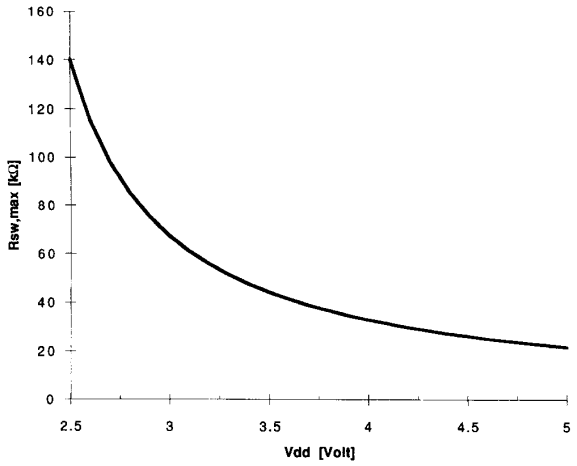

Fig. 3. Maximal resistivity of a complementary switch i.f.o. the power supply voltage V_{DD}.

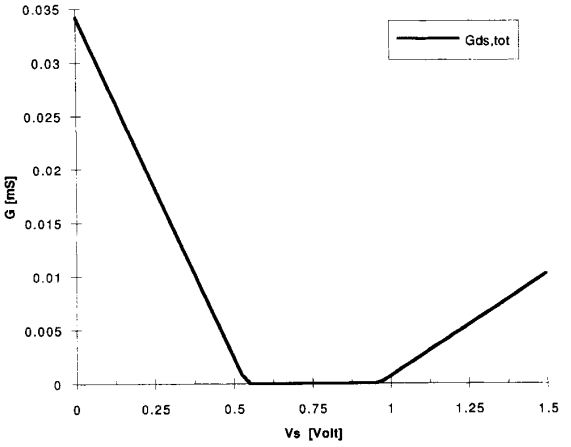

Fig. 4. Conductivity of a minimum size complementary switch for V_{DD} = 1.5 V.

as a rule of thumb, switched-capacitor circuits can be realized quite well in standard CMOS technologies down to a 3 V power supply. Lower voltages will require a special design to overcome the problems of the increased switch resistance.

The maximal resistance becomes infinite because there is no overlap region anymore where both transistors conduct. Consequently, either the NMOS or the PMOS must be used as switch and this can only be done in a limited signal range. Fig. 4 depicts this situation. It is the same as Fig. 2 but now V_{DD} = 1.5 V. The use of an NMOS device as single transistor switch is preferable because it has a better conductivity than a PMOS and in almost all processes V_{Tn} is lower than, or at least equal to, V_{Tp}. (5) is the necessary clock signal voltage of for NMOS switch. $V_{DSsat,n}$ is again, as in (2), the boundary set by the output swing of the OTA. $V_{DSsat,n} + V_{swing}$ is the maximal source voltage V_S that has to be switched with a conductivity larger than $g_{DSn,\min}$. A $\frac{W}{L}$ of 10 makes the term $\frac{g_{DSn,\min}}{\frac{W}{L} \cdot KP_n}$ equal to a V_{DSsat} for a conductivity of 50 μS. These are acceptable values for a single device NMOS switch used in a very low voltage application. A $\frac{W}{L}$ of 10 results in a clock feedthrough that is only 1.5 times higher than the clock feedthrough of a complementary switch driven at 5 V.

$$\begin{aligned} V_{DD,n\text{-}switch,\min} &= \frac{g_{DSn,\min}}{\frac{W}{L} \cdot KP_n} + V_{Tn} + V_{S,\max} \\ &= \frac{g_{DSn,\min}}{\frac{W}{L} \cdot KP_n} + V_{Tn} + V_{swing} + V_{DSsat,n} \\ &\approx V_{DSsat} + V_{Tn} + V_{swing} + V_{DSsat,n}. \end{aligned} \tag{5}$$

A comparison between (1) and (2) shows that it is possible to achieve rail-to-rail operation with a CMOS OTA if V_{Tn} or $|V_{Tp}| < \frac{V_{swing}}{2}$. (5) shows that a single device NMOS switch does not allow rail-to-rail operation. An extra voltage drop, equal to V_{Tn}, is always needed. An NMOS transistor is the only switch that is suited for very low voltage applications. These circuits can therefore only be realized with a reduced swing. The swing that can be applied at very low voltages is, however, far too small for any useful application.

B. Existing techniques

There are two known techniques that solve this problem. One is enlarging V_{swing} by using a dedicated process which has a special low V_T NMOS. In [4] an extra NMOS with V_T = 0.2 V is used. With this switch a voltage swing of 1 V is obtained for V_{DD} = 1.4 V. The low V_T gives rise to high unwanted leakage currents, resulting in a deformation of the transfer characteristics. This is not an unacceptable problem. It is the high cost of a dedicated process which makes this technique used only in occasional cases.

The only other available technique is the on-chip generation of a voltage higher than the power supply by means of a voltage multiplier [5]. This is, of course, an obvious solution but it can be seen from the previous paragraph that it is not necessary to let the complete switched-capacitor circuit run on this higher voltage. Only the switches have to be driven on a higher voltage. This greatly simplifies the design of the voltage multiplier and makes its size acceptable. In [6] and [7], this technique is used. The voltage multiplier needed for these circuits is derived from the EEPROM technology [8], [9]. In these circuits, the switches are always single device NMOS switches. Using complementary switches would be pointless because the overlap region would be situated outside the power supply range. The disadvantage of this technique is primerally its need for a voltage multiplier, a power and area consuming circuit. Furthermore, the use of higher voltages is not allowed anymore in advanced submicron CMOS technologies and in the future, all circuits will have to be true low or very low voltage designs.

III. The Switched-Opamp Technique

The basic idea of the switched-opamp technique is that (5) does not hold for all switches in a switched-capacitor circuit. Most switches do not require more power supply than an OTA

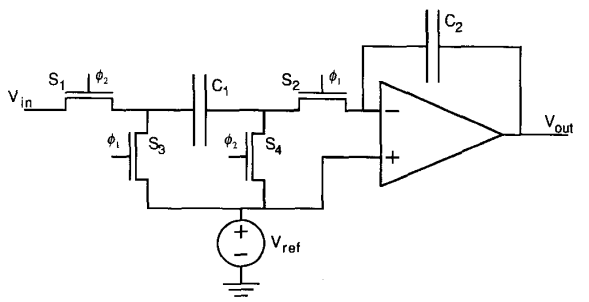

Fig. 5. A switched capacitor inverting integrator with NMOS switches.

or opamp does. Those switches which do require more can be replaced by switchable opamps.

Fig. 5 gives the topology of a switched-capacitor inverting integrator, the basic building block for switched-capacitor filters. Switches S_2, S_3, and S_4 are on one side connected to either the reference voltage V_{REF} or a node on virtual ground, which is also kept on V_{REF} by the feedback system. The maximal source voltage V_S is not $V_{DSsat,n} + V_{swing}$ for these switches but V_{REF}, equal to $V_{DSsat,n} + \frac{V_{swing}}{2}$, resulting in (only for S_2, S_3, and S_4) (6).

$$V_{DD,S_{2,3,4},\min} \approx V_{DSsat} + V_{Tn} + \frac{V_{swing}}{2} + V_{DSsat,n} \quad (6)$$

$$V_{DD,S_1,\min} \approx V_{DSsat} + V_{Tn} + V_{swing} + V_{DSsat,n}. \quad (7)$$

The only switch that has to be able to switch the total signal swing is the input switch S_1. It is connected to the output of the OTA of the previous stage. The minimum power supply for this switch is given by (7). Just eliminating this switch is not possible. Switch S_3 would then short the output of the preceding OTA during clock phase ϕ_2. This can, however, be solved by disabling the driving force of the OTA during ϕ_2. This is only possible if the OTA has to drive and integrate in the same phase. It is obvious that integrating is not possible when the OTA is turned off. As a result, a noninverting delay element has to be inserted everywhere where this problem occurs, resulting in an overhead of about 1.5 times more opamps. The power consumption decreases, however, to 0.75 of its original value because the opamps are switched off for 50% of the time. In Fig. 6, the topologies for a switched-capacitor and a switched-opamp low-Q lowpass biquad are presented. An extra non-inverting delay of half the clock period, realized with amplifier A_2, has to be added to the switched-opamp version.

(8) gives the voltage swing that is achievable with switched-opamps in function of the power supply and the V_T's. The bulk effect must be included in V_{Tn}. From this relation it is clear that a swing of $V_{DD} - 2 \cdot V_{DSsat}$ can be achieved when rail-to-rail operation is possible. As a result, an NMOS input pair is used.

$$\begin{cases} \text{if } V_{DD} > 2 \cdot \max(V_{Tn}, |V_{Tp}|) \text{ then} \\ \quad V_{swing} = V_{DD} - 2 \cdot V_{DSsat} \\ \text{if } V_{DD} < 2 \cdot \max(V_{Tn}, |V_{Tp}|) \text{ then} \\ \quad V_{swing} = V_{DD} - 2 \cdot V_{DSsat} \\ \qquad -[2 \cdot \max(V_{Tn}, |V_{Tp}|) - V_{DD}]. \end{cases} \quad (8)$$

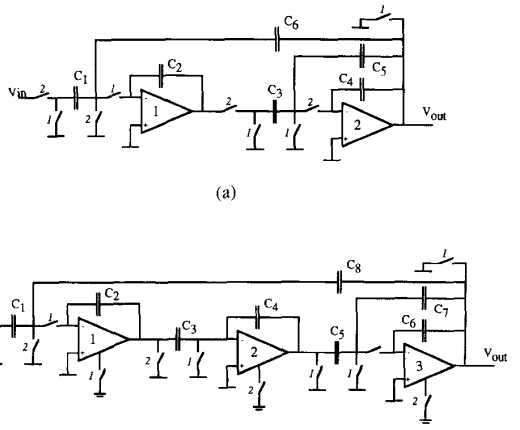

Fig. 6. Topology of a lowpass low-Q biquad: (a) switched-capacitor, (b) switched-opamp.

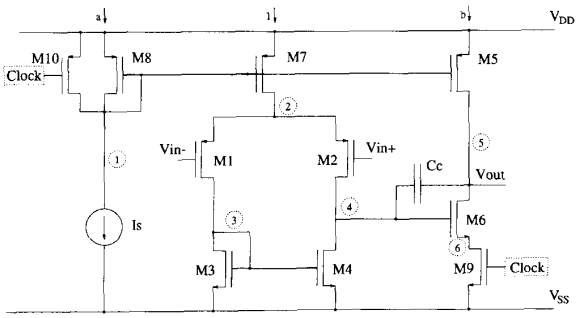

Fig. 7. Topology of the complete switchable opamp.

The switched-opamp technique can be used for all switched-capacitor circuits in which all switches either switch the output voltage of an OTA or else are connected to the reference voltage, directly or virtually. This means that almost all switched-capacitor circuits can be converted to an equivalent switched-opamp circuit.

IV. Design Of A Switchable Opamp

An OTA or opamp can be switched with its bias currents. In Fig. 7, the circuit of a switchable Miller-opamp is given. This opamp is used in our example. The Miller-compensated opamp structure is preferred in this very low voltage application over the one-stage folded cascode OTA structure, which is often used in standard switched-capacitor circuits [10]. The two-stage Miller structure gives a high amplification with only two transistors in the output stage which delivers the maximal possible signal swing.

The switch transistor M_{10} can short-circuit the current mirror M_8,M_5,M_7. This PMOS switch operates with any power supply voltage larger than $|V_{Tp}| + V_{DSsat}$ because its source is connected to the power supply. A high clock signal makes the conductivity of M_{10} equal to 0 and the current

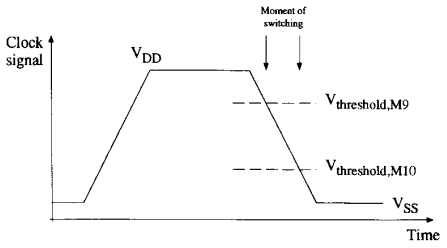

Fig. 8. Effect of a slow clock decay on the moment of switching.

mirror will act as if M_{10} is not present. A low clock signal makes the conductivity high. $V_{DS,M_{10}}$ is then about 10–20 mV and no current flows through M_5, M_7, and M_8 anymore. The opamp is switched off.

For a high switching speed however, M_8 must be relatively large because it has to charge the capacitance $C_{GS,tot}$ when the opamp is turned on. (9) gives the time constant for the total capacitance of the current mirror combined with the conductivity of M_8 working as a diode, assuming a fixed size for M_5 and M_7. This equation shows that M_8 is best about as big as the total size of the transistors which it is driving ($a = 1 + b$). The size of M_{10} is determined by its resistivity when it is turned on. This must be a fraction of the resistivity of M_8. Due to the higher gate source voltage V_{GS} which is applied to M_{10}, this is fulfilled when M_{10} is equal to M_8.

$$\tau_{\text{current mirror}} = \frac{C_{GS,tot}}{g_{m,M8}} = \frac{a \cdot C_{GSo} + C_{GSo} + b \cdot C_{GSo}}{a \cdot g_{mo}} = \left(1 + \frac{1+b}{a}\right) \cdot \frac{C_{GSo}}{g_{mo}}. \quad (9)$$

Although it is possible to turn off the opamp by turning off its supply currents, this is not enough. Special care has to be given to the output impedance and the compensation capacitors. The output impedance of the opamp has to be high in the off state. Compensation capacitors may not be charged or discharged during switching because their time constant is very high and consequently the maximal switching speed would then be very low. M_6 is the amplifying transistor in the Miller compensated output stage. The dc current flowing through this transistor is not changed when the current source M_5 is turned off and the capacitors C_C and C_L will be discharged during the off period. This unacceptable behavior can be avoided if the current pad through M_6 is interrupted as well. This is the function of M_9, a small switchable resistor. The size of M_9 is defined by two specifications. First of all, the voltage over M_9 must be small in the on state because the swing is directly decreased with twice this value. 20 mV is about the maximal voltage that can be accepted. Secondly, this resistor may not degrade the amplification of the output stage significantly. Herefore $g_{DS,M9}$ must be a lot higher than $g_{m,M6}$.

Not only the switches M_9 and M_{10} must be fast enough to avoid an uncontrollable loss of charge. The clock signal itself must also be fast enough. The moment when M_5 is switched off must be synchronized with the switch-off moment of M_6, otherwise the feedback path over the opamp is interrupted while M_6 is still drawing current from the load capacitors, resulting in nodes that begin to float. M_9 and M_{10} must therefore switch at the same time. They have, however, a different threshold level. The threshold level of M_9 is V_{Tno}; the threshold level of M_{10} is $V_{DD} - |V_{Tpo}|$. Fig. 8 shows that this means that M_6 is turned off faster than M_5 when the slope of the clock signal is too slow. Depending on the power supply voltage and the gap between the threshold voltages, a transition time between 1–10 ns is needed, a value easy to achieve on-chip.

TABLE I
MOST IMPORTANT PARAMETERS OF THE 2.4 μm CMOS PROCESS

	nMOS	pMOS
V_{To}	0.9	-0.9 V
KP	57 μA/V^2	17 μA/V^2
γ	0.3 $\sqrt{V}$	0.5 $\sqrt{V}$

TABLE II
TRANSISTOR SIZES

	W/L		W/L
S_n	10	M_6	86
M_1	10	M_7	6.6
M_2	10	M_8	290
M_3	1	M_9	20
M_4	1	M_{10}	290
M_5	290		

V. REALIZATION OF A SWITCHED-OPAMP FILTER

The second order low-Q lowpass biquad from Fig. 6 has been implemented, as an example, with a bandwidth of 1.5 kHz and a clock frequency of 115 kHz. The clock frequency value is imposed by the application and no special design effort towards a high clock speed has been made. It is implemented in a 2.4-μm CMOS process. The most important parameters are given in Table I. The relatively high V_T's make this process not ideally suited for low voltage application, but in this way it is shown that very low voltage switched-capacitor design is possible with all standard CMOS processes. The chip is designed for a power supply voltage V_{DD} of only 1.5 V. According to (8), rail-to-rail operation is not possible and the reference level V_{REF} has to be chosen below $V_{DD}/2$. The reference level is set by the maximal resistivity of the single device NMOS switch which has been chosen to be 20 kΩ. The switches have as a result a W/L of 10. With (6) the reference level is found as 0.425 V. The opamp can only handle this value when its input transistors are used in weak inversion. The voltage swing, set by the lower output boundary of the opamp, is 0.55 V_{ptp}.

The transistor sizes for the opamp are determined by speed and stability requirements. The output of the opamp has to reach its final value with a fault smaller than 0.1% without overshooting within half a clock period. This must, of course, be achieved for the highest possible signal change. From these specifications, the required GBW is derived. With the Miller structure, slewing of the opamp is unavoidable [11]. The opamp is allowed to slew for 1/3 of the time and the GBW, related to the settling time, therefore has to be 1 MHz. The

TABLE III
OPAMP PERFORMANCE FROM SIMULATION

Parameter	Value
GBW	1.3 MHz
Phasemargin	60°
Open loop gain	90 dB
Slew rate ↑	0.40 V/μs
Slew rate ↓	0.52 V/μs
Output voltage range	0.15 V–1.35 V
Input voltage range	0 V–0.6 V

TABLE IV
CAPACITOR VALUES FOR THE BIQUAD

Capacitor	Value
C_1	4.74 pF
C_2	12.69 pF
C_3	1.5 pF
C_4	1.5 pF
C_5	1.5 pF
C_6	12.69 pF
C_7	3.05 pF
C_8	1.5 pF

load capacitor C_L is taken equivalent to 10 pF, the maximal value on any output node. Table II gives the transistor sizes, Table III, the simulated opamp specifications. The capacitor values are given in Table IV.

Special attention has to be given to the switch resistor at the input of the circuit. It cannot be replaced with a switchable opamp because it is not preceded by one. Two input structures were implemented. The first one still uses a switch clocked at a higher voltage. This is shown in Fig. 6. It was used during the testing of the rest of the circuit. Fig. 9 shows a true, very low voltage solution. The input switch and capacitor are replaced by a large external resistor, making the input current driven. In this design, the input resistor is 1 MΩ. The circuit now starts with an active RC part which is not tuned. This has, however, no influence on the frequency response of filters. Only the overall amplification depends on the absolute value of the RC time constant. This replacement of a simulated resistor by a real resistor is not possible when there is a capacitor or the combination of a capacitor and a resistor required at the input. In these cases the input structure with the resistor can still be used if an extra noninverting amplifier is added at the input.

VI. EXPERIMENTAL RESULTS

Fig. 10 is a microphotograph of the realized circuit. The total chip area is 2.1 mm^2. It contains 3 opamps, switches, capacitor banks, and an output buffer. The area per pole is 0.57 mm^2. The measured filter transfertfunction is given in Fig. 11. The simulated bandwidth is 1534 Hz; the measured bandwidth is 1541 Hz. This indicates that the transfertfunction has a very high accuracy, a property that can be expected from a switched-capacitor filter.

According to (6), the swing is 0.55 V_{ptp}. Fig. 12 is a plot of the total harmonic distortion (THD) in function of the applied signal swing. The THD is -64 dB for the predicted

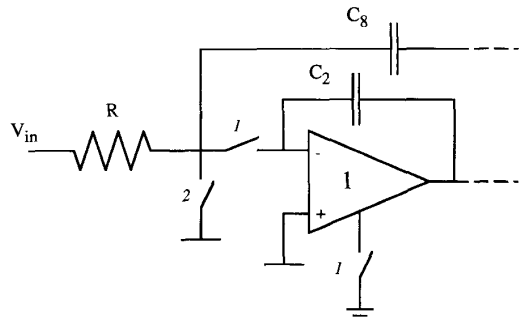

Fig. 9. Switched-opamp input structure with a resistor.

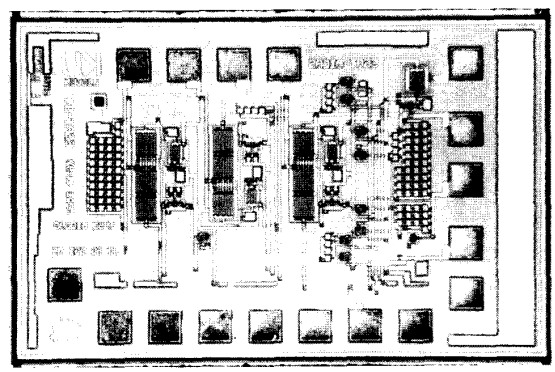

Fig. 10. Microphotograph of the lowpass biquad.

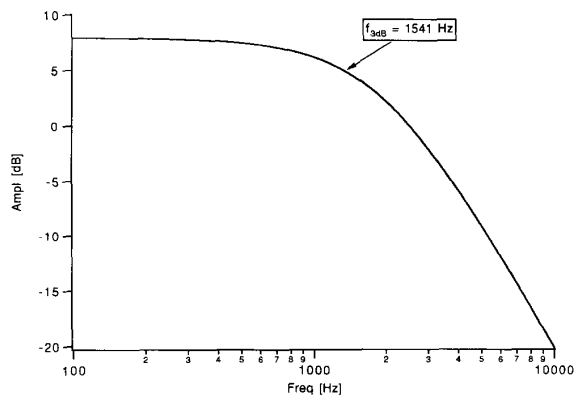

Fig. 11. Measured transfertfunction.

signal swing. Up to 0.6 V_{ptp}, the THD is less then -60 dB. Fig. 13 displays the THD versus the clock speed. The distortion increases rapidly for clock frequencies higher than 115 kHz. This speed limitation is imposed by the high on-resistance of the switches together with the low GBW of the OTA's. Their values were chosen in accordance with the design specification for the clock frequency.

The measured equivalent input noise is 140 μV_{rms}. This gives a dynamic range of 69 dB. The power consumption is

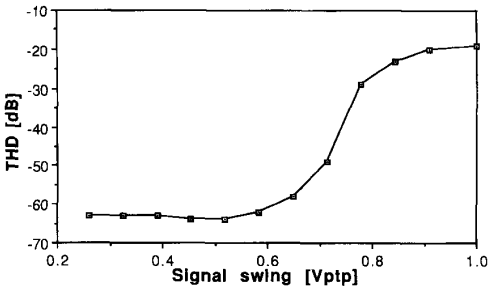

Fig. 12. THD i.f.o. the applied signal swing.

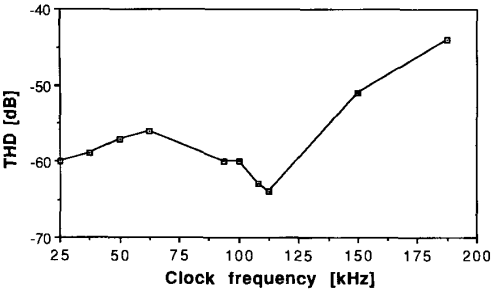

Fig. 13. THD i.f.o. the clock speed.

only 35 μA per pole. The filter operates down to a voltage supply of only 1.3 V.

VII. Conclusions

In this paper a new technique, called switched-opamp, has been presented. This technique is used for the realization in CMOS of switched-capacitor circuits which operate at very low power supply voltages (1–2 V).

The behavior of OTA's and switches at very low voltages has been fully analyzed in this paper. From this analysis it becomes clear that the OTA's and most of the switches in a switched-capacitor circuit can be used without any problem in very low voltage applications. With the introduction of the switched-opamp technique it is shown how the few switches which are unable to operate at very low voltages can be eliminated and replaced by switchable opamps. In this way it becomes possible to realize true, very low voltage switched-capacitor circuits in a standard CMOS process without the use of a voltage multiplier. This was not possible before.

A second order lowpass biquad has been implemented in the switched-opamp technique. Herefore a switchable opamp has been designed. The filter has a bandwidth of 1.5 kHz; it is clocked at 115 kHz. The filter operates at a power supply voltage of only 1.5 V. The filter has a total harmonic distortion of only -64 dB for the designed output swing of 550 mV_{ptp}.

Acknowledgment

The authors wish to thank S. Gogaert and S. Gierkink for their contribution to the realization of the chip.

References

[1] H. Tanimoto *et al.*, "Realization of a 1 V active filter using a linearization technique employing a plurality of emitter coupled pairs," *IEEE J. Solid-State Circuits*, vol. 26, pp.937-945, July 1991

[2] M. Steyaert, J. Crols, S. Gogaert, and W. Sansen, "Low-voltage analog CMOS filter design," in *Proc. ISCAS*, May 1993, pp.1447–1450.

[3] R. Gregorian, K.W. Martin, and G.C. Temes, "Switched capacitor circuit design," in *Proc. IEEE*, Aug. 1983, vol. 71, pp. 941–966.

[4] T. Adachi, A. Ishinawa, A. Barlow, and K. Takasuka, "A 1.4 V switched capacitor filter," in *Proc. CICC*, May 1990, pp. 8.2.1–8.2.4.

[5] F. Calias, F.H. Salchi, and D. Girard, "A set of four IC's in CMOS technology for a programmable hearing aid," *IEEE J. Solid-State Circuits*, vol. 20, no. 2, pp. 301–312, April 1989.

[6] R. Castello and L. Tomasini, "1.5-V High-performance SC filters in BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 26, no. 7, pp. 930–936, July 1991.

[7] M. Steyaert, J. Crols, and G. Van der Plas, "A high performance RDS-detector for low voltage applications," *Analog Integrated Circuits and Signal Processing*, Special issue on low-voltage low-power analog integrated circuits, 1994.

[8] J. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, pp. 374–378, June 1978.

[9] B. Gerber, J.C. Martin, and J. Fellrath, "A 1.5 V single-supply one-transistor CMOS EEPROM," *IEEE J. Solid-State Circuits*, vol. 16, no. 3, p. 195, Dec. 1985.

[10] T. Choi *et al.*, "High-frequency CMOS switched-capacitor filters for communiacations application," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 652–663, Dec. 1983.

[11] W. Sansen, H. Qiuting, and K. Halonen, "Transient analysis of charge transfer in SC filters—gain error and distortion," *IEEE J. Solid-State Circuits*, vol. 22, no. 2, pp. 268–278, April 1987

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