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Switched Z-Source/Quasi-Z-Source DC-DC Converters With Reduced Passive Components for Photovoltaic Systems

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ABSTRACT In this paper, switched Z-source/quasi-Z-source dc-dc converters (SZSC/SQZSCs) are proposed for the photovoltaic (PV) grid-connected power system, where the high step-up dc-dc converters are required to boost the low voltage to high voltage. The boost factor is increased by adding another one switch and diode to the output terminals of traditional Z-source/quasi-Z-source dc-dc converters. Not only does the output capacitor function as the filter capacitor; it is also connected in series into the inductors' charging loops when both switches are turned on. Compared with existing Z-source based structures, higher boost factor is realized through a small duty cycle (smaller than 0.25). On the one hand, the instability caused by the saturation of the inductors can be avoided. On the other hand, a larger range can be reserved for the modulation index of the backend H-bridge when they are used for the dc-ac conversion. Moreover, much fewer passive components are employed when compared with the recently proposed hybrid 3-Z-network topologies that have the same voltage gain, which can enhance the power density and decrease the cost. The performances of the proposed converters, including their operational principles in continuous and discontinuous current modes, voltage and current parameters of components, and impacts of parasitic parameters, are analyzed. The simulation and experimental results are given to verify the aforementioned characteristics and theoretical analysis.

INDEX TERMS PV systems, switched Z-source/quasi-Z-source, dc-dc converters, reduced passive components.

I. INTRODUCTION

The global energy crisis is becoming an increasing motivation for the use of renewable energy [1], [2]. PV source is one of the significant players for solving the energy crisis. Unfortunately, the PV arrays is low-voltage dc source, requiring a high step-up dc-dc converter to convert to a higher voltage level before connecting it to a dc-ac inverter for grid-connected applications, as illustrated in FIGURE (Fig). 1. How to realize high voltage gain, low cost, and high efficiency dc-dc conversions for PV systems is becoming a fast growing research field.

Recently, many methods are proposed for improving the boost ability of the dc-dc converters, such as cascaded techniques [3], switched-component techniques [4], [5], coupled techniques [6], voltage-lift [7], voltage multiplier [8]. However, the high voltage gain is realized and high duty cycle of switches is required, which may decrease the efficiency and cause the saturation of inductors.

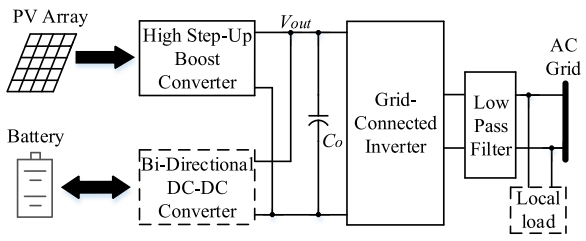

FIGURE 1. The PV grid-connected system.

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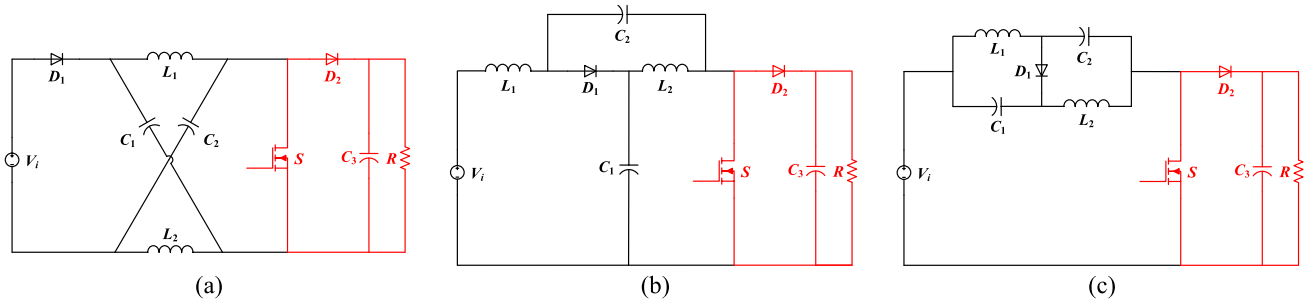


FIGURE 2. (a) The traditional Z-source dc-dc converter. (b) The traditional quasi-Z-source dc-dc converter with continuous input current. (c) The traditional quasi-Z-source dc-dc converter with discontinuous input current.

In [9], Z-source inverter (ZSI) is proposed with buck-boost ability. The problems of limited output voltage in the traditional voltage-source inverters can be solved. It has attracted many attentions in the recent years because of their flexible topologies. But the conventional ZSI has some disadvantages, including large inrush starting current, discrete input current and high voltage stress on capacitors [10]. In order to overcome shortcomings, the quasi-Z-source inverters are proposed in [11]. The boost factor of the ZSI is improved by the different techniques [12]–[14]. For example, a high dc-link voltage is generated by adding inductors, capacitors, and diodes to the Z-source network [12], [13]. The topology uses the cascaded quasi-Z-source network to get the higher voltage gain [14]. At present, the studies on Z-source network mainly focus on dc–ac power conversion, while the Z-source network can be also used in dc-dc conversion with its unique advantages [15], [16]. The original Z-source dc-dc converters with the boost factor of 1/(1-2D) (D is duty cycle of the switch S) are shown in Fig. 2. In [17], a family of hybrid 3-Z-network boost converters are proposed, which combine traditional Z-source networks in various methods. The boost factor can reach to 1/(1-4D), which is more suitable for PV applications. The major drawback is that it requires a lot of passive components, making the larger volume and more expensive.

This paper proposes a new family of dc-dc converters with reduced passive components for PV systems. By adding one more switch and diode to the output terminals of the traditional Z-source/quasi-Z-source topology, in which way, not only does the output capacitor function as the filter capacitor; it is also connected in series into the inductors' charging loops when the switches are turned on. Compared to the hybrid 3-Z-network boost converters in [17], the proposed one can reach the same voltage gain of 1/(1-4D) ($0 < D < 0.25$) with less components, enhancing the power density and decreasing the system cost. In other words, the new topologies require a lower duty ratio for the same boosting voltage, which results in the lower inductors, reducing the risk of inductive saturation [18]. Meanwhile, a larger range can be reserved for the modulation index of the backend H-bridge when they are used for the dc-ac conversion.

The remainder of this paper is constructed as follows. Circuit configurations of the proposed converters are presented in Section II. Operational principles of the proposed converters are illustrated in Section III. Voltage and current parameters of components are presented in Section IV. Impacts of the parasitic parameters in the proposed SZSC are analyzed in Section V. Section VI compares the proposed topologies with existing Z-source based converters. The simulation and experimental results are given in Sections VII. Finally, a conclusion is drawn in Section VIII.

II. CIRCUIT TOPOLOGIES OF THE PROPOSED CONVERTERS

A. CIRCUIT TOPOLOGIES OF THE PROPOSED SZSC/SQZSCs

The circuit topologies of the proposed SZSC/SQZSCs are shown in Fig. 3, including the proposed SZSC, the proposed SQZSC with continuous input current and the proposed SQZSC with discontinuous input current, respectively. These new topologies have the same pre-structure with the traditional Z-source topologies as shown in Fig. 2, respectively, except that the backend has one more switch (S_2) and diode (D_3). The capacitor (C_3) has two functionalities, one of which is output filter capacitor; the other one is to charge the inductors when the two switches (S_1 and S_2) are simultaneously turned on.

Therefore, the boost factor of the proposed SZSC/SQZSCs is significantly improved, which is 1/(1-4D) ($0 < D < 0.25$). Compared with the hybrid 3-Z-network boost converters in [17], the proposed topologies achieve the same voltage gain with less passive components, reducing the system cost and increasing power density. The advantage of the SQZSC over the SZSC is the voltage stress on the capacitor C_2 is reduced. The input current in CSQZSC is continuous, which can prolong the lifetimes of the input source. The advantage of the proposed DSQZSC over SZSC and CSQZSC is that the voltage stress on both capacitors C_1 and C_2 is reduced, while the input current is discontinuous in DSQZSC.

B. EXTENSIONS OF THE PROPOSED SZSC/SQZSCs TO DC-AC INVERTERS

By substituting the switch S_2 in the proposed SZSC/SQZSCs with an H-bridge and a LC filter, they can also be

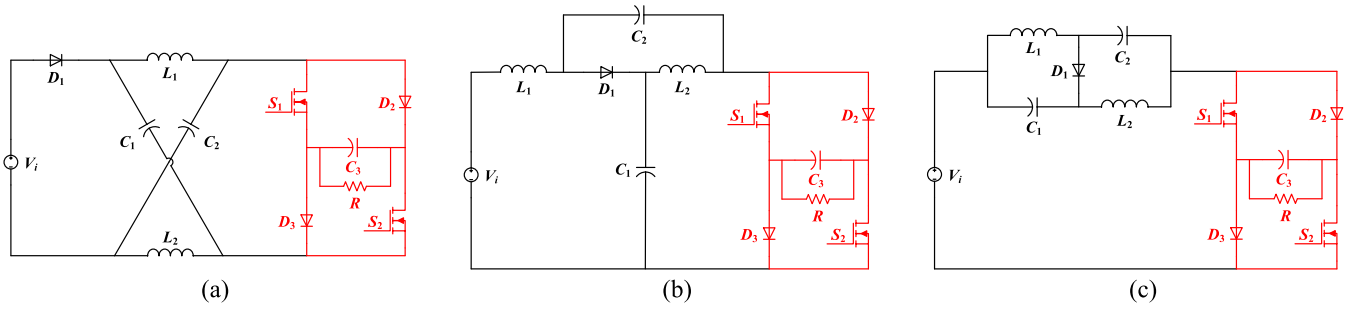


FIGURE 3. Circuit topologies of the proposed SZSC/SQZSCs. (a) Circuit topology of the proposed SZSC. (b) Circuit topology of the proposed CSQZSC. (c) Circuit topology of the proposed DSQZSC.

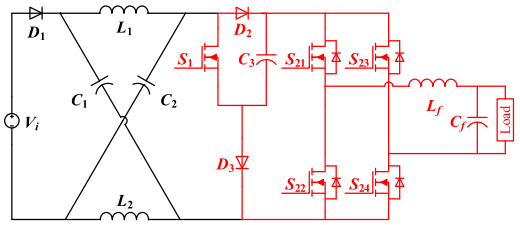


FIGURE 4. Circuit topology of the proposed switched-Z-source dc-ac inverter.

easily extended to dc-ac inverters. Fig. 4 shows the proposed switched-Z-source dc-ac inverter as an example. The boost factor of the frontend switched-Z-source network is 1/(1-4D), thus a high voltage gain can be realized by a small duty cycle. As a result, a larger range can be reserved for the modulation index of the backend H-bridge.

Since the proposed three converters have similar circuit configurations, the following analyses, as well as the simulation and experimental verification, are mainly conducted on the first topology, i.e., SZSC. The analysis method can also be adapted to the other two SQZSCs.

III. OPERATIONAL PRINCIPLES OF THE PROPOSED SZSC

The proposed SZSC can operate in both continuous and discontinuous current modes (CCM and DCM). The division basis is that whether the inductor currents reach zero in each cycle. The critical current mode (CRM) can be considered as a special case of either CCM or DCM. Under different combinations of the inductance, duty cycle, and load resistance, two cases (Case 1 and Case 2) may appear in CCM, and only one case (Case 3) in DCM. Each case has different circuit states in a whole cycle. Figs. 5(b)-(e) illustrate all the circuit states contained in the two modes. The reference directions of each variables are given in Fig. 5(a). Correspondingly, Case 1: State 1→State 2; Case 2: State 1→State 2→State 3; Case 3: State 1→State 2→State 3→State 4. The operational waveforms of the three cases are shown in Fig. 6. For simplicity, it is assumed that: 1) all the power components are ideal; 2) the free-wheeling diodes of switches S_1 and S_2 are ignored; 3) $L_1 = L_2$ and $C_1 = C_2$.

A. CASE 1 IN CCM

State 1 $[t_0, t_1]$*:* In this state, switches S_1 and S_2 are simultaneously turned on, and diodes D_1, D_2 and D_3 are reverse biased, namely, $i_{D1} = i_{D2} = i_{D3} = 0$. The capacitors C_1, C_2 and C_3 are discharged, while inductors L_1 and L_2 store energy, and energy stored in capacitor C_3 is transferred to load. As shown in Fig. 5(b), it can be observed from the current loop the capacitor C_1 has the same current with the inductor L_1, i.e., $i_{C1} = i_{L1}$; the capacitor C_2 has the same current with the inductor L_2, i.e., $i_{C2} = i_{L2}$; switches S_1 and S_2 have the same current, i.e., $i_{S1} = i_{S2}$. The following equations can be derived in state 1

$$\begin{cases} i_{S1} = i_{L1} + i_{L2} \\ i_{C3} = i_{S1} + i_o \end{cases} \tag{1}$$

$$\begin{cases} v_{L1} = v_{C1} + v_{C3} \\ v_{L2} = v_{C2} + v_{C3} \end{cases} \tag{2}$$

State 2 $[t_1, t_2]$*:* In this state, switches S_1 and S_2 are simultaneously turned off, namely, $i_{S1} = i_{S2} = 0$, and diodes D_1, D_2 and D_3 are forward conducted. The input source V_i and the inductor L_2 discharge the energy to capacitor C_1; the input source V_i and the inductor L_1 discharge the energy to capacitor C_2; the input voltage source V_i and the two inductors L_1 and L_2 discharge the energy to the capacitor C_3 and the load. It can be observed from the current loop in Fig. 5(c) that diodes D_1 and D_2 have the same current; According to KCL, one has

$$\begin{cases} i_{D1} = i_{L1} - i_{C1} \\ i_{D2} = i_{L1} + i_{C2} \\ i_{D3} = i_o - i_{C3} \end{cases} \tag{3}$$

According to KVL, the voltages over the three capacitors in this state, can be obtained

$$\begin{cases} v_{C1} = V_i - v_{L2} \\ v_{C2} = V_i - v_{L1} \\ v_{C3} = V_i - v_{L1} - v_{L2} \end{cases} \tag{4}$$

In the view of the symmetry of the Z-source network, the following equations can be obtained in both states.

$$\begin{cases} i_{L1} = i_{L2} \quad v_{L1} = v_{L2} \\ i_{C1} = i_{C2} \quad v_{C1} = v_{C2} \end{cases} \tag{5}$$

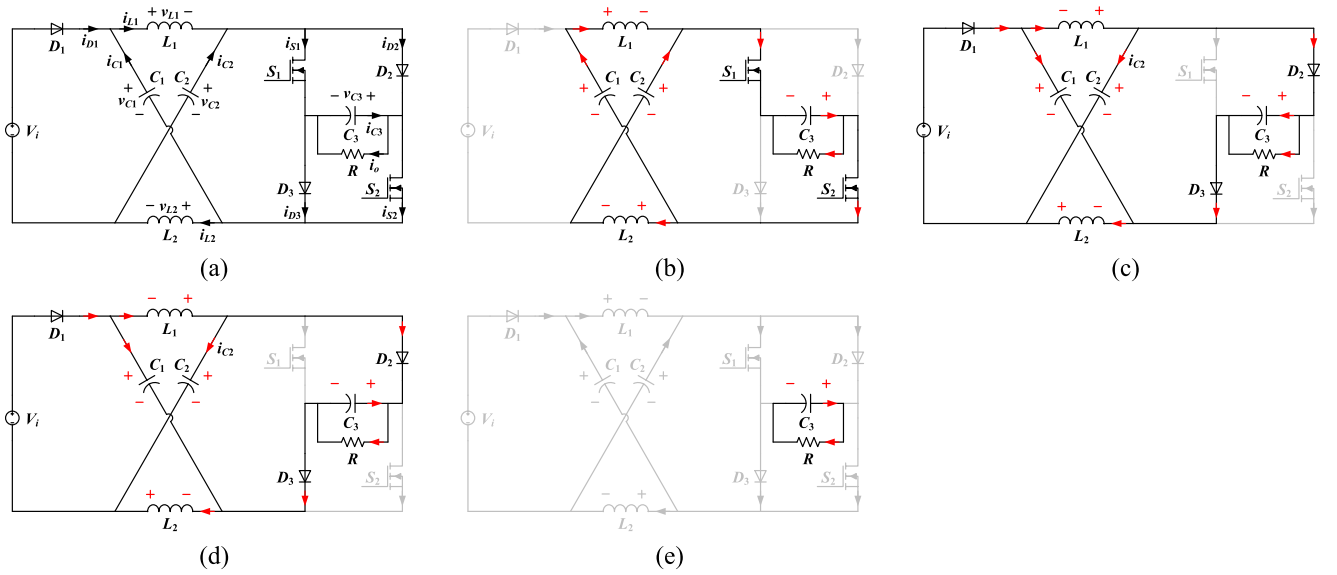


FIGURE 5. (a) Specifications of reference directions. (b) Current loop of the proposed SZSC in State 1: S1 and S2 on; D1, D2 and D3 off. (c) Current loop of the proposed SZSC in State 2: D1, D2 and D3 on; S1 and S2 off. (d) Current loop of the proposed SZSC in State 3: D1, D2 and D3 on; S1 and S2 off. (e) Current loop of the proposed SZSC in State 4: S1, S2, D1, D2 and D3 off.

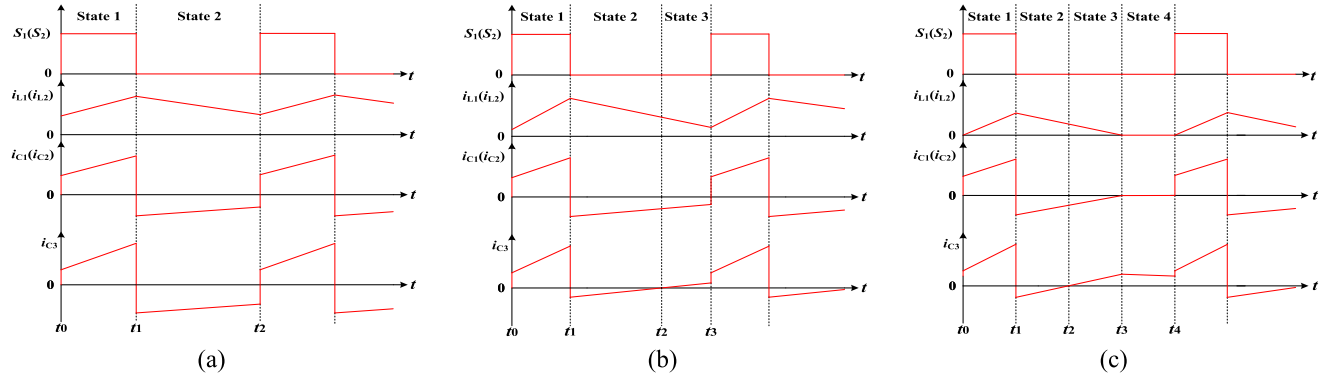


FIGURE 6. Operational waveforms of the proposed SZSC in three cases. (a) Case 1. (b) Case 2. (c) Case 3.

B. CASE 2 IN CCM

State 1 $[t_0, t_1]$ and State 2 $[t_1, t_2]$ in Case 2 are just like the two states in Case 1 according to Figs. 5 and 6. Differently at the end of State 2 in Case 2, the capacitor C_3 is discharged to supply the load along with the series-connected input source V_i and the two inductors L_1 and L_2. Therefore, one more state exists in Case 2 when compared with Case 1, namely, State 1→State 2→State 3.

In State 3 $[t_2, t_3]$, the voltage relationships among the components are the same as those in State 2, while the current relationships are different, as

$$\begin{cases} i_{D1} = i_{L1} - i_{C1} & i_{L1} = i_{L2} \\ i_{D2} = i_{L1} + i_{C2} & i_{C1} = i_{C2} \\ i_{C3} = i_o - i_{D3} \end{cases} \tag{6}$$

C. CASE 3 IN CCM

States 1 $[t_0, t_1]$, State 2 $[t_1, t_2]$ and State 3 $[t_2, t_3]$ in Case 3 are just like the three states in Case 2 according to Figs. 5 and 6. Differently at the end of State 3 in Case 3, the currents through the inductors L_1 and L_2 reach zero, and the proposed SZSC enters DCM. Therefore, four states exist in Case 3, namely, State 1→State 2→State 3→State 4.

$$\begin{cases} i_{L1} = i_{L2} = i_{C1} = i_{C2} = 0 \\ i_{S1} = i_{S2} = i_{D1} = i_{D2} = i_{D3} = 0 \\ i_{C3} = i_o \end{cases} \tag{7}$$

In State 4 $[t_3, t_4]$, the switches S_1 and S_2 remain turned off. Differently from States 2 and 3, the diodes D_1, D_2 and D_3 are reverse biased in this state. Thus, voltages over capacitors C_1 and C_2 remain unchanged, and one has

IV. PARAMETERS OF THE PROPOSED CONVERTERS IN CCM

It is recommended that the proposed converters should operate in CCM, as the input and output voltages are in a linear relationship regarding to the duty cycle of switches S_1 and S_2. Under this condition, the boost factor of the proposed SZSC, as well as the component voltages and currents, are

deduced according to the analyses of Cases 1 and 2. Then, the corresponding voltage and current parameters in SQZSCs are presented directly. The boundary condition between CCM and DCM and the small-signal model analysis of the proposed SZSC are also presented in this section for better understanding of its performances.

A. BOOST FACTOR AND COMPONENT VOLTAGE STRESSES IN SZSC

For simplicity, the voltages on capacitors remain constant, which are rephrased as V_{C1}, V_{C2} and V_{C3}, respectively. In terms of the voltage-second of the two inductors in a whole cycle, the capacitor voltages, as well as the output voltage V_o, can be obtained according to (2), (4) and (5), as

$$\begin{cases} V_{C1} = V_{C2} = \dfrac{1-2D}{1-4D} V_i \\ V_o = V_{C3} = \dfrac{1}{1-4D} V_i \end{cases} \tag{8}$$

where D is the duty cycle of switches S_1 and S_2, which equa1s to $(t_1\text{-}t_0)/T$ (T is the switching cycle). Compared to the hybrid 3-Z-network boost converter in [17], the proposed converter has the same voltage gain, which is 1/(1-4D), while larger than the traditional one at a fixed duty cycle. When switches S_1 and S_2 are simultaneously turned on, the diodes D_1, D_2 and D_3 withstand reversed voltages, which are $2V_i$/(1-4D), V_i/(1-4D) and V_i/(1-4D), respectively. Similarly, they have the same blocked voltage equaling to V_i/(1-4D) when the switches are turned off.

B. CURRENT STRESSES OF INDUCTORS, DIODES AND SWITCHES

When considering that the input power equals to the output power under ideal condition, the average input current I_i can be expressed by the output current I_o as

$$I_i = \frac{V_o I_o}{V_i} = \frac{1}{1-4D} I_o \tag{9}$$

The input voltage source is connected in series with the diode D_1, thus they have the same current, namely, $i_i = i_{D1}$. Then the average input current I_i can be obtained as

$$I_i = \frac{1}{T} \int_{DT}^{T} i_{D1} dt \tag{10}$$

Substituting (3) and (5) into (10) results in

$$\begin{cases} I_i = \frac{1}{T} \int_0^T i_{L1} dt \\ I_i = I_{L1} = I_{L2} = \dfrac{1}{1-4D} I_o \end{cases} \tag{11}$$

where I_{L1} and I_{L2} are the average currents through the inductors L_1 and L_2, respectively. According to the equations (1), (3) and (5), the component current stresses can be obtained as

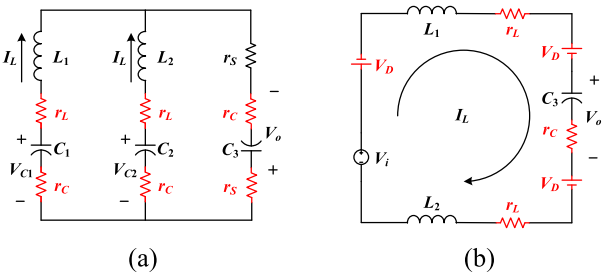


FIGURE 7. Equivalent current loops when considering the parasitic parameters. (a) In State 1. (b) In State 2.

$$\begin{cases} I_{D1} = \dfrac{1}{1-4D} I_o \\ I_{D2} = I_{D3} = \dfrac{1-2D}{1-4D} I_o \\ I_{S1} = I_{S2} = \dfrac{2D}{1-4D} I_o \end{cases} \tag{12}$$

where I_{D1}, I_{D2}, I_{D3}, I_{S1} and I_{S2} are the average currents through D_1, D_2, D_3, S_1 and S_2.

In the same way, voltage and current parameters of the proposed SQZSCs can be obtained, as listed in Tables 1. It can be observed that the proposed three converters have the same boost factor, i.e., 1/(1-4D) ($0 < D < 0.25$). In contrast, the voltage on the capacitor C_2 in CSQZSC and the voltages on both capacitors C_1 and C_2 in DSQZSC are all $2DV_i$/(1-4D), which is smaller than that in SZSC.

V. IMPACTS OF THE PARASITIC PARAMETERS IN SZSC

Some differences between ideal and actual case may occur in the proposed converters, such as the parasitic resistances of the inductors (r_L), the ESR of capacitors (r_C), the on-state resistances of switches (r_S), and the forward voltage drops of diodes (V_D). Fig. 7 shows the equivalent current loops of the proposed SZSC, where $I_L = I_{L1} = I_{L2}$. For simplicity, the ripples of inductor currents and capacitor voltages are neglected.

A. IMPACT OF THE PARASITIC PARAMETERS ON THE OUTPUT VOLTAGE

When considering parasitic parameters, the actual output voltage can be calculated by

$$V_o = \frac{V_i - 2I_L r_L - 8I_L r_S D - V_D(3-4D)}{1-4D} \tag{13}$$

From (13), voltage difference from the ideal one is independent of the input voltage. A surface is drawn in Fig. 8(a) to demonstrate the impact of the parasitic parameters on the output voltage, using the following parameters.

$$\begin{cases} V_i = 45\ V & r_S = 14.5\ \text{m}\Omega \\ I_L = 5\ A & r_L = 0 - 30\ \text{m}\Omega \\ D = 0.2 & V_D = 0 - 1.5\ \text{V} \\ r_C = 10\ \text{m}\Omega \end{cases} \tag{14}$$

TABLE 1. Voltage and current parameters of components in SZSC/SQZSCs.

Component voltages				Component currents			
Parameter modes	SZSC	CSQZSC	DSQZSC	Parameter modes	SZSC	CSQZSC	DSQZSC
Output voltage (V_o)	$\frac{1}{1-4D}V_i$	$\frac{1}{1-4D}V_i$	$\frac{1}{1-4D}V_i$	Input current (I_i)	$\frac{1}{1-4D}I_o$	$\frac{1}{1-4D}I_o$	$\frac{1}{1-4D}I_o$
Voltage on the capacitor C_1 (V_{C1})	$\frac{1-2D}{1-4D}V_i$	$\frac{1-2D}{1-4D}V_i$	$\frac{2D}{1-4D}V_i$	Current stress of the inductor L_1 (I_{L1})	$\frac{1}{1-4D}I_o$	$\frac{1}{1-4D}I_o$	$\frac{1}{1-4D}I_o$
Voltage on the capacitor C_2 (V_{C2})	$\frac{1-2D}{1-4D}V_i$	$\frac{2D}{1-4D}V_i$	$\frac{2D}{1-4D}V_i$	Current stress of the inductor L_2 (I_{L2})	$\frac{1}{1-4D}I_o$	$\frac{1}{1-4D}I_o$	$\frac{1}{1-4D}I_o$
Voltage stress on switches S_1 and S_2(V_{S1} and V_{S2})	$\frac{1}{1-4D}V_i$	$\frac{1}{1-4D}V_i$	$\frac{1}{1-4D}V_i$	Current stress of switches S_1 and S_2 (I_{S1} and I_{S3})	$\frac{2D}{1-4D}I_o$	$\frac{2D}{1-4D}I_o$	$\frac{2D}{1-4D}I_o$

As can be seen from the previous analysis, there is a voltage difference between the ideal output and the actual output. The actual output voltage is close to the ideal one by reducing the values of r_L and V_D. As a result, these parameters should be taken into account in the design of prototypes.

B. IMPACT OF THE PARASITIC PARAMETERS ON THE EFFICIENCY

According to the parasitic parameters mentioned above, the power loss of the proposed SZSC can be calculated as follow

1) POWER SWITCH LOSS

The power losses in switches include the conduction loss and switching loss. From Fig. 7, the conducting loss can be calculated by

$$P_{cond\_s} = 8I_L^2 r_S D \tag{15}$$

The switching loss can be estimated by linearizing the currents and voltages of the corresponding switches [20], [21], when they are changing their states, as

$$P_s = \frac{2f_s V_o I_L (t_{on} + t_{off})}{3} \tag{16}$$

where f_s is switching frequency; and t_{on}, t_{off} are the turn-on and turn-off delays of the switches, respectively.

2) DIODE LOSS

The power losses in diodes consist of the conduction loss and reverse recovery loss. The conduction loss can be expressed by

$$P_{cond\_D} = 3I_L V_D (1 - D) \tag{17}$$

The reverse recovery loss in diodes is

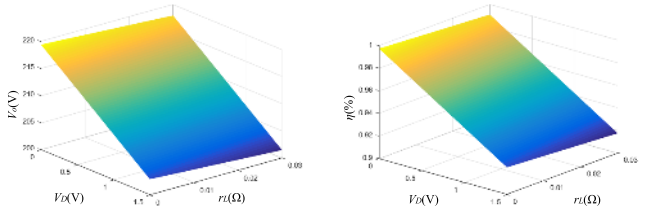
$$P_{RRD} = Q_{RR1} V_{C1} f_s + Q_{RR2} V_{C2} f_s + Q_{RR3} V_{C3} f_s \tag{18}$$

where Q_{RR1}, Q_{RR2} and Q_{RR3} represent the reverse recovery charge of diodes D_1, D_2 and D_3, respectively.

3) INDUCTOR LOSS

The main power losses in inductors is determined by the conduction loss, which can be calculated by

$$P_{cond\_L} = 2I_L^2 r_L \tag{19}$$



(a) (b)

FIGURE 8. Impacts of the parasitic on the output voltage and conversion efficiency. (a) Theoretical output voltage Vo as a function of rL and VD. (b) Theoretical conversion efficiency as a function of rL and VD.

4) CAPACITOR LOSS

The total power losses in capacitors is derived as

$$P_{cond\_C} = I_L^2 r_C (1 - 5D) \tag{20}$$

Then, the total conduction losses are calculated by

$$P_{cond} = P_{cond\_S} + P_{cond\_D} + P_{cond\_L} + P_{cond\_C} \tag{21}$$

The input power can be obtained according to (11) as

$$P_i = V_i I_i = V_i I_L \tag{22}$$

Afterwards, the efficiency of the proposed SZSC can be calculated by

$$\eta = \frac{P_o}{P_i} = \frac{P_i - P_{cond} - (P_s + P_{RRD})}{P_i} \tag{23}$$

Similarly, the impact of the parasitic parameters on the conversion efficiency is shown in Fig. 8(b), using the following parameters.

$$\begin{cases} V_i = 45\ V & r_S = 14.5\ \text{m}\Omega \\ I_L = 5\ A & r_L = 0 - 30\ \text{m}\Omega \\ D = 0.2 & V_D = 0 - 1.5\ \text{V} \\ r_C = 10\ \text{m}\Omega & f_s = 25\ \text{kHz} \end{cases} \tag{24}$$

Fig. 8(b) indicates that reducing the parasitic parameters can also contribute to higher efficiency.

TABLE 2. Component of the proposed converters and those in [17] and [22]–[25].

Refs.	Components	Voltage gain	Voltage stress on switches	Main features and drawbacks
[17]	4 Inductors 7 Capacitors 1 Switches 4 Diodes	$G=\frac{1}{1-4D}$	$V_s=\frac{1}{1-4D}V_i$	√ Using a small duty cycle to realize high voltage gain √ High boost ability □ The different common ground for the input and output □ Need a lot of passive components
[22]	1 Inductors 3 Capacitors 2 Switches 4 Diodes	$G=\frac{3-2D}{1-2D}$	$V_s=\frac{1}{1-2D}V_i$	√ Low voltage stress on device √ High boost ability □ The different common ground for the input and output
[23]	3 Inductors 7 Capacitors 1 Switches 5 Diodes	$G=\frac{2+D}{1-2D}$	$V_s=\frac{1}{1-2D}V_i$	√ Capability of adding extra stage for reaching higher voltage gain √ Low voltage stress on devices □ Need a lot of passive components □ The different common ground for the input and output
[24]	4 Inductors 4 Capacitors 1 Switches 3 Diodes	$G=\frac{2(1-D)}{1-3D}$	$V_s=\frac{2(1-D)}{1-3D}V_i$	√ The common ground for the input and output □ high voltage stress on devices □ Can't realize high voltage gain
[25]	2 Inductors 2 Capacitors 2 Switches 6 Diodes	$G=\frac{1+D}{1-3D}$	$V_{s1-2}=\frac{1+D}{1-3D}V_i$	√ Capability of adding extra stage for reaching higher voltage gain □ high voltage stress on devices □ Can't realize high voltage gain □ The different common ground for the input and output
Proposed	2 Inductors 3 Capacitors 2 Switches 3 Diodes	$G=\frac{1}{1-4D}$	$V_{s1-2}=\frac{1}{1-4D}V_i$	√ Using a small duty cycle to realize high voltage gain √ High boost ability □ The different common ground for the input and output

TABLE 3. Measured component voltages and currents in PSIM.

Converter type	Voltages/V				Currents/A					
	$V_o(V_{C3})$	V_{C1}	V_{C2}	$V_{S1}(V_{S2})$	I_o	I_i	$I_{L1}(I_{L2})$	I_{D1}	$I_{D2}(I_{D3})$	$I_{S1}(I_{S2})$
SZSC	212.1	129.1	129.1	213.3	1	5.04	5.00	5.04	3.02	1.94
CSZSC	212.1	129.1	84.1	213.3	1	4.79	4.79	4.84	2.91	1.83
DSZSC	186.5	73.8	73.8	186.5	1	5.00	4.99	4.98	2.99	2.01

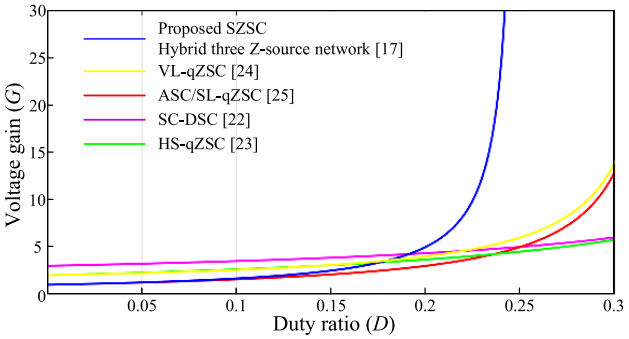


FIGURE 9. Relationships between the voltage gain and the duty ratio.

VI. COMPARISONS WITH EXISTING Z-SOURCE TOPOLOGIES

Furthermore, the performance of the proposed topology is compared to those converters in [17] and [22]–[25], as shown in Table 2. Boost ability is an important index to evaluate the performance of dc-dc converter. As shown in Fig. 9, the proposed topology produces a higher boost factor than other converters at the same duty ratio when the voltage gain $G > 5$, while the boost factor is the same as the complicated hybrid 3-Z-network boost converter in [17]. In other words, the new topology significantly reduces the number of passive devices for the same boosting ability. This brings two advantages. One is to reduce the risk of inductive saturation; the other one is a higher modulation index. As a result, a larger range can be reserved for the modulation index of the backend H-bridge when they are used for the two stage dc-ac conversion.

Table 2 also shows the comparison of component numbers among topologies in [17], and [22]–[25] and the proposed one. It is noted that these topologies are converted into dc-dc converters by replacing the backend H-bridge in each structure with a switch, a diode and an output capacitor. It can be seen that the proposed one has the same voltage gain of 1/(1-4D), with two less inductors, four less capacitors and one less diode and only one more switching device when comparing to the hybrid 3-Z-network boost converter proposed in [17], thus the higher power density and the lower cost.

VII. SIMULATION AND EXPERIMENT VERIFICATIONS

In order to validate the correctness of the previous analyses, Simulation models of the proposed SZSC/SQZSCs are

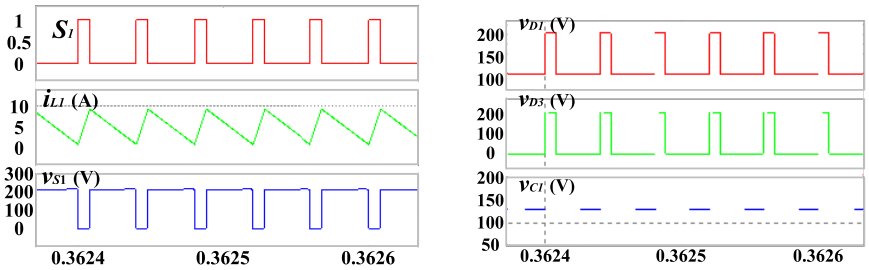


FIGURE 10. Simulation waveforms of the proposed SZSC at the duty cycle of 0.2. (a) Gate signal of S1, iL1 and vS1. (b) vD1, vD3 and vC1.

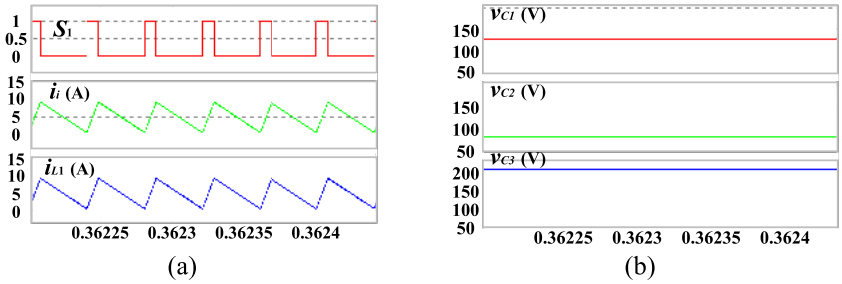


FIGURE 11. Simulation waveforms of the proposed CSQZSC at the duty cycle of 0.2. (a) Gate signal of S1, ii and iL1. (b) vC1, vC2 and vC3 (vo).

implemented in PSIM (Power Simulation). Afterwards, an experimental SZSC prototype is conducted, which can function as an interface to integrate the PV modules to a dc micro-grid. Previously, solutions to determining the inductance and capacitance are given.

A. DETERMINATION OF THE INDUCTANCE AND CAPACITANCE

Inductance ($L_1 = L_2$): The current ripple through the inductor L_1 (I_{L1}) has been deduced in Section IV.C. When considering that a $x_L\%$ peak-to-peak current ripple is tolerated for the inductor, the inductance can be then determined by

$$L_1 = L_2 = \frac{2V_i D(1-D)}{x_L\% I_o f_s} \tag{25}$$

Capacitance ($C_1 = C_2$): Similarly, the capacitors voltage ripple on C_1 can be obtained as follow

$$\Delta V_{C1} = \frac{I_{L1} D}{C_1 f_s} \tag{26}$$

Therefore, taking the $x_C\%$ peak-to-peak capacitor voltage ripple into consideration, the capacitance can be designed by

$$C_1 = C_2 = \frac{I_o D}{x_C\% f_s V_i (1-2D)} \tag{27}$$

B. SIMULATION RESULTS

The dc output voltage of 225 V is used for 110V dc/ac conversion, and the setting of input voltage is given as three photovoltaic panels in series. The simulation parameters are given according to the previous analyses: 1) $V_i = 45$ V; 2) $f_s = 25$ kHz; 3) the duty cycle is 0.2; 3) the rated output power is appropriately 185 W; 4) $L_1 = L_2 = 320$ μH, with a parasitic resistance of 28-mΩ; 5) $C_1 = C_2 = C_3 = 330$ μF, with a 10-mΩ equivalent series resistance; 6) the on-state resistance of switches S_1 and S_2 is 14.5 mΩ; 7) the forward voltage drop of the diodes D_1, D_2 and D_3 is 1 V. The measured component voltages and currents in PSIM are shown in Table 3, and simulation waveforms of the key points in SZSC/SQZSCs, such as the input and inductor currents, and the capacitor voltages, are shown in Figs. 10-12.

Ignoring the minor measurement errors, the measured results in Table 3 agree well with the equations in Table 1, which verify the correctness of the previous analyses. From Fig. 11(a), the proposed CSQZSC has continuous input current, which is the same as that through the inductor L_1. It is because that the input source and the inductor L_1 are directly connected in series in CSQZSC. In contrast, in Fig. 12(a), the input current of DSQZSC is discontinuous when the switches are turned off.

C. EXPERIMENTAL RESULTS

A prototype converter is built to validate the theoretical analysis and simulation results for the proposed topology. Table 4 shows the specifications of the used devices, and the parameters are the same as those in simulation.

Fig. 13(a) shows the relationships between the output voltages and the duty ratio when the load current is 1A. It can be found the simulation is in good agreement with

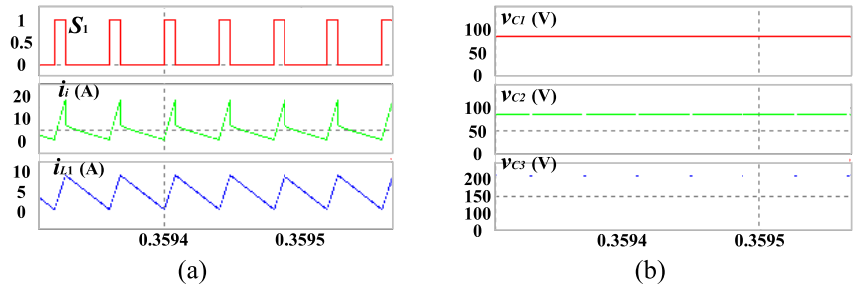


FIGURE 12. Simulation waveforms of the proposed DSQZSC at the duty cycle of 0.2. (a) Gate signal of S1, ii and iL1. (b) vC1, vC2 and vC3 (vo).

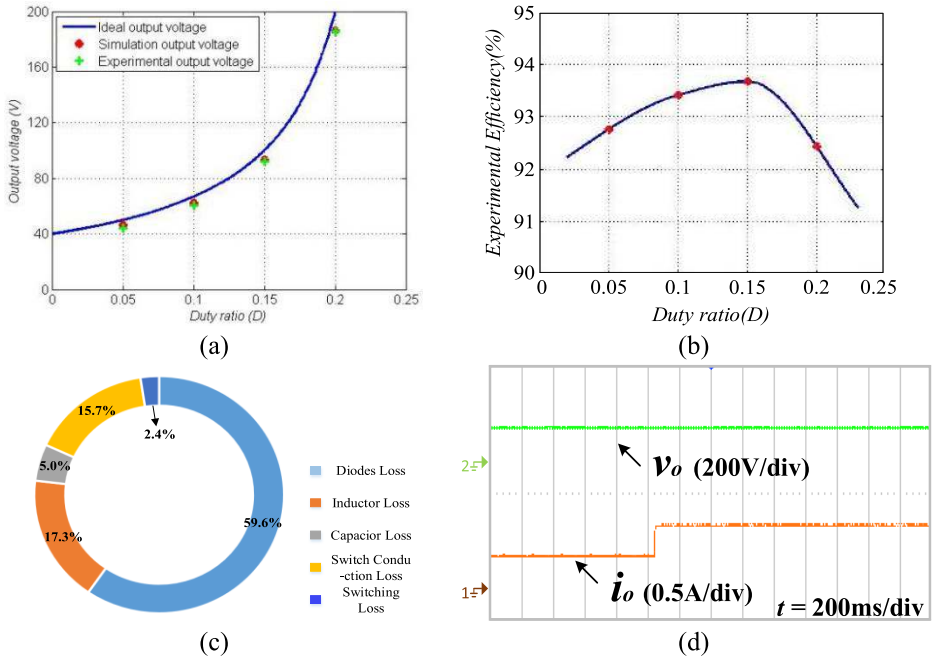


FIGURE 13. (a) Simulation and experimental output voltages versus the duty cycle when the input voltage Vi = 45 V and the load current io = 1 A. (b) Experimental efficiency versus the duty cycle when the input voltage Vi = 45 V and the load current io = 1 A. (c) Power loss distribution at the duty of 0.2. (d) Dynamic performance with 50% step-down change in dc load.

TABLE 4. Specifications of devices for experiment.

Devices	Specifications
Controller	TMS320F28335
Diodes D_1	MUR1660CT
Diodes D_2 and D_3	MUR1640CT
Switches S_1 and S_2	IRFP4768PbF
Inductors L_1 and L_2	320 H/12 A
Capacitors C_1 and C_2	330 F/250 V

the experimental results. Fig. 13(b) shows the curve of experimental efficiency versus the duty ratio in actual case. Fig. 13(c) shows the influence of parasitic parameter on the efficiency. This analysis proves that the overall efficiency can be improved by optimizing parasitic parameters.

TABLE 5. Efficiency of the proposed and conventional converters.

Voltage Gain	2	3	4	5
%Eff.(conventional)	95.1	92.7	89.6	87.2
%Eff.(proposed SZSC)	92.8	93.4	93.7	92.4

To verify the regulation and dynamic performance, a 50% step-down change is applied in dc load, as shown in Fig. 13(d).

The experimental waveforms at the duty cycle of 0.2, are shown in Fig. 14. The experimental output voltage is 207.5 V. A 17.5-V voltage difference exists when compared with the ideal 225-V output, which is in accordance with the surface in Fig. 8(a). Thus, the correctness of the theoretical analyses is further verified here. The efficiency comparison between the proposed converter and the conventional converter in [9] is shown in Table 5.

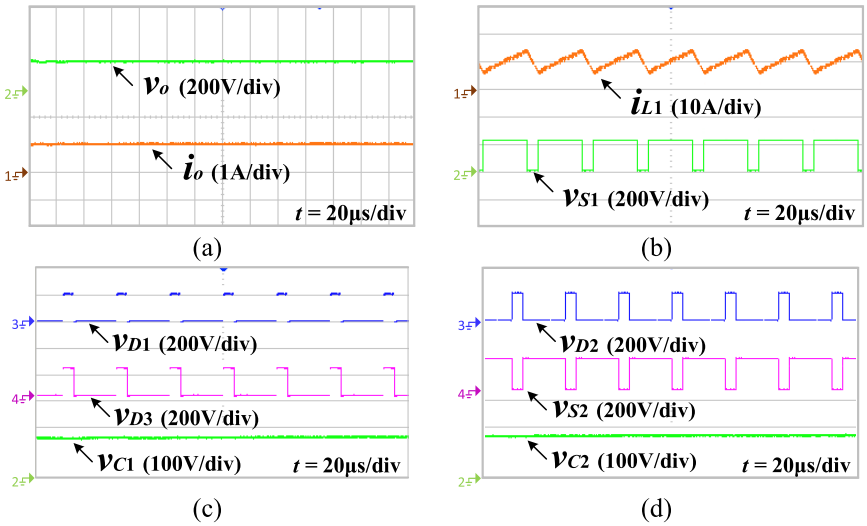


FIGURE 14. Experimental results of the proposed SZSC at the duty cycle of 0.2. (a) vo and io. (b) iL1 and vS1. (c) vD1, vD3 and vC1. (d) vD2, vS2 and vC2.

VIII. CONCLUSION

A family of SZSC/SQZSCs is proposed with simplified topologies for PV systems. The boost factor is increased to 1/(1-4*D*) by adding another one switch and diode to the traditional Z-source/quasi-Z-source dc-dc converters. High voltage gain is realized by small duty cycle, which can avoid the instability caused by saturation of the inductors. The proposed converters have the same high boost ratio as the recently proposed hybrid 3-Z-network boost converters with the less passive components, which can enhance the power density and decrease the system cost. Detailed descriptions have been presented in this paper, including their operational principles, voltage and current parameters of components, and the impacts of the parasitic parameters on the conversion efficiency. Finally, simulation and experimental results are given to verify the aforementioned characteristics and theoretical analysis.

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