Switching Converters with Wide DC Conversion Range

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Abstract—In dc-to-dc conversion applications that require a large range of input and/or output voltages, conventional PWM converter topologies must operate at extremely low duty ratios, which limits the operation to lower switching frequencies because of the minimum ON-time of the transistor switch. This is eliminated in a new class of single-transistor PWM converters featuring voltage conversion ratios with quadratic dependence on duty ratio. Practical circuit examples operating at 0.5 MHz are described.

I. INTRODUCTION

IN PWM (square-wave) dc-to-dc converter topologies, dc conversion ratio M ($M \equiv V_{out}/V_{in}$) is a function of duty ratio D of the active (transistor) switch. Both minimum and maximum attainable conversion ratios are limited in practical converters. The maximum conversion ratio M_{max} of the buck converter ($M(D) = D$) cannot be greater than 1, while in boost ($M(D) = 1/(1 - D)$), buck-boost or Ćuk converters ($M(D) = -D/(1 - D)$), M_{max} is limited by the degradation in efficiency as duty ratio D approaches 1. On the lower end, minimum ON-time of the transistor switch results in a minimum attainable duty ratio and, consequently, in a minimum conversion ratio M_{min}.

Evidently, the limit on M_{min} becomes more restrictive as the switching frequency is increased. It is possible that in practical applications a lower operating frequency has to be selected only because of the low-end limitation in D. One typical application is a low-voltage, on-board regulator ($V_{out} = 5$ V or less), supplied from an unregulated mid-voltage bus ($V_{in} \approx 50$ V). If isolation is not required, a converter without transformer is preferable but then, the converter itself has to provide a large step-down. One such converter, in which a capacitive voltage divider is embedded in the Ćuk topology, was suggested in [1]. Other possible applications that require an extremely large conversion range include laboratory power supplies, where wide range of adjustable output voltages is required, or universal 110/220 V off-line power supplies, where the converter is exposed to extremely wide range of input voltages.

Conversion range can be extended significantly if conversion ratio $M(D)$ has a quadratic dependence on duty-cycle. For example, two buck converters in a cascade (Fig. 1(a)) provide a conversion ratio $M(D) = D^2$ and a significantly lower M_{min} for
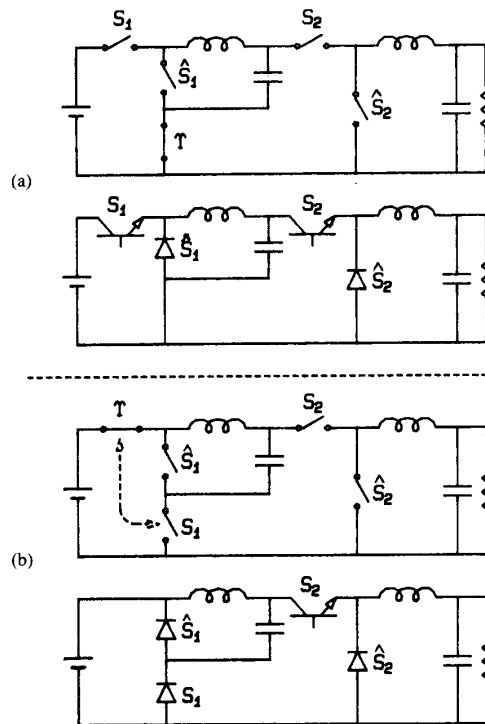
Fig. 1. (a) Cascade of two buck converters has $M(D) = D^2$, but requires two transistor switches. (b) If short Υ and switch S_1 interchange their positions, only single transistor is necessary to obtain converter with same dc conversion ratio.

the same minimum ON-time. Other advantageous conversion-ratio functions include $M(D) = D^2/(1 - D)$ and $M(D) = D^2/(1 - D)^2$. Of course, converters with such conversion ratios can be readily constructed by cascading two basic converters, as in [2]. Such realizations, however, require two transistor switches and additional complexity of the converter network may compromise potential advantages of the extended conversion range. It can be shown that $M(D)$ with quadratic dependence on d cannot be realized with less than two capacitors, two inductors, and four switches [3], but the number of transistor switches can be reduced to one. Indeed, a slight modification in the position of the S_1-switch in the buck-buck cascade results in a single-transistor converter with $M(D) = D^2$, as shown in Fig. 1(b). Note that the two topologies with ideal switches are electrically equivalent—the two switched networks,

$$S_1, S_2 \text{ ON}, \hat{S}_1, \hat{S}_2 \text{ OFF}, \qquad (1)$$

and

$$S_1, S_2 \text{ OFF}, \hat{S}_1, \hat{S}_2 \text{ ON}, \qquad (2)$$

are identical in the converter of Fig. 1(a) and in the converter of Fig. 1(b). The difference between the topologies becomes apparent only after the ideal (four-quadrant) switches are replaced by the single-quadrant semiconductor switches.

In Section II, new single-transistor converter topologies with quadratic conversion ratios are introduced. Operation and basic properties of the converters are discussed in Section III. Design considerations and experimental results for two practical examples operating at 0.5 MHz are presented in Sections IV and V.

II. QUADRATIC PWM CONVERTERS

A systematic procedure for construction of complete classes of PWM converters with a given number of reactive elements, a given number of switches and a required dc conversion ratio is described in [3]. The procedure is used to extract fourth-order, single-ended PWM converters with quadratic conversion ratios and a single active (transistor) switch. Parameters given at the input of the procedure are as follows.

- Required dc conversion ratio: $|M(D)| = D^2$, $D^2/(1 - D)$, or $D^2/(1 - D)^2$;
- Number of capacitors, inductors: $n_c = n_l = 2$;
- Number of switches: $n_s = 4$;
- Number of transistor switches; $n_t = 1$.

Implemented in a computer program, the synthesis procedure searches through all possible configurations and extracts those that satisfy the input specifications. As a result, quadratic converter topologies in Figs. 2–7 are uncovered.

The conversion ratio of converters α_1 and α_2 is $M(D) = D^2$, converters $\mathcal{B}_1$, $\mathcal{B}_2$ and $\mathcal{B}_3$ $M(D) = -D^2/(1 - D)$, while converter $\mathcal{C}_1$ features $M(D) = D^2/(1 - D)^2$. Versions with an isolation transformer are indicated where applicable. None of the above converter configurations were disclosed before, with the exception of the $\mathcal{B}_1$-converter, which was independently arrived at by Lambda Electronics.

It is interesting to note that some of the quadratic topologies (α_2 and $\mathcal{B}_3$ in particular) bear little resemblance to a cascade or some other combination of two basic converters. Thus, it is not likely that some intuitive circuit-manipulation technique (such as the one used to derive the α_1-converter in the introductory section) would uncover all converter topologies introduced in this section. On the other hand, the systematic synthesis procedure guarantees that all topologies with a specified set of properties are found.

III. OPERATION OF THE QUADRATIC CONVERTER TOPOLOGIES

In this section, we discuss operation and basic properties of the quadratic converters introduced in Section II.

A. Continuous Conduction Mode

Conversion ratio $M(D)$ of the quadratic converters in Figs. 2–7 is derived assuming that the converters operate in the continuous conduction mode (CCM). In CCM, all capacitor voltages and inductor currents are dc quantities with a relatively small superimposed ac ripple. Turn-ON and turn-OFF transitions of all diodes are synchronous with switching transitions of the
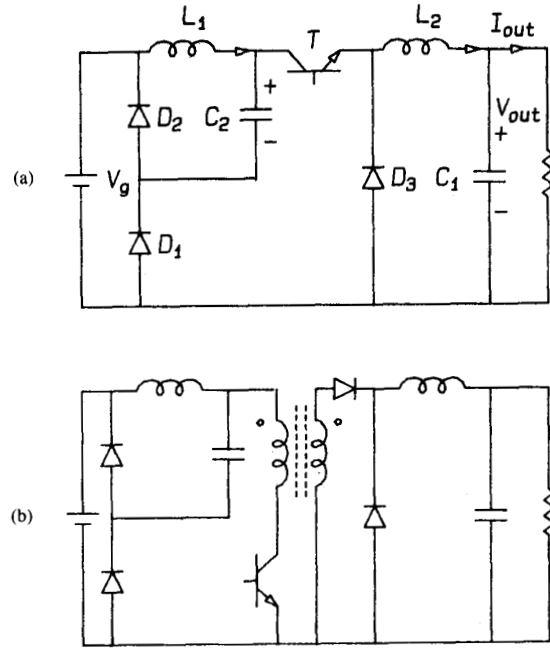

Fig. 2. Converter α_1 with dc conversion ratio $M(D) = D^2$ (a); and its version with an isolation transformer (b).
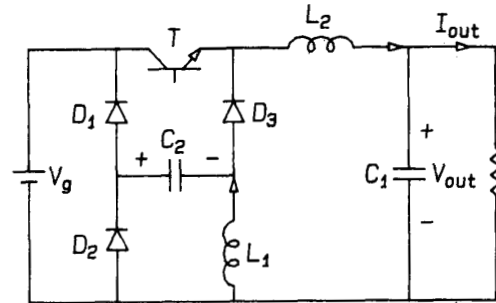

Fig. 3. Converter α_2 with dc conversion ratio $M(D) = D^2$.

transistor. In the following discussion, for simplicity, we assume that ac ripples in capacitor voltages and inductor currents are entirely negligible. Voltages are normalized to V_g, while currents are normalized to I_{out}.

In converter α_1, when the transistor switch is turned ON, diode D_1 is turned ON simultaneously, conducting the current $i_{D1} = I_{L2} - I_{L1}$. The average transistor current is equal to DI_{L2}. Since the average transistor current must also be equal to I_{L1}, we have

$$i_{D1} = I_{L2}(1 - D) > 0, \qquad (3)$$

which confirms that diode D_1 is indeed ON. During the transistor ON-time, diodes D_2 and D_3 are OFF. When the transistor is turned OFF, diode D_2 provides a path for current I_{L1}, while diode D_3 provides a path for current I_{L2}. Diode D_1 is OFF. Since the two switched networks in α_1 are electrically identical to the switched networks in a cascade of two buck converters, converter α_1 has the same dc conversion ratio, $M(D) = D^2$.

Converter α_1 can be viewed as a cascade of a passive buck stage (L_1, C_2, D_1, D_2) and an active buck stage (L_2, C_1, T, D_3). Switching of the diodes inside the passive buck is a result
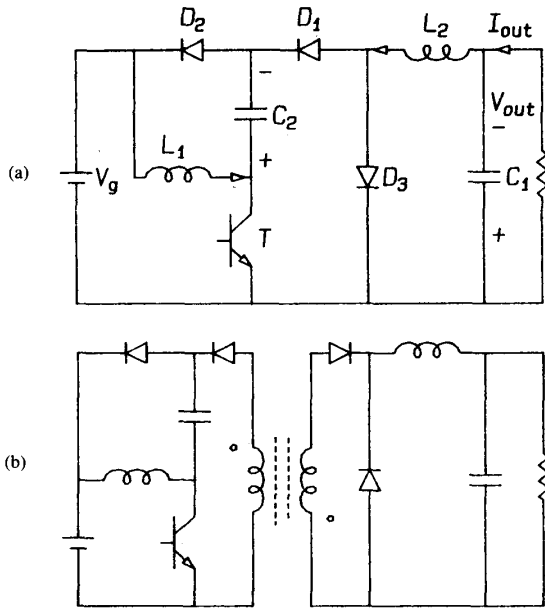
Fig. 4. Converter $\mathcal{B}_1$ with dc conversion ratio $M(D) = -D^2/(1 - D)$ (a); and its version with an isolation transformer (b).
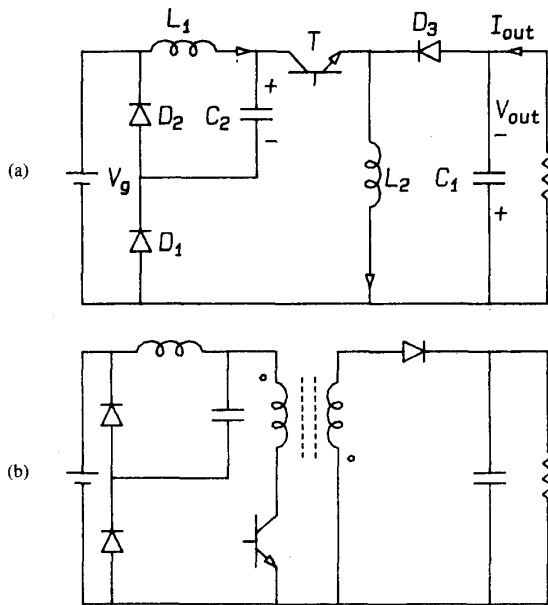

Fig. 5. Converter $\mathcal{B}_2$ with dc conversion ratio $M(D) = -D^2/(1 - D)$ (a); and its version with an isolation transformer (b).

Fig. 6. Converter $\mathcal{B}_3$ with dc conversion ratio $M(D) = -D^2/(1 - D)$.

Fig. 7. Converter $\mathcal{C}_1$ with dc conversion ratio $M(D) = D^2/(1 - D)^2$ (a); and its version with an isolation transformer (b).

of the pulsating input current of the active buck. Thus, if any other PWM converter with a pulsating input current is preceded by the passive buck stage, its dc conversion ratio gets multiplied by D. For example, converter $\mathcal{B}_2$ is a cascade connection of the passive buck and the buck-boost converter. One may also note that the passive buck itself has a pulsating input current. Thus, $n - 1$ passive buck stages can be cascaded in a row with a single active buck, resulting in a single-transistor PWM converter with $M(D) = D^n$.
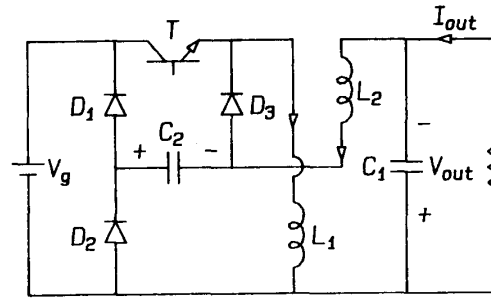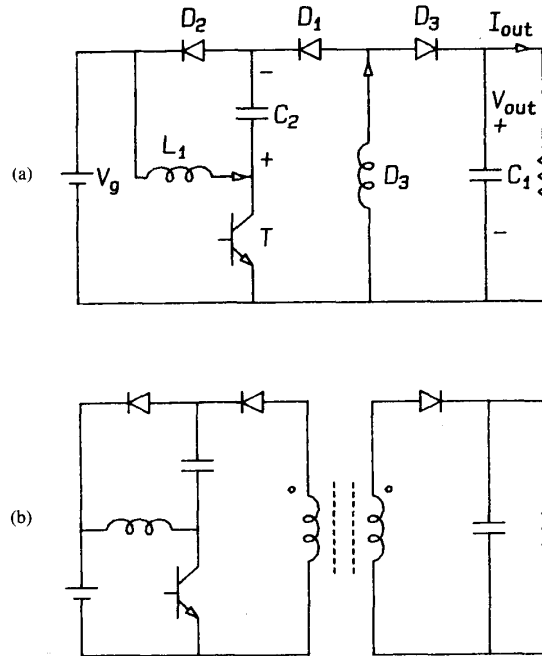
Elementary dc analysis is easily carried out for the remaining five quadratic converters. In all cases, diode D_1 is the diode that is ON during the transistor ON-time. For reference and comparison, average inductor currents, average capacitor voltages and stresses on switching devices are summarized in Table I. Ideal voltage and current stresses (computed under the assumption that ac ripples in capacitor voltages and inductor currents are negligible) should be taken as lower bounds for the actual stresses in practical circuits where the ac ripples may have significant values.

With respect to the parameters in Table I, the two $\mathcal{C}$-converters with $M(D) = D^2$ differ only in current I_{L1}, and the more favorable choice (the one with lower inductor current) depends on the steady-state duty ratio D. Among the $\mathcal{B}$-converters with $M(D) = -D^2/(1 - D)$, converter $\mathcal{B}_1$ has the lowest average inductor currents and switch currents. Consequently, if the same components were used to design the three converters, converter $\mathcal{B}_1$ would have the lowest conduction losses and the lowest stored energy for the same amount of processed power.

TABLE I

	α_1	α_2	β_1	β_2	β_3	C_1
V_{C1}	D^2		$\frac{D^2}{1-D}$			$\frac{D^2}{(1-D)^2}$
V_{C2}	D		$\frac{D}{1-D}$			$\frac{D}{1-D}$
I_{L1}	D	$1-D$	$\frac{D}{1-D}$		$\frac{1}{1-D}$	$\frac{D}{(1-D)^2}$
I_{L2}	1		1	$\frac{1}{1-D}$	1	$\frac{1}{1-D}$
V_T	$1+D$		$\frac{1}{1-D}$			$\frac{1}{1-D}$
I_T	1		$\frac{1}{1-D}$			$\frac{1}{(1-D)^2}$
V_{D1}	1		1			$\frac{1-2D}{(1-D)^2}$
I_{D1}	$1-D$		1			$\frac{1}{1-D}$
V_{D2}	1		$\frac{1}{1-D}$	1		$\frac{1}{1-D}$
I_{D2}	D		$\frac{D}{1-D}$			$\frac{D}{(1-D)^2}$
V_{D3}	D		$\frac{D}{1-D}$			$\frac{D}{(1-D)^3}$
I_{D3}	1		1	$\frac{1}{1-D}$		$\frac{1}{1-D}$

Capacitor dc voltages, inductor dc currents, and voltage/current stresses on switches in the quadratic converters operating in the continuous conduction mode. The stresses are computed assuming that ac ripples in inductor currents and capacitor voltages are negligible. Voltages are normalized to V_g, while currents are normalized to I_{out}.

B. Discontinuous Conduction Modes

In this section, we remove the assumption that ac ripples in inductor currents are negligible, while the assumption that ac ripples in capacitor voltages are relatively small is retained.

In basic single-transistor, single-diode PWM converters (buck, boost, buck-boost Ćuk, etc.), the discontinuous inductor current mode (DICM) occurs when the diode current drops to zero before the end of the transistor OFF-time. In a cascade of basic PWM converters, a DICM can be associated with each diode [5], but the same qualitative description holds—the diode turns OFF before the transistor is turned ON. In the quadratic converters, there exists a diode that conducts during the transistor on-time, so that the notion of DICM needs a slight generalization. An operating mode of a PWM converter will be called discontinuous if switching (turn-ON or turn-OFF) of a diode is not synchronous with switching (turn-ON or turn-OFF) of the transistor.

In every DICM, the conversion ratio is a function of duty ratio D and load current I_{out}. For the same duty ratio D, the conversion ratio in DICM is higher than the conversion ratio in CCM. Thus, a transition from CCM to DICM tends to increase the minimum attainable conversion ratio and therefore, to decrease the attainable range of conversion ratios. Hence, for a proper design of quadratic converters, it is important to determine the conditions for operation in the continuous conduction mode.

Define parameters k_1 and k_2 by

$$k_1 \equiv \frac{2L_1 f_s}{R}, \qquad k_2 \equiv \frac{2L_2 f_s}{R}, \tag{4}$$

where R is the load resistance at dc,

$$R \equiv V_{out}/I_{out}. \tag{5}$$

and f_s is the switching frequency. Consider, as an example, converter α_1 in Fig. 2(a). Familiar discontinuous modes can be associated with diodes D_2 and D_3. When the transistor is OFF, diode D_3 constructs current i_{L2}. The diode current decays linearly and reaches its minimum at the end of the transistor-OFF time. For operation in CCM, the minimum should be positive, i.e.,

$$I_{L2} - \frac{\Delta I_{L2}}{2} > 0, \tag{6}$$

where I_{L2} and ΔI_{L2} denote the average and the peak-to-peak ripple of the inductor L_2 current. After evaluating the average current and the ripple current in terms of V_g, R, L_2 and f_s, we obtain

$$k_2 > 1 - D. \tag{7}$$

TABLE II

$\mathcal{Q}_1$:	$k_1 > \frac{1-D}{D^2}$ (D_2), $\quad k_2 > 1 - D$ (D_3), $\quad \left| \frac{1}{k_2} - \frac{1}{Dk_1} \right| < 1$ (D_1).
$\mathcal{Q}_2$:	$k_1 > \frac{1}{D}$ (D_1), $\quad \left(\frac{1-D}{D^2} \frac{1}{k_1} + \frac{1-D^2}{D^2} \frac{1}{k_2} \right) < 1$ (D_2).
$\mathcal{B}_1$:	$k_1 > \frac{(1-D)^2}{D^2}$ (D_2), $\quad k_2 > 1 - D$ (D_3).
$\mathcal{B}_2$:	$k_1 > \frac{(1-D)^3}{D^2}$ (D_2), $\quad k_2 > (1 - D)^2$ (D_3), $\quad \left| \frac{1-D}{k_2} - \frac{(1-D)^2}{D} \frac{1}{k_1} \right| < 1$ (D_1).
$\mathcal{B}_3$:	$k_2 > \frac{(1-D)^2}{D}$ (D_1), $\quad \left(\frac{(1-D)^2}{D^2} \frac{1}{k_1} + \frac{(1-D)^3}{D^2} \frac{1}{k_2} \right) < 1$ (D_2).
$\mathcal{C}_1$:	$k_1 > \frac{(1-D)^4}{D^2}$ (D_2), $\quad k_2 > (1 - D)^2$ (D_3), $\quad D < 0.5$ (D_1).

Conditions for operation in the continuous conduction mode for the six quadratic converters. For each boundary condition, the diode responsible for the condition is indicated in brackets.

In fact, this is the CCM/DICM boundary condition for the buck converter [4]. A similar analysis for diode D_2 yields

$$k_1 > \frac{1 - D}{D^2}. \tag{8}$$

Again, this condition can be interpreted as the well-known condition for the simple buck converter, except that load R is reflected to the input stage by the square of the output-stage conversion ratio D.

Let us now examine the discontinuous mode associated with diode D_1. When the diode is ON, its current i_{D1} is equal to $i_{L2} - i_{L1}$, and the condition for operation in CCM is that

$$i_{L2} > i_{L1} \tag{9}$$

throughout the transistor ON-time. Since both i_{L2} and i_{L1} are linearly increasing during the transistor ON-time, this condition is equivalent to the following two inequalities:

$$I_{L2} - \frac{\Delta I_{L2}}{2} > I_{L1} - \frac{\Delta I_{L1}}{2}, \tag{10}$$

$$I_{L2} + \frac{\Delta I_{L2}}{2} > I_{L1} + \frac{\Delta I_{L1}}{2}. \tag{11}$$

The first inequality requires that the diode current is positive at the transistor ON-time, while the second inequality imposes the same condition at the end of the transistor ON-time. In terms of parameters k_1 and k_2, conditions (10) and (11) become

$$\left| \frac{1}{k_2} - \frac{1}{Dk_1} \right| < 1. \tag{12}$$

Analysis of boundary conditions for operation in CCM is carried out for all six quadratic converters. The results are summarized in Table II. Note that the conditions can be vastly different even for the converters that share the same conversion ratio in CCM.

Consider, for example, converters $\mathcal{Q}_1$ and $\mathcal{Q}_2$. Assume that operating conditions are the same and that the duty ratio is set to $D = 0.5$, so that all average inductor currents are the same. We want to examine in which converter lower conductances are necessary for operation in CCM. For $\mathcal{Q}_1$, the boundary condi-

tions become

$$k_1 > 2, \tag{13}$$

$$k_2 > 2, \tag{14}$$

$$\left| \frac{1}{k_2} - \frac{2}{k_1} \right| < 1. \tag{15}$$

The minimum energy storage or, equivalently, the minimum inductances are required if the sum $k_1 + k_2$ is minimized under the boundary conditions. The solution $k_1 = 2, k_2 = 2$ yields

$$\min (k_1 + k_2) = 4, \quad \text{for } \mathcal{Q}_1. \tag{16}$$

For $\mathcal{Q}_2$, the boundary conditions become

$$k_1 > 2, \tag{17}$$

$$\frac{2}{k_1} + \frac{3}{k_2} < 1, \tag{18}$$

and the solution $k_1 = 4.45, k_2 = 5.45$, results in

$$\min (k_1 + k_2) = 9.9, \quad \text{for } \mathcal{Q}_2. \tag{19}$$

Thus, in this example, more than two times larger inductances are necessary in converter $\mathcal{Q}_2$ than in converter $\mathcal{Q}_1$. Using the results of Tables I and II, a similar comparative analysis can be carried out for any particular design example.
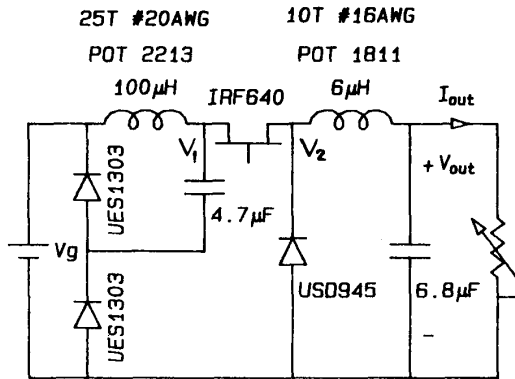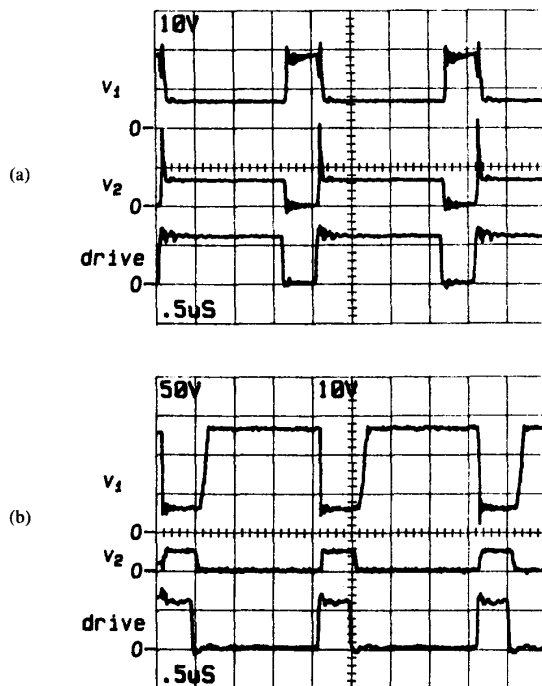
IV. AN EXPERIMENTAL $\mathcal{Q}_1$-CONVERTER

Topology $\mathcal{Q}_1$ in Fig. 2(a) is used to design a practical 500-kHz converter according to the following specifications:

- Input voltage: $10 \text{ V} < V_g < 100 \text{ V}$;
- Output voltage: $V_{\text{out}} = 5 \text{ V}$;
- Load: $1 \text{ A} < I_{\text{out}} < 4 \text{ A}$.

The power stage of the converter is shown in Fig. 8. Inductor values are chosen so that the converter operates in the continuous conduction mode under all operating conditions. For the minimum output current, $R = 5 \Omega$, $k_1 = 20$ and $k_2 = 1.2$. It is easy to verify that all CCM/DICM boundary conditions are satisfied for the worst-case operating condition

$$(I_{\text{out}})_{\text{min}} = 1 \text{ A}, \quad D_{\text{min}} = \sqrt{\frac{V_{\text{out}}}{(V_g)_{\text{max}}}} = 0.2. \tag{20}$$

Fig. 8. An experimental α_1-converter.

Fig. 9. Waveforms in experimental α_1-converter: (a) for the minimum input voltage ($V_g = 10$ V) and the maximum output current ($I_{out} = 4$ A); (b) for maximum input voltage ($V_g = 100$ V) and minimum output current ($I_{out} = 1$ A).

Waveforms recorded for extreme values of the input voltage and the load current are shown in Fig. 9. In spite of the extremely large variations in the input voltage, duty ratio of the transistor switch varies from $D_{min} = 0.2$ to $D_{max} = 0.8$, safely within the limits imposed by the speed of the transistor and its drive circuitry. There is also enough room left for dynamic variations of the duty ratio during the input-voltage or the output-current transients. Measured efficiency as a function of the input voltage with the output current as a varying parameter is shown in Fig. 10. For the low-end input voltage the efficiency exceeds 80% for all loads and it gradually decays as the input voltage is increased. Switching losses that result from the switch voltage/current overlaps during the switching transitions are
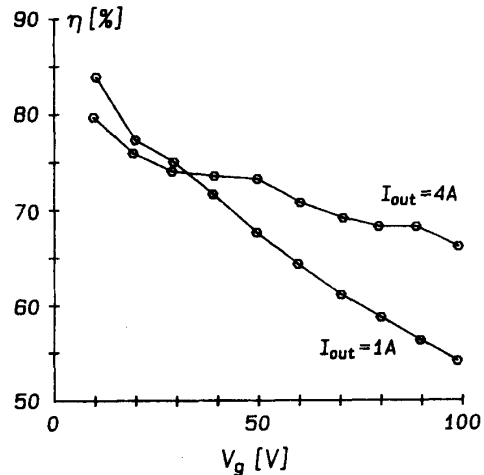
Fig. 10. Efficiency of experimental α_1-converter as a function of input voltage V_g, with output current I_{out} as varying parameter.
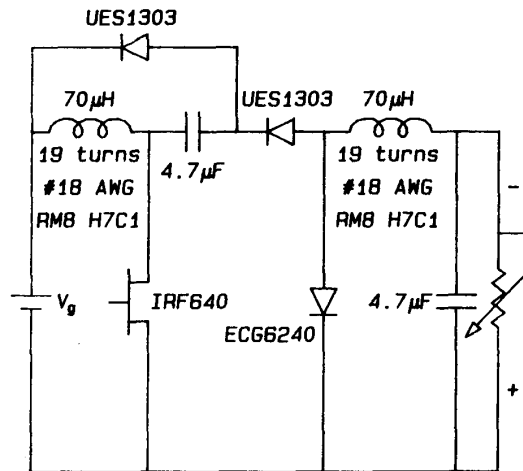
Fig. 11. An experimental $\mathcal{B}_1$-converter.

proportional to the voltage level. Also, the power lost because of the parasitic capacitances of the semiconductor switches is roughly proportional to the square of the voltage level. This explains why the efficiency decreases with the input voltage. The full-load efficiency goes from 80% at $V_g = 10$ V to 66% at $V_g = 100$ V.

V. AN EXPERIMENTAL $\mathcal{B}_1$-CONVERTER

Topology $\mathcal{B}_1$ shown in Fig. 4(a) is used to design a 500-kHz converter for a laboratory power supply application according to the following specifications:

- Input voltage: $V_g = 50$ V $\pm$ 20%;
- Output voltage: 1 V < V_{out} < 60 V;
- Load: $I_{out} \leq 1$ A.

The power stage of the converter is shown in Fig. 11. With the selected values of inductors, the full range of output voltages is accessible with the minimum duty ratio $D_{min} = 0.1$. The minimum output load required for the full output-voltage range is less than 1 W.
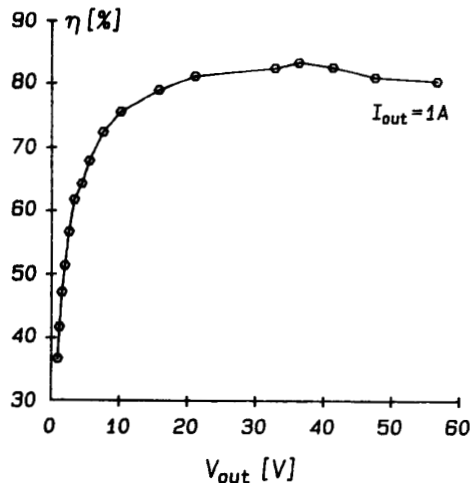
Fig. 12. Efficiency of experimental $\mathcal{B}_1$-converter as function of output voltage.

For the maximum output current, $I_{out} = 1$ A, and the nominal input voltage, $V_g = 50$ V, measured efficiency as a function of the output voltage is shown in Fig. 12. The efficiency exceeds 80% for output voltages greater than 18 V. As expected, the efficiency collapses for very low output voltages because of the conduction losses caused by the inevitable voltage drop of the semiconductor switches.

VI. CONCLUSION

Compared to basic converter topologies (buck, boost, buck-boost, Ćuk etc.), PWM converters with quadratic dc conversion ratios, $M(D) = D^2$, $M(D) = D^2/(1 - D)$ or $M(D) = D^2/(1 - D)^2$, offer a significantly wider conversion range. For a given minimum ON-time and, consequently, for a given minimum duty ratio D_{min}, D^2 in the numerator of $M(D)$ yields a much lower limit on the minimum attainable conversion ratio.

By applying a systematic synthesis procedure, six novel single-transistor converter configurations with quadratic dc conversion ratios are found. The simpler, single-transistor realization is the most important advantage over the straightforward cascade of two basic converters.

As far as conversion efficiency is concerned, it is quite clear that a single-stage converter is always a better choice than a two-stage converter. Therefore, the quadratic converters are proposed and intended for applications where conventional, single-stage converters are inadequate—for high-frequency applications where the specified range of input voltages and the specified range of output voltages call for an extremely large range of conversion ratios.

Following a discussion of basic properties of the quadratic converters in the continuous and the discontinuous modes, two illustrative experimental examples are included: a 20-W, 5-V-output converter supplied from a highly unregulated line voltage (10 V $< V_g < 100$ V), and a 60-W 1-V-to-60-V-output converter for a laboratory power supply. Although in both cases the step-down of more than 20 to 1 is required, the quadratic converters can operate at a relatively high switching frequency (500 kHz) because the minimum ON-time limitation is much less restrictive.

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