Switching Performance Improvement of IGBT Modules Using an Active Gate Driver

Zhiqiang Wang, Xiaojie Shi, Leon M. Tolbert, Benjamin J. Blalock
Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT)
Department of Electrical Engineering and Computer Science
The University of Tennessee
Knoxville, TN 37996-2250, USA
zwang38@utk.edu

***Abstract* —This paper addresses the issues of switching behavior of a high power insulated gate bipolar transistor (IGBT) that works in hard switching conditions. First, the voltage and current switching waveforms of IGBT modules are described for an IGBT phase-leg module with an inductive load, and the associated switching losses, reverse recovery current of free-wheeling diodes, voltage overshoot, and EMI noise are analyzed. Based on the analysis, an actively controlled gate drive circuit is proposed, which provides optimization of the fast driving for low switching losses and short switching time, and slow driving for low noise and switching stress. Compared to a conventional gate drive strategy, the proposed active gate driver (AGD) has the capability of reducing the switching losses, delay time, and Miller plateau duration effectively during both turn-on and turn-off transient. Experimental results verify the validity and effectiveness of the proposed gate driving method.**

I. INTRODUCTION

Efficiency is one of the most important issues among high power converters where IGBTs are widely used, and the gate drive circuit serving as the interface between the IGBT power switches and the logic-level signals can be optimized to achieve low losses. Conventional gate driver (CGD) circuits have employed fixed gate voltage and resistor networks, which are selected to minimize switching losses, suppress cross-talk and EMI noise, and also limit the power device stresses at switching transients. However, these conflicting requirements are difficult to be realized in a conventional gate driver.

Some work has been done on this topic during the last decade to reduce the switching losses by actively controlling the gate drive signals. A gate drive circuit for IGBTs with a snubber circuit was proposed in [1]. This circuit utilizes the recycled energy from the snubber circuit to drive the IGBT and cannot be directly applied to the hard-switched IGBTs. A multi-stage gate drive control concept has been proposed in [2] to realize optimal turn-on and turn-off performance. The switching delay and switching losses are effectively reduced using large gate current, and the current rising/falling rate are limited using small gate current. The main issues of this method are control complexity for accurate detection of the instances for changes in driving modes, and poor adaptivity to different IGBTs, even different current/voltage levels, due to fixed or predetermined control instants for certain switching stages. A gate driver based on the Miller's plateau detection by a phase-locked loop (PLL) was analyzed and proposed in [3-5]. This technique is able to reduce switching loss by injecting an additional gate current, while it can result in poor operation under transient load current conditions, and the inherent one switching period delay of the updated control instructions impairs the overall effectiveness. A sensorless gate driver with feedforward control of the turn-on dynamics to reduce switching losses is described in [6-7]. The gate signal reference was obtained from a shape generator composed primarily by a lightly dampened second-order filter which is difficult to be tuned. Also, the turn-off performance optimization is not considered, and turn-on delay is still quite large due to the intentionally designed low slew rate of the gate references.

Recently, there have been several research efforts on improving the switching performances using a digital approach [8-10]. These techniques could provide optimization between minimization of switching losses, reverse recovery current, and the collector emitter turn-off over-voltage by controlling the gate current in accordance with the desired switching operation. The main drawbacks associated with the digital method is the large delay times of the D/A and A/D conversion in the signal paths, as well as considerable cost for the high performance digital controller.

Other references focusing either on closed-loop/open-loop regulation of the collector current slope or collector emitter voltage slope was proposed and analyzed in [11-15]. Such techniques provided full *di/dt* or *dv/dt* control capability but sacrificed more or less switching losses during switching transients.

In this paper, a new gate drive circuit is proposed to reduce the switching delay time and switching loss under hard switching conditions. The proposed method can adaptively adjust the control parameters automatically regardless of different IGBTs, current and voltage levels. The fast response of the active gate driver further guarantees the control accuracy under different power levels. Experimental results verify the validity and effectiveness of the proposed gate driving method.

II. PROPOSED ACTIVE GATE DRIVE CIRCUIT

The proposed gate drive circuit (comprised of a turn-on and a turn-off section) based on *di/dt* feedback control focuses on reducing the switching loss, delay, and total switching time, while maintaining the switching stress and EMI noise level during both turn-on and turn-off transients.

A. Turn-on Active Gate Driver

The block diagram of the turn-on active gate driver is shown in Fig. 1. In addition to a conventional totem pole gate drive

structure, the proposed active gate driver is mainly composed of five parts: *di/dt* sensing, logic circuit, level shifter, source follower, and gate charger. The functionality of each part is described as follows.

The *di/dt* sensing network is used to detect the different turn-on phases. The feedback control signal is obtained using the measurement of voltage across the parasitic inductance L_{Ee} between the Kelvin emitter and power emitter of an IGBT module. This is a pragmatic choice since using a current sensor would make the circuit more complicated and expensive.

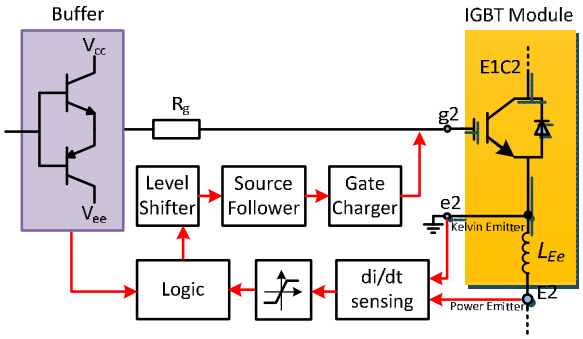


Fig. 1. Block diagram of the proposed AGD for turn-on.

The logic circuit powered by the negative gate drive supply V_{ee} receives both the feedback signal and the turn-on command to guarantee the circuit works properly at different stages. The circuit operation will explained below. Given that both signals may be out of the normal input voltage range of the logic circuit at high *di/dt* and large parasitic inductance L_{Ee}, a clamping circuit is employed to protect the logic circuits.

An open drain level shifter serves as an interface between the logic and source follower. The level shifter serves two purposes in this implementation: 1) it inverts the logic output, and 2) it references the logic output signal to the positive rail of the buffer. During operation of the level shifter, a small DC current flows in the level shifter keeping the source follower and gate charger biased in the correct state. Both the gate drive power and the level shift current are provided by a dc-dc power supply chip.

The source follower receives the logic signal from the level shifter, and activates/deactivates the gate charger. Another key function is that it reduces the resistive loss of the level shifter, as will be explained later.

The gate charger driven by the source follower injects an additional current into the gate at certain stages to minimize the turn-on delay time and switching losses. It also decouples the turn-on active gate driver from the conventional gate driver, as well as the turn-off active gate driver.

Fig. 2 illustrates the circuit implementation of the turn-on active gate driver. When the turn-on command V_{in} is applied at the turn-on delay stage, the voltage across parasitic inductance L_{Ee} is zero since no current is flowing through the IGBT. At this instant, the output of the AND logic gate is high, which activates the level shifter's small-signal MOSFET M_1, and subsequently the source follower MOSFET M_3 and gate charger MOSFET M_2 are turned on. Hence, the IGBT gate emitter capacitance C_{ge} is now charged by the conventional gate current i_{g1} together with an additional current i_{g2}.

The delay time can be significantly reduced by adjusting the control gate resistor R_x. However, the resistance should not be too small to prevent possible gate loop oscillation. The resistance is selected for reasonable damping and low gate loop equivalent resistance, i.e.

$$2\xi\sqrt{\frac{L_G}{C_{ge}}} < R_x < R_g \tag{1}$$

where, ξ is the damping factor (usually around 0.707).

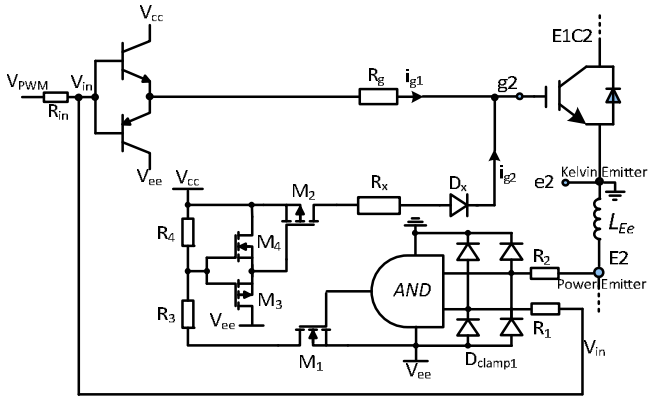


Fig. 2. Circuit implementation of the proposed AGD for turn-on.

The gate is continuously charged until the gate voltage hits the threshold V_{th} and the IGBT starts to conduct current. The collector current is increased with a rate of di_c/dt defined by (2)

$$\frac{di_c}{dt} = \frac{V_{cc} - v_{ge}}{R_g C_{ies} / g_m} \tag{2}$$

where g_m and C_{ies} (=C_{ge}+C_{gc}) are the transfer conductance and the input capacitance of the IGBT, and L_{Ee} represents the parasitic inductance between power and Kelvin emitters.

Accordingly, the negative voltage drop across parasitic inductance L_{Ee} is induced, given by

$$-L_{Ee}\frac{di_c}{dt} < V_{IL\max} \tag{3}$$

where $V_{IL\max}$ is the maximum allowable low-level input voltage of the AND logic circuit. The output of the AND logic circuit is flipped to low level close to V_{ee}. This low level output deactivates the M_1 of the level shifter, and consequently M_3 and M_2 are turned off, while M_4 is turned on.

The IGBT gate capacitance C_{ge} is only charged by the conventional gate current i_{g1}, which means the di_c/dt, peak reverse recovery current, and the corresponding EMI noise level stay the same as the conventional gate drive circuit. The energy loss during the current rising stage is also not changed.

The turn-on and turn-off speed of M_2 depend on R_3 and R_4, respectively. To have fast switching speed of M_2, the resistance of R_3 and R_4 should be small. However, the resistive loss of the level shift is increased. The total loss of the auxiliary circuit P_s can be estimated by

$$P_s = Q_2 \cdot V_{cc} \cdot f_s + \frac{V_{cc}^2 \cdot D_{logic}}{R_3 + R_4} \tag{4}$$

where Q_2 is the gate charge of M_2, f_s is the switching frequency, and D_{logic} is the duty cycle of the logic circuit's output signal. The first term represents the driving loss of M_2, which is much smaller than the resistive loss, as shown in the second term. The source follower is an integral part in accelerating the switching speed of M_2 under the large resistance of R_3 and R_4. The source follower effectively decouples M_2's gate capacitance from the level shifter resistors. M_3 and M_4 are selected based on (5) to guarantee fast switching of M_2,

$$C_{iss3} \approx C_{iss4} = \left(\frac{1}{5} \sim \frac{1}{10}\right) \cdot C_{iss2} \tag{5}$$

where C_{iss2}, C_{iss3}, and C_{iss4} represent the input capacitance of M_2, M_3 and M_4, respectively.

At the end of current rising stage, the reverse recovery current of the free-wheeling diode (FWD) decays from peak value back to zero. The FWD stops conducting and starts to block voltage. Meanwhile, the collector current flowing through the sensing inductance L_{E2} no longer changes. The output of the logic circuit is flipped back to a logic high level, and the gate charger is activated again. Higher gate current discharges the collector capacitor more rapidly. As a result, the duration of the Miller's plateau and the collector-emitter voltage tail are reduced. The second part of the total turn-on energy losses due to the tail voltage is considerably reduced.

The gate charger continuously injects current into the gate until the turn-off command is received by the logic circuit. The large gate current speeds up the gate voltage rising to the steady-state value V_{cc}, and minimizes the third part of turn-on switching losses. This ensures that the IGBT will spend less time in the active region while transitioning to the ohmic region. Hence, the total turn-on switching time and loss are reduced.

In the design of the proposed AGD, the dynamic and steady state behavior of the small signal transistors and the diodes should be taken into account. To realize a minimum control delay (below 50 ns) and high control accuracy, all of the active devices and logic gates should be selected to have small switching and propagation delay times. In addition, the on-state resistance $R_{ds(on)}$ of the transistor M_2 and the on-resistance of decoupling diode D_x should also be low for proper operation.

B. Turn-off Active Gate Driver

The block diagram of the turn-off active gate driver is shown in Fig. 3. It is mainly composed by four function blocks: di/dt sensing, logic circuit, level shifter, and gate discharger. The functionality of each part is similar to turn-on AGD except that the gate discharger is controlled to remove current from gate capacitance during certain period of turn-off transient.

Fig. 4 illustrates the circuit implementation of the turn-off active gate driver. When the turn-off command V_{in} is applied to the AGD, the voltage across parasitic inductance L_{Ee} stays zero during both turn-off delay stage and voltage rising stage since no current is flowing through the IGBT. The output of the NOR logic gate is high, which activates the paralleled level shifter small-signal MOSFETs, and the gate discharger. The IGBT gate-emitter capacitance is then effectively discharged by the conventional gate current i_{g1} together with an additional current i_{g3}. The higher total gate current charges the Miller capacitor more rapidly, and thus results in a shorter voltage tail duration and lower turn-off switching loss.

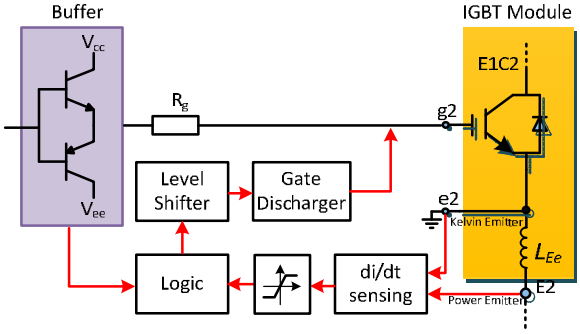


Fig. 3. Block diagram of the proposed AGD for turn-off.

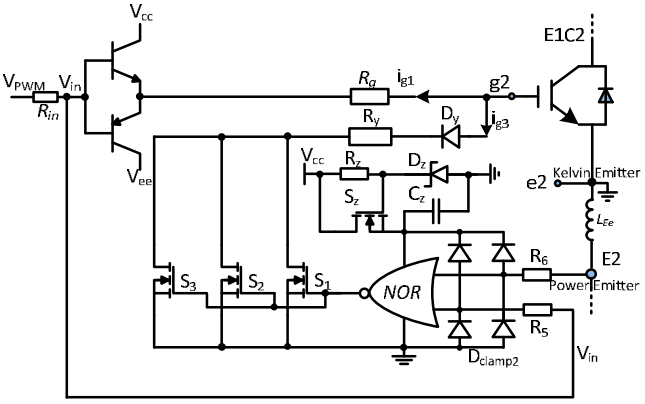


Fig. 4. Circuit implementation of the proposed AGD for turn-off.

Similar to the logic circuit of the turn-on active gate driver, the turn-off logic circuit receives not only the switching command V_{in} but also the power supply from the buffer. The difference is that the former one is powered by the negative power supply V_{ee}, while the latter is powered by a positive voltage, due to the reverse polarity of voltage across L_{Ee} during turn-on and turn-off transient. A source follower (R_z, C_z , S_z and D_z) based voltage regulator is used to supply the logic circuit.

The level shifter and gate discharger share the same group of small-signal transistors (S1, S2 and S3) paralleled with each other to enhance the sinking current from the gate. The design principle of the turn-off control gate resistor R_y is the same as that of the turn-on, as shown in (1).

During the current falling stage, the collector current is decreased with a rate of di_c/dt defined by (6).

$$\frac{di_c}{dt} = \frac{V_{ee} - v_{ge}}{R_g C_{ies} / g_m}. \tag{6}$$

A positive voltage drop across parasitic inductance L_{Ee} is induced accordingly. When there is

$$-L_{Ee}\frac{di_c}{dt} > V_{IH\min} \tag{7}$$

where $V_{IH\min}$ is the minimum high-level input voltage of the NOR logic gate, the output of the gate is flipped to a logic low

level. This low level output deactivates the level shifter and the gate discharger by turning S_1, S_2, and S_3 off. The gate is only discharged through the CGD. Therefore, the second part of turn-off switching loss, and voltage spike induced by power loop parasitic inductance are the same as that for a CGD.

As soon as the device enters into the current tail stage, the gate discharger is activated again to speed up the gate voltage to its final value, V_{ee}. The switching loss, however, caused by the tail current is not affected.

From the above analysis, several features of the active gate driver can be observed. 1) The operation process is independent of current/voltage levels, as well as IGBT types with some variation of parasitic inductance L_{Ee}. 2) Both the turn-on and turn-off AGD share the same power supply as the buffer. 3) They work in complementary mode due to the control of command V_{in} without interrupting each other. 4) High bandwidth detection and regulation circuits, e.g. current/voltage sensors, operational amplifier, etc. are avoided, which facilitates the potential integration into a gate drive chip [16].

III. Experimental Verification

Experimental results are presented for an IGBT module using both the CGD and AGD. The test set up is based on a double pulse tester illustrated in Fig. 5, which represents one phase leg of a three phase inverter with an inductive load.

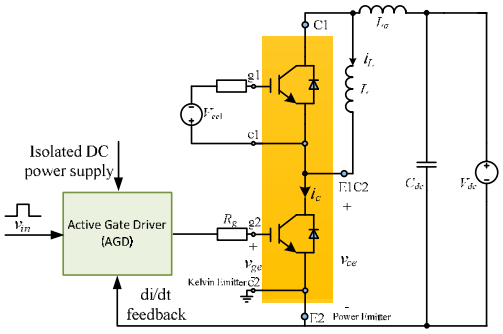


Fig. 5. Experimental test setup.

The device used for the experimental test is a 600 V, 400 A Powerex IGBT module (CM400DY-12NF). The experimental waveforms are recorded by a Tektronix DPO5204 2 GHz 4 channel Digital Phospher Oscilloscope. The voltage was measured with a calibrated active high voltage probe Tektronix P5205, with sufficient bandwidth of 100 MHz. The collector current was measured using a T&M RESEARCH SSDN-015 coaxial shunt with resistance of 0.015 Ω and high bandwidth of 1.2 GHz. The switching energy loss is calculated by the math function of the oscilloscope.

The experimental test bed is shown in Fig. 6. The IGBT module and DC capacitor bank are connected by an internal planar busbar structure within the PCB board. The turn-on and turn-off AGD are integrated together with an advanced overcurrent protection board (discussed in [17]).

A. Turn-on Performance Improvement Verification

Comparison of the turn-on switching waveforms at 300 V DC bus voltage and 200 A load current with 10 Ω gate resistance is shown in Fig. 7 (a) and (b), respectively.

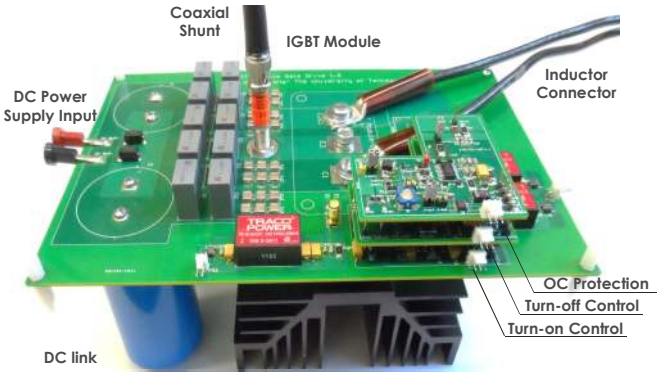
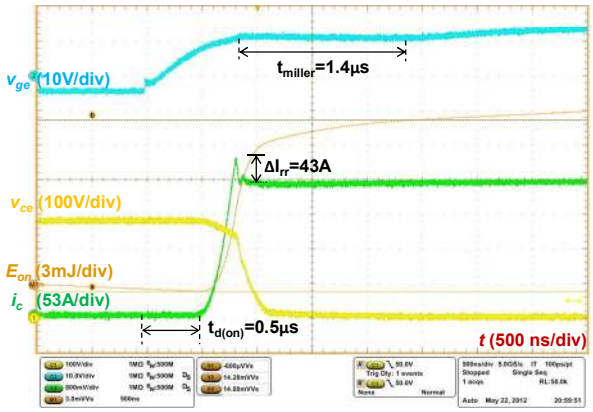
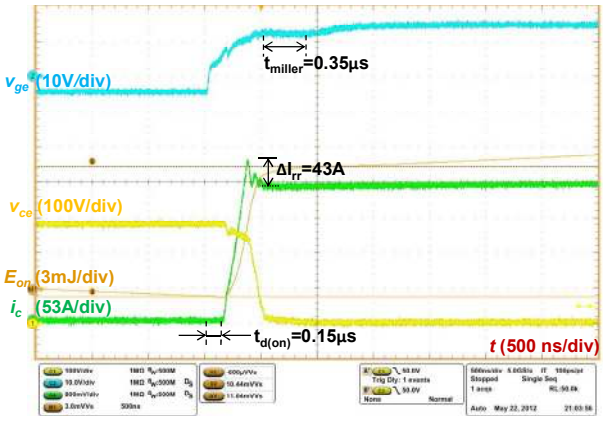


Fig. 6. Experimental testbed for the AGD verification.



(a) Conventional gate driver

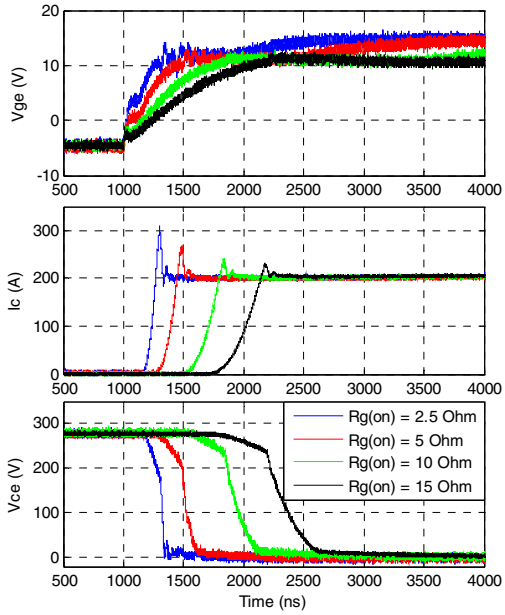


(b) Active gate driver

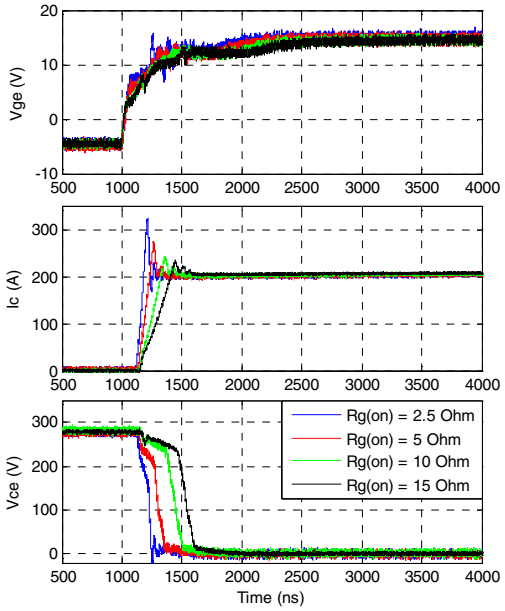
Fig. 7. Comparison of turn-on waveforms with different gate drivers.

The waveforms plotted from top to bottom are the gate voltage, collector emitter voltage, turn-on energy loss, and collector current. With the conventional gate drive, the turn-on delay is around 0.5 μs, while it is reduced to around 0.15 μs when the active gate driver is used. The reverse-recovery current of both cases are kept at the same value (43 A). The Miller plateau time is reduced from 1.4 μs with CGD to 0.35 μs with AGD, which leads to a shorter voltage tail and turn-on energy loss decrease from 14.9 mJ to11.0 mJ.

Different turn-on gate resistors (2.5 Ω, 5 Ω, 10 Ω, 15 Ω) are used under a constant load current of 200 A and DC bus voltage of 300 V are also tested. The results are imported into MATLAB and compared, as shown in Fig. 8 (a) and (b).



(a) Conventional gate driver



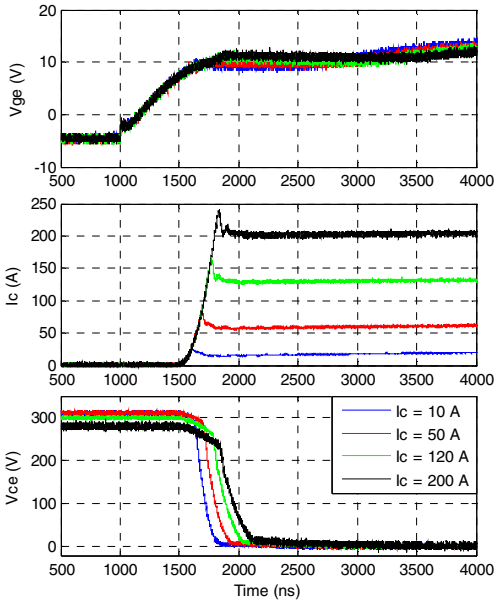
(b) Active gate driver

Fig. 8. Comparison of turn-on waveforms with different gate resistors using CGD and AGD.

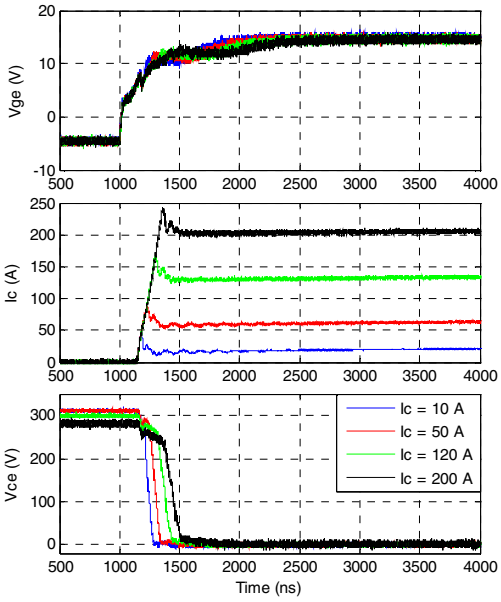
Experimental waveforms are also measured under different current levels (10 A, 50 A, 120 A, 200 A), with a gate resistor of 10 Ω and DC bus voltage of 300 V for both the CGD and proposed AGD. The results are imported into MATLAB and compared, as shown in Fig. 9 (a) and (b).

Based on the above experimental results, the turn-on energy loss, delay time, peak reverse-recovery current, and Miller plateau duration as functions of the gate resistance R_g and current level I_c are plotted for both gate drive circuits under 300 V DC bus voltage, as shown in Fig. 10 (a) to (d), respectively.

As the turn-on gate resistor is increased, the delay time and the dissipated turn-on energy increases monotonically, while the peak reverse-recovery current decreases. The delay time of the proposed AGD circuit only changes from 100 ns to 150 ns, even shorter than that of a CGD with gate resistance of 2.5 Ω. The reverse recovery current peak values are nearly the same. The switching energy is reduced by 20% to 35% in the plotted gate resistor and current level range, and the turn-on delay is reduced by 50% to 80%. The Miller plateau duration, which represents a significant part of total turn-on switching time, is reduced by 30% to 80% in the plotted range. Moreover, there is a trend that more switching time and energy loss are saved with larger gate resistance and higher current levels.



(a) Conventional gate driver

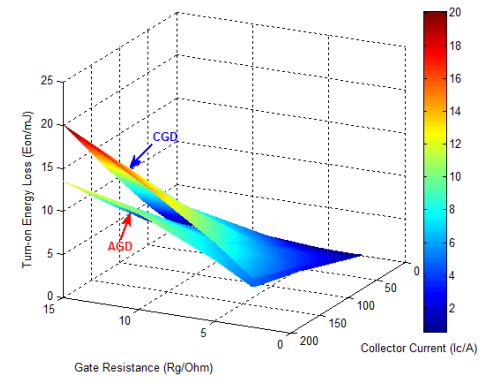


(b) Active gate driver

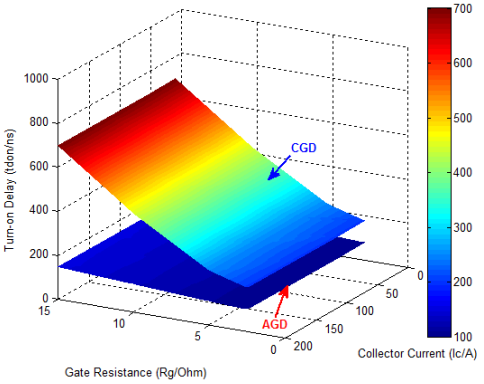
Fig. 9. Comparison of turn-on waveforms with different current levels using CGD and AGD.

B. Turn-off Performance Improvement Verification

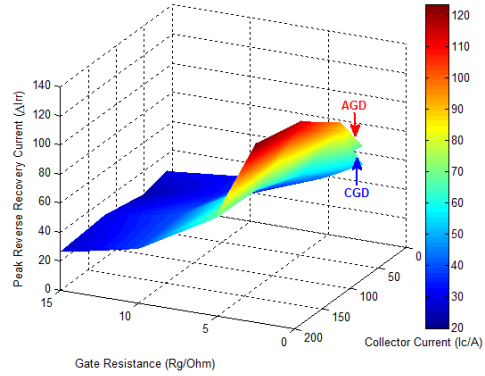
The turn-off experimental results with the same power module and test conditions as turn-on are obtained. Comparison of the



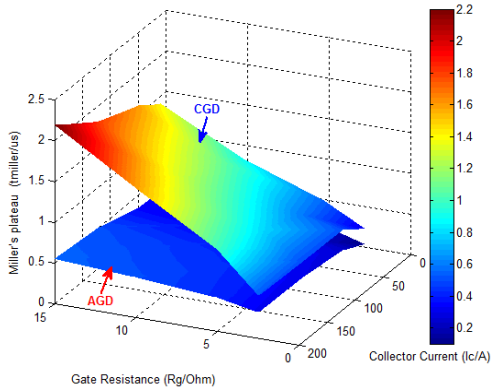
(a) Turn-on energy loss



(b) Turn-on delay



(c) Turn-on reverse recovery current peak

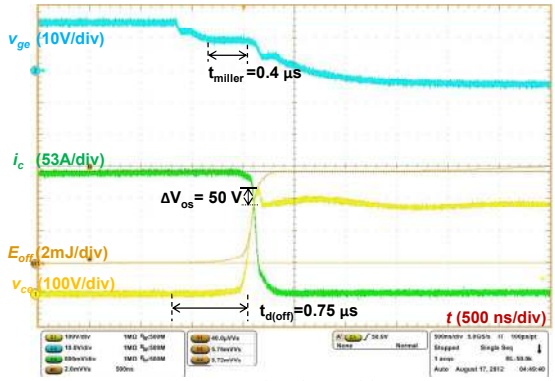


(d) Turn-on Miller plateau duration

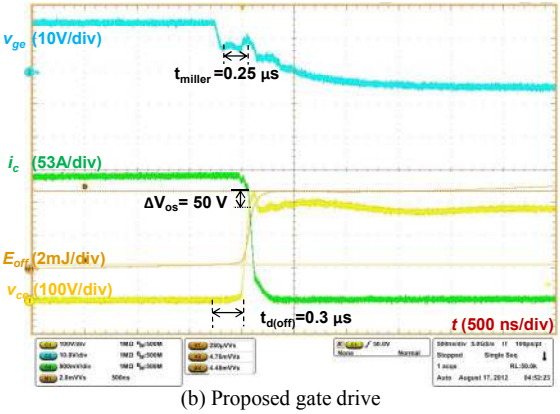
Fig. 10. Comparison of the two gate drivers under different current levels and gate resistances.

turn-off switching waveforms at 300 V DC bus voltage, and 200 A load current with 10 Ω gate resistance is shown in Fig. 11 (a) and (b), respectively.

The proposed AGD circuit reduces the turn-off delay time from 0.75 µs to 0.3 µs, and turn-off switching energy loss from 5.72 mJ to 4.48 mJ, while keeping the same turn-off overvoltage (50 V) as that of using the CGD. The Miller plateau time is reduced from 0.4 µs to 0.25 µs, which contributes to the contraction of voltage tail and turn-off energy loss.

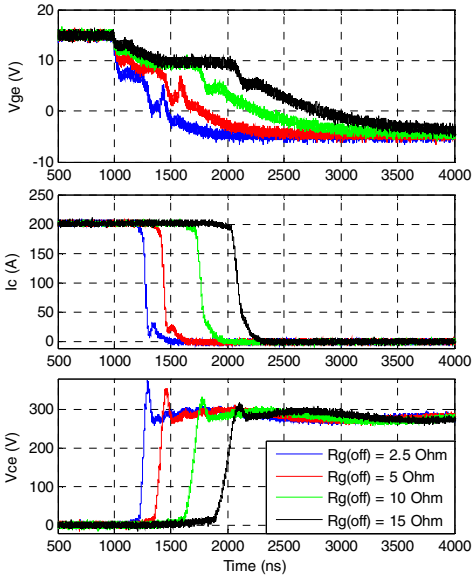


(a) Conventional gate drive

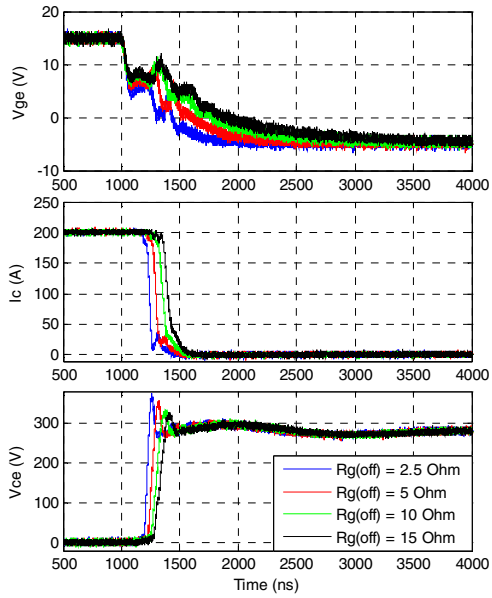


(b) Proposed gate drive

Fig. 11. Comparison of turn-on waveforms for the two methods.

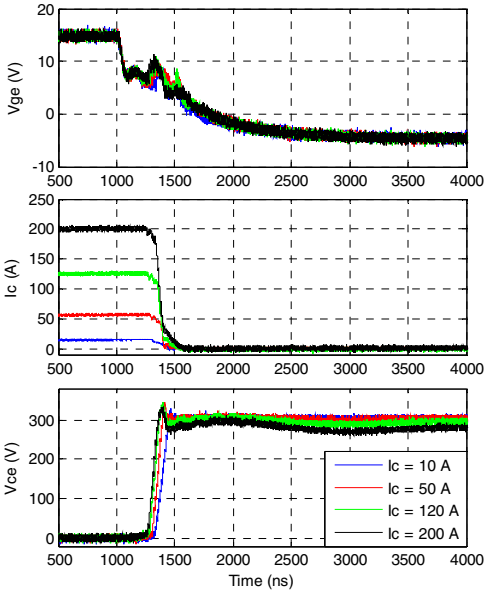


(a) Conventional gate driver



(b) Active gate driver

Fig. 12. Comparison of turn-off waveforms with different gate resistors using CGD and AGD.



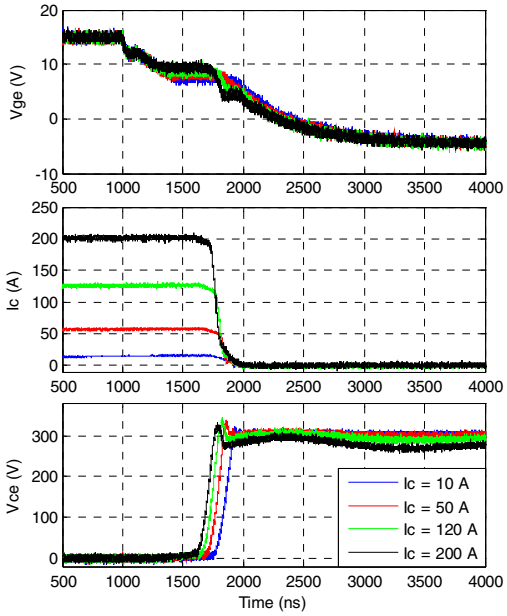
(b) Active gate driver

Fig. 13. Comparison of turn-off waveforms with different current levels using CGD and AGD.

Different turn-off gate resistors (2.5 Ω, 5 Ω, 10 Ω, 15 Ω) are used under a constant load current of 200 A and DC bus voltage of 300 V for both the CGD and proposed AGD to compare their switching characteristics, as shown in Fig. 12 (a) and (b).

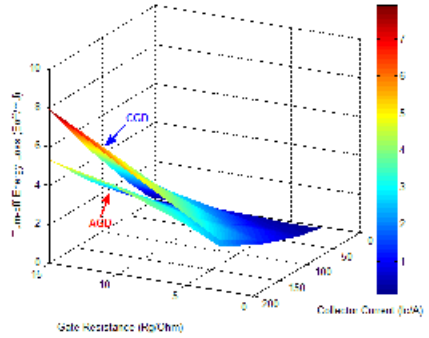
Turn-off experimental waveforms are also measured and compared under different current levels (10 A, 50 A, 120 A, 200 A), with a gate resistor of 10 Ω and DC bus voltage of 300 V for the CGD and proposed AGD, as shown in Fig. 13 (a) and (b).

The turn-off energy loss, delay time, overshoot voltage, and Miller plateau duration during turn-off transient as functions of the gate resistance R_g and current level I_c are plotted for both gate drive circuits from Fig. 14 (a) to (d) respectively.

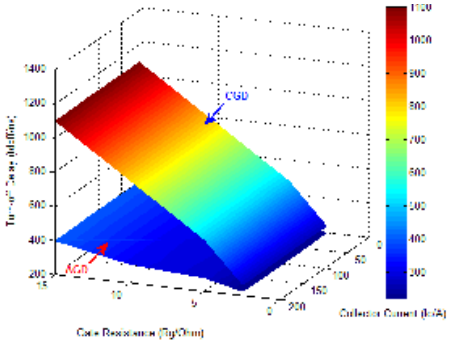


(a) Conventional gate driver

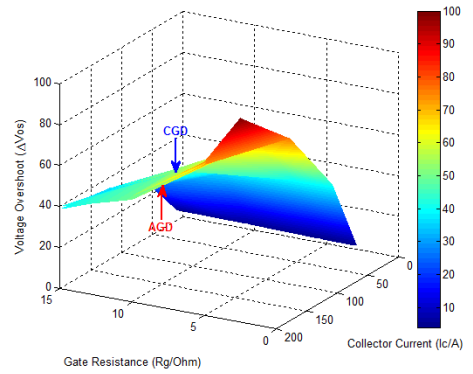
The delay time and the dissipated turn-off energy are increased with the increase of gate resistance, while the voltage overshoot decreases. When the AGD is used, the delay time fluctuation is small (around from 220 ns to 400 ns), compared with the delay time of 260 ns to 1100 ns with the CGD. The voltage overshoot is nearly the same. The turn-off switching energy is reduced by 15% to 33% in the plotted gate resistor and current level range, and the turn-off delay is reduced by 15% to 64%. The Miller plateau duration is reduced by 36% to 47% in the plotted range.



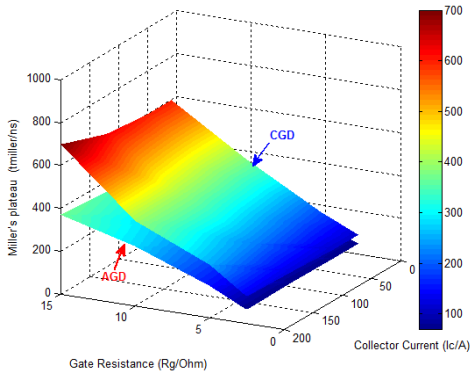
(a) Turn-off energy loss



(b) Turn-off delay



(c) Turn-off voltage overshoot



(d) Turn-off Miller plateau duration

Fig. 14. Comparison of the two methods under different current levels and gate resistances.

Like the turn-on test results, more switching time and energy loss are saved with larger gate resistance and higher current levels, which indicates that the proposed AGD is preferable for EMI sensitive applications that usually have larger gate resistance, and high power converters with high current levels.

IV. Conclusion

A novel active gate drive circuit of high power IGBT modules useful for switching performance improvement is proposed. The proposed active gate driver receiving the feedback signal from the parasitic inductance between Kelvin emitter and power emitter of an IGBT module, can adaptively control the gate voltage regardless of different gate resistors, power levels, and IGBT modules, which make it compatible with a wide range of IGBT applications, especially for EMI sensitive applications and high power converters.

A double pulse tester based experimental setup was constructed and switching waveforms with both types of gate drivers were measured and compared. The experimental results verify that the proposed active gate driver has the capability of reducing the switching losses, delay time, and Miller plateau duration effectively during both turn-on and turn-off transients.

The proposed solution is flexible in that it can be used as an active gate driver or a conventional one, depending on the user's needs. Conversion between them is effortless, requiring the simple removal or connection of the jumper in series with the gate charger/discharger to disconnect or connect the auxiliary circuit. Moreover, given that the auxiliary circuit only contains several small-signal active devices, simple logic circuits, and passive components, and does not require any independent isolated power supply, it is appropriate for chip integration.

Acknowledgement

This work was partially funded by the II-IV Foundation and Oak Ridge National Laboratory under the U.S. Department of Energy's Vehicle Technologies Program. This work made use of Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and DOE under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

References

[1] T. Shimizu and K. Wada, "A gate drive circuit of power MOSFETs and IGBTs for low switching losses," in *IEEE 7th International Conference on Power Electronics*, 2007, pp. 857-860.

[2] V. John, B. S. Suh, and T. A. Lipo, "High-performance active gate drive for high-power IGBTs," *IEEE Transactions on Industrial Electronics*, vol. 35, no. 5, pp. 1108-1117, Nov. 1999.

[3] S. Musumeci, A. Racati, A. Galluzzo, A. Testa, and M. Melito, "A new adaptive driving technique for high current gate controlled devices," in *Proc. IEEE Power Electronics Specialists Conference*, 1994, pp. 480–486.

[4] C. Licitra, S. Musueci, A. Racati, A. Galluzzo, R. Letor, and M. Melito, "A new driving circuit for IGBT devices," *IEEE Transactions on Power Electronics*, vol. 10, no. 3, pp. 373–378, May 1995.

[5] S. Musumeci, A. Racati, A. Testa, A. Galluzzo, and M. Melito, "Switching behavior improvement of isolated gate-controlled devices," *IEEE Transactions on Power Electronics*, vol. 12, no. 4, pp. 645–653, Nov. 1997.

[6] P. J. Grbovic, "An IGBT gate driver for feed-forward control of turn-on losses and reverse recovery current," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 643-652, Mar. 2008.

[7] P. J. Grbovic, "Turn-on performance of reverse blocking IGBT (RB IGBT) and optimization using advanced gate driver," *IEEE Transactions on Power Electronics*, vol. 25, no. 4, pp. 970-980, Apr. 2010.

[8] L. Michel, X. Boucher, A. Cheriti, P. Sicard, and F. Sirois, "FPGA implementation of an optimal IGBT gate driver based on Posicast control," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1-7, Jul. 2012.

[9] H. Kuhn, "Adaptive Ansteuerverfahren für Hochleistungs-IGBTs mit einer digitalen Treibereinheit (in German)," Ph.D. dissertation, University of Hannover, Germany, 2011.

[10] L. Dang, H. Kuhn, and A. Mertens, "Digital adaptive driving strategies for high-voltage IGBTs," in *IEEE Energy Conversion Congress and Exposition*, Phoenix, AZ, USA, Sep. 2011, pp. 2993–2999.

[11] N. Idir, R. Bausier, and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 849–855, Jul. 2006.

[12] K. Fink and S. Bernet, "Advanced Gate Drive Unit with closed-looped di/dt-control," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–9, Aug. 2012.

[13] L. Chen and F. Z. Peng, "Closed-loop gate drive for high power IGBTs," in *IEEE Applied Power Electronics Conference*, 2009, pp. 1331–1337.

[14] B. Wittig and F. W. Fuchs, "Analysis and comparison of turn-off active gate control methods for low-voltage power MOSFETs with high current ratings," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1632–1640, Mar. 2012.

[15] Y. Lobsiger and J. W. Kolar, "Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control," in *IEEE Energy Conversion Congress and Exposition*, Sep. 2012, pp. 4754–4761.

[16] R. L. Greenwell, B. M. McCue, M. I. Laurence, C. Fandrich, B. J. Blalock, L. M. Tolbert, S. K. Islam, "SOI-Based Integrated Gate Driver Circuit for High-Temperature Applications," *IMAPS International Conference on High Temperature Electronics*, Albuquerque, New Mexico, May 8-10, 2012, pp. 233-244.

[17] Z. Wang, X. Shi, L. M. Tolbert, B. J. Blalock, and M. Chinthavali, "A fast overcurrent protection scheme for IGBT modules through dynamic fault current evaluation," in *IEEE Applied Power Electronics Conference and Exposition*, 2013, 8 pages.