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Switching Transient Analysis and Design of a Low Inductive Laminated Bus Bar for a T-type Converter

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Abstract

Distributed stray inductance exerts a significant influence on the turn-off voltages of power switching devices. Therefore, the design of low stray inductance bus bars has become an important part of the design of high-power converters. In this study, we first analyze the operational principle and switching transient of a T-type converter. Then, we obtain the commutation circuit, categorize the stray inductance of the circuit, and study the influence of the different types of stray inductance on the turn-off voltages of switching devices. According to the current distribution of the commutation circuit, as well as the conditions for realizing laminated bus bars, we laminate the bus bar of the converter by integrating the practical structure of a capacitor bank and a power module. As a result, the stray inductance of the bus bar is reduced, and the stray inductance in the commutation circuit of the converter is reduced to more than half. Finally, a 10 kVA experimental prototype of a T-type converter is built to verify the effectiveness of the designed laminated bus bar in restraining the turn-off voltage spike of the switching devices in the converter.

Key words: Laminated bus bar, Reverse blocking IGBT, Switching transient, T-type converter, Turn-off voltage

I. INTRODUCTION

In practical engineering applications, the capacitance of electrolytic capacitors and their capability to withstand voltages are limited. Hence, the DC side of high-power converters generally requires a large number of capacitors with a series–parallel connection to support the DC bus voltage. The use of a general connection may result in high stray inductances, which in turn lead to the following two problems [1]-[5]. First, stray inductances significantly influence the turn-off characteristics of power switching devices [1]-[3], especially high-power converters with large d*i*/d*t*. Huge mutation currents may cause large voltage spikes in stray inductances, which could generate serious electromagnetic interference that affects electrical power systems or even cause damage to the semiconductor devices of converters. These conditions consequently affect the reliability of power systems. Second, stray inductances can cause the uneven distribution of the high-frequency current between parallel capacitors [4], [5]. Capacitors near power components endure a current that is higher than the rated current and thus rapidly generates heat, which seriously affects the operating life of capacitors.

The traditional method for solving the first problem is to add RCD snubber circuits to suppress voltage spikes [6]-[9]. However, in high-power applications, this approach necessitates capacitors with large capacity absorption and resistances, which increase system cost and loss. For the second problem, the general approach involves using high-frequency capacitors in parallel between electrolytic capacitors to balance the high-frequency current passing through the electrolytic capacitors. Similarly, this setup entails an increase in system cost. The two methods are limited to the elimination of the adverse effects of stray inductances and are thus ineffective in suppressing the root (stray inductance) of the problem.

An effective method for reducing stray inductances involves the use of a laminated bus bar [10]-[13]. A laminated bus bar is a type of connecting structure that links electrolytic capacitors and power devices. It is composed of thin copper conductors with different voltage potentials. Moreover, its interlayer is insulated by a dielectric [10] (Fig. 1). As a result of the proximity effect, the current in two flat coppers overlaying one another induces a reverse mirror current on the surface of each copper [11]. A mirror current can offset the external electromagnetic field radiation to some extent such that the

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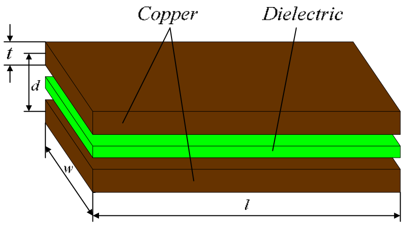


Fig. 1. Structural diagram of a laminated bus bar.

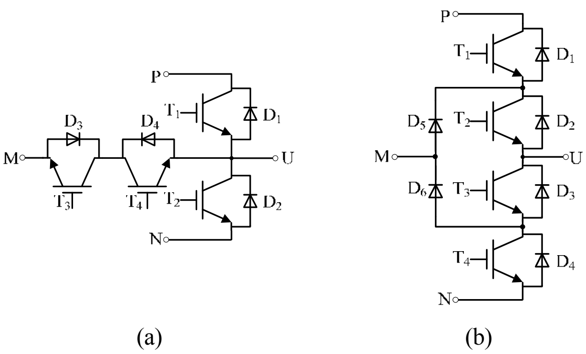


Fig. 2. Two types of NPC converter topology. (a) T-type NPC. (b) Diode NPC.

copper stray inductance can be effectively suppressed. A large surface area ($w \times l$) equates to a small distance (d) between layers and to an effective suppression of stray inductance.

Compared with traditional two-level inverters, multi-level inverters offer a more significant advantage in terms of power capacity and the capability to withstand voltages. A T-type converter topology is an improved three-level (multi-level) neutral point clamped (NPC) circuit [14]-[17], as shown in Fig. 2(a). It uses a bidirectional switch formed by two insulated-gate bipolar transistors (IGBTs; S_3, S_4) and two diodes (D_3, D_4) to achieve the neutral-to-ground function of clamping and a bidirectional energy flow. Compared with the widely used diode-clamped NPC circuit shown in Fig. 2(b), the T-type converter requires fewer switching devices and achieves a more balanced loss for the upper and lower bridge arms. Therefore, this type of circuit has become a central research area. In the engineering applications of T-type converters, the two aforementioned problems emerge as a result of stray inductances. To solve these problems, we design a low inductive laminated bus bar for a 10 kVA T-type converter.

This paper is organized as follows. The operational principle and switching transient of a T-type converter are analyzed in Section 2. The influences of the different types of stray inductances on the turn-off voltages of switching devices are presented in Section 3. The design process for the proposed laminated bus bar is illustrated in Section 4. The experiment results and analyses are presented in Section 5. Relevant conclusions are given in Section 6.

II. Operational Principle and Switching Transient Analysis

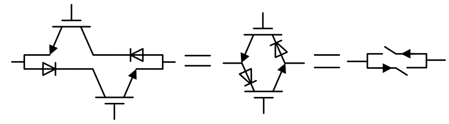


Fig. 3. Equivalent circuit of two anti-paralleled RB-IGBTs.

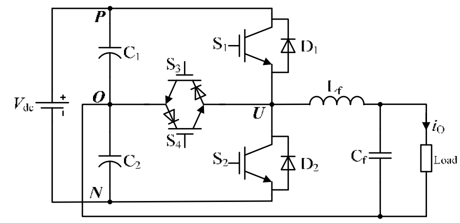


Fig. 4. Single-phase T-type converter with RB-IGBTs.

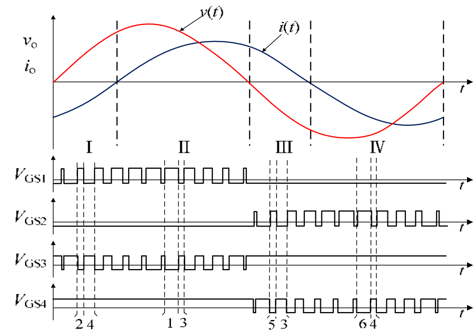


Fig. 5. Waveforms of v_o, i_o, and V_{GS}.

A low inductive laminated bus bar must be designed according to the commutation circuit of the given converter. Therefore, we must determine the distribution condition of the stray inductances and commutation circuit in the converter by analyzing the operational principle and switching transient before initiating the design process.

A. T-type Converter with RB-IGBTs

A reverse blocking IGBT (RB-IGBT) is a new IGBT device [18]-[20]. Unlike ordinary IGBTs, RB-IGBTs are capable of enduring reverse voltages. Thus, they can be used as controllable one-way switches, and their function can be equivalent to that of a diode in series with an ordinary IGBT; however, their voltage drop is smaller than the combination of diode and IGBT [20]. As shown in Fig. 3, two anti-paralleled RB-IGBTs can form a controllable bidirectional switch.

A T-type converter with RB-IGBTs is shown in Fig. 4. RG-IGBTs can further improve the efficiency of T-type converters and thereby widen their application prospect in the areas of photovoltaic, distributed generation, and micro-grids.

B. Operational Principle Analysis

The waveforms of the output voltage (v_o), current (i_o), and driving signals (V_{GS}) of the converter under an assumed resistive and inductive load are shown in Fig. 5. In one operation cycle, v_o and i_o exhibit four types of phase relationships (I: v_o>0, i_o<0; II: v_o>0, i_o>0; III: v_o<0, i_o>0; IV:

v_o<0, i_o<0), and each phase comprises two alternating operation modes.

According to the direction of the output current i_o and the on/off state of each switching device, one operation cycle involves six types of operation modes.

1) *Mode 1:* In this mode, i_o flows from the input to the load in a positive direction. When the driving signal $V_{GS1}>0$, $V_{GS4}>0$, $V_{GS2}<0$, $V_{GS3}<0$, and $i_o>0$, S_1 is conducting. The output voltage $v_o = 1/2\ V_{dc}$; thus, S_4 can withstand a reverse voltage in the off state despite its positive driving signal. This working status is defined as mode 1, as shown in Fig. 6(a).

2) *Mode 3:* In this mode, V_{GS1} switches from positive to negative, and V_{GS3} switches from negative to positive. The other driving signals remain unchanged. Thus, S_1 is turned off from its conducting state. Given that $V_{GS4}>0$, S_4 is turned on to maintain the continuous flow of i_o to the load. At this point, the output voltage $v_o = 0$. This working status is defined as mode 3, as shown in Fig. 6(b).

3) *Mode 5:* If the direction of i_o remains constant and $V_{GS2}>0$, $V_{GS3}>0$, $V_{GS1}<0$, and $V_{GS4}<0$, then i_o freewheels through the anti-parallel diode D_2 of S_2. At this point, the output voltage $v_o = -1/2V_{dc}$. This working status is defined as mode 5, as shown in Fig. 6(c).

When the direction of i_o is negative under different combinations of driving signals, the converter operates in modes 2, 4, and 6; the corresponding equivalent circuits are shown in Figs. 6(a), (b), and (c). These modes are similar to modes 1, 3, and 5 and are no longer analyzed in detail.

C. Switching Transient and Commutation Circuit Analysis

A single-phase T-type converter with a stray inductance parameter (excluding load) is shown in Fig. 7. The inductors shown in the picture are stray inductances between the bus nodes ***P***, ***O***, ***N***, ***P′***, ***U***, and ***N′***. These inductances include the lead inductances of capacitance, lead inductances of switching devices, inductances of bolt connection, and stray inductances of the bus bar, which make up a large portion of the inductances. Thus, the overall stray inductance of the converter can be effectively reduced with an effective laminated bus bar design.

According to whether the driving signals of switches change during commutation, commutation is divided into two modal types: *forced commutation* and *natural commutation*. Changed driving signals cause the mutation of operation modes, which results in a mutant current in the commutation circuit. The current acting on the stray inductance of the commutation circuit generates large interferences and voltage spikes. We refer to this commutation process as *forced commutation*. On the contrary, in the *natural commutation* process, the driving signal remains unchanged, and the circuit current decreases to zero and then increases. In this case, voltage spikes are not generated.

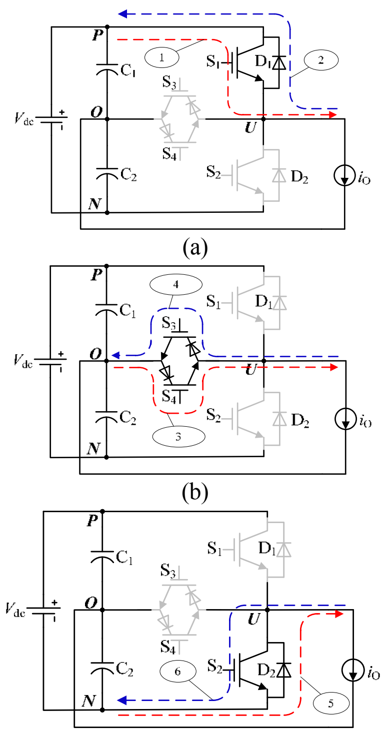


Fig. 6. Equivalent circuit of each mode. (a) Modes 1, 2. (b) Modes 3, 4. (c) Modes 5, 6.

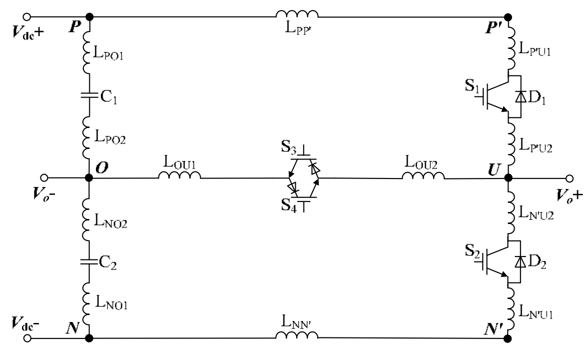


Fig. 7. Stray inductance distribution of a single-phase T-type converter (excluding load).

1) Forced Commutation I (for example, mode switching from 2 to 4 to 2) : In area I (Fig. 5), the operation modes of the converter switch between modes 2 and 4 continually. The switching transients are shown in Fig. 8.

When the operation mode switches from mode 2 to mode 4, the switching of the driving signals V_{GS2} and V_{GS4} remains unchanged; that is, V_{GS1} switches from positive to negative, and V_{GS3} switches from negative to positive. Diode D_1 withstands a negative voltage and reaches the off state, and S_3 starts conducting. At this moment, the current i_{D1} decreases while i_{S3} increases and then begins to shift from D_1 to S_3 quickly, as shown in Fig. 8(b). D_1 cannot immediately reach the off state when its current is reduced to zero; in such a

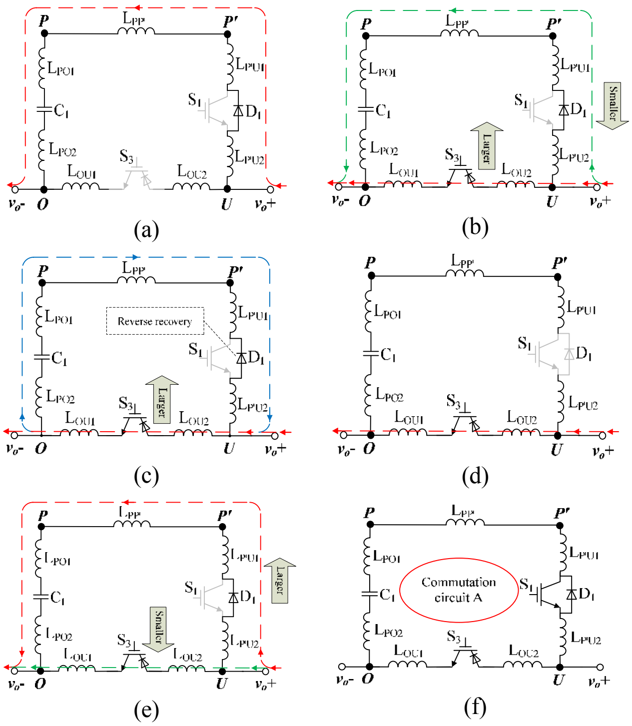


Fig. 8. Switching transient of mode 2 switching to 4 and then to 2. (a) Steady state of mode 2. (b) Transient state 1 from modes 2 to 4. (c) Transient state 2 from modes 2 to 4. (d) Steady state of mode 4. (e) Transient state from modes 4 to 2. (f) Equivalent circuit of forced commutation circuit A.

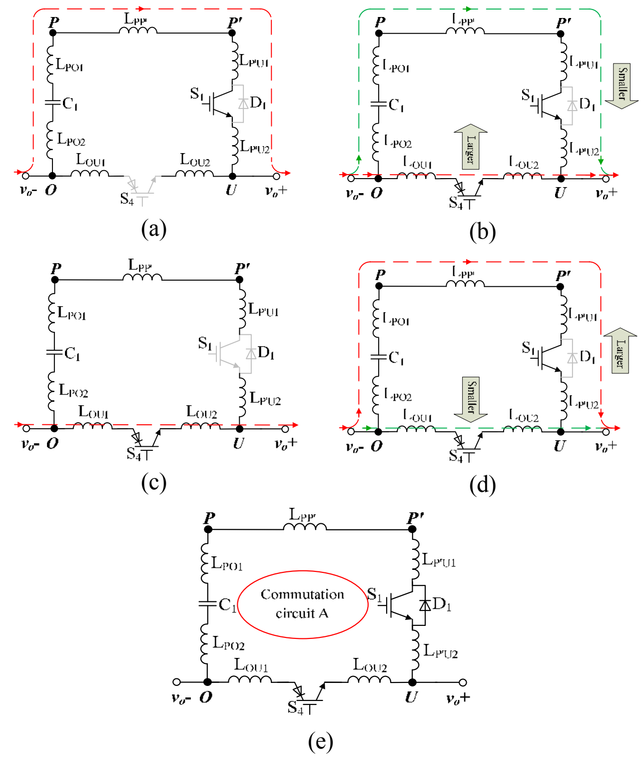


Fig. 9. Switching transient of mode switching from 1 to 3 to 1. (a) Steady state of mode 1. (b) Transient state from mode 1 to 3. (c) Steady state of mode 3. (d) Transient state from mode 3 to 1. (e) Equivalent circuit of forced commutation circuit A.

case, it enters the reverse recovery process, which generates a large reverse current, as shown in Fig. 8(c). This condition is equivalent to an instantaneous short circuit between the midpoint and positive DC bus bar, and the bus current produces transient spikes. When the reverse blocking capability of D_1 is restored, the converter enters the steady state in mode 4, which is shown in Fig. 8(d).

When the operation mode switches from mode 4 to mode 2, the switching driving signals V_{GS2} and V_{GS4} remain unchanged; that is, V_{GS1} switches from negative to positive, and V_{GS3} switches from positive to negative. S_3 exits the conducting state and reaches the off state, and i_{S3} decreases rapidly. To maintain the output current, D_1 starts freewheeling and conducting, i_{D1} increases, and the current starts to shift from S_3 to D_1 quickly, as shown in Fig. 8(e). When the current completes its shift from S_3 to D_1, the diode enters a stable freewheeling process in mode 2, as shown in Fig. 8(a).

As indicated in the analysis above, mode switching between modes 2 and 4 results in a forced commutation circuit A, as shown in Fig. 8(f). The stray inductance of the circuit is

$$L_A = L_{PP'} + L_{PO1} + L_{PO2} + L_{OU1} + L_{OU2} + L_{P'U2} + L_{P'U1} \quad (1)$$

2) Forced Commutation Ⅱ (for example, mode switching from 1 to 3 to 1) : In area II (Fig. 5), the operation modes of the converter switch between modes 1 and 3 continually. The switching transients are shown in Fig. 9.

When the operation mode switches from mode 1 to mode 3, the switching of the driving signals V_{GS2} and V_{GS4} remains unchanged; that is, V_{GS1} switches from positive to negative, and V_{GS3} switches from negative to positive. S_1 begins to enter the off state, and S_4 starts conducting. At this moment, the current i_{S1} decreases while i_{S4} increases and begins to shift from S_1 to S_4 quickly, as shown in Fig. 9(b). After S_1 shuts off completely, the converter enters the steady state in mode 3, as shown in Fig. 9(c).

When the operation mode switches from mode 3 to mode 1, the switching of the driving signals V_{GS2} and V_{GS4} remains unchanged; that is, V_{GS1} switches from negative to positive, and V_{GS3} switches from positive to negative. At this moment, the current i_{S1} increases while i_{S4} decreases and begins to shift from S_4 to S_1 quickly, as shown in Fig. 9(d). After S_4 shuts off completely, the converter enters the steady state in mode 1, as shown in Fig. 9(a).

As indicated in the analysis above, mode switching between modes 1 and 3 also forms a forced commutation circuit A, as shown in Fig. 9(e). The circuit stray inductance remains to be L_A.

The same process is observed when the converter operates in areas III and IV (Fig. 5). Mode switching between modes 5 and 3 and between modes 6 and 4 forms a forced commutation circuit B, as shown in Fig. 10.

The circuit stray inductance is

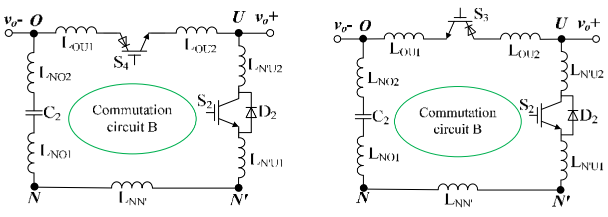


Fig. 10. Equivalent circuit of forced commutation circuit B. (a) Switching between modes 5 and 3. (b) Switching between modes 6 and 4.

$$L_B = L_{NN'} + L_{NO1} + L_{NO2} + L_{OU1} + L_{OU2} + L_{N'U2} + L_{N'U1} \quad (2)$$

3) Natural Commutation : During the operation states of the converter cycling between areas I, II, III, and IV (Fig. 5), a transient process occurs between modes 1 and 2, 3 and 4, and 5 and 6. In the transition process, the driving signals and device voltages remain constant, and the current gradually declines to zero and then increases. This process is referred to as natural commutation. The corresponding transition process is shown in Figs. 6(a), (b), and (c).

III. Impact of Different Types of Stray Inductance on Turn-off Voltage

We choose the integrated power module 4MBI300VG-120R-50 as the switching device of the experimental prototype. Each module contains two 1,200 V/300 A IGBTs and two 600 V/300 A RB-IGBTs. Thus, one module can be used as a single-phase T-type converter. The equivalent circuit and packaging of the module are shown in Fig. 11.

The converter comprises two forced commutation circuits. The detailed distribution of the stray inductance of the main circuit of the prototype (excluding load) is shown in Fig. 12.

The distribution is as follows:

a) Stray inductance of capacitor bank bus ($L_{s\text{-}cbb}$): L_{PP1}, L_{P1P2}, ⋯, $L_{P(n-1)Pn}$, L_{NN1}, L_{N1N2}, ⋯, $L_{N(n-1)Nn}$

b) Stray inductance of connection bus ($L_{s\text{-}cb}$): $L_{Pn\,P''}$, $L_{On\,O''}$, $L_{Nn\,N''}$

c) Stray inductance of power module ($L_{s\text{-}pm}$): $L^*_{P'U1}$, $L^*_{P'U2}$, etc.

d) Stray inductance of power module bus ($L_{s\text{-}pmb}$): $L_{P''P'}$, $L_{O''M}$, $L_{N''N}$

e) Stray inductance of capacitance leads ($L_{s\text{-}cl}$): $L_{(PO)1}$, $L_{(PO)2}$, ⋯, $L_{(PnOn)1}$, $L_{(PnOn)2}$, $L_{(NO)1}$, $L_{(NO)2}$, ⋯, $L_{(NnOn)1}$, $L_{(NnOn)2}$

To study the influence of the different types of stray inductance on the turn-off voltages of switching devices, we built a simulation model comprising the aforementioned stray parameters with the PSIM software. The major simulation parameters are shown in Table I. Among these parameters, V_{dc},' f_s, V_o, f_o, P_o, and I_o are the major working indexes of the prototype, and C_1, C_2, L_f, and C_f are calculated with the working indexes. The values are consistent with those of the experimental prototype used in the present study.

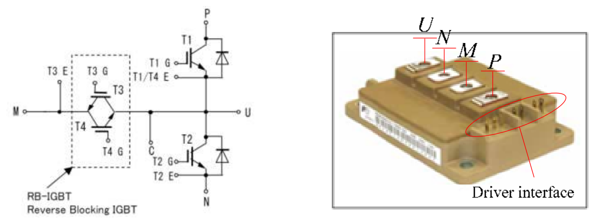


Fig. 11. Equivalent circuit and packaging of the power module. (a) Equivalent circuit. (b) Packaging.

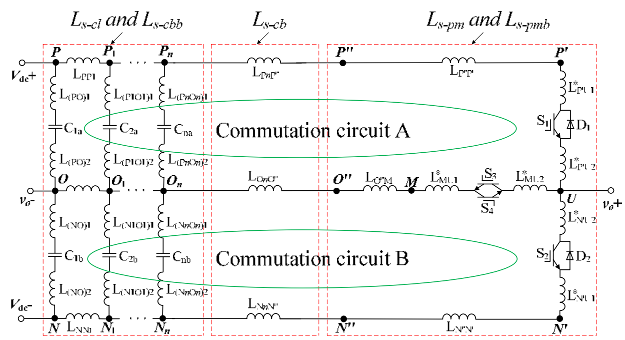


Fig. 12. Stray inductance distribution of the main circuit.

TABLE I
Major Simulation Parameters

V_{dc}/V	f_s/kHz	V_o/V	f_o/Hz	P_o/kW
700	5	220 (rms)	50	10
I_o/A	**C_1/uF**	**C_2/uF**	**L_f/mH**	**C_f/uF**
15(rms)	13,200	13,200	1.2	47

Theoretically, switches S_1 and S_2 can withstand a maximum voltage of V_{dc}, whereas switches S_3 and S_4 can withstand a maximum voltage of $1/2V_{dc}$. Thus, the voltage environment when S_1 and S_2 are in the off state is obviously severe. Therefore, this study mainly focuses on the effects of stray inductance on the terminal voltage V_{CE1} of S_1.

A. Impact of Ls-cbb on Turn-off Voltage

The simulation waveform of V_{CE1} with no stray parameter considered is shown in Fig. 13(a). Resonance or voltage spike is not observed. The simulation waveform of V_{CE1} with $L_{s\text{-}cbb}$ in the commutation circuit (10 nH) considered is shown in Fig. 13(b).

The results of the fast fourier transform (FFT) analysis of V_{CE1} when $L_{s\text{-}cbb}$ decreases from 100 nH progressively are shown in Fig. 14.

The simulation results indicate that during the off state of S_1, $L_{s\text{-}cbb}$ resonates with the electrolytic capacitors. This effect causes the switching device to withstand fluctuating voltages.

When $L_{s\text{-}cbb}$ is 100 nH, the resonant peak voltage of V_{CE1}

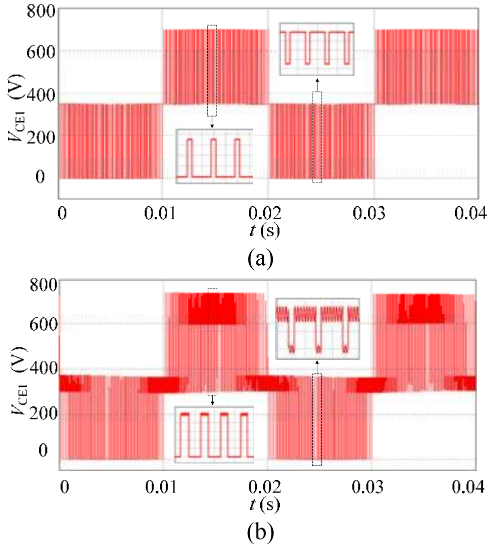


Fig. 13. Simulation waveform of V_{CE1}. (a) Without stray parameters. (b) With $L_{s\text{-}cbb}$ (10 nH) considered.

approaches the output voltage (220 V, 50 Hz), and the waveform of V_{CE1} undergoes serious distortion. The FFT analysis shows that along with a reduction of $L_{s\text{-}cbb}$, the resonant frequency increases, but the resonant peak decreases. When the stray inductance is reduced to the lowest level, the resonance disappears or can be ignored.

B. Impact of Ls-cb, Ls-pm, and Ls-pmb on Turn-off Voltage

As shown in Fig. 12, the stray inductance distributions of $L_{s\text{-}cb}$, $L_{s\text{-}pm}$, and $L_{s\text{-}pmb}$ are the same, and their effects on the terminal voltage of the switching device are similar. Therefore, we analyze them collectively.

According to the simulation results of the non-laminated bus bar, $L_{s\text{-}pm}$ (including $L_{s\text{-}cb}$) is approximately 50 nH. $L_{s\text{-}pmb}$ is 33 nH according to the datasheet of the power model, and it cannot be reduced. The simulation waveforms of V_{CE1} when $L_{s\text{-}pm}$ and $L_{s\text{-}pmb}$ are taken as 50 and 33 nH and as 5 and 33 nH, respectively, are shown in Fig. 15.

When $L_{s\text{-}pm}$ (including $L_{s\text{-}cb}$) is reduced from 50 nH to 5 nH, the total stray inductance of the commutation circuit is reduced significantly, and the voltage spikes are suppressed effectively. $L_{s\text{-}cb}$, $L_{s\text{-}pm}$, and $L_{s\text{-}pmb}$ are the main factors that influence the voltage spikes.

C. Impact of Ls-cl on Turn-off Voltage

The simulation waveforms of V_{CE1} when $L_{s\text{-}cl}$ is 10 nH and when the electrolytic capacitor is parallel with a 0.1 uF high-frequency capacitor are shown in Figs. 16(a) and (b), respectively. $L_{s\text{-}cl}$ also causes voltage spikes in the switching device. However, $L_{s\text{-}cl}$ is not significant; thus, its impact on the voltage spikes is inferior to that of $L_{s\text{-}cb}$, $L_{s\text{-}pm}$, and $L_{s\text{-}pmb}$. We can solve this problem by paralleling a number of high-frequency non-inductive capacitors between the large-capacity electrolytic capacitors.

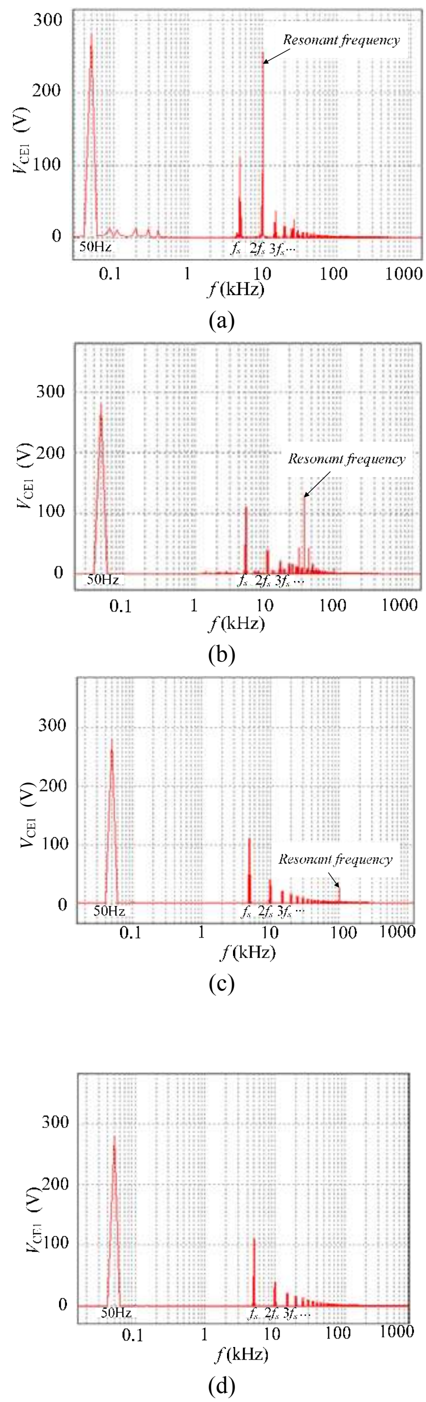
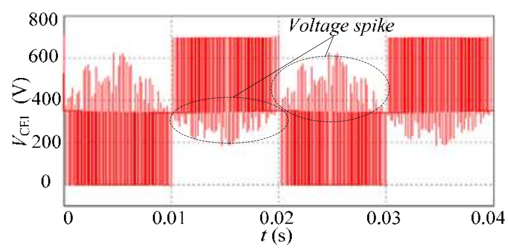
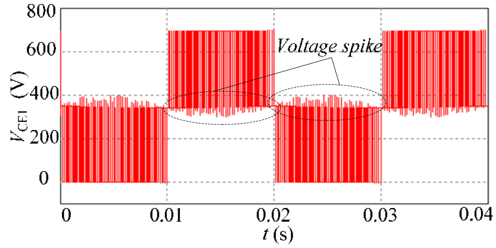


Fig. 14. FFT analysis results of V_{CE1}. (a) 100 nH. (b) 10 nH. (c) 1 nH. (d) 0.1 nH.

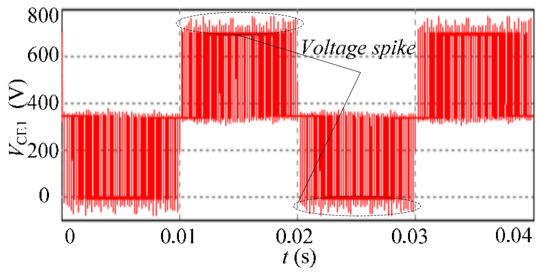


(a)

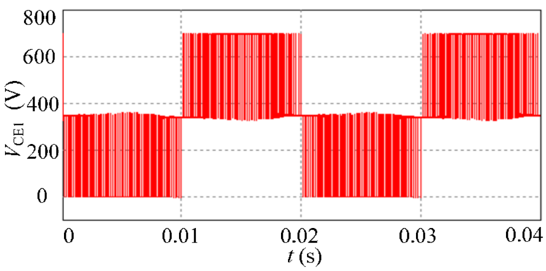


(b)

Fig. 15. Simulation waveform of VCE1. (a) 50 and 33 nH. (b) 5 and 33 nH.



(a)



(b)

Fig. 16. Simulation waveform of V_{CE1}. (a) 10 nH. (b) In parallel with a 0.1 uF.

IV. Design of the Laminated Bus Bar

A. Achieving the Conditions for the Laminated Bus Bar

According to mirror current theory of laminated bus bars, the following conditions should be met to effectively reduce stray inductances.

a) The commutation processes must have the same high-frequency commutation current flowing through all the coppers of the commutation circuits.

b) All the coppers constituting the commutation circuit must participate in the lamination.

The commutation circuit A shown in Fig. 17 is taken as an example to verify whether the commutation circuits A and B meet the conditions above. The mode switching between modes 2 and 4 changes the load current i_{LD} from i_{D1} (U-D_1-P'-P-O) to i_{S3} (U-S_3-O).

Assuming a strong inductive load, the load current during the commutation process remains unchanged. Given that S_1, S_2, S_4, and D_2 are in the off state, the current flowing through them is 0. The following result can be obtained from Kirchhoff's current laws:

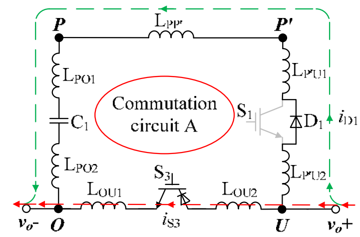


Fig. 17. Equivalent circuit of forced commutation circuit A.

$$i_{D1} + i_{S3} = i_{LD} = I \tag{3}$$

As Kirchhoff's current law is valid for the full current, it is also valid for each harmonic component after Fourier decomposition. Therefore, i_{S1} and i_{S3} can be divided into AC and DC components.

$$I_{D1(dc)} + i_{D1(ac)} + I_{S3(dc)} + i_{S3(ac)} = I \tag{4}$$

The load current during the commutation remains unchanged. As a result,

$$I_{D1(dc)} + I_{S3(dc)} = I \tag{5}$$

Therefore,

$$i_{D1(ac)} = -i_{S3(ac)} \tag{6}$$

The DC component of the commutation current does not act on the stray inductances. Thus, we can only consider the AC component. In (6), we can see that the high-frequency AC current flowing through D_1 flows back to S_3. As a result, they are in the same current loop. Therefore, condition *a* is met. Commutation loop B can also be proved using a similar method. The next step is to meet condition *b* by employing all the coppers of the commutation circuits A and B in the stack of the designed bus bar.

B. Design and Simulation of the Laminated Bus Bar

At the input side of the converter, the electrolytic capacitors in series–parallel connection generate significant connection inductances. As a result of the large dimension of the electrolytic capacitors, the distance between them and the distance between power devices considerably differ. If we use an ordinary connection, then the connection inductances may cause the uneven distribution of the high-frequency current between adjacent and distant electrolytic capacitors. Consequently, the adjacent electrolytic capacitors become heated easily and thus exhibit a short operating life. Therefore, in addition to the circuit inductances of the commutation circuits A and B, the stray inductances of the capacitor bank bus need to be reduced with the laminated bus bar. According to the distribution of the stray inductances and condition *b*, the laminated bus bar is designed in groups; one group connects the electrolytic capacitors, and another group is connected to the power modules, as shown in Fig. 18.

The stray inductances of the capacitor bank bus can be reduced with the designed laminated bus bar. However, we cannot eliminate them completely, and stray inductances

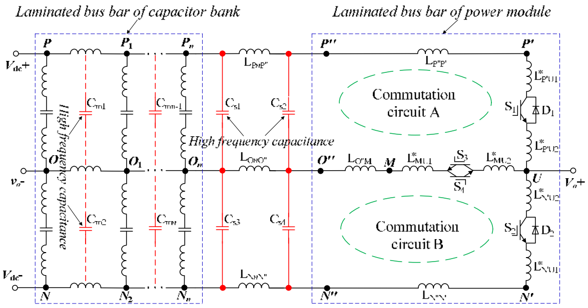


Fig. 18. Structural diagram of the laminated bus bar.

remain in the leads of the capacitance. Therefore, the high-frequency capacitors C_{m1}, C_{m2}, … ,C_{mn} shown in Fig .18 are added between the electrolytic capacitors. These high-frequency capacitors can absorb voltage spikes when the IGBT is turned off. They can also share the high-frequency electric current for the electrolytic capacitors.

The packet design introduces the connection inductances $L_{PnP''}$, $L_{OnP''}$, and $L_{NnP''}$ at the junction surface of the bus bar. A small amount of connection inductances $L_{P''P'}$, $L_{P''M}$, and $L_{N''N'}$ are also observed between the bus bar terminals ***P''***, ***O''***, and ***N''*** and the power modules. Connection inductances can reduce the current stress of the electrolytic capacitors but also increase the turn-off voltage spikes. Thus, the snubber capacitors C_{s1}, C_{s2}, C_3, and C_{s4} are installed at the junction surface of the bus bar and the side near the power modules to allow the easy absorption of the energy of the connection inductances. With such design, the energy absorption problem of the stray inductance in the commutation circuit and the distribution of a high-frequency current between different capacitors are effectively resolved. Furthermore, the inductances of the commutation circuits A and B are reduced to a portion behind the snubber capacitors, as shown in Fig .18.

According to the actual structure of the capacitor bank and the power module, the laminated bus bar is designed using the Ansoft Q3D software. The laminated bus bar and its surface current distribution are shown in Fig. 19. The surface current distribution is uniform, which indicates that their stray inductances are small. The simulation results of the stray inductances and capacitance parameters of each bus are shown in Tables II and III, respectively.

The non-laminated bus bar of the power module and its surface current distribution are shown in Fig. 20. The eddy and proximity effect of the surface current is obvious.

The simulation results of the stray inductances and capacitance parameters of the non-laminated bus bar is shown in Table IV. The stray inductance is large.

According to the simulation results and the data sheet of the power module, the commutation circuit inductances of A and B when using the laminated bus bar are

$$L_A = \underbrace{L_{PP'} + L_{PO1} + L_{PO2} + L_{OU1}}_{L_{A1}} + \underbrace{L_{OU2} + L_{P'U2} + L_{P'U1}}_{L_{A2}} \quad (7)$$
$$= 16.711nH + 33nH = 49.71nH$$

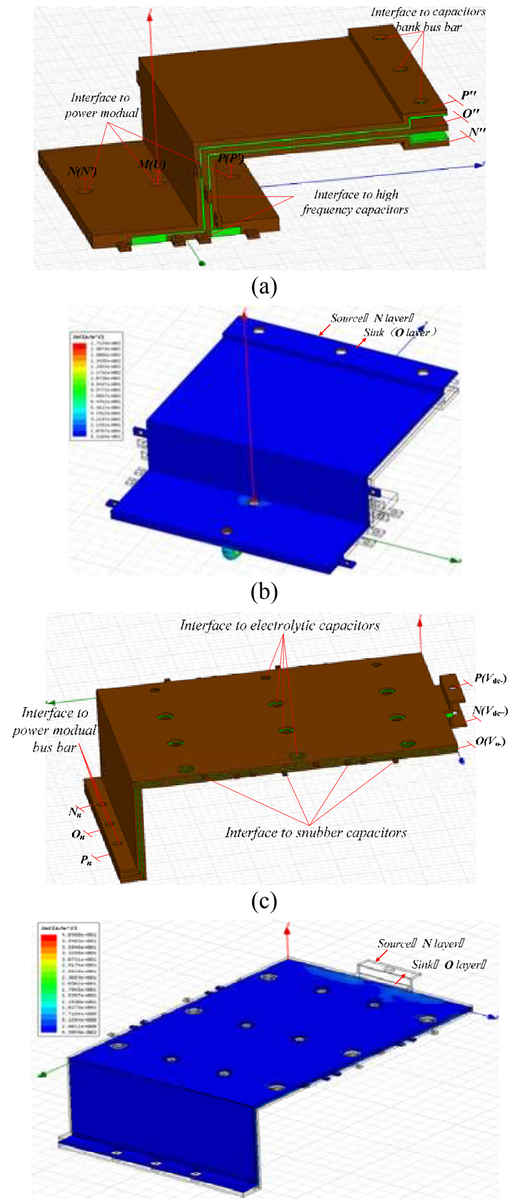


Fig. 19. Laminated bus bar and the surface current distribution of the power module and capacitor bank. (a) Laminated bus bar of the power module (single phase). (b) Surface current distribution of the power module bus bar (single phase). (c) Laminated bus bar of capacitor bank. (d) Surface current distribution of capacitor bank bus bar.

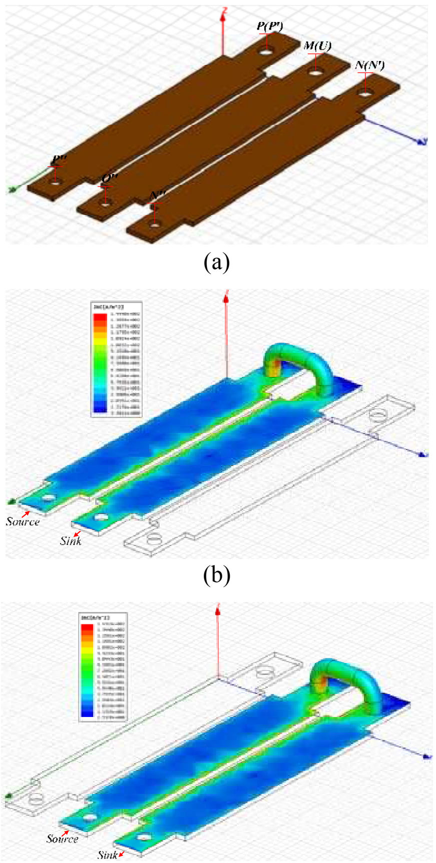
TABLE II
RESULTS OF THE STRAY PARAMETER SIMULATION OF THE LAMINATED BUS BAR OF THE POWER MODULE

Circuit	C/(pF)	L_{dc}/(nH)	L_{ac}/(nH)
P''-P'-U-O''	539.02	16.711	11.909
N''-N'-U-O''	569.32	17.718	12.176

$$L_B = \underbrace{L_{NN'} + L_{NO1} + L_{NO2} + L_{OU1}}_{L_{B1}} + \underbrace{L_{OU2} + L_{N'U2} + L_{N'U1}}_{L_{B2}} \quad (8)$$
$$= 17.718nH + 33nH = 50.718nH$$

TABLE III
RESULTS OF THE STRAY PARAMETER SIMULATION OF THE LAMINATED BUS BAR OF THE CAPACITOR BANK

Circuit	C/(pF)	L_{dc}/(nH)	L_{ac}/(nH)
P-P$_n$-O$_n$-O	2808.1	8.9569	5.1867
N-N$_n$-O$_n$-O	2904.1	9.0746	5.2751



(a)

(b)

(c)

Fig. 20. Non-laminated bus bar and the surface current distribution of the power module. (a) Non-laminated bus bar of the power module (single phase). (b) Surface current distribution 1. (c) Surface current distribution 2.

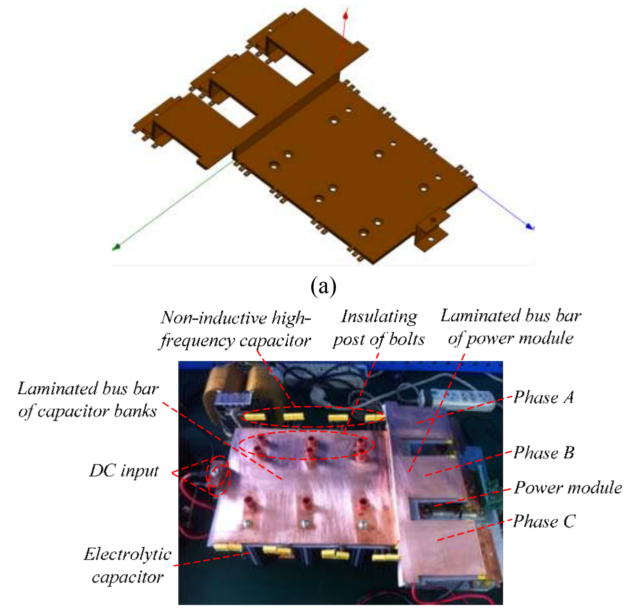
TABLE IV
RESULTS OF THE STRAY PARAMETER SIMULATION OF THE NON-LAMINATED BUS BAR OF THE POWER MODULE

Circuit	C(pF)	L_{dc}(nH)	L_{ac}(nH)
P''-P'-U-O''	4.6503	73.798	53.398
N''-N'-U-O''	4.6491	73.745	53.013

where L_{A1} and L_{B1} are the stray inductances of the power module bus bars of the commutation circuits A and B;

L_{A2} and L_{B2} are the internal stray inductances of the power module. The stray inductance of the device itself cannot be reduced.

Similarly, when using the non-laminated bus bar, the stray



(a)

(b)

Fig. 21. Design of the laminated bus bar. (a) Simulation design result. (b) Physical design result.

inductances of the commutation circuits A and B are

$$\begin{aligned} L'_{\rm A} &= \underbrace{L_{\rm PP'} + L_{\rm PO1} + L_{\rm PO2} + L_{\rm OU1}}_{L'_{A1}} + \underbrace{L_{\rm OU2} + L_{\rm P'U2} + L_{\rm P'U1}}_{L_{A2}} \\ &= 73.798nH + 33nH = 106.798nH = 2.148L_A \end{aligned} \quad (9)$$

$$\begin{aligned} L'_{\rm B} &= \underbrace{L_{\rm NN'} + L_{\rm NO1} + L_{\rm NO2} + L_{\rm OU1}}_{L'_{B1}} + \underbrace{L_{\rm OU2} + L_{\rm N'U2} + L_{\rm N'U1}}_{L_{B2}} \\ &= 73.745nH + 33nH = 106.745nH = 2.105L_B \end{aligned} \quad (10)$$

By contrasting (7), (8), (9), and (10), we deduce the following:

a) L_{A1}=22.7%L'_{A1}, L_{B1}=24.1%L'_{B1}. The stray inductance can be reduced significantly with the laminated bas bar.

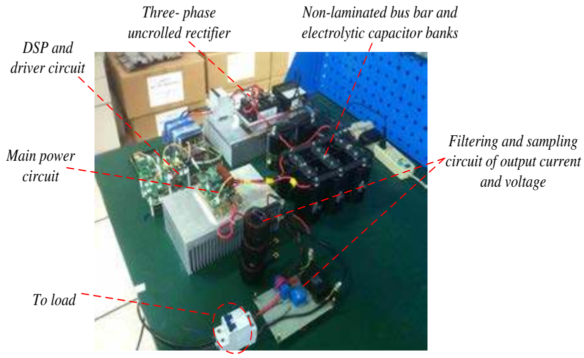
b) L'_A=2.148L'_A, L'_B=2.105L'_B. The stray inductance of the power module (33 nH) is significant. Thus, the whole stray inductance of the commutation circuits can be reduced by half through the laminated bus bar design. In this way, the voltage spikes caused by the stray inductance can be effectively reduced.

To solve the problem of insulation and the large connection inductance at the interface caused by packet design, we develop an integrated optimization design between two bus bar groups. The final effect and real bus bar are shown in Fig. 21.

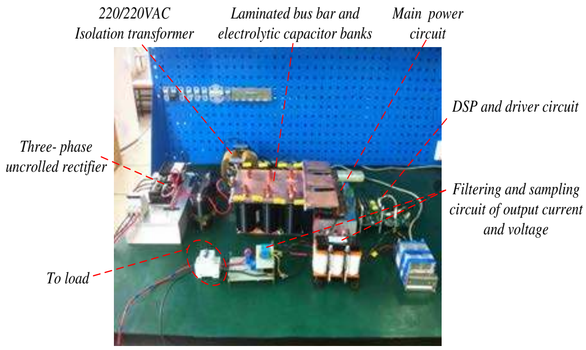
V. EXPERIMENT AND ANALYSIS

To verify the theoretical and simulation results, we build two T-type converter prototypes using non-laminated and laminated bus bars, as shown in Figs. 22(a) and (b), respectively.

The waveforms of the output voltage v_o and terminal voltages V_{CE1} and V_{CE2} of switches S_1 and S_2 are shown in Fig.

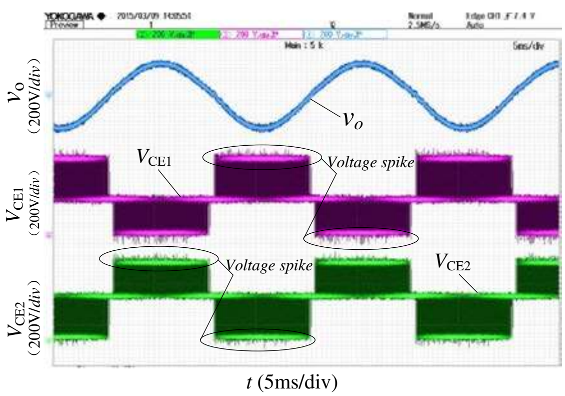


(a)

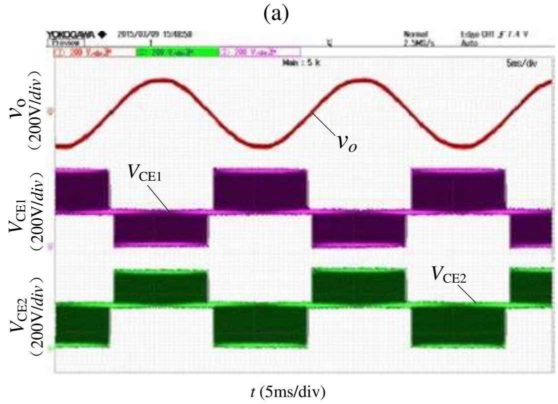


(b)

Fig. 22. Two 10 kVA prototypes with different bus bars. (a) Non-laminated bus bar. (b) Laminated bus bar.

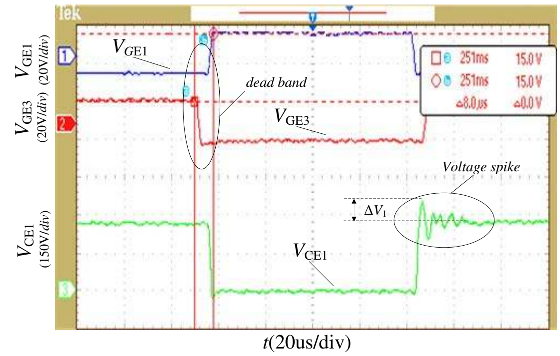


(a)

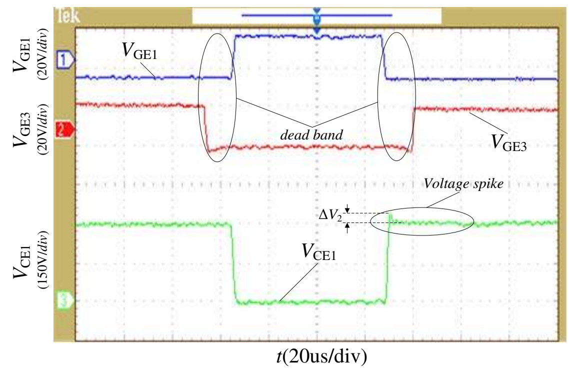


(b)

Fig. 23. v_o, V_{CE1}, and V_{CE2} waveforms with different bus bars. (a) Non-laminated bus bar. (b) Laminated bus bar.



(a)



(b)

Fig. 24. Turn-off voltage waveform of S_1 with different bus bars. (a) Non-laminated bus bar. (b) Laminated bus bar.

Fig. 23. V_{CE1} and V_{CE2} of Fig. 23(a) show large voltage spikes because of the commutation circuit current acting on the stray inductance at the off state. The terminal voltage waveform of S_1 at the off state is shown in Fig. 24(a); the voltage spike $\Delta V_1 \approx 1/4V_{CE1}$. By contrast, the voltage spikes of V_{CE1} and V_{CE2} in Fig. 23(b) are extremely small and insignificant.

The waveform of the terminal voltage of S_1 at the off state for the prototype with the laminated bus bar is shown in Fig. 24(b); the voltage spike $\Delta V_2 \approx 1/8V_{CE1} \approx 1/2\Delta V_1$. $V_L = L \cdot di/dt$; thus, under the same commutation circuit current, the half inductance reduces the switch voltage spikes by half. This outcome is consistent with the results of the loop inductance simulation. It also shows that the laminated bus bar effectively reduces the loop stray inductance of the T-type converter and that the turn-off voltage spike is significantly suppressed. Reducing the conduction EMI of the converter and improving its electromagnetic compatibility are favorable.

VI. Conclusions

The complex stray inductances distributed within T-type converters affect the terminal voltages V_{CE} of switches in different ways. The stray inductance of the capacitor bank bus mainly causes the resonance of V_{CE} at a high voltage level during the off state of the switch. The stray inductances of the power module, power module bus, connection bus, and

TABLE V
INTERNAL INDUCTANCE OF THE POWER MODEL

Terminal	L(nH)
P-N	40
P-M	33
M-N	33

electrolytic capacitor cause the voltage spikes of V_{CE} when the switch is turned off. The laminated bus bar design can effectively reduce the stray inductance of the bus. In this work, we develop a simulation and a physical design of a laminated DC bus bar in a T-type three-level converter with RB-IGBTs. Two 10 kVA experimental prototypes using non-laminated and laminated bus bars are built. The comparative experimental results show that the laminated bus bar design can significantly reduce the stray inductance of the commutation circuit of T-type converters and effectively suppress the turn-off voltage spikes of power devices. The experimental results verify the accuracy of the simulation and design. The laminated bus bar design can effectively reduce the conducted EMI and voltage stress of converters. It can also reduce system cost and improve system reliability.

APPENDIX

The internal inductance of the power model (refer to the data sheet of 4MBI300VG-120R-50, http://www.fujielectric.com /products/semiconductor) is shown in Table V.

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