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SymBIST: Symmetry-Based Analog and Mixed-Signal Built-In Self-Test for Functional Safety

Antonios Pavlidis, Marie-Minerve Louërat, Eric Faehn, Anand Kumar, and Haralampos-G. Stratigopoulos, *Member, IEEE*

***Abstract*—We propose a Built-In Self-Test (BIST) paradigm for analog and mixed-signal (A/M-S) Integrated Circuits (ICs), called symmetry-based BIST (*SymBIST*). *SymBIST* exploits inherent symmetries in an A/M-S IC to construct signals that are invariant by default, and subsequently checks those signals against a tolerance window. Violation of invariant properties points to the occurrence of a defect or abnormal operation. *SymBIST* is designed to serve as a functional safety mechanism. It is reusable ranging from post-manufacturing test, where it targets defect detection, to on-line test in the field of operation, where it targets low-latency detection of transient failures and degradation due to aging. We demonstrate *SymBIST* on a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). *SymBIST* features high defect coverage, short test time, low overhead, zero performance penalty, and has a fully digital interface making it compatible with modern digital test access mechanisms.**

***Index Terms*—Analog and mixed-signal integrated circuit testing, built-in self-test, design-for-test, defect-oriented test, defect simulation, on-line test, concurrent error detection.**

I. INTRODUCTION

The purpose of Built-In Self-Test (BIST) is to migrate part of the functionality of the Automated Test Equipment (ATE) onto the chip with the aim to facilitate test and reduce test cost. At an abstract level, BIST consists of (a) embedded test instruments, whose role is to generate test stimuli, perform measurement acquisition, and process measurements for building a comprehensive test response, and (b) a mechanism for accessing and controlling these test instruments from external pins. BIST can be defect-oriented, in which case it targets the detection of structural defects, or functional, in which case it targets measuring performances that are promised in the datasheet of the Integrated Circuit (IC).

Functional safety refers to the requirement to: (a) avoid IC malfunctions in the field by following robust design guidelines; (b) perform comprehensive post-manufacturing testing with proven high defect coverage and effective outlier screening; (c) detect reliability hazards in the field before failures occur; (d) prevent failures in the field that could be detrimental; (e) detect failures in the field when they occur; (f) adding automatic protection to control failures when they occur in the field and recovering from them at an acceptable time span using fault-tolerance, self-repair, or self-healing principles; (g) ensure correct and uninterrupted operation in response to all inputs even under non-intended use or sometimes even misuse. Functional safety is regulated by standards depending on the application domain, e.g. ISO 26262 for automotive.

Nowadays, the number of ICs used in safety- and mission-critical applications, i.e., automotive, smart health-care, defense, critical infrastructure, etc., is ever increasing. This implies that more ICs should be equipped with functional safety mechanisms. Moreover, modern systems include increasing numbers of ICs, i.e., the number of ICs in a typical automobile today exceeds 400 and continues to increase. This implies that the functional safety of individual ICs must increase to prevent decrease in the system's functional safety. More specifically, it is desired that test escapes are in the order of sub-ppm [1].

Functional safety has emerged as a new major application domain for BIST. In this context, BIST can help gaining better insight into the IC and improving defect coverage. In fact, many case studies have shown that the standard specification tests performed on an ATE offer no guarantee to meet the quality requirement [2]. A defect is always considered a potential threat and reliability hazard. An IC with a detected defect should be preferably discarded for safety reasons [1], [3], [4]. Even if from a functional viewpoint the performance complies with the specifications promised in the datasheet during post-manufacturing test time, e.g. time zero of the application, a defect may manifest itself later in the field of application referred to as a latent defect [5]. For example, it may be triggered in the context of system operation in the field or provoked by environmental stress, i.e., heat, humidity or vibration. To this end, performing defect-oriented BIST on top of the standard specification tests and proving high defect coverage can address safety concerns. Thus, defect-oriented BIST is no longer expected to replace standard specification tests, which was the use case the community was hoping for in the early days, but it aims at enhancing confidence in ICs passing the test. In the same context, a BIST that can be performed on-line in the field concurrently with the application or in idle times can help detecting reliability hazards and failures at the time of occurrence [6]. It is also a key block in feedback loops that enable fault-tolerance, self-repair, or self-healing. Finally, it can facilitate fault diagnosis to understand

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the root-causes of errors towards improving the design and manufacturing processes [7].

It should be mentioned that there are additional approaches towards meeting quality requirements before deployment in the field, i.e., burn-in stress [8] and outlier screening [9]–[11].

Embedding BIST into Analog and Mixed-Signal (A/M-S) ICs is a complex task presenting several challenges. In particular: (a) the BIST circuitry should be transparent to the IC without degrading its performance and without requiring significant re-configuration or re-design; (b) the BIST circuitry should incur low and justifiable area overhead; (c) for defect-oriented BIST the simulation should be fast for enabling large-scale defect simulation in reasonable time and for allowing to perform defect simulation multiple times for several refined BIST versions; (d) for on-line BIST real-time response should be fast for enabling low-latency error detection; (e) the BIST ideally should be flexible and reusable for different IC classes and different architectures within each IC class; (f) the BIST principle ideally should have proven quality before moving to high-volume production; (g) the BIST circuitry should be more robust than the IC having low failure probability, which typically implies that ideally the BIST wrapper should be fully digital; (h) the BIST ideally should be portable from one technology node to another without requiring significant re-design; and (i) the BIST instruments ideally should be interfaced to standard digital test access mechanisms.

In this paper, we propose a generic BIST paradigm for A/M-S circuits, called Symmetry-based BIST or *SymBIST*. *SymBIST*, originally introduced in [12], exploits existing symmetries into the design so as to construct invariant properties that hold true in the error-free case but are violated in the occurrence of a failure. Checkers with tolerance windows are used to monitor the invariant properties and flag an error in case of violation. *SymBIST* can run off-line for post-manufacturing testing or on-line for detecting failures in the field. Off-line mode is defect-oriented, while on-line mode detects errors of various sources, i.e., latent defects, aging, and transient errors. We apply *SymBIST* on a 65nm 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) IP by ST Microelectronics (STM), and we demonstrate that *SymBIST* meets all the aforementioned criteria that make up an effective BIST.

The rest of the paper is structured as follows. In Section II, we present the *SymBIST* concept. In Section III, we provide a review of previous work on A/M-S BIST with a focus on ADCs. In Section IV, we present the SAR ADC case study. In Section V, we show how *SymBIST* successfully applies to our case study. In Section VI, we discuss the defect simulation framework, including the defect modeling and defect simulator. In Section VII, we present the results, including *SymBIST* transient simulations and defect coverage analysis. Section VIII concludes the paper.

II. *SymBIST*

A. *Principle of operation*

As illustrated in Fig. 1, the underlying idea in *SymBIST* is to build invariant signals by monitoring internal nodes, where

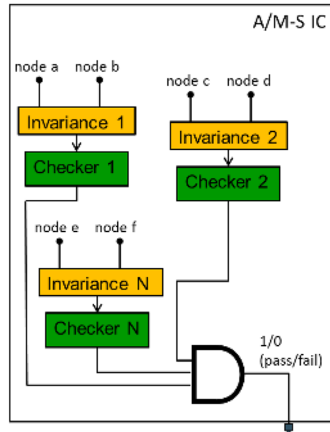

Fig. 1: *SymBIST* principle.

invariance in this context means a signal that by design should be fixed to a default value regardless the input of the circuit. These invariances are monitored by checkers and, if one or more invariances deviate from their default value, then this points to an anomaly in the operation and the corresponding checkers will flag an error. The convention used is that 1/0 checker outputs correspond respectively to pass/fail decision. The checker outputs are connected to an AND gate to provide a single combined 1-bit pass/fail decision.

In practice, the invariant signal is not expected to match exactly its nominal default value due to noise and process, voltage, and temperature (PVT) variations. For this reason, the checkers implement a window comparison and verify that the invariant signal lies within a tolerance window in error-free operation. This tolerance window is set to $[\alpha-\delta, \alpha+\delta]$, where α is the invariant signal nominal value and $\delta > 0$. $\alpha-\delta$ and $\alpha+\delta$ are the lower test limit (LTL) and upper test limit (UTL), respectively. In this case, a checker flags an error when the invariant signal slides outside this window. A first estimate of the parameters α and δ can be computed by performing a Monte Carlo analysis. Specifically α and δ are set to μ and $k \cdot \sigma$, respectively, where μ and σ are the mean and standard deviation, respectively, of the invariant signal across the Monte Carlo runs. The extracted k from Monte Carlo analysis can be fine-tuned taking into account worst-case specifications and environmental conditions. Moreover, the comparison window may shift due to thermal noise. For this reason, as is typical in all test programs, *SymBIST* is repeated several times and a voting scheme is used to decide on pass or fail, similar to averaging of a measurement. If one or more trials result in failure, this points to an outlier device which can be discarded for safety reasons.

Note that the invariance is typically violated by large in the presence of a defect, thus the comparison window can be approximate. This means that the checker, as well as the internally generated reference voltages UTL and LTL, can be of low-precision.

In general, there is a trade-off between false positives, e.g. yield loss, and false negatives, e.g. test escapes, and the coefficient k should be set accordingly to meet the desired trade-off. A low k favors test escape reduction at the expense

of some yield loss, while a high k guarantees high yield at the expense of some test escapes. For improving safety, a defect should be rejected in post-manufacturing even if it does not produce a fault. During on-line test, however, it is critical to reduce the false positive risk. Thus, for on-line test we can envision a larger tolerance window than in post-manufacturing testing. Overall, *SymBIST* can be tuned to result in high defect coverage, i.e. few test escapes, while warranting negligible yield loss.

B. Invariances

Invariances can be built by exploiting symmetries that are inherent to virtually all A/M-S ICs. Such symmetries exist thanks to fully-differential (FD) signal processing [13], complementary signal processing, and replication of identical blocks. Symmetries can also be created artificially with re-configuration using switches, duplication of blocks, or pseudo-duplication of blocks. The goal of pseudo-duplication is to avoid fully replicating an entire block but instead creating a less complex block which produces the same output. In essence, pseudo-duplication constructs two nominally identical signals that are carried via distinct circuit paths. As we will see later, for our case study it was not necessary to perform any re-configuration, duplication, or pseudo-duplication, but we list these techniques as options for applying successfully *SymBIST* to other designs.

For node pairs carrying FD or complementary signals we can build an invariance in the form of $V_1 + V_2 = \alpha$, where V_1 and V_2 are the node voltages. For example, in the case of FD signals, $\alpha = 2V_{\text{cm}}$, where V_{cm} is the common-mode voltage. Notice that differential signaling has been conceived precisely to shield the performance of the circuit from many non-idealities affecting common-mode, i.e. poor power supply, temperature variations, noise, etc., thus deviation in common-mode may be innocuous for the circuit under test. This is taken into account by implementing a tolerance window in the checker operation. In contrast, a defect affecting the operation is expected to invalidate the FD encoding and bring the invariance outside this tolerance window.

For identical blocks, duplicated blocks, or pseudo-duplicated blocks, we can drive them with the same input and build an invariance in the form of $V_1 - V_2 = \alpha$, where in this case V_1 and V_2 are outputs of the two blocks and α has a default value of 0.

The pseudo-duplication concept and checking the FD code were the basis for building perhaps the first ever on-line test mechanisms for analog circuits. Pseudo-duplication techniques have been proposed for time-invariant linear analog circuits, e.g. analog filters. In [14], a strategy is proposed for switched-capacitor filters where a programmable biquad that can mimic every filter stage is configured to monitor successively the filter stages. In [15], the matrices of the state-variable equations are encoded into a continuous checksum which is implemented by small extra hardware. In [16], it is shown how to generate with small extra hardware an estimator that monitors some observable nodes of the circuit and, once fully connected to the circuit, produces an output that converges exponentially fast to the output of the circuit and follows the output for any input change. Analog comparators or checkers that compare duplicate or FD signals with adaptive tolerance windows are proposed in [17], [18].

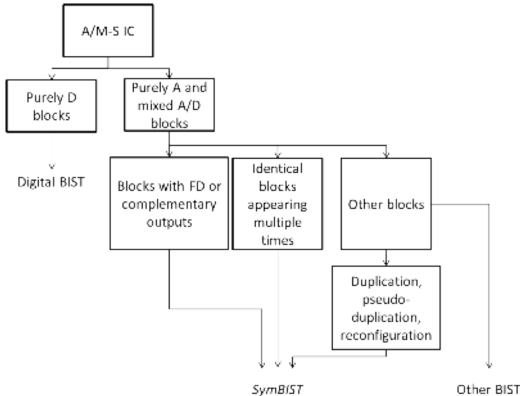

Fig. 2: *SymBIST* strategy.

While *SymBIST* is a generic BIST paradigm and similar invariances based on symmetry can be derived for any A/M-S circuit class, the invariances need to be handcrafted on a circuit by circuit basis and it is likely that distinct invariances can be defined for a given circuit.

C. Strategy

A high-level abstraction of the proposed *SymBIST* strategy is illustrated in Fig. 2. The A/M-S IC is divided into purely digital (D) blocks on one side and analog (A) and mixed analog-digital (A/D) blocks on the other side. We assume that the purely digital blocks are tested with standard digital BIST, i.e., with scan insertion and a combination of stuck-at, bridging, I_{ddq}, and transitional Automatic Test Pattern Generation (ATPG). The A and A/D blocks are divided into three groups. The first two groups include blocks that are FD, they perform single-to-FD conversion, they provide complementary outputs, they appear multiple times, etc. For these blocks invariances exist naturally and the *SymBIST* strategy applies directly. The third group includes the rest of the blocks. For some of the blocks it may be possible to perform re-configuration or pseudo-duplication so as to build invariances and apply the *SymBIST* strategy. We also have the option to perform direct duplication of blocks. For the remaining blocks that are not handled with *SymBIST*, we need to develop other BIST approaches.

D. Modes of operation

SymBIST is designed to serve as a functional safety-mechanism that is reusable starting from post-manufacturing test, where it is defect-oriented targeting the detection of structural defects and screening of outliers, to on-line test in the field of operation, where it targets low-latency detection of transient failures, reliability hazards, and degradation due to aging.

More specifically, the A/M-S IC with embedded *SymBIST* has four possible modes of operation enabled by a signal EN:

$$\text{EN} < 0:1 >= \begin{cases} 00: \textit{SymBIST}\ \text{self-test} \\ 11: \text{off-line test} \\ 10: \text{on-line test} \\ 01: \textit{SymBIST}\ \text{disabled} \end{cases} \quad (1)$$

The first mode consists in a self-test of the *SymBIST* infrastructure. The *SymBIST* infrastructure occupies considerably smaller area on the die compared to the area of the A/M-S IC itself and, thereby, the probability of a defect occurrence within the *SymBIST* infrastructure is considerably smaller compared to a defect occurrence within the A/M-S IC. Nevertheless, a good strategy is to test the *SymBIST* infrastructure first before using it to test the A/M-S IC. For example, a defective checker may result in a misleading test decision for the A/M-S IC, i.e., it can mask a defect within A/M-S IC resulting in a test escape.

The second mode is the off-line test mode that employs *SymBIST* for post-manufacturing defect-oriented test. This mode requires a built-in test stimulus generator and possibly a re-configuration of the A/M-S IC that should be non-intrusive when the A/M-S IC runs in normal mode.

The third mode is the on-line test mode that employs *SymBIST* for concurrent error detection during the normal operation of the A/M-S IC. In this case, the running input in normal operation is used and the checkers monitor the invariances on-the-fly flagging errors in real-time, possibly with some low latency since the error needs to propagate to a pair of nodes that are used for building an invariance.

The fourth and last mode allows switching-off *SymBIST* during normal operation so as to save power. In this case, periodic test can be performed either during normal operation by enabling periodically the on-line test mode or in idle times by enabling the off-line test mode.

III. Related work

There is a large body of literature on A/M-S BIST. In general, A/M-S BIST is proposed for three uses, namely: (a) defect-oriented test; (b) direct on-chip measurement of performances, e.g. functional test; and (c) on-line test, either concurrently with the operation or in idle times. For any of these uses, BIST is in general specific to the circuit class and very often specific to different architectures within a given circuit class. Furthermore, BIST is in general designed and/or demonstrated for one use only.

SymBIST is a generic BIST virtually applicable to any circuit class and is an one-off solution for two uses (a) and (c). For use (a), other generic BIST proposals include topology transformations by inserting pull-up or pull-down transistors [19] and oscillation-based test [20]. For use (c), generic BIST includes duplication or triple modular redundancy, but these approaches are very costly. Cost-effective BIST for use (c) has been proposed only for linear time-invariant circuits [14]–[16] and FD circuit implementations [13], [17], [18].

Existing ADC BIST proposals concern use (b) only, aiming at measuring on-chip dynamic performances [21]–[29], i.e. signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), etc., static performances [30]–[35], i.e. DNL, INL, etc., or variations of important design variables [36]. A simulation flow to examine the equivalence of BIST to the standard performance measurement procedure is proposed in [37]. No ADC BIST has been demonstrated for use (a). The reason is that ADC simulation time is prohibitively long to be able to run large-scale defect simulation. *SymBIST* achieves this objective since as we will see the test is completed extremely fast in only 2.67x the time to convert an analog input sample. Furthermore, no ADC BIST has been demonstrated for use (c). *SymBIST* achieves this objective since it consists in monitoring invariances that should hold true in error-free operation irrespective of the ADC input.

IV. Case study

Our case study is a 65nm 10-bit SAR ADC IP by STM. In section IV-A, we provide a brief overview of the operation principle of SAR ADCs. The reader is referred to a textbook for a more complete treatment of SAR ADCs [38]. In Section IV-B, we will give a concise top-down description of the architecture of the SAR ADC IP.

A. SAR ADC principle

The SAR ADC is used in applications that require low power consumption and medium conversion rate, such as data acquisition. The high-level architecture of a SAR ADC is shown in Fig. 3. In order to process rapidly changing signals, SAR ADCs have an input sample-and-hold (S&H) to keep the signal constant during the conversion cycle. The conversion cycle takes $n+2$ clock periods, where n is the number of bits or resolution and the extra two clock periods are for sampling and capturing the n-bit digital output. In each clock period, one bit is determined, starting from the Most Significant Bit (MSB) and continuing in each clock period to the next MSB. In each bit conversion, the input voltage is compared to a comparison level created from a Digital-to-Analog Converter (DAC), and the outcome of this comparison determines whether the bit will be set to 1 or 0. The SAR Logic controls the DAC and also sets the bit resulting from the comparison. In the first clock period of a conversion cycle, the comparison level from the DAC is set to the midscale voltage $V_{\text{FS}}/2$, where V_{FS} is the full scale voltage, and the comparison with the input voltage determines the MSB $B[n]$. In the second clock period, the comparison level is set to $3V_{\text{FS}}/4$ if $B[n]=1$ or to $V_{\text{FS}}/4$ if $B[n]=0$ and the comparison with the input voltage determines the MSB-1 $B[n-1]$. In the third clock period, the comparison level is set to $7V_{\text{FS}}/8$ if $B[n]B[n-1]=11$, to $5V_{\text{FS}}/8$ if $B[n]B[n-1]=10$, to $3V_{\text{FS}}/8$ if $B[n]B[n-1]=01$ or to $V_{\text{FS}}/8$ if $B[n]B[n-1]=00$, and the comparison determines the MSB-2 $B[n-2]$. For n bits, the DAC implements 2^n-1 comparison levels. The conversion continues until all n bits are determined, in which case a new input sample is held and a new conversion cycle begins.

B. SAR ADC IP

The top-level architecture of the 10-bit SAR ADC IP is illustrated in Fig. 4. The circuit accepts a FD analog input ΔIN = IN+ − IN- with a peak-to-peak voltage 2*VREFP=

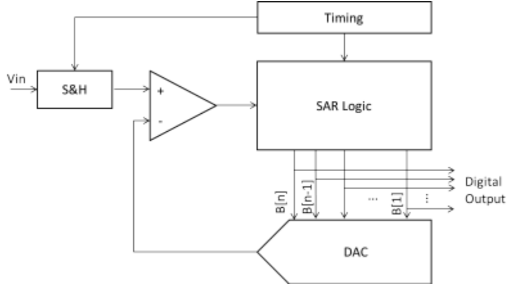

Fig. 3: High-level architecture of a SAR ADC.

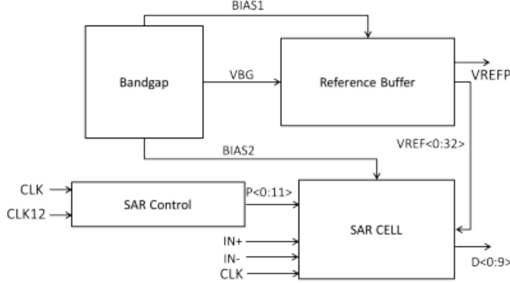

Fig. 4: Top-level architecture of the SAR ADC IP.

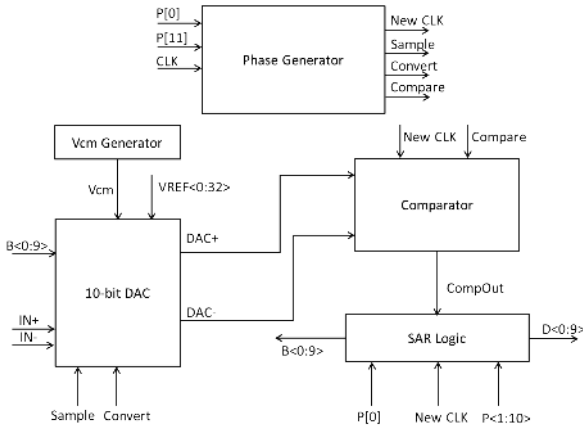

Fig. 5: SARCELL block architecture.

$1V$, where VREFP is nominally $0.5V$. The common mode of the two inputs IN+ and IN- is VDD$/2 = 0.6V$, where VDD$= 1.2V$ is the power supply. CLK is the master clock of the ADC with frequency $f_{clk} = 156$ MHz and CLK12 is the conversion clock of the ADC with frequency $f_{clk12} = f_{clk}/12$. The 10-bit digital output is denoted by D$< 0 : 9 >$. The top-level blocks are as follows:

SARCELL: It is the main block of the SAR ADC which implements the architecture in Fig. 3.

SAR Control: It creates 12 pulses P$< 0 : 11 >$ used to control the sampling, conversion, and digital output capture phases in the SARCELL.

Bandgap: It creates the required biasing for all the blocks of the SAR ADC.

Reference Buffer: It creates the comparison levels VREF$< 0 : 32 >$ that are used by the DAC during the conversion. As we will see below, the DAC is a combination of two sub-DACs with a 5-bit digital input each. Thus, each sub-DAC can set $2^5 - 1 = 31$ comparison levels. VREF[1] to VREF[31] denote these comparison levels, VREF[0]=GND, and VREF[32]=VREFP. The midscale voltage is VREF[16]. These voltages are generated from a resistive ladder with 32 equal resistors forming a voltage divider. Therefore, VREF[k]=$\frac{k}{16}$VREF[16], $k = 1, \cdots, 32$.

The SARCELL block comprises the following blocks as illustrated in Fig. 5:

Phase Generator: It controls the timing of the ADC operation by generating the phases for sampling, comparison, conversion, etc.

V_{cm} Generator: It generates the common mode voltage V_{cm} used inside the DAC.

SAR Logic: It controls the conversion process by providing the digital input to the DAC, it stores the result of each comparison, and provides the digital output once the conversion is completed.

10-bit DAC: The DAC is a resistive plus charge redistribution DAC. As shown from its architecture in Fig. 6, it is composed of two structurally identical sub-DACs, namely SUBDAC1 and SUBDAC2, with a 5-bit digital input each, and a SC array. The sampling operation is performed within the DAC. SUBDAC1 converts the 5 MSBs to comparison levels M+ and M-, while SUBDAC2 converts the 5 LSBs to comparison levels L+ and L-. The Boolean functions implemented by SUBDAC1 and SUBDAC2 are given by:

$$\begin{aligned}
\text{M+} &= \text{VREF}[\sum_{j=5}^{9} B[j] \cdot 2^{j-5}] \\
\text{M-} &= \text{VREF}[32 - \sum_{j=5}^{9} B[j] \cdot 2^{j-5}] \\
\text{L+} &= \text{VREF}[\sum_{j=0}^{4} B[j] \cdot 2^{j}] \\
\text{L-} &= \text{VREF}[32 - \sum_{j=0}^{4} B[j] \cdot 2^{j}]
\end{aligned} \tag{2}$$

Let $x(i)$ denote the value of signal x at the i-th conversion cycle. It can be shown that the difference between the DAC output voltages DAC+ and DAC- is given by:

$$\begin{aligned}
\Delta\text{DAC}(i) = \frac{1}{\sum_{k=1}^{3} C_k} \Big[& C_1 \cdot \Delta\text{M}(i) + C_2 \Delta\text{L}(i) \\
& - C_1 \Delta\text{IN} + C_2 \cdot (\text{VREF}[32] - \text{VREF}[0]) \Big]
\end{aligned} \tag{3}$$

where $\Delta\text{M}(i) = \text{M+}(i) - \text{M-}(i)$ and $\Delta\text{L}(i) = \text{L+}(i) - \text{L-}(i)$. The capacitors are $C_1 = 32C_U$, $C_2 = C_U$, and $C_3 = 16C_U$, where C_U is the unit capacitor. C_1 and C_3 are implemented with capacitor banks.

Comparator: It compares the two outputs of the DAC and the outcome of the comparison is driven to the SAR Logic block in order to set the corresponding digital bit. The block-level architecture of the comparator is shown Fig. 7. It comprises a pre-amplifier, a comparator latch, an RS latch, and a offset compensation circuit for the pre-amplifier.

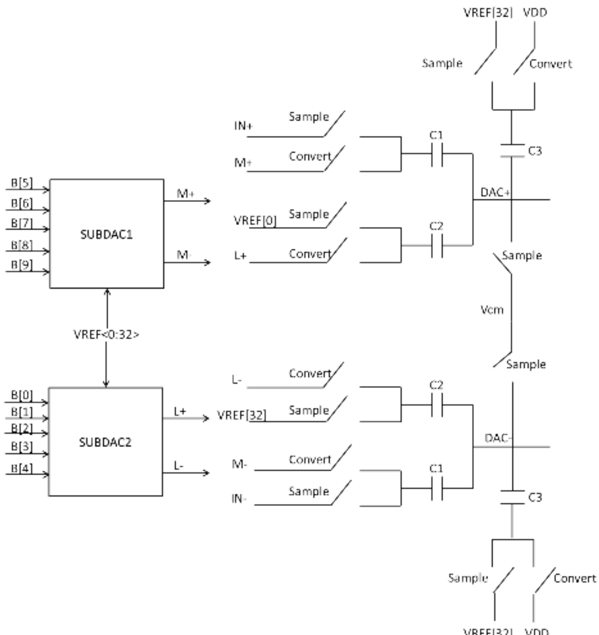

Fig. 6: 10-bit DAC block architecture.

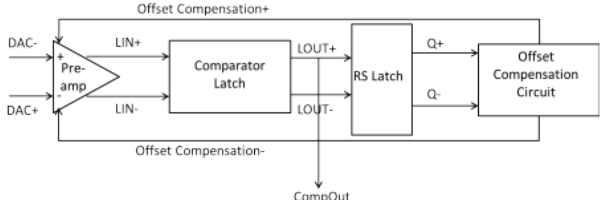

Fig. 7: Comparator block architecture.

A conversion cycle starts with setting the sample signal high, which samples the FD input signal by charging the capacitors C_1 inside the DAC. Next, the sample signal becomes low and the convert signal becomes high. The SAR Logic assigns B[9]=1 while all the other bits B[j], $j < 9$, are kept at 0. In this case, M+(1) = M-(1) = VREF[16], L+(1) = VREF[0], and L-(1) = VREF[32], which gives $\Delta\text{DAC}(1) = -\frac{C_1}{\sum_{k=1}^{3} C_k}\Delta\text{IN}$ from Eq. (3). Therefore, the comparator checks the sign of the FD input and if it is positive the SAR Logic block sets B[9]=1, otherwise if it is negative the SAR Logic block sets B[9]=0. The bit B[9] is kept fixed for the rest of the conversion. In the next conversion cycle, the SAR Logic block assigns B[8]=1, while all the other bits B[j], $j < 8$, are kept at 0. If B[9]=1, then M+(2) = VREF[24], M-(2) = VREF[8], L+(2) = VREF[0], and L-(2) = VREF[32], which gives $\Delta\text{DAC}(2) = \frac{C_1}{\sum_{k=1}^{3} C_k}\left[(\text{VREF}[24] - \text{VREF}[8]) - \Delta\text{IN}\right]$ from Eq. (3). Since VREF[24] − VREF[8] = VREF[16], the comparator compares VREF[16] − ΔIN to 0. If B[9]=0, then it can be shown from Eq. (3) that $\Delta\text{DAC}(2) = \frac{C_1}{\sum_{i=k}^{3} C_k}\left[(\text{VREF}[8] - \text{VREF}[24]) - \Delta\text{IN}\right]$, that is, the comparator compares −VREF[16] − ΔIN to 0. In other words, in this second conversion cycle the comparator compares |ΔIN| to VREF[16]. In the third conversion cycle, it can be shown from Eq. (3) that the comparator compares |ΔIN| to VREF[24] = 3VREF[16]/2 if B[8]=1 or to VREF[8] = VREF[16]/2 if B[8]=0, and so forth. When the 10 conversion cycles are completed, the digital output D$< 0 : 9 >$=B$< 0 : 9 >$ is driven at the output pins.

V. *SymBIST* APPLIED TO SAR ADC IP

A. Invariances

We observe that the two sub-DACs within the DAC are structurally identical, each sub-DAC has complimentary outputs, the SC array has symmetrical paths, the pre-amplifier is FD, and the comparator and RS latches have complimentary outputs. Based on these observations, we can build the following invariances that hold true for any FD input ΔIN and at every conversion cycle.

1) SymBIST1: By construction, as shown from Eq. (2), the outputs of the two sub-DACs regardless of their inputs take complimentary values. Therefore, the following two invariances should always hold true:

$$\text{M+}(i) + \text{M-}(i) = \text{VREF}[32] \tag{4}$$

$$\text{L+}(i) + \text{L-}(i) = \text{VREF}[32] \tag{5}$$

These invariances can flag failures within the circuitry of the two sub-DACs. In addition, since all comparison levels VREF[j], $j = 0, \cdots, 32$, are used by the DAC, as shown from Eq. (2), these invariances can also flag failures within the bandgap and reference buffer.

2) SymBIST2: It can be shown that the sum of the DAC output voltages is given by:

$$\begin{aligned}&\text{DAC+}(i) + \text{DAC-}(i) = \\ &2V_{\text{cm}} + \frac{1}{\sum_{k=1}^{3} C_k}\Big[C_1 \cdot (\text{M+}(i) + \text{M-}(i)) - C_1 \cdot (\text{IN+} + \text{IN-}) \\ &\quad + C_2 \cdot (\text{L+}(i) + \text{L-}(i)) - C_2 \cdot (\text{VREF}[32] - \text{VREF}[0]) \\ &\quad + 2C_3 \cdot (\text{VDD} - \text{VREF}[32])\Big]\end{aligned} \tag{6}$$

Using Eqs. (4)-(5), substituting $C_3 = C_1/2$, and considering that IN+ + IN- = VDD, Eq. (6) gets simplified as follows:

$$\text{DAC+}(i) + \text{DAC-}(i) = 2V_{\text{cm}} \tag{7}$$

This invariance can flag failures within the complete DAC, including the sub-DACs and the SC array, within the circuits that provide the voltage references to the DAC, i.e. V_{cm} generator and reference buffer, as well as within the bandgap that provides the biasing to the reference buffer.

3) SymBIST3: Thanks to the FD structure of the pre-amplifier within the comparator, the following invariance should be satisfied at the outputs of the pre-amplifier regardless of the difference ΔDAC(i) being amplified:

$$\text{LIN+}(i) + \text{LIN-}(i) = 2V_{\text{cm2}} \tag{8}$$

where LIN+ and LIN- are the FD outputs of the pre-amplifier and V_{cm2} is the common mode at the outputs of the pre-amplifier. This invariance can flag failures within the pre-amplifier and the offset compensation circuit, as well as within the bandgap that provides the biasing to these circuits.

Blocks	*Sym-BIST1*	*Sym-BIST2*	*Sym-BIST3*	*Sym-BIST4*	Digital BIST
SAR Control					X
Phase Generator					X
SAR Logic					X
Bandgap	X	X	X		
Reference Buffer	X	X			
SUBDAC1	X	X			
SUBDAC2	X	X			
SC Array	X	X			
V_{cm} Generator		X			
Pre-amplifier			X		
Comparator Latch				X	
RS Latch				X	
Offset compensation circuit			X	X	

TABLE I: Matrix showing correspondence between BIST approaches and SAR ADC IP blocks.

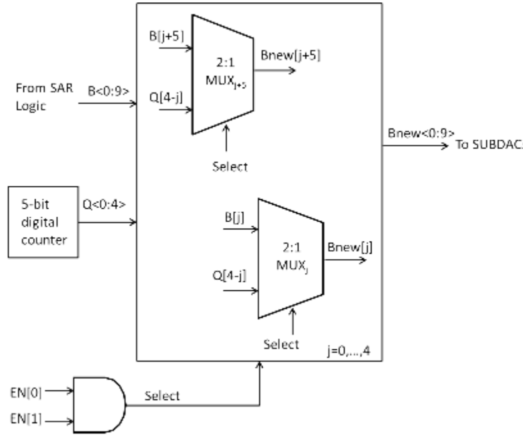

Fig. 8: Re-configuration for applying the test stimulus in off-line test mode.

4) SymBIST4: More tests can be constructed for the comparator latch and RS latch within the comparator block by checking the invariances:

$$\text{Q+}(i) + \text{Q-}(i) = \text{VDD} \tag{9}$$

$$\text{sgn}\left(\text{Q+}(i) - \text{Q-}(i)\right) - \text{sgn}\left(\text{LIN+}(i) - \text{LIN-}(i)\right) = 0 \tag{10}$$

where $\text{sgn}(\cdot)$ denotes the sign function and Q+ and Q- are the complementary outputs of the RS latch. This invariance can flag failures within the comparator latch, RS latch, and offset compensation circuit.

Table I summarizes the BIST approaches corresponding to the different blocks of the SAR ADC IP. BIST approaches are divided into *SymBIST* for the A/M-S blocks and digital BIST for the purely digital blocks, namely the SAR control, phase generator, and SAR Logic. As it can be seen, the 6 *SymBIST* invariances in Eqs. (4)-(5) and (7)-(10) are capable of covering the complete A/M-S part of the SAR ADC IP.

B. Test stimulus and re-configuration in off-line test mode

The same test stimulus is used to exercise all the invariances. It is composed of a static and a dynamic part. The static part is a DC value applied to the input of the ADC which can be set arbitrarily. Herein, we use $\Delta\text{IN} = 0.1V$. The dynamic part is a digital signal applied to the input of the two sub-DACs. In particular, a 5-bit digital counter is used that cycles through all possible 2^5 bit combinations. The rationale of this dynamic part of the test stimulus is that it activates all components within the DAC and also extensively exercises the comparator since various differences $\Delta\text{DAC}(i)$ are generated at its input. The components within the bandgap and reference buffer are also activated since during this test all comparison levels $\text{VREF}[j]$, $j = 0, \cdots, 32$, are used within the DAC, as shown from Eq. (2). The V_{cm} Generator is checked directly with the invariance in Eq. (7).

The non-intrusive re-configuration to enable the off-line test mode is shown in Fig. 8. 2:1 multiplexers are used to switch the input of the sub-DACs, denoted by Bnew$< 0 : 9 >$, between the SAR Logic output B$< 0 : 9 >$ and the 5-bit digital counter output, denoted by Q$< 0 : 4 >$. During normal operation, which includes the on-line test mode, e.g. EN$< 0 : 1 >$=10, or the disabling of *SymBIST*, e.g. EN$< 0 : 1 >$=01, the 5-bit digital counter is disconnected, e.g. Bnew$< 0 : 9 >$=B$< 0 : 9 >$. In off-line test mode, i.e. EN$< 0 : 1 >$=11, the 5-bit digital counter drives simultaneously both sub-DACs. In our experiments, we observed that randomly cycling through the 2^5 bit combinations at the inputs of the sub-DACs, as opposed to incremental counting, results in higher defect coverage. Intuitively, this is because the two sub-DACs are exercised more intensively generating large steps at their outputs. Fig. 8 shows the configuration that was implemented, e.g. Bnew[j+5]=Q[4-j] for SUBDAC1 and Bnew[j]=Q[4-j] for SUBDAC2, $j = 0, \cdots, 4$. For example, for SUBDAC1, the input sequence is $\{2^4, 2^3, 2^4 + 2^3, 2^2, 2^2 + 2^4, \cdots\}$.

C. Checker design

Invariances are of two types, e.g. one type $V_1 + V_2 = \alpha$ which concerns invariances in Eqs. (4)-(5) and (7)-(9), and one type $V_1 - V_2 = 0$ which concerns the invariance in Eq. (10). A dedicated checker is designed for each type.

Fig. 9 shows the checker design for the invariances of type $V_1 + V_2 = \alpha$. A straightforward design would be based on a summing amplifier. Herein, we propose a simplified design to reduce the area of the checker. In particular, let V_j=$V_j^{DC} + v_j$, where V_j^{DC} denotes the large-signal DC quantity and v_j denotes the small-signal AC quantity of V_j, $j = 1, 2$. The proposed checker is composed of four stages. The first stage includes two buffers implemented with two source follower amplifiers using identical PMOS transistors M1 and M2. The buffers are used so as to avoid loading the nodes that are being monitored. The second stage is a voltage divider, where $R_2 \gg R_1$, that generates the signal V_o:

$$V_o = f(V_1^{DC}, V_2^{DC}) + G \cdot (V_1 + V_2), \tag{11}$$

where

$$f(V_1^{DC}, V_2^{DC}) = \left(V_{DD} - \frac{R_1}{2}\left(I_1^{DC} + I_2^{DC}\right)\right) - G \cdot (V_1^{DC} + V_2^{DC}), \tag{12}$$

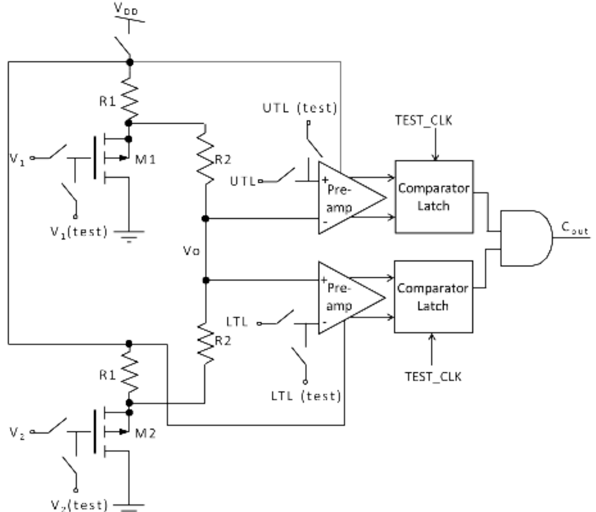

Fig. 9: Checker design for the invariances in Eqs. (4)-(5) and (7)-(9).

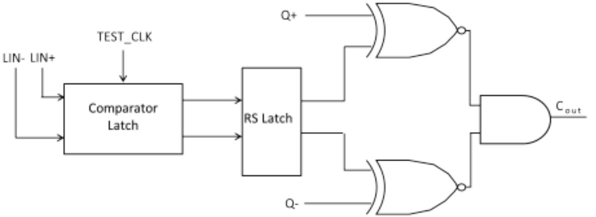

Fig. 10: Checker design for the invariance in Eq. (10).

$$G = \frac{g_m R_1}{2(g_m R_1 + 1)}, \tag{13}$$

g_m denotes the transconductance of transistors M1 and M2, and I_1^{DC} and I_2^{DC} denote the DC biasing currents of transistors M1 and M2, respectively. Ideally, in error-free operation, V_o is a DC signal with value $V_o = f(V_1^{DC}, V_2^{DC}) + G \cdot \alpha$. A defect will shift the DC component of V_o and/or will add an AC component to it. The third stage includes two comparators that compare V_o to the test limits UTL=$\mu + k\sigma$ and LTL=$\mu - k\sigma$, where μ and σ are the mean and standard deviation of V_o computed over several Monte Carlo runs and over the 2^5 values observed during the duration of the test stimulus for each Monte Carlo run. The UTL and LTL are generated internally using resistor voltage dividers. Note that the comparison window defined by the lower and upper test limits eliminates false positives due to noise and PVT variations within both the SAR ADC and the first two stages of the checker. The fourth stage passes the outputs of the two comparators through an AND gate to obtain a checker output C_{out} in the form of an 1-bit pass/fail response. When the invariance is satisfied, i.e. V_o lies within the range defined by the test limits, the output of the checker is high, e.g. $C_{\text{out}} = 1$, whereas when the invariance is violated the output of the checker is low, e.g. $C_{\text{out}} = 0$. Fig. 9 also shows the insertion of switches to disconnect the checker when *SymBIST* is disabled or to set the checker into self-test mode.

Fig.10 shows the checker design for the invariance in Eq. (10). It monitors the LIN+ and LIN- outputs of the pre-amplifier and the outputs Q+ and Q- of the RS latch within the comparator in the SARCELL block. It is easy to verify that $C_{\text{out}} = 1$ when the invariance in Eq. (10) holds true and $C_{\text{out}} = 0$ when it is violated. Note that this checker does not implement a tolerance window since the invariance is constructed from digital signals.

Given that the checker design for the invariances in Eqs. (4)-(5) and (7)-(9) is identical, we have two options. The first option is to use a single checker and use it to check these invariances sequentially by using corresponding test limits. The second option is to use one checker per invariance, thus checking the invariances in parallel. In off-line test mode, the first option offers a trade-off between area overhead and test time. However, in on-line test mode, the first option has the disadvantage that a transient error may be detectable by a unique invariance that is momentarily not being checked when the transient error occurs. In our implementation, we adopted the second option.

D. Checker self-test

As discussed in Section II-D, it is advised to test the *SymBIST* infrastructure prior to its usage for testing the ADC itself. This is desired especially for the checker in Fig. 9 whose first three stages are analog and, thereby, less robust. To this end, we propose to implement a simple sequence of DC tests to exercise this checker, in order to first decide on its health status prior to its usage. More specifically, referring to Fig. 9, we can assume different DC test stimuli for the four checker inputs, i.e. V_1, V_2, UTL, and LTL. A set of possible convenient DC values are $V_1 = \{\text{GND}, \text{VREF[32]}, \text{VDD}\}$, $V_2 = \{\text{GND}, \text{VREF[32]}, \text{VDD}\}$, and $k = \{3, 5\}$, where VREF[32] can be drawn directly from the reference buffer. A test uses a combination of such DC values. For each test, the checker is expected to give a high or low output. A flipped output points to a faulty checker. The goal is to create a minimum sequence of N tests that achieves sufficiently high defect coverage for the checker. Fig. 9 includes the addition of switches for the self-test mode of the checker. All checkers can be tested in parallel, thus the checker self-test time is $N \cdot (1/f_{clk}) = N \cdot 6.41ns$.

E. SymBIST test time in off-line test mode

In the off-line test mode, all invariances are checked in parallel. The maximum duration of the test is fixed. It equals $2^5 \cdot (1/f_{clk}) = 0.205\mu s$ which is the full duration of the dynamic part of the test stimulus consisting of applying all 2^5 possible bit combinations at the inputs of the two sub-DACs. A checker examines whether the corresponding 2^5 samples of the invariant signal lie within the comparison window and flags an error if this condition is violated. If we use stop-on-detection, e.g. stop the test when the condition is violated, then the duration of the test is smaller for defective devices. Each conversion cycle, e.g. the time to convert one analog input sample, is $(1/f_{clk12}) = 0.0769\mu s$. Thus, the maximum off-line test time is 2.67x the time to convert one analog input sample, which is extremely low and is key also for performing a large-scale defect simulation in reasonable time.

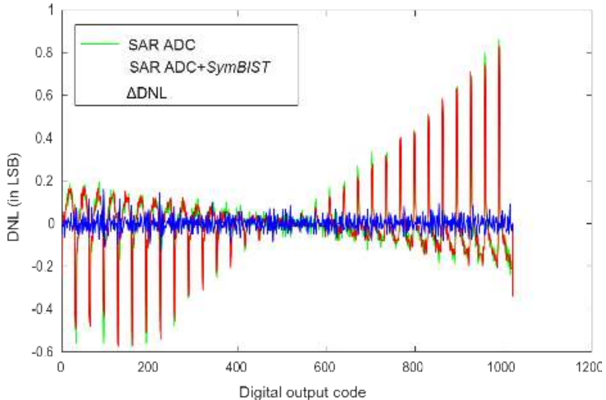

Fig. 11: DNL of original design and design with embedded *SymBIST*.

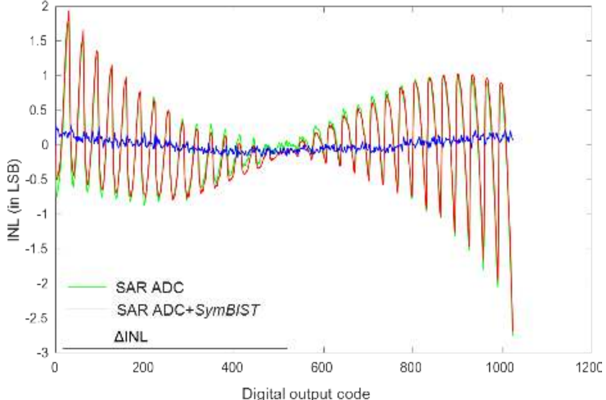

Fig. 12: INL of original design and design with embedded *SymBIST*.

F. Test access and control mechanism

The mode of operation is set by the 2-bit signal EN, the test stimulus in off-line test mode is digital and is generated internally, the checker self-test uses DC stimuli generated internally while the checker response is digital, and finally *SymBIST* outputs a 1-bit pass/fail test decision. Thus, *SymBIST* can be interfaced to a digital test access and control mechanism based on two external pins which is the minimum [39].

G. Overhead

The *SymBIST* infrastructure comprises the 5-bit digital counter used in the off-line test mode, multiplexers to re-configure the design in the off-line test mode, switches to enable the different modes of operation, and 6 checkers, e.g. one checker per invariance. The multiplexers are inserted in a digital signal path between the SAR Logic and 10-bit DAC, the checker in Fig. 9 taps into nodes via switches and include buffers as a first stage, and the checker in Fig. 10 is digital. Therefore, the modifications are non-intrusive to the design and no design re-iterations are required. To confirm that *SymBIST* does not incur any performance penalty, we simulated at transistor-level the differential non-linearity (DNL) and integral non-linearity (INL) for the original design and the design with embedded *SymBIST* using a ramp histogram test [40]. The result is shown in Figs. 11 and 12, which also include the Δ of the DNL and INL curves. As it can be seen, the forms of the curves are similar and practically there is no change in the maximum observed DNL and INL values. Finally, from the layout of the SAR ADC IP that is available, and noticing that the checkers are built using existing blocks of the SAR ADC IP, i.e., pre-amplifier, comparator latch, and RS latch, we estimate the area overhead between 5% and 10%.

VI. Defect coverage estimation framework

The fast response of *SymBIST* for the SAR ADC IP in off-line test mode is key for performing a large-scale defect simulation campaign to assess defect coverage. As the SAR ADC IP is a large-size circuit, we rely on the Tessent®DefectSim mixed-signal defect simulator by Mentor®, A Siemens Business [3], to perform defect simulation at transistor-level in an automated workflow.

A. Defect model

We make a single fault assumption, that is only one defect will occur at a time.

We adopt a standard defect model, which is also the default defect model used by the Tessent®DefectSim tool [3]. In particular, for MOS transistors traditionally six defects are injected, i.e., shorts across gate-to-source, gate-to-drain, and drain-to-source, and opens in each terminal. However, all shorts have a similar effect on the transistor being stuck-on and all opens have a similar effect on the transistor being stuck-off. Thus, for MOS transistors we use only gate open and drain-to-source short defects, as suggested in [3]. Similarly, for Bipolar transistors, we consider base open and collector-emitter short defects. For diodes, we consider open and short defects. Regarding shorts, the defect resistance varies in practice. To avoid simulating many defects, we consider the default resistance of 10Ω. Regarding opens, a weak pull-up or pull-down is assigned to each open defect to account for the facts that an ideal open does not exist and, besides, it cannot be handled by a SPICE simulator [3]. For example, for MOS transistors, we rely on the modeling approach in [41] where V_{GS} is a voltage controlled by V_{DS} with a gain proportional to $C_{\mathrm{gdo}}/W \cdot L \cdot C_{\mathrm{ox}}$. For simplicity, the gain coefficient is set to the default value of 0.5. For passive elements, i.e. resistors and capacitors, we consider $\pm 50\%$ variations.

B. Defect simulator

Defects are assigned a relative likelihood of occurrence that is estimated by combining global defect-type likelihoods, i.e. the likelihood of short-circuits is typically higher than the likelihood of open-circuits, and component-specific likelihoods, i.e. the expected component area on the layout, as explained in [3]. For this reason, we report the Likelihood-Weighted (L-W) defect coverage computed by the tool. L-W defect coverage is essentially the percentage of detected defects over the total number of defects, likelihood-weighted according to the likelihood of occurrence of defects.

To reduce defect simulation time, we use the stop-on-detection and Likelihood-Weighted Random Sampling (LWRS) [42] options of the tool. With the stop-on-detection

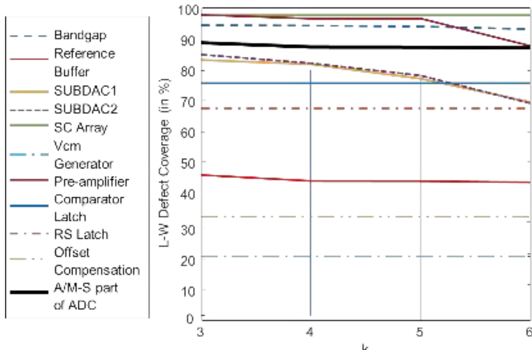

Fig. 13: L-W defect coverage as a function of tolerance window placement.

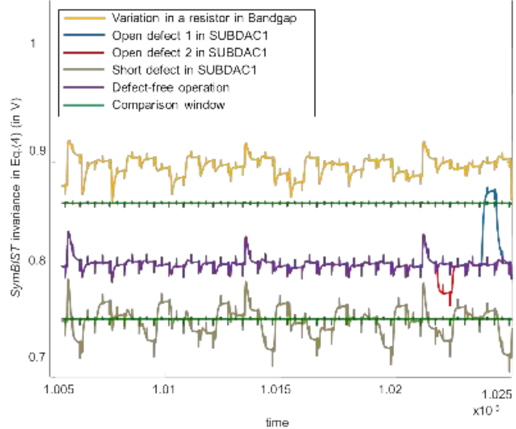

Fig. 14: Transient simulation of *SymBIST* invariance in Eq. (4) for different defect scenarios.

option, while defect simulation progresses, the simulation of a defect is stopped as soon as an invariance violates the tolerance window and the simulation of the next defect in the list begins. The LWRS option reduces the number of defects to be simulated by sampling a user-defined target number of defects based on the relative likelihood of defect occurrence. When the LWRS option is used, the 95% confidence interval of the L-W defect coverage is also reported by the tool.

VII. Results

A. Checker self-test

We performed a defect simulation of the checker considering all possible defects within the checker for a total of 176 defects. We considered sequences of DC tests that use the 18 different combinations of DC values for the four checker inputs, namely V_1, V_2, UTL, and LTL, as discussed in Section V-D. The resultant L-W defect coverage is 94.45%. Thereafter, we searched to eliminate tests such that the set of retained tests achieves the same fault coverage. It turns out that N=3 tests suffice to achieve the same fault coverage. These are: $\{\mathrm{V}_1, \mathrm{V}_2, k\}$=$\{\mathrm{VDD}, \mathrm{VDD}, 3\}$, $\{\mathrm{VREF[32]}, \mathrm{GND}, 3\}$, $\{\mathrm{GND}, \mathrm{GND}, 3\}$.

B. Setting the comparison window for desired test coverage vs. yield loss trade-off

Herein, we study the effect of the width of the comparison window, which is set by the coefficient k, on the trade-off between yield loss and defect coverage.

Fig. 13 shows the L-W defect coverage values achieved with *SymBIST* for the individual blocks of the SAR ADC IP and for its complete A/M-S part as a function of k, where k is varied from 3 to 6. μ and σ are computed based on a defect-free Monte Carlo analysis with 100 runs. For simplicity, Fig. 13 does not include the 95% confidence intervals.

As it can be seen, the expected drop of L-W defect coverage as we increase k is evident only for three blocks, namely the pre-amplifier and the two sub-DACs, while for the rest of the blocks the curves are practically flat and for the entire A/M-S part only a slight drop is observed. This implies that the majority of the detectable defects result in substantial deviation of the invariance outside its tolerance window, thus by enlarging the window we can reduce yield loss probability without inadvertently increasing test escapes. The fact that the L-W defect coverage curve of the A/M-S part does not follow the drop observed for the pre-amplifier and the two sub-DACs is due to LWRS. In particular, defects within these blocks have lower likelihood of occurrence compared to defects in other blocks and, thereby, they are less frequently sampled to estimate the L-W defect coverage of the A/M-S part.

The observed L-W defect coverage curve of the A/M-S part helps us to draw two important conclusions. First, as already mentioned, we can use a wide comparison window to minimize yield loss without affecting defect coverage. In this regard, a value of $k = 5$ is a good compromise since it guarantees a negligible yield loss. Having verified that invariant signals follow a normal distribution, for $k = 5$ the expected fraction of functional defect-free circuits within the comparison window will be 99.9999426%. In other words, the false positive rate will be $5.74 \cdot 10^{-5}$. Second, the fact that the curve drops with a slight rate as we increase k implies that in a neighborhood of k the L-W defect coverage is practically constant. As a result, the UTL and LTL of the comparison window of the checkers do not have to be precisely set, thus making the *SymBIST* infrastructure overall robust.

In Section VII-D, we will analyze in detail the defect coverage for $k = 5$.

C. SymBIST transient simulations

Herein, we show transient simulations of *SymBIST* for the SAR ADC IP in both off-line and on-line test modes. In all simulations, the comparison window is set for $k = 5$. Moreover, the stop-on-detection option was disabled.

1) SymBIST in off-line test mode: Fig. 14 shows the *SymBIST* invariance in Eq. (4) during the whole duration of the test stimulus for the nominal defect-free case and for four chosen defect scenarios. Since the stop-on-detection option is disabled, after defect detection the test continuous until its maximum duration of 0.205μs. The instantaneous glitches are due to the switching operation, either due to changes in the digital test stimulus or due to the sampling and conversion operations. As it can be seen from Fig. 14, in the defect-free

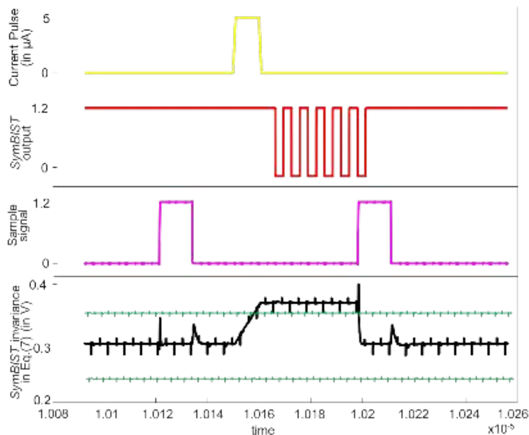

Fig. 15: *SymBIST* response to transient error injected in the DAC.

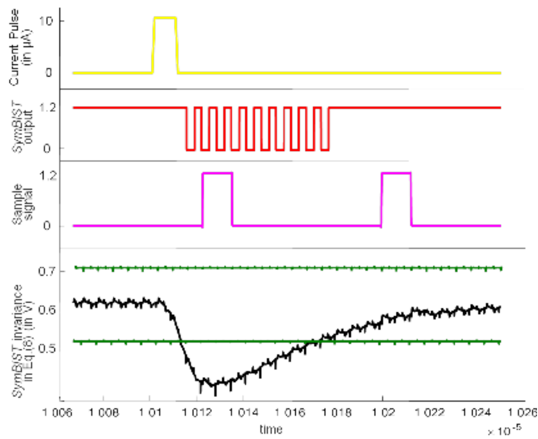

Fig. 16: *SymBIST* response to transient error injected in the bandgap.

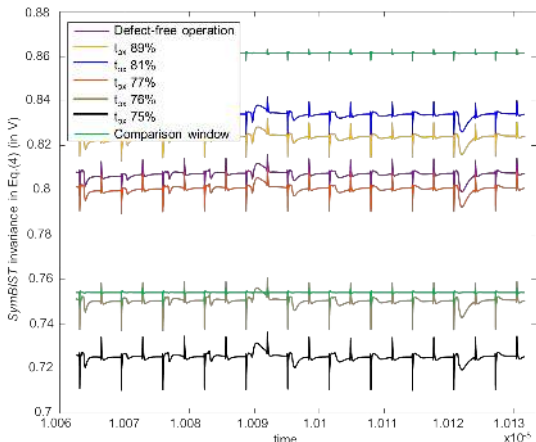

Fig. 17: *SymBIST* response to a latent defect.

case the invariance lies within the comparison window, while in the four defect scenarios there are four distinct cases: (a) the invariance is permanently violated (variation in resistor in the bandgap); (b) the invariance is violated during several conversion periods (short defect in SUBDAC1); (c) the invariance is violated only during one conversion period towards the end of the test stimulus duration, otherwise for the rest of the conversion periods the transient response matches the transient response of the defect-free operation (open defect 1 in SUBDAC1); (d) a defect is activated during one conversion cycle resulting in clear excursion of the invariant signal, but still the signal does not slide outside the window and the defect goes undetected (open defect 2 in SUBDAC1). This last defect simulation shows that certain defects may be undetected due to lenient test limits set at $k = 5$, yet making the test limits strict may result in inadvertent false positives.

2) SymBIST in on-line test mode: We demonstrate *SymBIST* for two scenarios of lifetime failure, namely transient errors and latent defects. In our simulations, we consider sinusoidal FD analog inputs with peak-to-peak voltage $1V$, common mode $0.6V$, and frequency 2MHz.

a) Transient error: We model a transient error by injecting a short current pulse into a node of the circuit. Fig. 15 shows the *SymBIST* response to a transient error occurring in the node DAC- of the 10-bit DAC shown in Fig. 6. The current pulse has amplitude $5\mu A$ and is injected at around $10.15\mu s$. Shortly after the invariance in Eq. (7) slides outside the tolerance window and the global *SymBIST* output switches to logical 0 at time stamps when the test clock is high to indicate the error. As it can be seen, although the pulse has a short duration, *SymBIST* flags an error for all the subsequent conversion periods until a new input analog value is sampled. The reason is that the current pulse charges the capacitors to a different DC level than V_{cm} until the new sampling phase.

A second example of a transient error in shown in Fig. 16. A current pulse with amplitude $10\mu A$ is injected in a node inside the bandgap circuit affecting the biasing conditions. Fig. 16 shows the detection via the *SymBIST* invariant signal in Eq. (8). *SymBIST* flags an error for a relative long period after the current pulse settles to zero since it requires some time for the bandgap to settle back to the nominal biasing conditions.

b) Latent defect: The most common latent defect is the rupture of the gate oxide of MOS transistors known as pinhole which accelerates the time-dependent dielectric breakdown (TDDB) [5]. It has been recently shown that a pinhole can be modeled as a decrease in the effective value of the oxide thickness t_{ox} [5]. Fig. 17 shows an example where we gradually decrease the t_{ox} of a transistor inside the reference buffer and eventually this decrease is captured by the invariance in Eq. (4). As it can be seen, as t_{ox} decreases gradually to around 80% of its nominal value, the invariant signal shows an increasing positive offset but still remains within the tolerance window. Further t_{ox} decrease causes an abrupt negative offset to the invariant signal and when t_{ox} drops below 76% of its nominal value the invariant signal abruptly drops below the lower bound of the tolerance window.

D. Defect coverage analysis

Table II shows for the individual A/M-S blocks of the SAR ADC IP and for its complete A/M-S part the L-W defect coverage values achieved using *SymBIST* with the comparison window set at $k = 5$. Notice that any differences in L-W defect coverage values compared to the results in [12] is due to the fact that herein the simulation considers the

Blocks	# defects	# defects simulated	defect simulation time (sec)	L-W defect coverage for k=5
BandGap	104	104	7305	95.46%
Reference Buffer	160	160	10640	43.32%
SUBDAC1	1260	107	7413	77.32%±6.62%
SUBDAC2	1260	107	7331	78.01%±6.55%
SC Array	44	44	3139	97.7%
V_{cm} Generator	6	6	591	20%
Preamplifier	24	24	1797	96%
Comparator Latch	38	38	2835	76%
RS Latch	40	40	2899	68%
Offset Compensation circuit	20	20	1400	32.73%
Complete A/M-S part of SAR ADC IP	2956	100	6376	87.56%±4.34%

TABLE II: L-W defect coverage results with the comparison window set at $k = 5$.

full on-chip integration of *SymBIST* at transistor-level into the SAR ADC IP, while in [12] mathematical expressions of the invariances were used in the analysis. For the larger blocks, namely the two sub-DACs, as well as for the complete A/M-S part, we use the LWRS option to respect a reasonable defect simulation time budget and, therefore, we report also the corresponding 95% confidence intervals. Table II includes in addition the total number of defects in a block according to the defect model in Section VI-A, the number of defects simulated which is different than the total number of defects when the LWRS option is used as explained in Section VI-B, and the defect simulation time. The defect simulation campaign was performed on a server with 4 cores@3.5 GHz and 7.55 GB RAM. The defect simulation times are proportional to the number of defects simulated, as well to the detection time stamps during the test duration since we are using the stop-on-detection option.

As it can be seen from Table II, for the complete A/M-S part of the SAR ADC IP, the L-W defect coverage is $87.56\% \pm 4.34\%$. As an indicative comparison, for two considerably smaller industrial A/M-S IPs, namely a bandgap and a power-on-reset circuit, the reported defect coverage values are 74% and 51%, respectively [3].

The reported L-W defect coverage of around 87% is considered to be very high. For A/M-S ICs, it is not expected to approach near-100% defect coverage, as is typical of scan-tested digital ICs [3]. The reason is that A/M-S ICs have redundancy and defect tolerance, intentional or not. Undetected defects can be examined one by one, which of course is a very tedious and time-consuming process, in order to report also the modified fault escape rate [4], defined as the percentage of undetected defects that result in at least one specification being violated. As the reason behind an undetected defect is understood, systematic efforts can be made to tune the BIST towards higher defect coverage. For example, this involves designing a new test stimulus to better activate the circuit in the vicinity of the inserted defect and propagating the defective signals at activated defect sites to circuit outputs with sufficient amplitude [3].

On another note, safety standards, e.g., ISO 26262 for automotive, are not written in a quantified way. For BIST certification, the IC manufacturer delivers a safety manual that clearly defines the defect model and the defect coverage accounting method, and describes the results of the analysis done. Moreover, safety-relevant application failure modes defined by the user can be mapped to specific defects, and the analysis should prove that those defects are caught.

To shed more light in the low L-W defect coverage values observed for certain blocks, namely the reference buffer, V_{cm} generator, and offset compensation circuit, we further analyzed their undetected defects. Nevertheless, these rather low L-W defect coverage values do not have a significant impact on the L-W defect coverage for the complete A/M-S part. The reason is that compared to defects in other blocks, most defects within these blocks have considerably lower relative likelihood. The V_{cm} generator is a simple voltage divider serially connected to ground with a switch. It is used only during the sampling phase to set V_{cm} equal to $V_{DD} \cdot R_2/(R_1 + R_2)$, where R_1 and R_2 are the two resistors in the voltage divider. Out of the 6 defects only 1 is undetected, e.g. the absolute defect coverage is 83.33%. The undetected defect is the stuck-on defect in the switch and has a very high relative likelihood, thus dominating the L-W defect coverage which is 20%. However, this defect has no effect on the operation of the block since it only forces the V_{cm} generator to operate uninterruptedly, thus it only increases the power consumption of the V_{cm} generator. For the reference buffer, there are two undetected defects with very high relative likelihood, namely the $\pm 50\%$ variations in the Miller capacitor of the op-amp inside the reference buffer. This capacitor is used for stability; however, the circuit is working at DC and the comparison levels VREF $< 0 : 32 >$ manage to settle during the warm-up phase of the ADC despite the $\pm 50\%$ variations. For this reason, these defects have no effect on the operation of this block.

VIII. Conclusions

We proposed a BIST paradigm, called *SymBIST*, virtually applicable to all A/M-S ICs. *SymBIST* relies on constructing or identifying inherent invariances and checking whether those invariances are satisfied. Invariance violation indicates abnormal operation. *SymBIST* has a double scope of application in the context of functional safety. It is used for defect-oriented post-manufacturing test and can be reused for in-field on-line test, either concurrently with the operation or in idle times. *SymBIST* was demonstrated for a SAR ADC IP showing high defect coverage, low-latency in-field error detection, and no performance penalty, while incurring low overheads, requiring minimum and non-intrusive design re-configuration, and being compatible with modern digital test access and control mechanisms.

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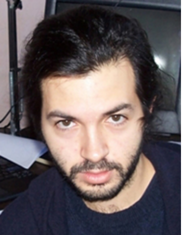

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