

Symmetric GTO and Snubber Component Characterization in PWM Current-Source Inverters

Steven C. Rizzo, *Member, IEEE*, Bin Wu, *Member, IEEE*, and Reza Sotudeh, *Member, IEEE*

Abstract—The pulsewidth-modulated (PWM) current-source inverter (CSI) used in ac-drive applications can be implemented with symmetric gate turn-off thyristors (GTO's). One of the major difficulties in the optimization of the GTO switch and the snubber components of the inverter is the variation in different switching conditions encountered during normal operation. Past work has concentrated on the GTO and snubber components in voltage-source applications, where commutation of the GTO device is an independent process and does not affect the operation of the other inverter devices. This paper proposes the characterization of the GTO and the snubber components by formulation of the CSI equivalent circuit during the device commutation period. From the equivalent circuit, the state equations are derived, thereby obtaining accurate voltage and current waveforms of the GTO and associated snubbers. From the analysis, the component power loss can be calculated and optimization performed. Simulation results are verified by using both a laboratory prototype and medium-voltage drive system.

Index Terms—Current-source inverter, snubber, symmetric GTO.

I. INTRODUCTION

LARGE ac-drive applications have resulted in various inverter topologies. For medium-voltage (2300–6900 V) applications, pulsewidth modulation (PWM) current-source inverters (CSI's) [PWM CSI's] with symmetric gate turn-off thyristors (GTO's) have been successfully implemented on induction machine applications. The simplified circuit diagram is shown in Fig. 1. The power switches T1–T6 are comprised of devices connected in a series string. The number connected in series is dependent on the system voltage and the blocking capability of the GTO implemented. The symmetric GTO has the capability of blocking both forward and reverse voltage up to 6500 V, making it ideal for a PWM CSI topology. Past studies of this topology have mainly concentrated on the control and harmonic elimination techniques, however, work related to the power switch and snubber design for GTO PWM CSI drives has been brief [1]–[3]. Investigation of the commutation process of the GTO and its effects on the snubber components has been well documented for voltage-source inverters (VSI's) [4], [5]. The GTO commutation process in a PWM CSI drive differs substantially. The commutation process of one device in the VSI does not affect the operation of the other inverter power switching devices. For the PWM

CSI, the commutation process involves two legs of the inverter and three snubber networks simultaneously. Due to the number of possible commutation conditions which can be encountered, an accurate method in the evaluation of the turn-off and turn-on process becomes valuable in determining GTO and snubber component stresses. In this paper, a model for the GTO commutation in the PWM CSI drive is presented with emphasis on the following contributions:

- 1) formulation of the equivalent circuit and identification of the possible commutation states for the PWM CSI;
- 2) modeling of the commutation process, including nonlinear characteristics of the GTO;
- 3) simulation results which can be used to minimize the GTO switching loss and snubber loss;
- 4) verification with laboratory experiments;
- 5) overview of snubber optimization.

II. EQUIVALENT CIRCUIT AND STATE EQUATIONS

The circuit of Fig. 2 is the basis for the derivation of the equivalent circuit during the commutation process. There are six possible conducting pairs: T1, T2; T2, T3; T3, T4; T4, T5; T5, T6; and T6, T1. For any chosen pair, the resultant equivalent circuit is identical with the exception of the initial voltages of the output filter capacitors impressed upon the commutating devices. For the derivation of the equivalent circuit, device T1 and device T2 will be the initial conducting pair where the constant current I_{dc} will be transferred from device T1 to device T3. Just prior to device T1 commutating, the output filter capacitors can be modeled by constant voltage sources for a short instant. Thus, the equivalent circuit during commutation can be illustrated as in Fig. 3 and used for the derivation of the state equations. The equivalent circuit illustrates the necessary components to develop an accurate model. The GTO snubber is comprised of a typical resistor, capacitor, and diode (RCD) polarized network with stray inductances L2, L4, and L6. The stray inductance in the snubber is easily measured by isolating the GTO and snubber components from the circuit and removing the snubber resistor. By charging the snubber capacitor to an appropriate voltage and shorting the GTO, an LC ringing circuit will result, giving one pulse of current through the diode. The inductance can be obtained by the following:

$$L_{\text{stray}} = \frac{t_w^2 / \pi^2}{C_s} \quad (1)$$

where t_w is the measured period of the pulse of current. Typical values of stray inductance range from 0.1 to 0.4

Manuscript received January 23, 1997; revised October 2, 1997. Recommended by Associate Editor, L. Xu.

S. C. Rizzo is with Rockwell Automation/Allen-Bradley, Cambridge, Ont., N1R 5X1, Canada.

B. Wu is with Ryerson Polytechnic University, Toronto, Ont., Canada.

R. Sotudeh is with the University of Teesside, Middlesbrough, Cleveland, U.K.

Publisher Item Identifier S 0885-8993(98)04844-3.

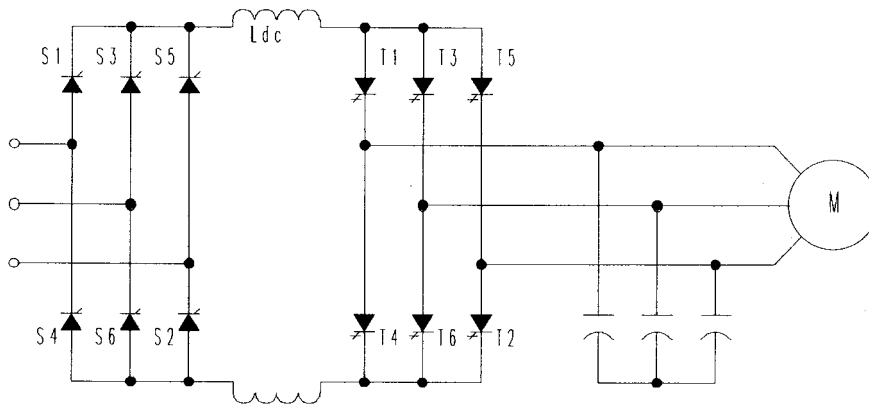


Fig. 1. Power circuit of GTO PWM CSI induction motor drive.

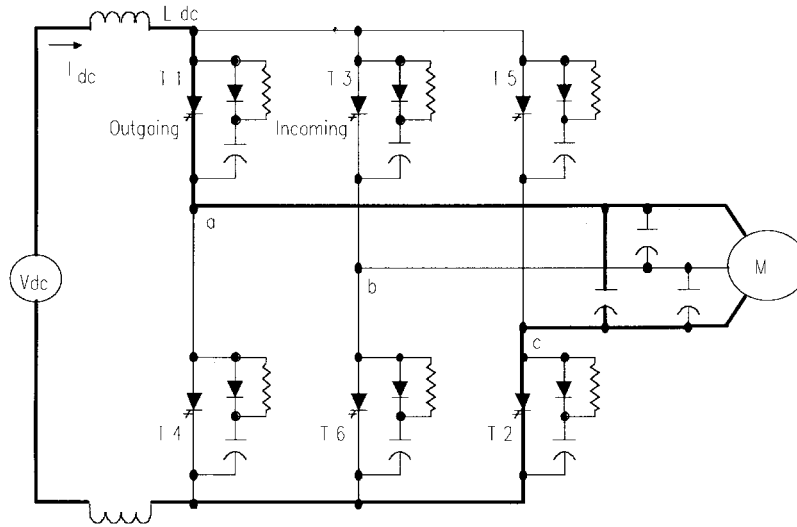


Fig. 2. Current paths T1 and T2 conducting.

μH . Inductances L_1 , L_3 , and L_5 are used to control the rate of rise of current through the GTO during turn on and load commutation. These inductances can be obtained from measurement. Under load commutation the rate of fall of current is determined by the voltage and inductance ratio. The inductance can be calculated, accounting for the lead length of the output filter capacitors by the following:

$$L = \frac{v_{ca} + v_{bc}}{2(di_{T_1}/dt)} \tag{2}$$

The di/dt inductance per leg is typically 15–25 μH per leg for a 4160-V system.

Depending on the status of devices D1, T3, D3, and D5, which can be either “on” or “off,” there is a possibility of 16 states when commutating the current from device T1 to device T3. The 16 possible states are defined in Table I. For each state, a set of state equations is derived with the state variables defined to be i_{L_1} , i_{L_3} , i_{L_5} , v_{C_1} , v_{C_3} , and v_{C_5} . The state equations are derived by summing the voltages in loops 1 and 2 of Fig. 3. Using the initial conditions of I_{dc} , v_{ca} , v_{bc} , and device models for the symmetric GTO and snubber diode, the voltages and currents can be determined for all of the inverter components during the commutation interval. The technique

used to solve the differential equations was the fourth-order Runge–Kutta method. A typical set of state equations is listed below.

A. Equations for State 9

$$\begin{aligned} \frac{di_{L_3}}{dt} &= \frac{v_{ab} - v_{bc} + v_{C_1} - 2R_3i_{L_3} + R_5i_{L_5} - 2v_{C_3} + v_{C_5} - v_{L_2}}{3(L_1 + L_2)} \end{aligned} \tag{3}$$

$$\begin{aligned} \frac{di_{L_5}}{dt} &= \frac{v_{ab} + 2v_{bc} + v_{C_3} + R_3i_{L_3} - 2R_5i_{L_5} - 2v_{C_5} + v_{C_1} - v_{L_2}}{3(L_1 + L_2)} \end{aligned} \tag{4}$$

$$\frac{dv_{C_1}}{dt} = \frac{i_{L_2}}{C_1} = \frac{(I_{DC} - i_{L_3} - i_{L_5} - i_{T_1})}{C_1} \tag{5}$$

$$\frac{dv_{C_3}}{dt} = \frac{i_{L_3}}{C_3} \tag{6}$$

$$\frac{dv_{C_5}}{dt} = \frac{i_{L_5}}{C_5} \tag{7}$$

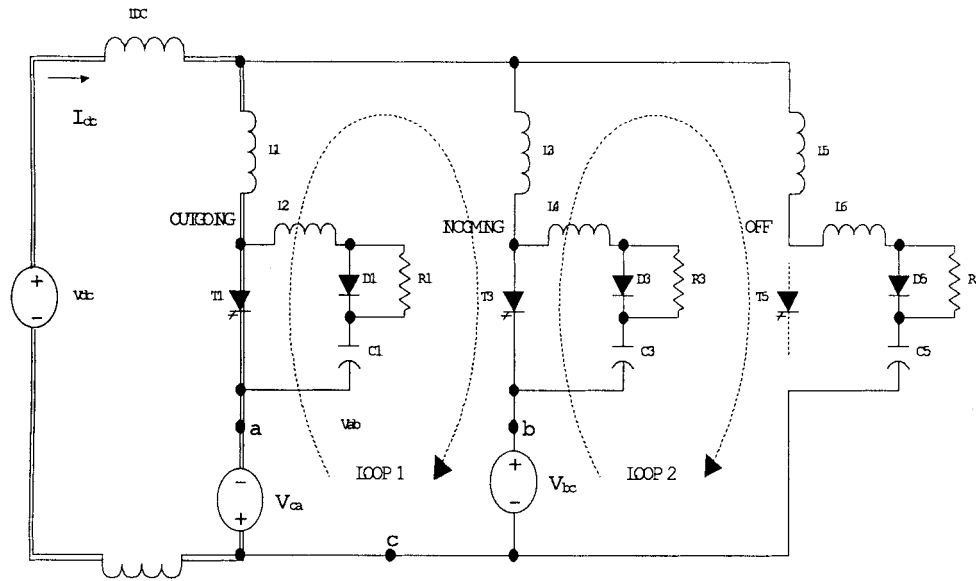


Fig. 3. Equivalent circuit for T1 commutation and T3 turn on.

 TABLE I
 DEFINITION OF STATES

State	D1	T3	D3	D5
1	OFF	OFF	OFF	OFF
2	OFF	OFF	OFF	ON
3	OFF	OFF	ON	OFF
4	OFF	OFF	ON	ON
5	OFF	ON	OFF	OFF
6	OFF	ON	OFF	ON
7	OFF	ON	ON	OFF
8	OFF	ON	ON	ON
9	ON	OFF	OFF	OFF
10	ON	OFF	OFF	ON
11	ON	OFF	ON	OFF
12	ON	OFF	ON	ON
13	ON	ON	OFF	OFF
14	ON	ON	OFF	ON
15	ON	ON	ON	OFF
16	ON	ON	ON	ON

For a typical GTO commutation process, three or more states will be involved. The state of devices D1, T3, D3, and D5 are computed and the appropriate set of state equations are selected for the calculation of the component voltages and currents. For the PWM CSI, there are two types of commutation. The most familiar being forced commutation where the voltage v_{ab} of Fig. 3 is negative. Prior to the commutation, the voltage across device T3 will be negative since device T1 is on. After the commutation, the voltage across device T1 will be positive. The characteristic equations defining forced commutation are given below. A model similar to that used by Ohashi [4] is used to characterize the GTO for forced commutation.

B. Characteristic Equations for Forced Commutation

1) Switch T1 Turn Off:

$$v_{T1} = v_{L2} + v_{D1} + v_{C1} \quad (8)$$

$$i_{T1} = i_{T_{dc}} \left(1 - \frac{t^2}{t_{fo}^2} \right), \quad \text{for } 0 < t \leq t_{fall} \quad (9)$$

$$i_{T1} = i'_{T1} e^{-\frac{t-t_{tail}}{\tau_1}} - i''_{T1} e^{-\frac{t-t_{tail}}{\tau_2}}, \quad \text{for } t_{fall} < t \leq t_{tail}. \quad (10)$$

2) Switch T3 Turn On:

$$v_{T3} = v_{L4} + v_{D3} + v_{C3} \quad (11)$$

$$i_{T3} = i_{L3} - i_{L4} \quad (12)$$

where

- $i_{T_{dc}}$ current through the GTO prior to commutation;
- t_{fo} defines the fall time period;
- t_{tail} defines the tail time;
- i'_{T1}, i''_{T1} constants defining the tail current;
- τ_1, τ_2 time constants defining the tail current decay time.

The constants defining the tail current i'_{T1} and i''_{T1} and the time constants τ_1 and τ_2 are not included in standard specification sheets. The excess minority charges and carrier lifetime data required to characterize the tail current are not available to the device user. These values must be formulated experimentally using curve fitting. The tail current is sensitive to initial anode current and gate current. Experimentation showed that values of i'_{T1} and i''_{T1} of 0.167 and 0.007 of the initial anode current and time constants of 0.6 and 0.12 for τ_1 and τ_2 , respectively, gave acceptable results for the tail current under a variety of operating conditions. The gate circuit used was based on typical gate characteristics provided by the manufacturer.

The condition for load commutation exists when the voltage v_{ab} of Fig. 3 is positive. Prior to commutation, the voltage across device T3 will be positive. When device T3 is

commanded to turn on, its voltage will collapse and it is dependent on the device turn-on time t_{gt} . Device T1 will be reverse biased when device T3 is fully on. The turn off of T1 is dependent on the device storage time t_s . If the rate of fall of current $v_{ab}/(2L_1)$ of device T1 is large enough [i.e., $I_{dc}/(v_{ab}/(2L_1))$ is significantly less than the storage time t_s], then the commutation is solely load dependent. Thus, little or no current will be transferred to the snubber diode D_1 and the device voltage v_{T_1} will not increase positively. Since the device is reverse biased during this interval, the P-doped gate and N-doped cathode which form junction J3 is also reversed biased and will be the first to recover. Junction J3 can only support tens of volts. Thus, when the device current becomes negative, the gate cathode junction will avalanche to approximately -25 V. Once the device current has reached its maximum reverse recovery current, device T1 will begin to block voltage and subsequently fully commute.

A combination of both forced and load commutation exists when the rate of fall of current $v_{ab}/(2L_1)$ is such that $I_{dc}/(v_{ab}/(2L_1))$ is greater than t_s . When this occurs, the current will fall at a rate governed by t_f , the device fall time, and a significant portion of device current will be transferred to the snubber network, thus resulting in v_{T_1} values comparable to forced commutation. If both forced and load commutation exist, then the algorithm for the calculation of the component voltages and currents uses the characteristic equations of both types of commutation.

C. Characteristic Equations for Load Commutation

1) Before Switch T1 Blocks Voltage:

$$v_{T_1} = \text{on-state voltage, for } i_{T_1} \text{ positive} \quad (13)$$

$$v_{T_1} = v_{\text{gate-cathode avalanche, for } i_{T_1} \text{ negative}} \quad (14)$$

$$di_{T_1}/dt = (v_{ca} + v_{bc})/(2 \times L_1) \quad (15)$$

$$v_{T_3} = (-v_{bc} - v_{ca}) - (\sqrt{(-v_{bc} - v_{ca})/(t_d - t_{gt})} \times t)^2. \quad (16)$$

2) After Switch T1 Blocks Voltage:

$$i_{T_3} = i_{L_3} - i_{L_4} \quad (17)$$

$$v_{T_1} = v_{L_1} + v_{D_1} + v_{C_3} \quad (18)$$

$$di_{T_1}/dt = -(v_{ca} + v_{bc})/(2 \times L_1), \quad \text{from } .5t_{rr} \text{ to } .9t_{rr} \quad (19)$$

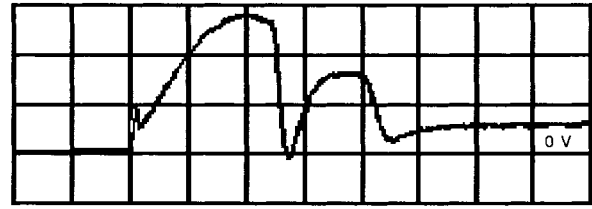
$$i_{T_1} = i_{T@tr.9} \times e^{-t/\tau_{\text{decay}}}, \quad \text{from } .9t_{rr} \text{ to } t_{rr} \quad (20)$$

$$v_{T_3} = 0, \quad (T_3 \text{ is fully on}) \quad (21)$$

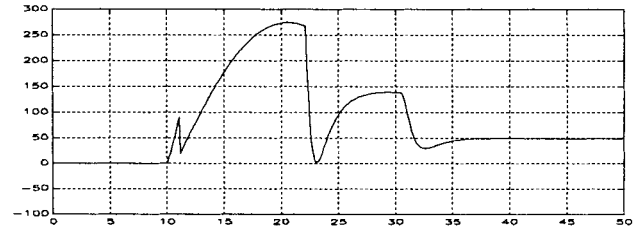
$$i_{T_3} = i_{L_3} - i_{L_4} \quad (22)$$

where

- t_{gt} device turn-on time;
- t_d device delay time;
- τ_{decay} time constant defining the reverse-recovery current in final portion of recovery phase;
- t_{rr} device total reverse-recovery time.



(a)



(b)

Fig. 4. (a) v_{T_1} , 100 V/div, and 5 μ s/div. (b) v_{T_1} , 50 V/div, and 5 μ s/div.

The characteristic equations given above purposely avoid numerous device parameters in order to simplify the computation. The simulation relies only on entry of GTO fall time t_f , a percentage of initial anode current for the formulation of the tail current, GTO tail time, reverse-recovery time, and turn-on time. It is well known that the value of these parameters is affected by circuit switching conditions, however, parameter values from the device specification sheets when entered into the simulation give results which correlate to the measurements obtained. Thus, with standard device data, voltage and current waveforms of GTO and snubber components are easily obtainable.

III. EXPERIMENTAL AND SIMULATION RESULTS

A. Experimental and Simulation Results on Laboratory Unit

The circuit of Fig. 3 was used to verify the characteristic equations formulated for the GTO during turn on and turn off. The circuit parameters were as follows:

$$L_1 = L_3 = L_5 = 10 \mu\text{H};$$

$$L_2 \cong L_4 \cong L_6 \cong 0.45 \mu\text{H measured};$$

$$R_1 = R_3 = R_5 = 20 \Omega;$$

$$C_1 = C_3 = C_5 = 2 \mu\text{F};$$

$$I_{dc} = 110 \text{ A};$$

$$V_{DC} = 150 \text{ V};$$

$$V_{ab} = -50 \text{ V, for forced commutation};$$

$$V_{ab} = 140 \text{ V, for the condition where both forced and load commutation exist.}$$

The device used was manufactured by Toshiba SG800GXH21, 4500 V and 800 A. Figs. 4–8 show the results obtained in the laboratory for the forced commutation of T1, the outgoing device, and the turn on of T3, the incoming device. Experimental results are given in (a) of Figs. 4–8. Simulation results using the characteristic equations and state equations are given in (b) of Figs. 4–8. The simulation results

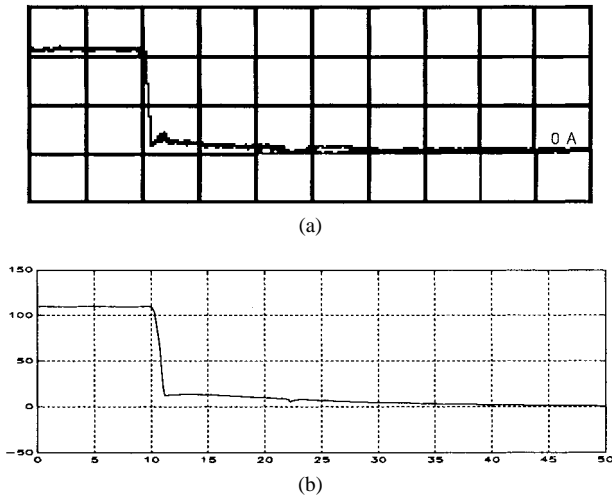


Fig. 5. (a) i_{T1} , 50 A/div, and 5 μ s/div. (b) i_{T1} , 50 A/div, and 5 μ s/div.

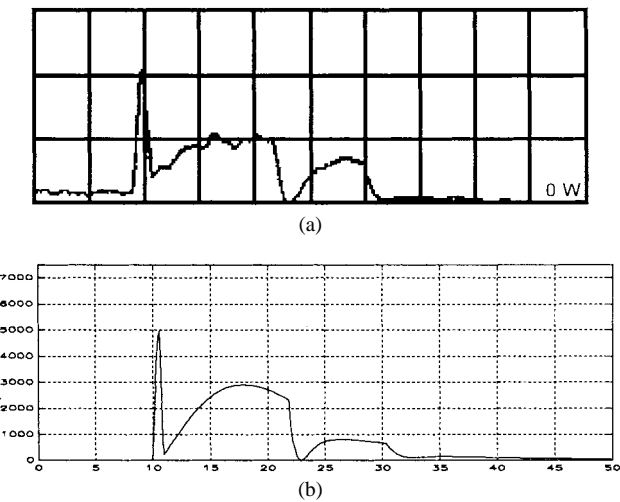


Fig. 6. (a) P_{T1} , 2500 W/div, and 5 μ s/div. (b) P_{T1} , 1000 W/div, and 5 μ s/div.

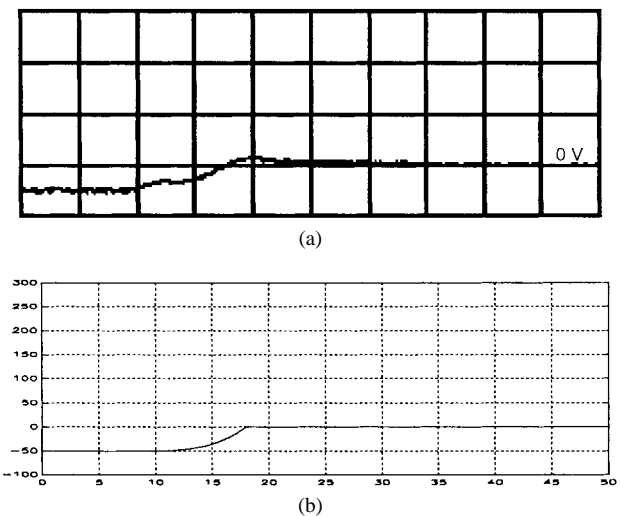


Fig. 7. (a) v_{T3} , 100 V/div, and 5 μ s/div. (b) v_{T3} , 50 V/div, and 5 μ s/div.

correlate closely with the experimental data obtained. The instantaneous power can be calculated using the simulation

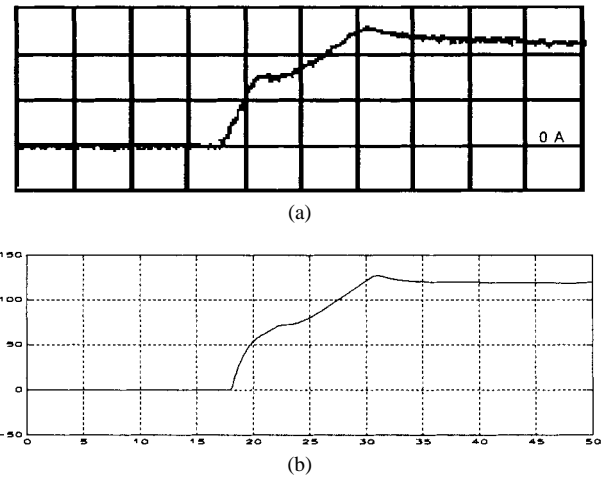


Fig. 8. (a) i_{T3} , 50 A/div, and 5 μ s/div. (b) i_{T3} , 50 A/div, and 5 μ s/div.

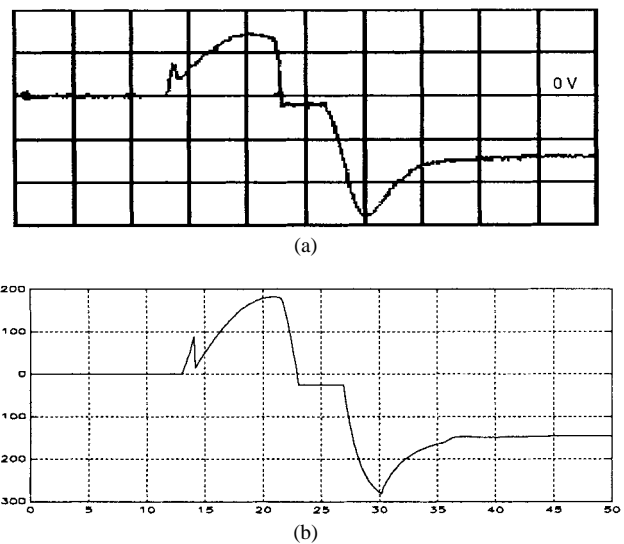


Fig. 9. (a) v_{T1} , 100 V/div, and 5 μ s/div. (b) v_{T1} , 100 V/div, and 5 μ s/div.

program as seen in Fig. 6(b). Thus, calculation of device losses for a given PWM switching pattern can be obtained provided the commutation voltages are known. The turn-on loss of device T3 is zero when device T1 is forced commutated. Device T3 conducts only after the voltage across it has decayed from its initial negative value to zero, afterward assuming its on-state voltage. Figs. 7 and 8 indicate that the current through device T3 only commences when the GTO is forward biased. Thus, device T3 experiences no turn-on switching loss. Note that the simulation results only indicate the switching losses and any loss prior to or after commutation or turn on is ignored.

The PWM CSI topology under certain operating conditions undergoes both forced and load commutation. Figs. 9 and 10 illustrate such a condition. The first part of the commutation is forced with the voltage across device T1 increasing positively. In the second portion, the device voltage is reversed and the waveforms are characteristic of typical reverse recovery. The current of device T1 during the first portion has the characteristic fall and tail current, but also goes negative typical of load commutation.

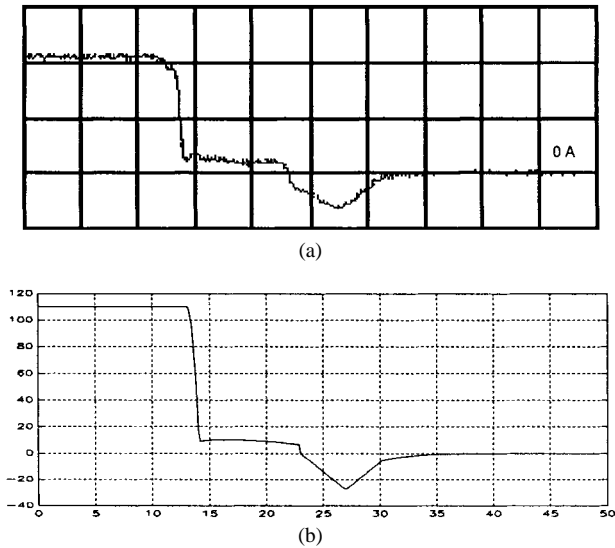


Fig. 10. (a) i_{T1} , 50 A/div, and 5 μ s/div. (b) i_{T1} , 20 A/div, and 5 μ s/div.

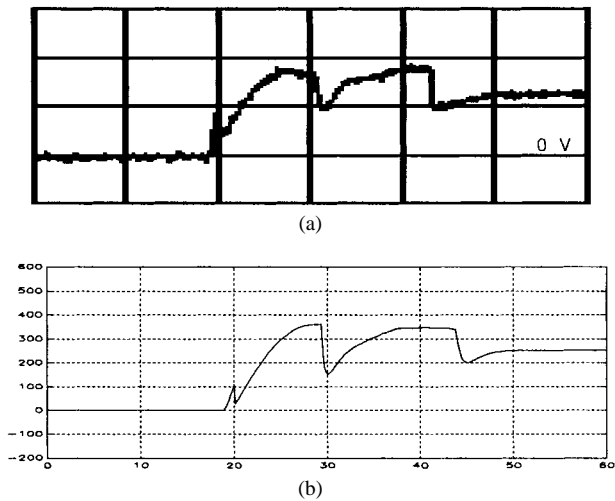


Fig. 11. (a) v_{T1} , 200 V/div, and 10 μ s/div. (b) v_{T1} , 100 V/div, and 10 μ s/div.

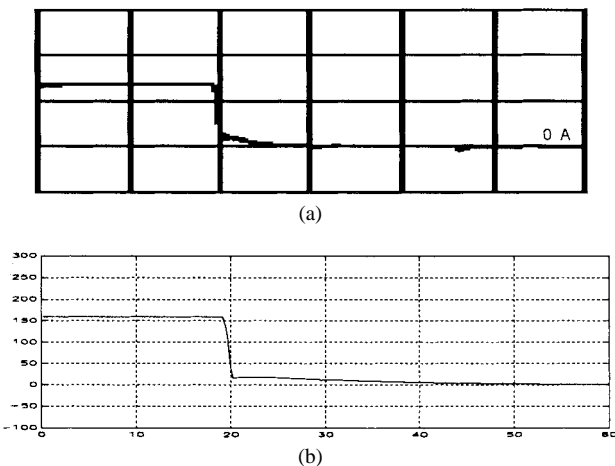


Fig. 12. (a) i_{T1} , 100 A/div, and 10 μ s/div. (b) i_{T1} , 50 A/div, and 10 μ s/div.

B. Experimental and Simulation Results for a Medium-Voltage Drive System Under Forced Commutation

A medium-voltage PWM CSI drive system connected to a 1250-HP 4160-V 1200-RPM motor was used to further

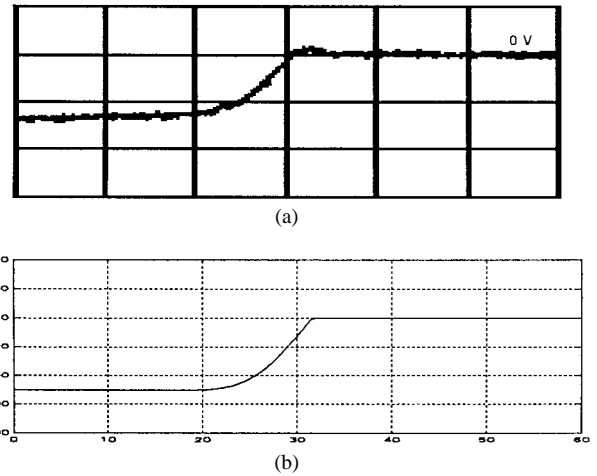


Fig. 13. (a) v_{T3} , 200 V/div, and 10 μ s/div. (b) v_{T3} , 100 V/div, and 10 μ s/div.

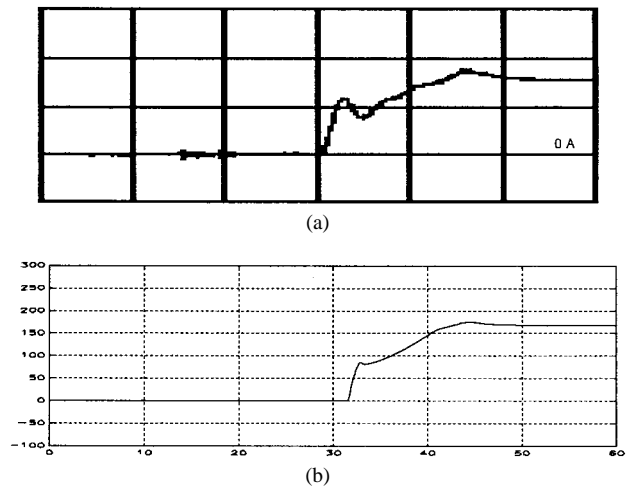


Fig. 14. (a) i_{T3} , 100 A/div, and 10 μ s/div. (b) i_{T3} , 50 A/div, and 10 μ s/div.

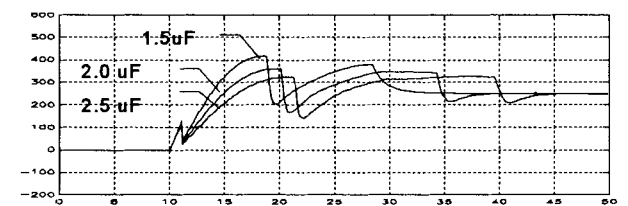


Fig. 15. Variation of v_{T1} with C_s .

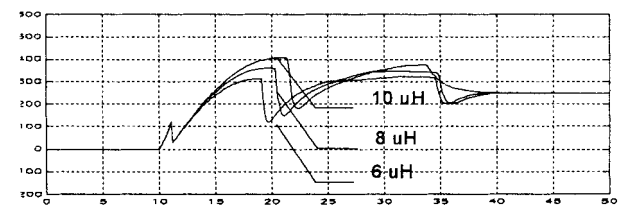


Fig. 16. Variation of v_{T1} with L_1 .

verify the model. The 4160-V drive system uses three GTO's in series to make up the power switch of one leg of the inverter. The experimental data presented is for a single switch with the device voltage and di/dt inductance appropriately scaled. Although the GTO's are matched as closely as possible using

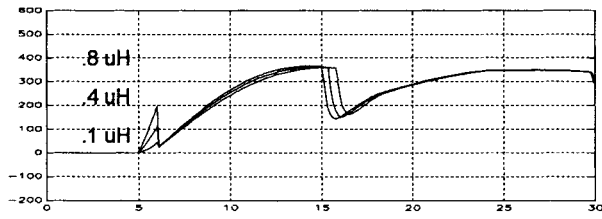


Fig. 17. Variation of v_{T1} with L_2 .

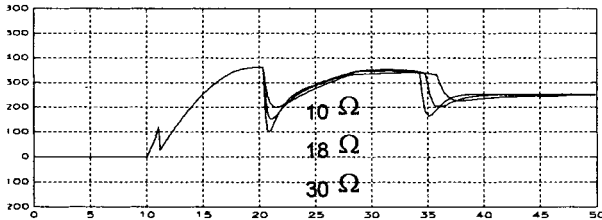
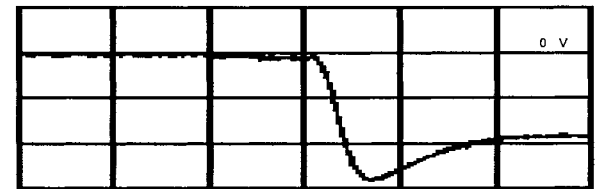
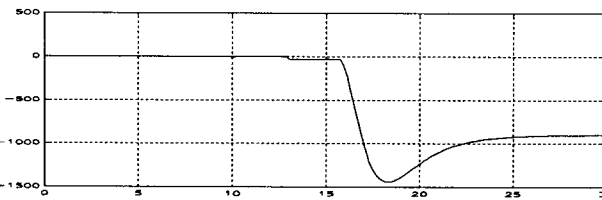


Fig. 18. Variation of v_{T1} with R_s .

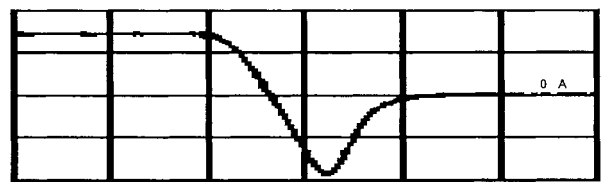


(a)

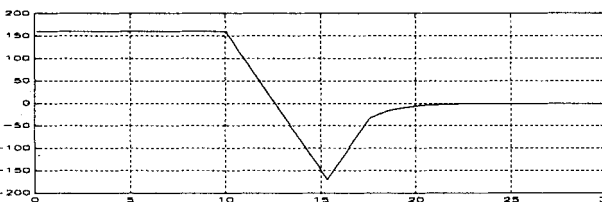


(b)

Fig. 19. (a) v_{T1} , 500 V/div, and 10 $\mu\text{s}/\text{div}$. (b) v_{T1} , 500 V/div, and 10 $\mu\text{s}/\text{div}$.



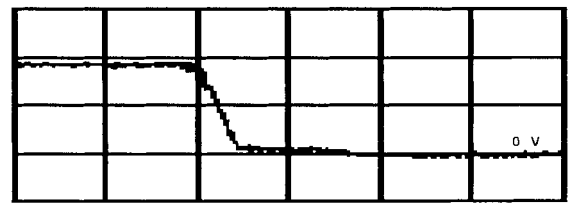
(a)



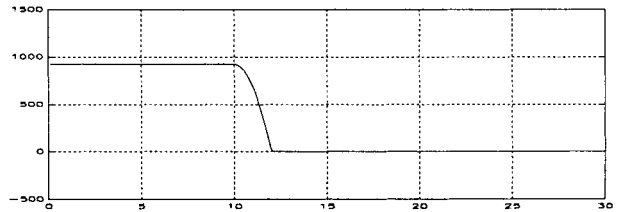
(b)

Fig. 20. (a) i_{T1} , 100 A/div, and 10 $\mu\text{s}/\text{div}$. (b) i_{T1} , 50 A/div, and 10 $\mu\text{s}/\text{div}$.

the manufacturer's device data for fall time, storage time, reverse-recovery charge, and turn-on time, there will be differences in the device parameters. The simulation assumes that the behavior of each device in the series string is identical.

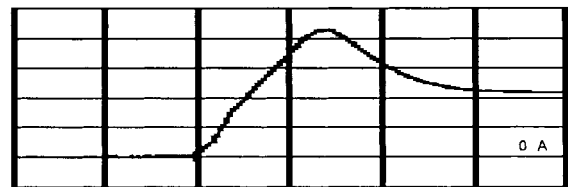


(a)

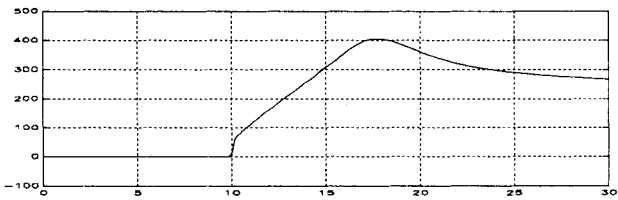


(b)

Fig. 21. (a) v_{T3} , 500 V/div, and 10 $\mu\text{s}/\text{div}$. (b) v_{T3} , 500 V/div, and 10 $\mu\text{s}/\text{div}$.



(a)



(b)

Fig. 22. (a) i_{T3} , 100 A/div, and 10 $\mu\text{s}/\text{div}$. (b) i_{T3} , 100 A/div, and 10 $\mu\text{s}/\text{div}$.

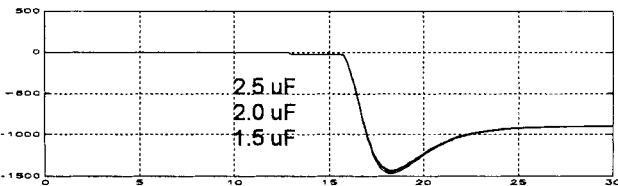


Fig. 23. Variation of v_{T1} with C_s .

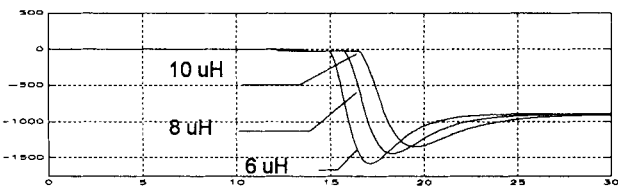


Fig. 24. Variation of v_{T1} with L_1 .

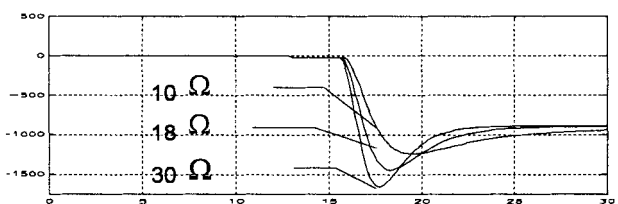


Fig. 25. Variation of v_{T1} with R_s .

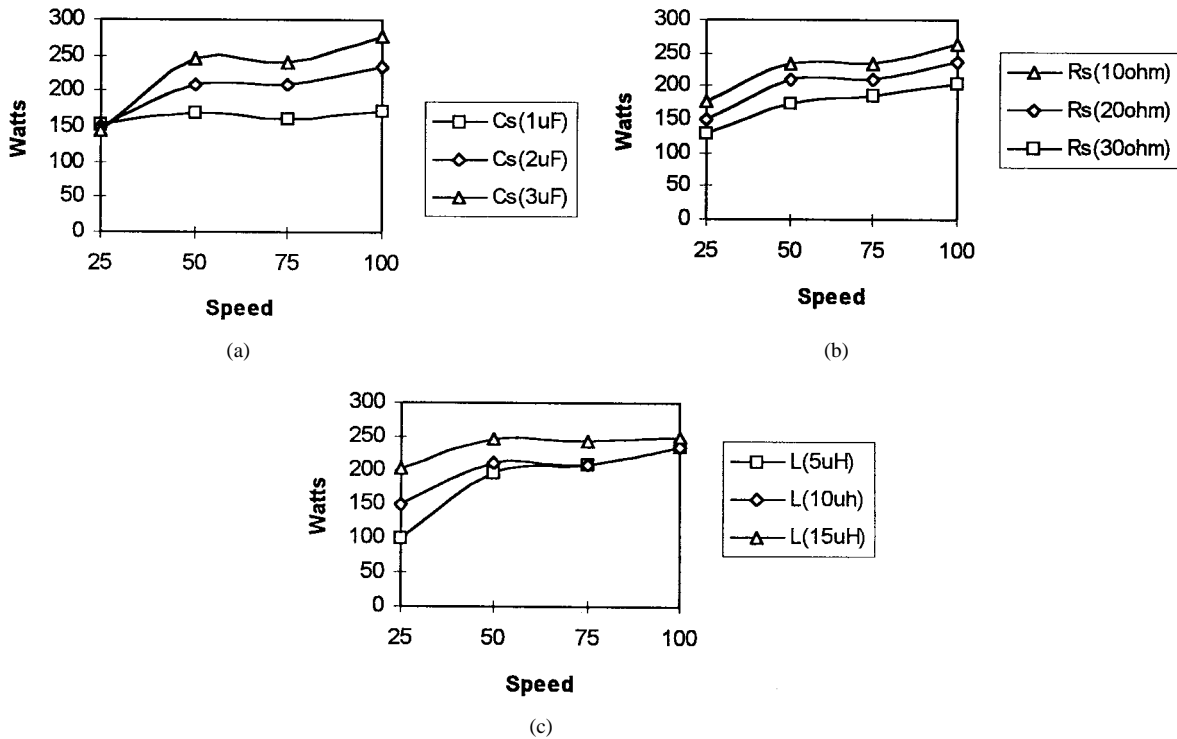


Fig. 26. Total of switching and snubber loss versus speed for a constant torque application.

The circuit parameters for the drive system were as follows:

$$\begin{aligned}
 L_1 &\cong L_3 \cong L_5 \cong 8 \mu\text{H measured}; \\
 L_2 &\cong L_4 \cong L_6 \cong 0.4 \mu\text{H measured}; \\
 R_1 &= R_3 = R_5 = 18 \Omega; \\
 C_1 &= C_3 = C_5 = 2 \mu\text{F}; \\
 I_{\text{dc}} &= 160 \text{ A}; \\
 v_{\text{bc}} &= -1328 \text{ V} \quad v_{\text{ca}} = 1579 \text{ V}.
 \end{aligned}$$

The devices used in the system were Toshiba SG800GXH21, 4500 V and 800 A. Figs. 11–14 give the experimental data and simulation results. The medium-voltage drive system measurements are very similar to those obtained in the laboratory with the low-voltage equivalent circuit test setup, thus indicating the equivalent circuit model and device GTO model is viable for the PWM CSI system. Figs. 15–18 show variation of circuit parameters and their effect on v_{T1} , the voltage of device T1. GTO overshoot voltage for the forced commutation condition is influenced by the snubber capacitor C_s and di/dt snubber inductance. Larger values of C_s will reduce the device voltage overshoot, while larger values of di/dt inductance will increase the overshoot voltage since the stored energy in the inductor will increase and thus be transferred to the capacitor at device turn off. The snubber stray inductance contributes to the initial overshoot voltage as seen in Fig. 17. The larger the stray inductance, the higher will be the initial spike. The value of snubber resistor has little effect on the device overall voltage under forced commutation. Its impact on device voltage is only seen in the interval of snubber diode recovery. This is illustrated in Fig. 18. The resistor power dissipation, however, is directly linked to the size of snubber capacitor. Larger values

of C_s will help reduce the overshoot voltage, but also increase the resistor loss proportionally.

C. Experimentation and Simulation Results for a Medium-Voltage Drive System Under Load Commutation

For load commutation, the circuit parameters were identical to forced commutation, however, the initial voltage conditions on the output filter capacitors were $v_{\text{bc}} = -1872 \text{ V}$ and $v_{\text{ca}} = 902 \text{ V}$. Figs. 19–22 give the current and voltage waveforms for device T1, the outgoing device, and T3, the incoming device. The experimental data and the simulation results are very similar. The device modeling for the reverse recovery of the symmetric GTO requires the reverse-recovery time which can be obtained from the standard specification sheets. Data is available indicating reverse-recovery current versus rate of fall of forward current and reverse-recovery charge versus rate of fall of forward current. This information allows one to obtain the reverse-recovery time t_{rr} at specific operating points. The simulated reverse-recovery current of Fig. 20(b) is representative of the actual current measured in Fig. 20(a). The current decay in the last portion of the waveform uses the exponential function of (20). The influence of component variation is shown in Figs. 23–25. The snubber capacitor has virtually no effect on the peak reverse voltage during load commutation. However, the di/dt inductance and snubber resistance R_s impact the device voltage significantly. The di/dt inductance controls the rate of fall of current. Thus, larger values of inductance will reduce the reverse-recovery current I_{rr} , resulting in lower values of reverse peak voltage. For a given value of R_s , the peak voltage during reverse recovery will be partially set by the resistance and I_{rr} . Thus, higher values of R_s will result in higher values of peak reverse voltage.

D. Snubber Optimization

The simulation program can be used to optimize the snubber component selection. The drive/motor system of 1250 HP and 4160 V uses an 800-A GTO. The device specification recommends that a 2- μ F 20- Ω snubber be utilized for commutation of 800 A. The full load current of the 1250-HP motor is 152 A. Since the device rating exceeds the required amperage of the load, the snubber components can be tailored to minimize switching and snubber loss. The snubber was examined using simulation for a constant torque application at speeds of 25%, 50%, 75%, and 100%. Fig. 26 shows the sum of the GTO switching loss and snubber loss with three values of snubber capacitance, snubber resistance, and di/dt inductance at the different speeds. From the simulation, the lowest loss is associated with a capacitance of 1 μ F, a resistance of 30 Ω , and a di/dt inductance of 5 μ H. The capacitor reduction is limited to 1 μ F for safe operation of the system since the commutable current is reduced to 400 A. Various load types and horsepower ratings can be examined provided the voltages of commutation are calculated. When selecting components, care must be taken to ensure that the capacitor does not reduce the commutable current below safe margins for the system, the resistor, and capacitor time constant allows for the discharge of the capacitor under PWM conditions, and the di/dt inductance is not reduced whereby the reverse-recovery current during GTO load commutation is excessive, causing device failure.

IV. CONCLUSION

An equivalent circuit during device commutation and turn on for PWM CSI operation is proposed. The equivalent circuit was used to derive the state equations which formed the basis for the simulation. The results show that component characterization can be accurately obtained and used to evaluate peak voltage stress, peak current stress, snubber component loss, and device switching loss at different commutation conditions. A unique characteristic of the topology has been shown indicating that turn-on loss is zero for the incoming device when the device being turned off is force commutated. Models for forced, load, and a combination of both forced/load commutation have been formulated and proven experimentally. The model formulated allows variation of circuit components and parameters critical for the optimization of the topology. A brief overview of snubber optimization was presented. Further study can be done evaluating the tradeoffs between device turn-on and turn-off loss with varying circuit parameters and at different commutating conditions. A comparison of the simulation results and experimental waveforms has shown excellent correlation.

REFERENCES

- [1] P. M. Espelage, J. M. Nowak, and L. H. Walker, "Symmetric GTO current source inverter for wide speed range control of 2300 to 4160

- V, 350 to 7000 HP, induction motors," in *IEEE IAS Annu. Meet.*, 1988, pp. 302-307.
 [2] B. Wu, S. B. Dewan, and G. Slemon, "PWM-CSI inverter for induction motor drives," in *IEEE IAS Annu. Meet.*, 1989, pp. 508-513.
 [3] C. Namuduri and P. Sen, "Optimal pulse width modulation for current source inverters," *IEEE Trans. Ind. Applicat.*, vol. IA-22, no. 6, pp. 1052-1072, 1986.
 [4] H. Ohashi, "Snubber circuit for high-power gate turn-off thyristors," *IEEE Trans. Ind. Applicat.*, vol. IA-19, no. 4, pp. 655-664, 1983.
 [5] L. Eriksson, J. Donlon, and R. Chokhawala, "Assignment of turn-on and turn-off power and energy losses in a GTO," in *IEEE IAS Annu. Meet.*, 1989, pp. 1286-1295.



Steven C. Rizzo (S'85-M'93) received the B.Eng. degree from McMaster University, Hamilton, Ont., Canada, in 1986. He is currently working toward the Master's degree at Ryerson Polytechnic University, Toronto, Ont., Canada.

From 1986 to 1992, he was with Inver-power Power Controls, where he worked in the development of low- and medium-voltage power converters. Since 1992, he has been with Rockwell Automation/Allen-Bradley, Cambridge, Ont., Canada, and is presently the Manager of the Electrical and Power Electronic Medium Voltage Development Group. His research interests are in the application of high-power semiconductor devices in medium-voltage applications and simulation of power converters. He is a registered Professional Engineer in the Province of Ontario, Canada.



Bin Wu (S'89-M'91) received the M.A.Sc. and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, Ont., Canada, in 1989 and 1993, respectively.

After being with Rockwell Automation/Allen-Bradley, Inc. as a Senior Development Engineer, he joined Ryerson Polytechnic University, Toronto, where he is currently an Associate Professor. His research interests include power converter topologies, motor drives, computer simulation, and DSP applications in power engineering.

Dr. Wu was awarded the Gold Medal of the Governor General of Canada in 1990. He is a Registered Professional Engineer in the Province of Ontario, Canada.

Reza Sotudeh (M'90) received the B.Sc. and Ph.D. degrees from the University of Sunderland, U.K., in 1981 and 1984, respectively.

From 1990 and 1994, he was a Reader at the University of Teesside, Middlesbrough, Cleveland, U.K. In 1995, he was a Full Professor at the University of Teesside. He was a Research Fellow at the Central Electricity Generating Board (CEGB), U.K., from 1981 to 1984 and Group Leader at Microtechnology Ltd., U.K., from 1984 to 1986. He was a Lecturer at the University of Sunderland, U.K., from 1986 to 1987 and Senior Lecturer at the University of Teesside from 1987 to 1989. From 1991 to 1997, he was Head of Division of Electronics and Computer Engineering, University of Teesside. He is presently SONY Professor of Computer Engineering, University of Teesside, where his research interests are in application of microelectronics to power engineering problems, computer architecture, high-speed computer buses, and media processing.

Dr. Sotudeh has been a Chartered Engineer since 1990, a Member of the Institute of Electrical Engineers since 1990, and a Fellow of the Royal Society for the Arts, Commerce and Manufactures (FRSA96).