SYNCHRONOUS STATE IN A FULLY CONNECTED PHASE-LOCKED LOOP NETWORK

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Fully connected phase-locked networks are built with all nodes exchanging phase and frequency signals. The nodes are phase-locked loops (PLLs) with slightly different free-running frequencies. The synchronous state emerges from a dynamic process with the phase interactions generating a common frequency steady state. In this work, an estimation is analytically obtained for the synchronous state in a generic N-node network. Numerical experiments complete the analysis of the fully connected network relating free-running frequencies, node gains, and propagation delays.

1. Introduction

Phase-locked loops (PLLs) are circuits for synchronizing phase and frequency of a local oscillator with a variable reference signal [14]. They started to be used in synchronous detection for radio communication systems in 1932 and, during the 40s, they were used in vertical and horizontal synchronizations of TV receptors [1, 23].

In the middle of the 60s, PLLs started to be available as low-cost integrated circuits [6] easing the implementation of modulation and demodulation circuits, frequency synthesizers [8], and motor speed control systems [17]. In the 70s, the advancement of integration technologies allowed the construction of digital PLLs [1] that play an important role in modern digital communications. Nowadays, analog and digital PLLs are used in digital telecommunication networks, in modern mobile phone systems [4, 6], in remote measuring systems, and in computer networks [15].

Here, synchronization strategies using PLLs are studied and a fully connected network with spatially distributed nodes, designed to dynamically acquire a common frequency from slightly different local free-running frequencies, is considered [11, 12, 16, 19, 21].

Our main motivation is concentrated in the telecommunication networks and their standards developed by ITU-T, ETSI, and ANSI, covering synchronous digital hierarchy

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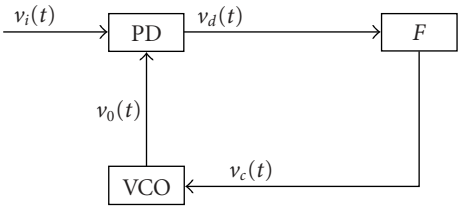

Figure 2.1. PLL block diagram.

(SDH) and synchronous optical networks (SONET) [3, 20]. These standards indicate that the master-slave (MS) architecture is better than the fully connected (FC) architecture for clock distribution systems. Additionally, the international standards suggest that the fully connected architecture needs further studies because the synchronous state of the network depends on gains and propagation delays [16].

However, when one compares the costs of MS and FC networks, it seems that FC networks are cheaper [16] and also are more reliable, maintaining the synchronous state even if any node fails [13].

A generic N-node fully connected PLL clock distribution network is studied, in order to obtain the frequency of the synchronous state. Numerical simulations are also performed showing how the dynamics depends on free-running frequencies, gains, and propagation delays.

2. Network architecture

The nodes of the fully connected network studied here are second-order nonlinear PLLs [2, 9, 10, 12, 18] with the following individual characteristics:

(i) they are closed loops composed of a phase detector (PD), a low-pass filter (F), and a voltage controlled oscillator (VCO), as shown in Figure 2.1;

(ii) PD is a signal multiplier;

(iii) F is a first-order linear low-pass and its output controls the VCO.

The signal $v_i(t)$ is supposed to be periodic with central angular frequency ω and time-varying phase $\theta_i(t)$. The VCO signal $v_o(t)$ has also a periodic form with central angular frequency ω and adjustable phase $\theta_o(t)$.

Defining local phase error by $\Phi(t) = \theta_i(t) - \theta_o(t)$, the dynamics of an individual PLL is described by [8],

$$\ddot{\Phi} + \mu_1\dot{\Phi} + \mu_1\mu_2 \sin\Phi = \ddot{\theta}_i + \mu_1\dot{\theta}_i. \tag{2.1}$$

In (2.1), μ_1 represents the cut-off frequency of F, and μ_2, called PLL gain, depends on the phase detector and VCO gains [22].

The PLLs are spatially distributed and topologically structured with all nodes fully connected and each node is configured as shown in Figure 2.2. In this scheme, each node receives the signals from all other nodes. These signals are individually multiplied by the output of the local VCO. The mean value of the outputs of the PDs is applied to the

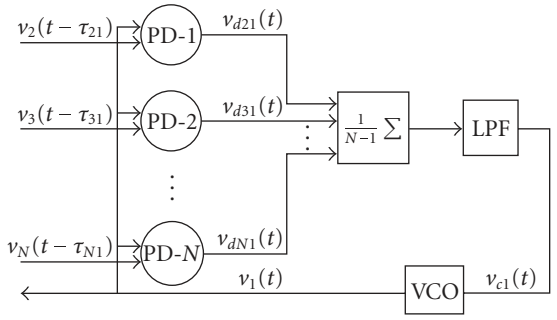

Figure 2.2. Mathematical model for fully connected PLL network.

filter that eliminates the high-frequency terms and whose output controls the phase of the VCO signal.

Phase of the VCO from node i is denoted by $\phi_i(t)$ and its frequency by $\omega_i = \dot{\phi}_i(t)$, for $i = 1,2,\ldots,N$. Propagation delays between two nodes are represented by τ_{ij} with $i,j = 1,2,\ldots,N$. The synchronous state is obtained when all VCOs operate at the same frequency with phase differences, $\phi_j(t) - \phi_i(t)$, constant for $i,j = 1,2,\ldots,N$.

3. Mathematical model and synchronous state estimation

Consider a fully connected second-order PLL N-node network with each node i receiving signals from all other nodes $j \neq i$, with propagation delay $\tau_{i,j}$, and processing them as shown in Figure 2.2.

The VCO of each PLL node has the state represented by its phase $\phi_i(t)$ and frequency $\omega_i = \dot{\phi}_i(t)$. Spatial phase and frequency errors between the nodes i and j are, respectively, defined as $\Delta\phi_{ji}(t) = \phi_j - \phi_i$ and $\Delta\dot{\phi}_{ji}(t) = \dot{\phi}_j - \dot{\phi}_i$.

PLLs belonging to the nodes are characterized by the following parameters:

(i) PD multiplying factors: $k_{m_1} = k_{m_2} = \cdots = k_{m_i} = k_m$, in volts^{-1}, with $i = 1,2,\ldots,N$;

(ii) gains of the VCOs: $k_1 = k_2 = \cdots = k_i = k_0$, in rad/s$V$, with $i = 1,2,\ldots,N$;

(iii) cut-off frequencies of F: $\mu_{1_1} = \mu_{1_2} = \mu_{1_i} = \cdots = \mu_1$, in rad/s, with $i = 1,2,\ldots,N$.

The output of each VCO is

$$v_i(t) = V\cos\phi_i(t); \tag{3.1}$$

and signals received by the phase detector of node i from node j, with propagation delays τ_{ji}, can be written as

$$v_j(t-\tau_{ji}) = V\sin\left[\phi_j(t-\tau_{ji})\right], \tag{3.2}$$

where V is the controlled amplitude of the outputs of VCOs and PDs.

Considering the implementation from Figure 2.2, in each phase detector $j \neq i$, belonging to node i, its output is

$$v_{d_{ji}}(t) = k_m v_j(t-\tau_{ji})\, v_i(t). \tag{3.3}$$

Replacing (3.1) and (3.2) in (3.3), we have the output of each phase detector $j \neq i$, belonging to node i, given by

$$v_{d_{ji}}(t) = k_m V^2 [\sin \phi_j(t - \tau_{ji}) \cos \phi_i(t)]. \tag{3.4}$$

Each resulting signal given by (3.4) is multiplied by $1/(N-1)$ and added, in order to compose the filter input that, neglecting the double-frequency terms [8], is given by

$$v_{d_i}(t) = \left(\frac{1}{N-1}\right)\left(\frac{k_m V^2}{2}\right)\left\{\sum_{j=1, j\neq i}^{N} \sin[\phi_j(t - \tau_{ji}) - \phi_i(t)]\right\}. \tag{3.5}$$

Defining $k_d = (1/2)(k_m V^2)$, expression (3.5) is simplified to

$$v_{d_i}(t) = \frac{k_d}{N-1}\left\{\sum_{j=1, j\neq i}^{N} \sin[\phi_j(t - \tau_{ji}) - \phi_i(t)]\right\}. \tag{3.6}$$

The dynamics of the phase of the VCO is obtained considering the filter transfer function $F_i(s) = \mu_1/(s+\mu_1)$, resulting the expression

$$\dot{v}_{c_i}(t) + \mu_1 v_{c_i}(t) = \mu_1 v_{d_i}(t). \tag{3.7}$$

Replacing v_{d_i}, given by (3.6), and the VCO control signal $v_{c_i} = \dot{\theta}_i(t)/k_0$ in (3.7), the equation for the node phase is

$$\ddot{\theta}_i(t) + \mu_1 \dot{\theta}_i(t) - \mu_1\left(\frac{k_o k_d}{(N-1)}\right)\left\{\sum_{j=1, j\neq i}^{N} \sin[\phi_j(t - \tau_{ji}) - \phi_i(t)]\right\} = 0. \tag{3.8}$$

Then, considering $\phi_i(t) = w_i t + \theta_i(t)$ in (3.8), defining $\mu_2 = k_o k_d$ and $k = \mu_1\mu_2/(N-1)$, the dynamics of each VCO phase in a fully connected network is given by

$$\ddot{\phi}_i(t) + \mu_1 \dot{\phi}_i(t) - \mu_1 \omega_i - k\left\{\sum_{j=1, j\neq i}^{N} \sin[\phi_j(t - \tau_{ji}) - \phi_i(t)]\right\} = 0. \tag{3.9}$$

Examining (3.9) one can see that it is similar to the pendulum equation, containing a dissipation component $\mu_1 \dot{\phi}_i(t)$, a delayed conservative term $k\{\sum_{j=1, j\neq i}^{N} \sin[\phi_j(t - \tau_{ji}) - \phi_i(t)]\}$, and a forcing part $\mu_1 \omega_i$ [7].

Consequently, it is reasonable to suppose that the long-term solution of the system is a synchronous state with the phases of all nodes oscillating with the same frequency ω_s that can be estimated.

In order to estimate this frequency, the following hypotheses are considered [18]:

(a) $\dot{\phi}_i(t) = \omega_s$;

(b) $\ddot{\phi}_i(t) = 0$;

(c) $\phi_j(t - \tau_{ji}) \approx \phi_j(t) - \omega_s \tau_{ji}$.

Therefore,

$$\mu_1(\omega_s - \omega_i) - k\left[\sum_{j=1, j\neq i}^{N} \sin(\Delta\phi_{ji} - \omega_s\tau_{ji})\right] = 0. \tag{3.10}$$

For small values of $[\Delta\phi_{ji} - \omega_s\tau_{ji}]$, expression (3.10) can be written as a linear approximation, considering $\sin[\Delta\phi_{ji} - \omega_s\tau_{ji}] \approx \Delta\phi_{ji} - \omega_s\tau_{ji}$, resulting, for each node i,

$$\mu_1\omega_s - \mu_1\omega_i - k\left[\sum_{j=1, j\neq i}^{N} \Delta\phi_{ji}\right] + k\omega_s\left[\sum_{j=1, j\neq 1}^{N} \tau_{ji}\right] = 0. \tag{3.11}$$

Using (3.11) for an N-node network, with $i, j = 1, \ldots, N$ and $j \neq i$, and adding the N resulting equations, as the sum of the terms $\Delta\phi_{ji}$ is equal to zero, because $\Delta\phi_{ji} = -\Delta\phi_{ij}$, one can write

$$N\mu_1\omega_s - \mu_1\sum_{i=1}^{N}\omega_i + k\omega_s\left(\sum_{i=1}^{N}\sum_{j=1, j\neq i}^{N}\tau_{ji}\right) = 0. \tag{3.12}$$

Calculating ω_s from (3.12)

$$\omega_s = \frac{\mu_1\left(\sum_{i=1}^{N}\omega_i\right)}{N\mu_1 + k\left(\sum_{i=1}^{N}\sum_{j=i, j\neq i^N}\tau_{ji}\right)}. \tag{3.13}$$

Dividing (3.13) by $N\mu_1$, and replacing $k = \mu_1\mu_2/(N-1)$, the estimation of the synchronous state frequency (ω_s) is obtained:

$$\omega_s = \frac{1/N\left(\sum_{i=1}^{N}\omega_i\right)}{1 + \mu_2/N(N-1)\left(\sum_{i=1}^{N}\sum_{j=i, j\neq i}^{N}\tau_{ji}\right)}. \tag{3.14}$$

Therefore, expression (3.14) is an estimation for the frequency of the synchronous state for a fully connected second-order PLL network, depending on the individual free-running frequencies and propagation delays. Notice that when the delays are zero, ω_s is given by the mean value of ω_i.

In the next section, numerical simulations are conducted to investigate the accuracy of expression (3.14) and to analyze how gains and delays change the behavior of the network.

4. Numerical simulations

Fully connected PLL networks were implemented by using MATLAB-Simulink [5] for 3, 5, and 15 nodes. Free-running frequencies are normalized to 1 rad/s considering 5% and 10% of dispersion, with and without propagation delays.

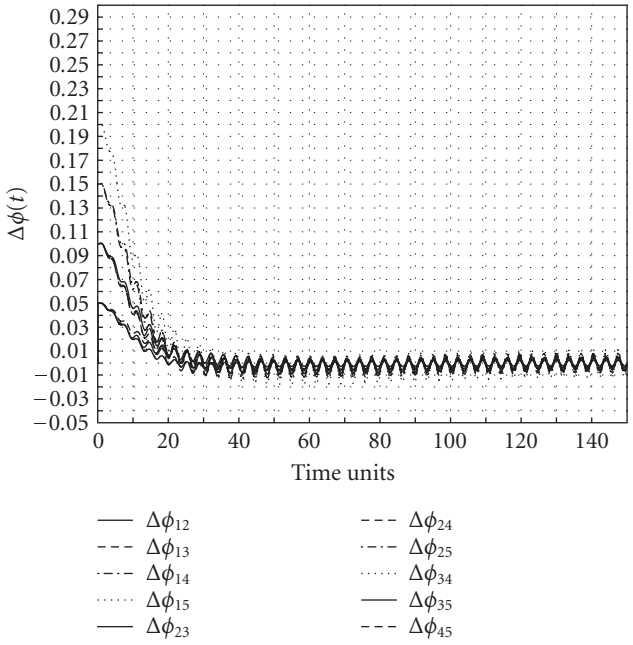

Figure 4.1. Frequency errors: $N = 5$, $\mu_2 = 0.0625$, $\tau_{i,j} = 0$.

The goals of the simulations are:

(i) verifying whether the synchronous state, with frequency errors $\Delta\dot{\phi}$ vanishing and phase errors $\Delta\phi$ tending to constant values, is reachable;

(ii) validating the estimation of the synchronous state frequency given by (3.14);

(iii) measuring the acquisition time.

All the simulations use MATLAB built-in PLLs and Runge-Kutta (Dormand-Prince) method with constant step time 0.02 [5]. We show the results for the 5-node network and 10% of free-running frequency dispersion, because the results are similar to the results for networks with different number of nodes and 5% of dispersion.

Starting without propagation delays, $\omega_1 = 1.0$, $\omega_2 = 0.95$, $\omega_3 = 0.90$, $\omega_4 = 0.85$, and $\omega_5 = 0.80$ are chosen, that is, $\omega_s = 0.90$. Figures 4.1 and 4.2 show the behavior of the frequency and phase errors between nodes. In the same conditions, the behavior of the node frequencies is shown (Figure 4.3).

Considering a propagation delay of 0.18, corresponding approximately to 10% of the period of the normalized frequency signal, Figure 4.4 shows the frequency errors, Figure 4.5 the phase errors, and Figure 4.6 the node frequencies.

In order to complete the investigation about the expression (3.14), Figure 4.7 presents for the same 5-node delayed network how the synchronous state frequency depends on the gain μ_2.

Considering communication networks, it is important to evaluate the acquisition time for the clock distribution system. Figure 4.8 shows how the acquisition time depends on the gain μ_2 and on the propagation delays for a 5-node network.

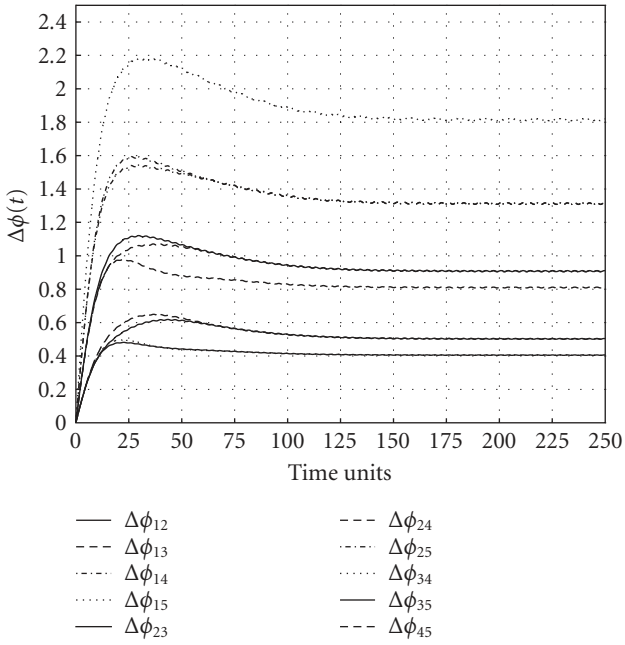

Figure 4.2. Phase errors: $N = 5$, $\mu_2 = 0.0625$, $\tau_{i,j} = 0$.

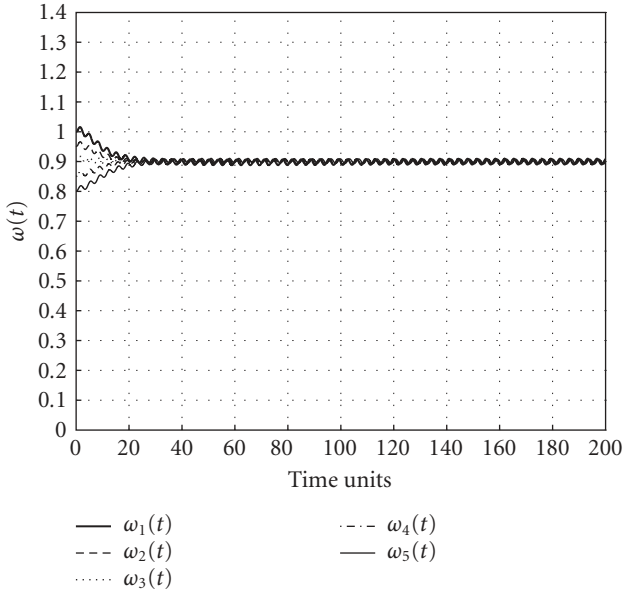

Figure 4.3. Node frequencies: $N = 5$, $\mu_2 = 0.0625$, $\tau_{i,j} = 0$.

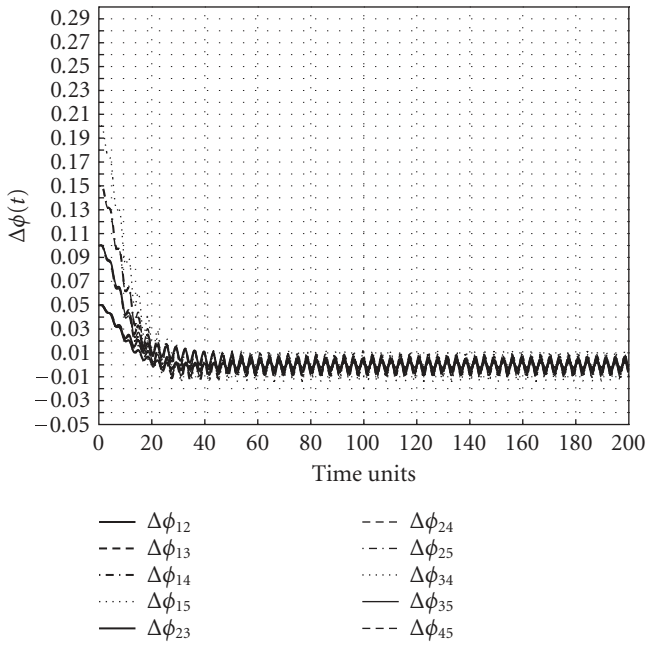

Figure 4.4. Frequency errors: $N = 5$, $\mu_2 = 0.0625$, $\tau_{i,j} = 0.18$.

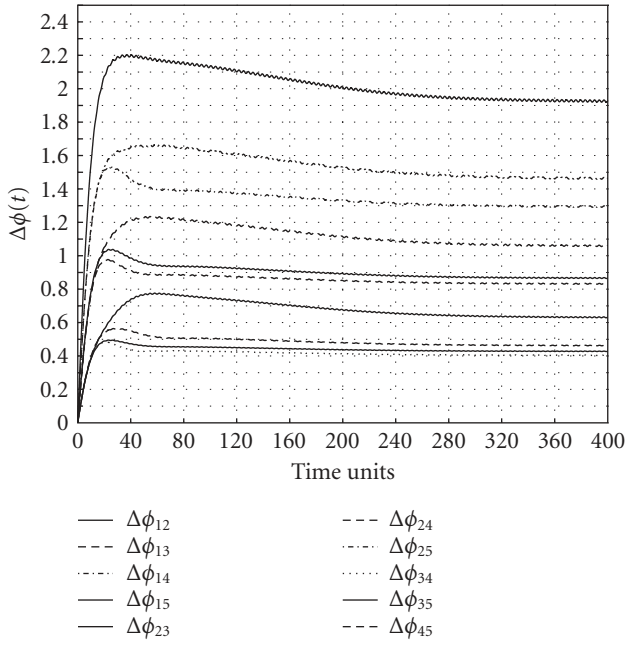

Figure 4.5. Phase errors: $N = 5$, $\mu_2 = 0.0625$, $\tau_{i,j} = 0.18$.

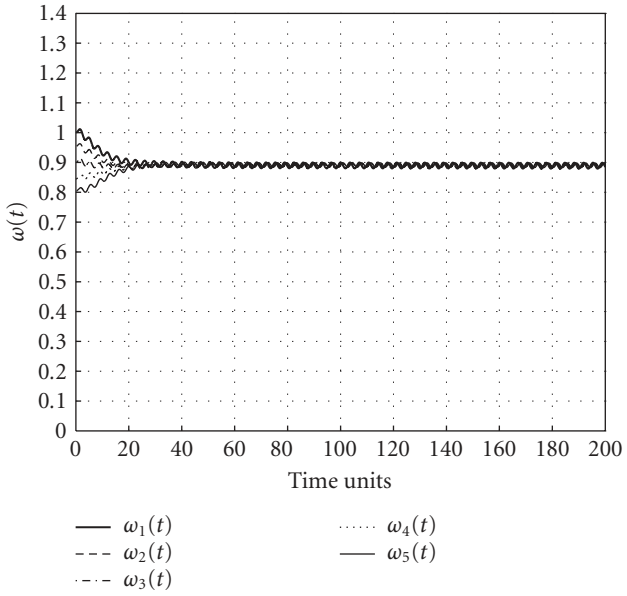

Figure 4.6. Node frequencies: $N = 5$, $\mu_2 = 0.0625$, $\tau_{i,j} = 0.18$.

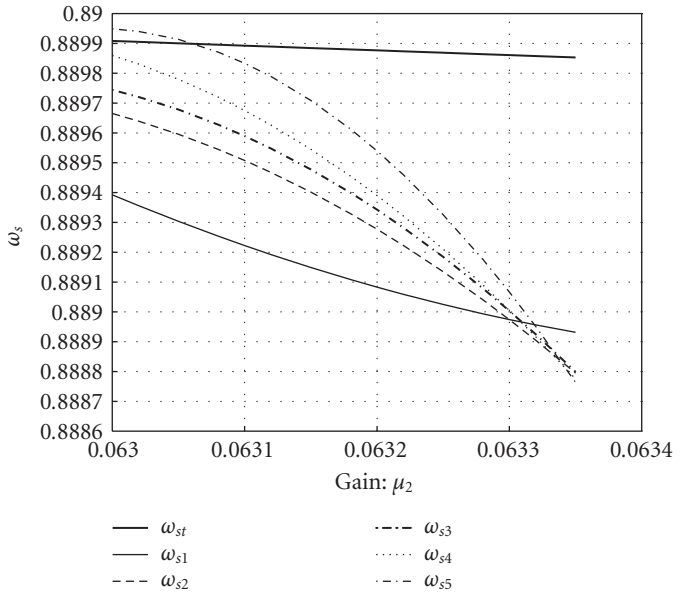

Figure 4.7. Synchronous state frequency versus PLL gain: $N = 5$, $\mu_2 = 0.0625$, $\tau_{i,j} = 0.18$.

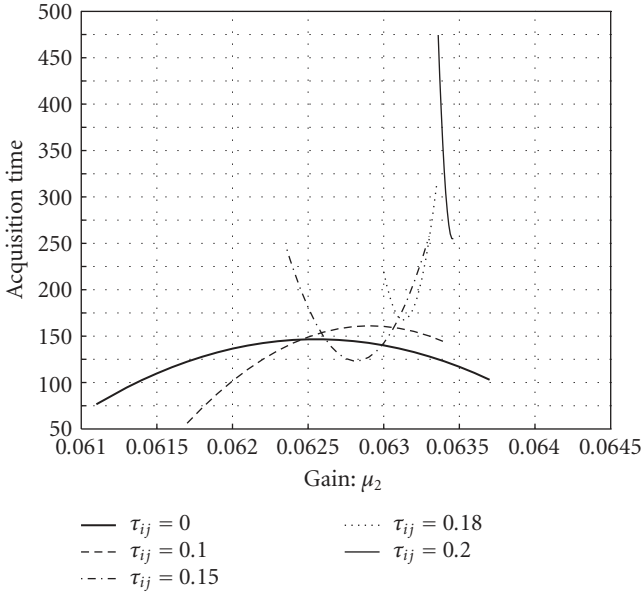

Figure 4.8. Acquisition time: $N = 5$.

5. Conclusions

In a previous work of Hoppensteadt and Izhikevich [10], fully connected PLL network was proposed as a neural network showing that the synchronous state is an emergent property of the whole network and that the computation performed is robust to the variation of PLL parameters.

Their work was complemented by studying an 4-node network under gain and delay variations [22] and an additional interest arose to generalize the results for a N-node network, to be applied as a clock distribution system in a communication network.

Expression (3.14), derived here, represents a good estimation for frequency of the synchronous state, as Figures 4.3 and 4.6 show. Besides, observing how this frequency depends on the gain (Figure 4.7) and comparing it with the theoretical value given by (3.14), less than 0.1% deviations were observed, in the worst case.

Figure 4.8 shows that for small values of the propagation delays there is a value for the gain corresponding to the maximum acquisition time. For high-propagation delays the capture range, μ_2 allowing synchronous state, is more restrict and the acquisition time is too high. In spite of this, the synchronous state is reachable, as Figures 4.1, 4.2, 4.4, and 4.5 show. Consequently, given the propagation delays, it is possible to choose a set of PLL gains in order to allow the network to synchronize.

These results confirm that the fully connected PLL architecture, that is generally cheap and reliable, could be an interesting solution for distributing clock information in a communication network.

Acknowledgment

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