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Synthesis of Averaged Circuit Models for Switched Power Converters *

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Abstract

Averaged circuit models for switching power converters are useful for purposes of analysis and obtaining engineering intuition into the operation of these switched circuits. This paper develops averaged circuit models for switching converters using an in-place averaging method. The method proceeds in a systematic fashion by determining appropriate averaged circuit elements that are consistent with the averaged circuit waveforms. The averaged circuit models that are obtained are syntheses of the state-space averaged models for the underlying switched circuits. An important feature of our method is that it is applicable to switched circuits whose non-switch elements may be nonlinear. Our approach is compared and contrasted with the results on averaged circuit models currently available in the literature.

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1 Introduction

This paper studies the existence and synthesis of non-switched circuits that exhibit the dynamics described by the state-space averaged model of a given switching power converter. An averaged circuit representation for a switching converter is of use for purposes of analysis (e.g. circuit-based simulation) and for obtaining engineering intuition into the operation of a given switching converter. In order that the averaged circuit be most useful, it is desired that this model resemble as closely as possible the underlying switched circuit. The method of *in-place averaging* pioneered by Wester and Middlebrook [14] is a natural approach for obtaining averaged circuit models. With this method, one attempts to replace each element of the switched converter circuit by an appropriate "averaged element." The main contribution of this paper is in extending the earlier results of [14] (and others) on averaged circuit synthesis. In particular, we give a systematic approach for synthesizing averaged circuit models that realize their respective state-space averaged models. One of the most interesting extensions offered by our work is that our synthesis procedure is applicable to switched circuits whose non-switch elements may be nonlinear. This is not a feature of any previous work.

The paper is organized as follows. Section 2 of the paper presents background on modeling of switching power converters; an up-down converter is used as the main example in that section and in the remainder of the paper. Undoubtedly, the ideas developed in this paper are applicable to other areas where switched circuits are used, but we focus our attention on switching power converters since this application area motivated our research. As mentioned above, there has been significant previous work on the synthesis of averaged circuit models. We give a brief summary of this work in Section 3. The relationships between our results and previous ones are also discussed as our development proceeds. Our main results on averaged circuit synthesis are contained in Section 4 along with a number of examples. Summarizing remarks and suggestions for future research are included in Section 5.

2 State-Space Models for Power Electronic Circuits

This section develops a state-space model for an up-down converter to illustrate the nature of state-space models for power electronic circuits. This model and certain variants of it are used extensively as examples in the remainder of the paper. For more details on modeling of power electronic circuits, see [1,2,3,16].

Consider the up-down converter shown in Figure 1a). The nominal steady state operation of such a converter involves a cyclic process. The transistor is turned on in the first part of the cycle, so that the inductor current ramps up. During this time, the diode is reverse biased (a non-conducting state) so that the capacitor voltage decays into the load. Then, in the second part of the cycle, the transistor is turned off and the diode becomes forward biased (a conducting state), so that the inductor current flows through the diode into the capacitor and the load. Typical waveforms are displayed in Figure 1b). With this type of cyclic operation, the average value of the capacitor voltage v in the steady state can be made either larger or smaller in magnitude than the source voltage V_s. This is why the circuit is termed an *up-down converter*. One can determine the approximate steady state transfer ratio from source voltage to average capacitor voltage by noting that the average voltage across the inductor is zero in steady state, and hence

$$(d)V_s + (1-d)v_n = 0 \tag{1}$$

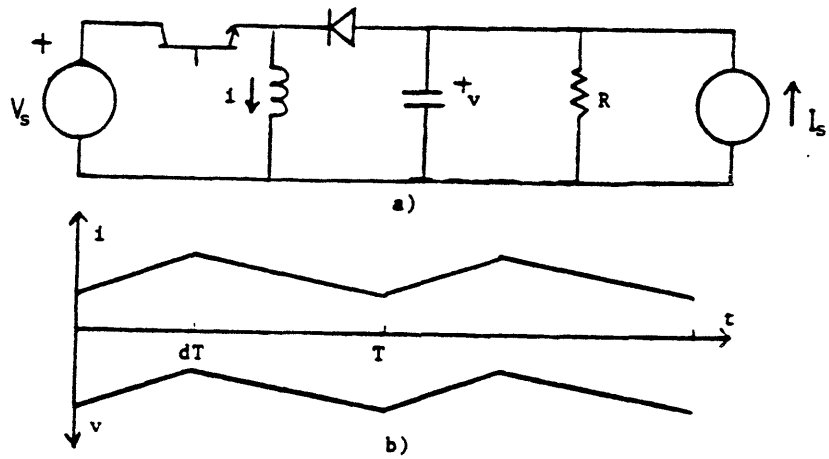

Figure 1: a) Up-Down Converter, and b) Typical Waveforms

where v_n is the nominal steady state value of the capacitor voltage and d is the *duty ratio*, that is, the fraction of each cycle that the transistor is on. From (1), we readily obtain

$$v_n = -\frac{d}{1-d}V_s. \tag{2}$$

Under the restriction that the inductor current i is always positive (so-called continuous conduction), we can model the transistor-diode pair as a single pole, double throw (SPDT) switch. Note that the position of the switch can always be dictated by turning the transistor on ($u = 1$) or off ($u = 0$). When either switch position is specified, the circuit can be characterized by a linear, time-invariant (LTI) model. Suppose that under $u = 1$, the model is given by

$$x' = A_1 x + B_1 w \tag{3}$$

and under $u = 0$, is given by

$$x' = A_0 x + B_0 w \tag{4}$$

where x is the state vector of the capacitor voltage and the inductor current, x' is its time derivative, and w is the vector of voltage and current source values. Note that we have not explicitly noted the time dependence in the state x and its derivative x', and we shall continue this omission throughout the paper when such dependence is clear from the context. An ensemble model can be obtained by combining (3) and (4) as

$$x' = [A_0 + u(A_1 - A_0)]x + [B_0 + u(B_1 - B_0)]w. \tag{5}$$

This is termed a bilinear state-space model because the control u enters multiplicatively with the state, as well as linearly. For the up-down converter of Figure 1, the state-space representation

takes the form:

$$\begin{bmatrix} i' \\ v' \end{bmatrix} = \left\{ \begin{bmatrix} 0 & 1/L \\ -1/C & -1/RC \end{bmatrix} + u \begin{bmatrix} 0 & -1/L \\ 1/C & 0 \end{bmatrix} \right\} \begin{bmatrix} i \\ v \end{bmatrix} + u \begin{bmatrix} V_s/L \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ I_o/C \end{bmatrix} \tag{6}$$

Note that the control variable u takes on only the values 0 and 1.

In the more general case where nonlinear circuit elements are present in a switching converter, the ensemble model (5) would take the more general form

$$x' = f_0(x) + u(f_1(x) - f_0(x)). \tag{7}$$

Note that terms corresponding to independent sources may be absorbed into $f_0(\bullet)$ and $f_1(\bullet)$ in (7). In some applications involving time-varying source and/or load waveforms, the vector-valued functions $f_0(\bullet)$ and $f_1(\bullet)$ may be time dependent. For all cases of interest in this paper, $f_0(\bullet)$ and $f_1(\bullet)$ will be continuous functions of their arguments.

There are many converters of interest that admit more than two switch configurations. For details on modeling these converters and on deriving averaged circuit representations, see [28].

State-Space Averaged Models To facilitate the use of well established control design methods based on state-space models that have a continuously variable input, *state-space averaged* models for switching converters have been developed [4,5,16]. A state-space averaged model is an approximation to a model that contains discrete control inputs (such as (6)), and can be obtained by replacing the instantaneous values of all state and control variables by their one-cycle averages, i.e.

$$\overline{x}(t) = \frac{1}{T}\int_{t-T}^{t} x(s)\,ds, \tag{8}$$

$$d(t) = \overline{u}(t) = \frac{1}{T}\int_{t-T}^{t} u(s)ds, \tag{9}$$

in the case where the converter is operated cyclically with period T. The symbol d is used to represent the duty ratio, that is the one-cycle averaged value of u. See [14,16] for discussions on the use of one-cycle averaging for developing state-space averaged models.

To develop some intuition on the approximations involved, consider applying the one-cycle average to the model (7). We obtain

$$\overline{x'} = \overline{f_0(x)} + \overline{u[f_1(x) - f_0(x)]}. \tag{10}$$

Note that the one-cycle averaging operation commutes with differentiation (as demonstrated in Section 4), and hence the left-hand side of (10) is equal to $\overline{x}'$. Under the conditions that the states do not vary much over the period of length T (small ripple assumption), and that the functions $f_0(\bullet)$, $f_1(\bullet)$ are continuous, the right-hand side of (10) can be approximated as

$$f_0(\overline{x}) + d[f_1(\overline{x}) - f_0(\overline{x})]. \tag{11}$$

This approximation can be justified by first noting that the small ripple and continuity conditions assure that the relative variation in the functions $f_0(\bullet)$, $f_1(\bullet)$ is small over the period T, and hence

$$\overline{u\,[f_1(x) - f_0(x)]} \approx \overline{u}\;\overline{[f_1(x) - f_0(x)]} = d\;\overline{[f_1(x) - f_0(x)]}. \tag{12}$$

The small ripple and continuity conditions also permit the approximations

$$\begin{aligned} \overline{f_0(x)} &\approx f_0(\overline{x}) \\ \overline{f_1(x)} &\approx f_1(\overline{x}). \end{aligned} \tag{13}$$

which lead to our result. (Note that in the case where the functions $f_0(\bullet)$, $f_1(\bullet)$ are linear or affine, (13) involves no approximation.) In summary, the state-space averaged model for (7) takes the form

$$\overline{x}' = f_0(\overline{x}) + d\,[f_1(\overline{x}) - f_0(\overline{x})]. \tag{14}$$

For the up-down converter, the state-space averaged model has an identical form to that of (6), except that the discrete input u is replaced with the continuous duty ratio d, which can take on any value satisfying $0 \leq d \leq 1$. In the remainder of the paper, we shall omit (except where otherwise indicated) the overbar notation when considering state-space averaged models, to simplify the presentation. The nature of the model of interest should be clear from the context.

In the case where the functions $f_0(\bullet)$ and $f_1(\bullet)$ possess bounded and continuous first partial derivatives with respect to x, the trajectories of the averaged model can be shown to approximate those of the underlying switched system model on a finite interval with arbitrarily small error, for sufficiently small T. See [24] for results of this type. Also see [4,5,12] for discussions of the approximations involved in averaging. Reference [24] also proves that the underlying switched system is exponentially stable if the state-space averaged system is exponentially stable (provided T is sufficiently small). Our focus in this paper is not on the approximations involved in averaging, but on the relationship between state-space averaged models and circuit realizations for these. Therefore, we omit further discussion of the approximations involved in averaging.

3 Previous Work on Averaged Circuits

The earliest work on averaged circuit models for switching converters was that of Wester and Middlebrook [14]. In [14], the technique used to obtain an averaged circuit realization for a given switching converter could be termed an *in-place* averaging scheme, where the averaging is performed directly on the circuit. In particular, [14] suggested the construction of an averaged circuit model whose branch variables are one-cycle averages (see Section 2) of the corresponding branch variables of the underlying switched circuit. This very physical approach results in an averaged circuit that closely resembles the underlying circuit. However, [14] did not adequately realize the elements required to replace the switch branches. Rather, each ideal switch pair was simply replaced by an ideal transformer. A consequence of this is that the state-space model that governs the dynamics of the obtained averaged circuit is not always equivalent to the state-space averaged model for the underlying circuit.

The later synthesis method of Middlebrook and Cuk [5,12], termed 'hybrid modeling', is based on the state-space averaged model (and proceeds apparently by inspection). This technique results in circuit syntheses that do indeed realize the state-space averaged models for their underlying models. The development by Cuk and Middlebrook in [17] illustrated an analogous approach for synthesizing averaged circuits for switching converters operating in the discontinuous conduction mode. It is claimed in [5,12,17] that the technique is applicable to any converter; however, syntheses are only given for a set of example converters. A more recent paper of Tymerski et al. [13] reverts to the technique of simply replacing an ideal switch pair by an ideal transformer.

Averaged circuit models have also been developed for the analysis of switched capacitor filters. In particular, the paper of Tsividis [18] illustrates the replacement of a capacitor and switch pair by a simple resistor. This equivalent circuit modeling involves a reduction of the order of the state-space, as is required in modeling a switching converter operating in the discontinuous conduction mode. Similar ideas were applied by other authors [19,20] for the analysis of switched capacitor circuits.

4 Averaged Circuit Synthesis

In this section, we apply the method of in-place averaging to obtain averaged circuit models that do indeed realize their appropriate state-space averaged models. Our approach will be based on compact network representations for various subnetworks in a given converter, and will typically permit the replacement of a switch pair with a simple non-switched two-port network. This development will also permit nonlinear circuit elements to be present in the converter. The question of existence of averaged circuit models is answered by a constructive synthesis procedure. See [28] for a treatment of the existence question that is independent of any synthesis technique.

The in-place averaging method is based on the application of the one-cycle averaging operation to each branch variable in a switched circuit, e.g.

$$\bar{i}(t) = \frac{1}{T}\int_{t-T}^{t} i(s)ds \tag{15}$$

for some branch current where the averaging interval T is selected to be equal to the fundamental period of the cyclic operation of the switches. A fundamental property of the resulting averaged branch variables is that these variables satisfy the same topological constraints, namely Kirchhoff's current and voltage laws (KCL and KVL), as the respective variables in the non-averaged circuit. This follows from the facts that the constraints imposed on the circuit branch variables by KCL and KVL are inherently linear algebraic constraints, and apply identically at each time instant. A first step in the synthesis of an averaged circuit is then to consider a circuit that is topologically equivalent to the underlying switched circuit. (For the present time, we can regard each switch as a two-terminal branch element.) In order to complete the synthesis, we need to specify averaged circuit elements that are consistent with the one-cycle averaged branch variables. We consider below the two distinct types of circuit elements (namely reactive and resistive) to clarify this procedure.

Reactive Elements If it is possible to obtain an averaged circuit model, such a model should include all the reactive elements of the underlying circuit. To see why, we can consider without loss of generality either a nonlinear multiport capacitor or a nonlinear multiport inductor. A nonlinear multiport capacitor can be represented by the state-space description

$$\begin{aligned} q' &= i \\ v &= f(q) \end{aligned} \tag{16}$$

where $f(\bullet)$ (assumed to be continuous) is the gradient of a scalar function, i.e. $f(q) = \nabla W(q)$ where $W(q)$ is the internal energy of the capacitor to within an additive constant. Consider the

application of the one-cycle averaging operation to this element, i.e.

$$\begin{aligned} \overline{q}(t) &= \frac{1}{T}\int_{t-T}^{t} q(s)ds \\ \overline{i}(t) &= \frac{1}{T}\int_{t-T}^{t} i(s)ds \\ \overline{v}(t) &= \frac{1}{T}\int_{t-T}^{t} v(s)ds. \end{aligned} \tag{17}$$

The averaging operation commutes with differentiation with respect to time since

$$\overline{q}'(t) = \frac{d}{dt}\frac{1}{T}\int_{t-T}^{t} q(s)ds = \frac{q(t)-q(t-T)}{T} = \frac{1}{T}\int_{t-T}^{t} q'(s)ds = \overline{q'(t)}, \tag{18}$$

and therefore, we have $\overline{q}' = \overline{i}$. In general $\overline{v} \neq f(\overline{q})$. However, because of the small ripple assumption and the continuity of $f(\bullet)$, this will be a good approximation (see the discussion in Section 2). For sufficiently small T, the approximation $\overline{v} \approx f(\overline{q})$ approaches equality arbitrarily closely. Since we are concerned with infinitesimally small T in the case of state-space averaging, it is an appropriate step in the construction of the averaged circuit model to include in the averaged circuit each nonlinear capacitor of the underlying circuit. An analogous argument applies for the nonlinear inductors. Naturally, this argument is applicable to linear reactive elements, as well.

Let us note at this point that if it is possible to synthesize an averaged circuit via the method of in-place averaging, the resulting circuit will be a synthesis of the state-space averaged model. This follows from the facts that such a circuit will include all the reactive elements of the underlying circuit, and that the port variables of these elements will exhibit the one-cycle averaged waveforms. Therefore, the time derivatives of all inductor fluxes and all capacitor charges in the averaged circuit will coincide with those of the state-space averaged model that has as its state variables the one-cycle averages of the fluxes and charges.

It is clear that the reactive elements do not pose any significant problems in the synthesis of an averaged circuit. However, the nonlinear resistive elements can present some difficulties, as discussed below.

Resistive Elements Assume that the constitutive relations for all nonlinear resistive elements are continuous. In a given switched circuit, it is possible to identify two types of resistive branch elements: (i) those with continuous current or continuous voltage waveforms and (ii) those with discontinuities in both their current and their voltage waveforms. (Note that the classification is with respect to terminal waveforms rather than constitutive relation.) It is in the latter branch type that difficulties can arise. In fact, the switch branches can be thought of as elements of this type.

To see that those resistive branch elements that have continuous current *and* continuous voltage waveforms present no difficulties, consider such a two-terminal resistor characterized by $v = r(i)$. For such a resistor, the approximation $\overline{v} \approx r(\overline{i})$ approaches an equality for infinitesimally small T. This is a consequence of the small ripple assumption and the continuity of $r(\bullet)$. Hence, the corresponding resistive element of the averaged circuit can be realized with a resistive component that is identical to that of the underlying circuit. This argument is applicable to a multiport resistor, as well. Any resistive branch that has a discontinuity in only one of its waveforms for

all admissible operation must be a source, either independent or dependent. (If the element was not a source, the normally continuous waveform would necessarily exhibit a discontinuity for some discontinuity in the complementary waveform.) The source branches can be replaced with identical ones in the averaged circuit.

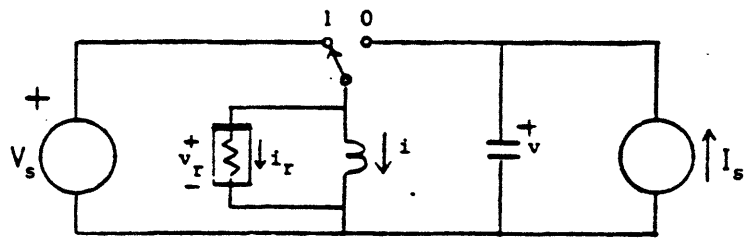

Figure 2: Switched Circuit that Violates Conditions for Simple In-Place Averaging

In the case of nonlinear resistive branches that have discontinuities in both their current and voltage waveforms, there may not exist an approximate constitutive relation that is consistent with the one-cycle averaged waveforms. To see why, consider the up-down converter of Figure 2 that has a nonlinear resistor with relation $i = g(v)$ in parallel with the inductor. The average voltage across this resistor is given by

$$\overline{v}_r = (d)V_s + (1-d)\overline{v},$$

while the average current takes the form

$$\overline{i}_r = (d)g(V_s) + (1-d)g(\overline{v}).$$

It is clear that for this resistor $\overline{i}_r \neq g(\overline{v}_r)$, and that there is no general relationship between the average current and the average voltage. The relationship depends upon the particular values of the capacitor voltage and the voltage source. Hence, for this example, it is not possible to construct an averaged circuit that simply replaces this two-terminal resistor with some other two-terminal element. Therefore, it is not possible in general to directly apply the in-place averaging procedure to switched circuits that contain nonlinear resistive elements that have discontinuities in both their current and voltage branch waveforms. However, we shall demonstrate that it is typically possible to obtain averaged circuit models for switched circuits that contain nonlinear resistive elements with discontinuous current and voltage waveforms. Our method will lump all such elements including the switch branches into a multiport element, and then attempt to replace the entire multiport with an appropriate averaged multiport element.

Note that any LTI resistive element can be replaced in the averaged model by an identical resistive element. This is a consequence of the fact that the one-cycle averaging operation commutes with any LTI constitutive relation. For the example above, if $g(\bullet)$ was linear, we would have obtained $\overline{v}_r = g(\overline{i}_r)$, despite the discontinuous waveforms.

Keeping the preceding discussion in mind, the in-place averaging synthesis technique is developed in the following two subsections. The first will treat the case where all resistive elements are

LTI and the circuit has one controlled switch pair (a two configuration circuit). The second subsection will consider the case where nonlinear resistive elements are present. See [28] for a treatment of the case where there are more than two switch configurations.

4.1 Averaged Circuit Synthesis: LTI Resistive Elements, Ideal Sources, and One Controlled Switch

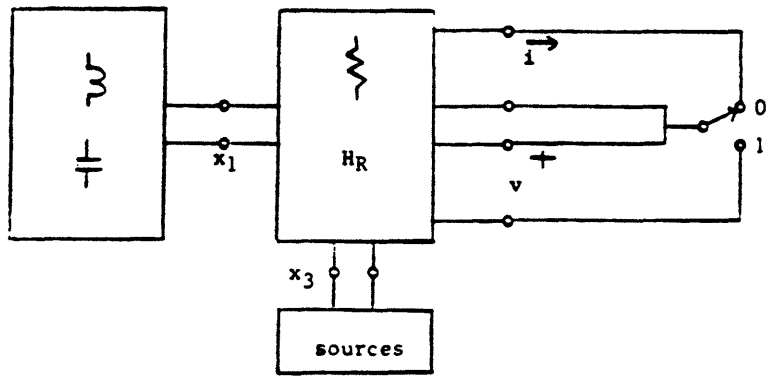

Figure 3: Partitioned Switching Converter

In this subsection, a rather simple and elegant result for a switched circuit with a single controlled switch will be demonstrated. Our approach is reminiscent of the method of reactance extraction [8] for impedance synthesis, where a given passive LTI circuit is partitioned into purely reactive and purely resistive multiports. However, the circuit diagram for a given switching converter is partitioned further into reactive, resistive, source, and switch multiports as shown in Figure 3. It was already argued earlier in this section that an averaged circuit synthesis should include all the reactive elements, all the linear resistive elements, and all the source elements of the underlying switched circuit. The motivation for the partitioning in Figure 3 is to allow us to focus on the switch subnetwork, since it is not necessary to examine the internal behavior of any other subnetwork. All that remains is to determine a resistive two-port network that can replace the switch two-port in Figure 3, and have the resulting circuit exhibit waveforms consistent with the one-cycle averaged waveforms of the underlying converter. This can be done provided Assumption 4.1 (below) holds, as will be demonstrated in the broader framework of Subsection 4.2. For the present, we state a result that gives a simple form for the averaged resistive two-port network. This requires an additional assumption (Assumption 4.2) on the existence of a particular hybrid representation for the resistive multiport in Figure 3.

Assumption 4.1 *Each branch voltage and each branch current in the underlying switching converter circuit has a unique solution corresponding to each value of the state vector of capacitor charges (or voltages) and inductor fluxes (or currents).*

Assumption 4.2 *There exists a hybrid representation for the resistive multiport (H_R) in Figure 3 with controlling port variables taken as currents for those ports connected to current source or*

inductive ports, as voltages for those ports connected to voltage source or capacitive ports, and with exactly one current-controlled switch port and one voltage-controlled switch port.

A first result is the following.

Theorem 4.1 *Suppose Assumptions* 4.1 *and* 4.2 *hold, then an averaged circuit model for the partitioned circuit of Figure 3 can be obtained by replacing the two-port switch network with a resistive two-port with hybrid representation*

$$H_s(d) = \frac{d}{1-d} H_{22} \tag{19}$$

for $d \neq 1$, where H_{22} is the hybrid immittance seen by the switch two-port when all sources and reactive variables are null. (The switch positions must be labeled so that $u = 0$ corresponds to the position where the current-controlled switch port is open and the voltage-controlled switch port is shorted.) Further, the resulting averaged model is a synthesis of the state-space averaged model for the underlying switched converter circuit.

Proof: See Appendix A.

To obtain the averaged model, one therefore only needs to compute the hybrid immittance H_{22} seen by the switch two-port, and then determine a synthesis for a scaled version of this hybrid immittance function. The linear resistive two-port synthesizing $H_s(d)$ is passive (reciprocal) if the resistive multiport H_R is also passive (reciprocal), since scaling a hybrid matrix by a positive real number preserves these properties. This result gives rise to a relatively simple approach to circuit-based analysis since one may use the non-switched averaged circuit model for analytical or computer-aided studies. There are many other ways to formulate the above problem by reorienting the switch branches inside their two-port representation. We have used one of the possible orientations that leads to a relatively uncluttered result. The following example illustrates the use of this result.

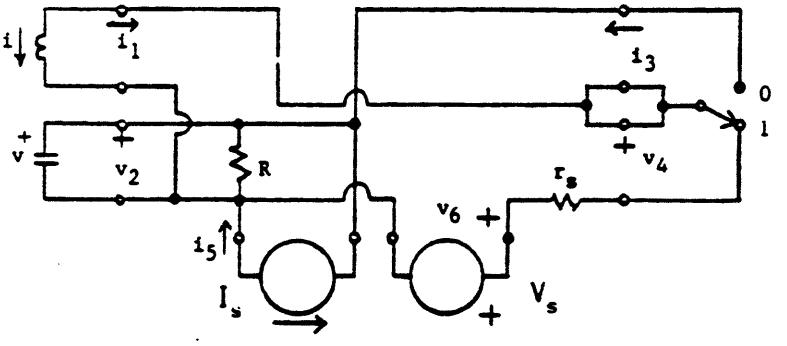

Figure 4: Partioning of Up-Down Converter with Source Resistance

Example: Up-Down Converter Figure 4 shows how we would partition a version of the up-down converter introduced in Section 2. This particular model includes parasitic resistance in series with the voltage source. It is straightforward to evaluate the immittance seen by the switch

two-port:

$$H_{22} = \begin{bmatrix} r_s & -1 \\ 1 & 0 \end{bmatrix}. \tag{20}$$

To realize the resistive two-port that replaces the switch network, we synthesize a resistive two-port (see [8]) for $H_s(d) = \frac{d}{1-d} H_{22}$. The resulting averaged circuit is shown in Figure 5. Note

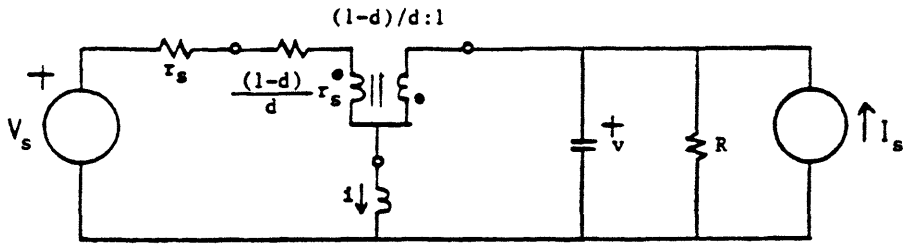

Figure 5: Averaged Circuit for Up-Down Converter with Source Resistance

that the averaged circuit includes one more two-terminal resistor than the original switched circuit. This 'extra' resistance is required to appropriately realize the one-cycle averaged behavior. Some previous work [13,14] on this problem resulted in averaged circuit models that did not include this resistance, but simply replaced the switch pair with an ideal transformer. Wester and Middlebrook [14] used a similar approach, but did not adequately model the averaged network required to replace the switch elements. Middlebrook and Cuk [5,12] synthesized averaged circuit models that included this resistance for certain example switched circuits, but their approach to averaged circuit synthesis was not as general as that given here.

Note that this averaged circuit can be used in applications where the duty ratio is a function of time (or other time-dependent variables) by inserting the appropriate time-varying value for d in the averaged circuit. One such application is in the simulation of a transient under a closed-loop control scheme. •

4.2 Nonlinear Circuit Elements

This subsection deals with the synthesis of non-switched averaged circuit models for switched converter circuits that contain nonlinear resistances and nonlinear reactances. Our development proceeds along the lines of the in-place averaging method [14], outlined earlier in this section, and relies on constraint relations (discussed briefly in Appendix B) for multiports whose internal behavior is not of interest. Our method will permit a simple replacement of the switch network in certain cases, as in the previous subsection, but when this is not possible, we shall also consider replacement of a larger portion of the resistive network than that consisting of just the switch branches. In the interest of keeping the presentation uncluttered, we shall restrict attention to the case where there are only two distinct switch configurations. The extension to the case where there are more than two switch configurations can be treated in a straightforward manner, but will not

be given here. See [28] for a treatment of the multi-switch case where all resistive elements are linear.

To carry out the averaged circuit synthesis, we require Assumption 4.1 along with an assumption on the smoothness of the network constitutive relations, namely:

Assumption 4.3 *All network constitutive relations are* C^1.

Note that a consequence of Assumption 4.1 is that the state-space model for the switching converter is well defined in each switch configuration. This holds since the inductor voltages and capacitor currents must be uniquely defined if Assumption 4.1 is in force.

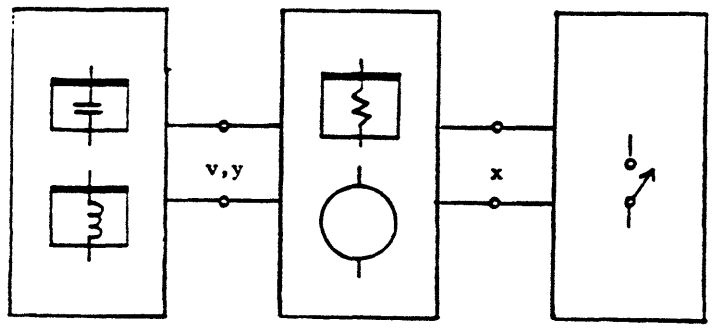

Figure 6: Partitioned Nonlinear Switched Network

Our development follows along the lines of the preceding subsection, but with the various subnetworks of the switching converter modeled by constraint relations. We organize the relevant constraint relations for a switching converter below.

Consider the partitioned switched circuit of Figure 6 where all sources are absorbed into the nonlinear resistive multiport. The multiport on the right-hand side of the figure includes all the nonlinear resistive elements that have discontinuous waveforms. For convenience, we shall refer to this multiport as the switch multiport, since it contains at least the switch branches. Let x denote the vector of switch port variables, v denote the vector of inductor currents and capacitor voltages, and y denote the vector of inductor voltages and capacitor currents. We shall construct the constraint relation for the nonlinear resistive multiport in two stages. Firstly, denote the constraints imposed by this network on the switch port variables with the relation

$$\mathcal{C}_2(v, x) = 0 \tag{21}$$

where the vector of controlling reactive port variables v is viewed as a parameter. Secondly, let the constraints imposed by the resistive multiport on the reactive port variables (v, y) be written in the form

$$-y = \mathcal{C}_1(v, x). \tag{22}$$

This can be done as a consequence of Assumption 4.1 which guarantees an explicit solution for y, the vector of inductor voltages and capacitor currents. The constraint imposed by the switch multiport will be represented by the relation

$$\mathcal{C}s_u(x) = 0 \tag{23}$$

where the dependence upon the switch configuration is noted with the subscript u. The composite constraint imposed by the interconnection of the three multiport networks takes the form

$$\begin{aligned} -y &= \mathcal{C}_1(v,x) \\ 0 &= \mathcal{C}_2(v,x) \\ 0 &= \mathcal{C}s_u(x). \end{aligned} \tag{24}$$

The composite constraint relation (24) determines the state-space model since for each value of v, this constraint determines a unique value of y. Further, this set of constraints uniquely determines the vector x of switch variables for each value of v.

With the in-place averaging method, the one-cycle averaged switch variables take the form

$$\overline{x} = d\,x|_{u=1} + (1-d)x|_{u=0} \tag{25}$$

where $x|_u$ is the value of the vector of switch branch variables when the switch configuration is u. Since, by hypothesis, each branch variable in the circuit is well defined for each switch configuration, we can determine the functional form of $x|_u$ in terms of the vector v from the constraints (24), i.e.

$$x|_u = g_u(v). \tag{26}$$

We conclude that the averaged switch vector $\overline{x}$ assumes the functional form

$$\overline{x} = g_d(\overline{v}) = d\,g_1(\overline{v}) + (1-d)g_0(\overline{v}). \tag{27}$$

Now we require conditions under which we can characterize a manifold in which the vector $\overline{x}$ is constrained to lie. Such a characterization can be made implicitly via a constraint relation, i.e.

$$\mathcal{C}s_d(\overline{x}) = 0, \tag{28}$$

or with an explicit parametrization. In the previous subsection where we considered the case in which the resistances were linear, this manifold was a subspace of $\mathcal{R}^4$.

Our main result is the following:

Theorem 4.2 *A sufficient condition for the construction of an explicit characterization of the manifold in which the averaged switch vector $\overline{x}$ must lie is that the function $\mathcal{C}_2(v,x)$ that appears in the second constraint of (24) is separable into two additive terms, i.e.*

$$0 = \mathcal{C}_2(v,x) = \mathcal{C}_{2v}(v) + \mathcal{C}_{2x}(x). \tag{29}$$

This separability condition is necessary as well as sufficient in the case where all resistances in the circuit are reciprocal.

Note that a representation $\mathcal{C}_2(v,x)$ is not unique, and the separability property may depend upon the particular choice for this representation. However, the statement holds as long as there exists some representation $\mathcal{C}_2(v,x)$ that is separable.

Proof: To demonstrate sufficiency, we give a constructive procedure for characterizing the desired manifold. See Appendix C for a proof of necessity in the case where all resistances are reciprocal. Begin by forming the two functions $g_0(\bullet)$ and $g_1(\bullet)$ which give the explicit solution x for each value of v. Note that these functions take the form (for $u = 0, 1$)

$$g_u(v) = \mathcal{D}_u^{-1}\left(\begin{bmatrix} w \\ 0 \end{bmatrix}\right) \tag{30}$$

where

$$\mathcal{D}_u(x) = \begin{bmatrix} \mathcal{C}_{2x}(x) \\ \mathcal{C}s_u(x) \end{bmatrix} \tag{31}$$

and $w = -\mathcal{C}_{2v}(v)$. Next, compute the function $g_d(\bullet)$ according to (27) which takes the form

$$g_d(\overline{v}) = \tilde{g}_d(\overline{w}) = \mathcal{D}_d^{-1}\left(\begin{bmatrix} \overline{w} \\ 0 \end{bmatrix}\right) = \{(1-d)\mathcal{D}_0^{-1} + (d)\mathcal{D}_1^{-1}\}\left(\begin{bmatrix} \overline{w} \\ 0 \end{bmatrix}\right). \tag{32}$$

The image of $\tilde{g}_d(\bullet)$ where $\overline{w}$ ranges over $\mathcal{R}^2$ (more properly the subset of $\mathcal{R}^2$ where $\tilde{g}_d(\bullet)$ is well defined) defines the manifold in which the vector $\overline{x}$ of averaged switch port variables must lie. This is typically a two dimensional manifold embedded in $\mathcal{R}^4$, and is certainly two dimensional for the extreme cases $d = 0, 1$. •

Equation (32) gives an explicit parametrization of the manifold in which the vector $\overline{x}$ of averaged switch port variables must lie. In many cases, it is possible to determine a global implicit representation for this manifold of the form (28) by eliminating the parameter $\overline{w}$ in (32). We illustrate this procedure with two examples, below.

Example: Converter with Nonlinear Source Resistance In some cases, it is possible to lump the nonlinear resistive branches that have discontinuous waveforms with the switch network, but without increasing the number of ports of this network. Such an example is the up-down converter with nonlinear source resistance that is shown in Figure 7. For the circuit of Figure

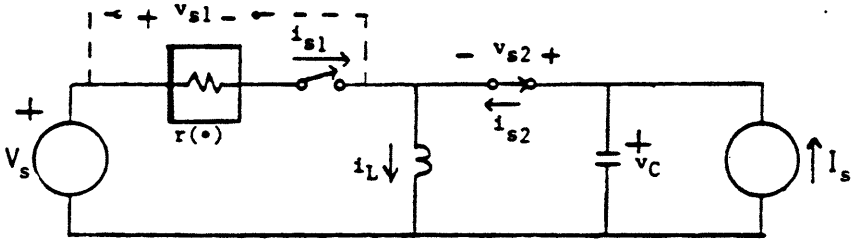

Figure 7: Up-Down Converter with Nonlinear Source Resistance

7, we can lump the nonlinear source resistance with its series switch branch, as illustrated in the

figure. With the modified port variables, we obtain the following constraint relation imposed by the remainder of the circuit:

$$\begin{aligned} -i_C &= -I_s + i_{s2} \\ -v_L &= -v_C + v_{s2} \\ 0 &= i_L - i_{s1} - i_{s2} \\ 0 &= -V_s + v_C + v_{s1} - v_{s2}. \end{aligned} \tag{33}$$

The first two lines in (33) form the constraint $-y = C_1(v, x)$. The last two lines of (33) form the constraint relation $0 = C_2(v, x)$ which can clearly be expressed in the form $C_{2x}(x) = -C_{2v}(v) = w$, as follows:

$$\begin{aligned} i_{s1} + i_{s2} &= i_L = w_1 \\ v_{s1} - v_{s2} &= V_s - v_C = w_2. \end{aligned} \tag{34}$$

To proceed, we form the constraint relations imposed by the modified switch network:

$$\begin{aligned} Cs_0 \;:\; & i_{s1} = 0 \\ & v_{s2} = 0 \end{aligned} \tag{35}$$

$$\begin{aligned} Cs_1 \;:\; & v_{s1} - r(i_{s1}) = 0 \\ & i_{s2} = 0. \end{aligned} \tag{36}$$

Next. form the two functions $\mathcal{D}_0^{-1}(\bullet)$ and $\mathcal{D}_1^{-1}(\bullet)$ by combining (34) and (35) and by combining (34) and (36), respectively. We obtain

$$\begin{aligned} \mathcal{D}_0^{-1}(\bullet) \;:\; & i_{s1} = 0 \\ & v_{s1} = w_2 \\ & i_{s2} = w_1 \\ & v_{s2} = 0 \end{aligned} \tag{37}$$

$$\begin{aligned} \mathcal{D}_1^{-1}(\bullet) \;:\; & i_{s1} = w_1 \\ & v_{s1} = r(w_1) \\ & i_{s2} = 0 \\ & v_{s2} = -w_2 + r(w_1). \end{aligned} \tag{38}$$

The function

$$\mathcal{D}_d^{-1}(w_1, w_2) = (1-d)\mathcal{D}_0^{-1}(w_1, w_2) + (d)\mathcal{D}_1^{-1}(w_1, w_2)$$

gives an explicit parametrization of the desired two dimensional manifold in terms of the parameters w_1 and w_2. This function takes the form

$$\begin{aligned} i_{s1} &= (d)w_1 \\ v_{s1} &= (1-d)w_2 + (d)r(w_1) \\ i_{s2} &= (1-d)w_1 \\ v_{s2} &= (d)(-w_2 + r(w_1)). \end{aligned} \tag{39}$$

The characterization (39) in terms of the variables w_1 and w_2 is an adequate representation of the two-dimensional manifold to which the average switch variables are constrained. However, it is possible to eliminate the parameters w_1 and w_2 by combining the lines of (39) to obtain an implicit representation of the manifold, i.e. a constraint relation. The constraint relation takes the form

$$\begin{aligned} 0 &= (1-d)i_{s1} - (d)i_{s2} \\ 0 &= (1-d)v_{s2} + (d)v_{s1} - (d)r\left(\frac{i_{s1}}{d}\right). \end{aligned} \tag{40}$$

We can obtain an equivalent hybrid representation for the resistive network described by (40) as follows:

$$\begin{aligned} i_{s2} &= \frac{1-d}{d} i_{s1} \\ v_{s1} &= -\frac{1-d}{d} v_{s2} + r\left(\frac{i_{s1}}{d}\right). \end{aligned} \tag{41}$$

The hybrid representation suggests a synthesis involving an ideal transformer and a two terminal nonlinear resistor. This synthesis is shown in Figure 8. •

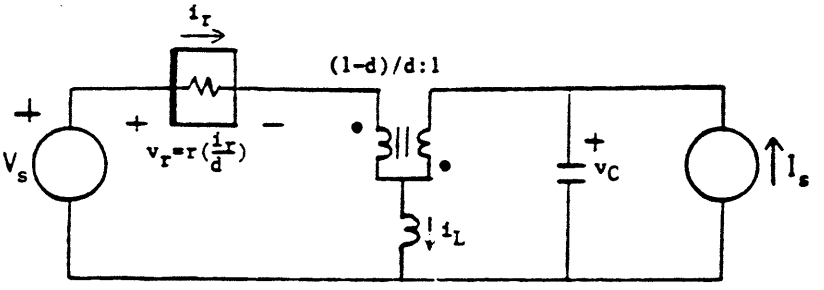

Figure 8: Average Circuit Realization for Up-Down Converter with Nonlinear Source Resistance

The following example shows how to apply our method to obtain an averaged circuit model for a converter operating in the discontinuous conduction mode. This problem was addressed in the paper of Cuk and Middlebrook [17] using the so-called 'hybrid modeling' technique, which apparently proceeds by inspection. Our approach is somewhat more systematic.

Example: Converter Operating in the Discontinuous Conduction Mode Consider the up-down converter and the typical inductor current waveform for operation in the discontinuous conduction mode shown in Figure 9. The other state variable waveforms exhibit relatively small ripple, and so are not shown. The diode in the figure is necessary to capture the circuit behavior in the discontinuous conduction mode. If the diode was not present, the L_1 inductor current could reverse, violating a basic constraint for this circuit (that this inductor current remains nonnegative at all times). In order to apply any averaged circuit synthesis technique for such a circuit, we need to recognize that a switching converter operating in the discontinuous conduction mode is governed by a reduced order state-space averaged model. This is a consequence of the fact that the L_1 inductor

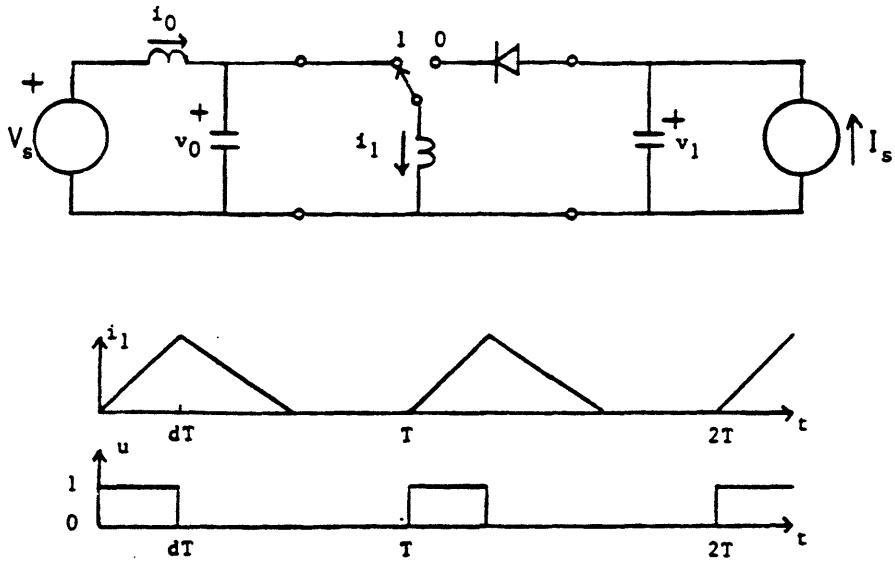

Figure 9: Model and Waveforms for Discontinuous Conduction Mode of Up-Down Converter

current is identically zero during a portion of each cycle. Therefore, in our scheme, we would treat this inductor as a nonlinear resistive element. We depart slightly from our usual framework because the waveforms for the L_1 inductor are so different from those of the other resistive elements that typically appear in a converter. Even though this inductor has a continuous current waveform, we lump it with the switch branches and the diode into a modified two-port switch network as shown in Figure 9. (If this was not done, it would not be possible to obtain an averaged circuit model.) With the indicated partitioning, it is now straightforward to apply our procedure.

The constraint $\mathcal{C}_2(v,x) = 0$ takes the form

$$\begin{aligned} v_{s1} - v_0 &= 0 \\ v_{s2} - v_1 &= 0. \end{aligned} \tag{42}$$

This constraint clearly satisfies the separability condition, and can easily be expressed in the form $\mathcal{C}_{2x}(x) = -\mathcal{C}_{2v}(v) = w$ as follows

$$\begin{aligned} v_{s1} &= v_0 = w_1 \\ v_{s2} &= v_1 = w_2. \end{aligned} \tag{43}$$

The next step is to obtain the constraints imposed by the extracted (and modified) switch network for each of the two switch configurations. Since the inductor current i_1 varies significantly over each cycle, we shall compute an averaged constraint for each of the two configurations. When the switch is in the 0 position during an interval $[t_j, t_j + dT)$, the current $i_{s2} = 0$ and the current

i_{s1} is equal to the L_1 inductor current. The average value of the latter current over this interval can readily be seen to be $\frac{v_0 dT}{2L_1}$ from the form of the waveform in Figure 9. Hence, we obtain the averaged constraint for this interval as

$$\begin{aligned} \mathcal{C}s_0 \quad : \quad & i_{s1} - \frac{v_{s1} dT}{2L_1} = 0 \\ & i_{s2} = 0. \end{aligned} \tag{44}$$

With a similar calculation for the interval $[t_j + dT, t_j + T)$ when the switch is in the 1 position, we obtain

$$\begin{aligned} \mathcal{C}s_1 \quad : \quad & i_{s1} = 0 \\ & i_{s0} + \frac{v_{s1}^2 d^2 T}{2v_{s2} L_2 (1-d)} = 0. \end{aligned} \tag{45}$$

Next. we form the two funtions $\mathcal{D}_0^{-1}(\bullet)$ and $\mathcal{D}_1^{-1}(\bullet)$ by combining (43) and (44) and by combining (43) and (45), respectively.

$$\begin{aligned} \mathcal{D}_0^{-1}(\bullet) \quad : \quad & v_{s1} = w_1 \\ & v_{s2} = w_2 \\ & i_{s1} = \frac{w_1 dT}{2L_1} \\ & i_{s2} = 0 \end{aligned} \tag{46}$$

$$\begin{aligned} \mathcal{D}_1^{-1}(\bullet) \quad : \quad & v_{s1} = w_1 \\ & v_{s2} = w_2 \\ & i_{s1} = 0 \\ & i_{s2} = -\frac{w_1^2 d^2 T}{2w_2 L_1 (1-d)} \end{aligned} \tag{47}$$

We can then form the function $\mathcal{D}_d^{-1}(w_1, w_2)$ as in the previous example, i.e.

$$\begin{aligned} \mathcal{D}_d^{-1}(\bullet, \bullet) \quad : \quad & v_{s1} = w_1 \\ & v_{s2} = w_2 \\ & i_{s1} = \frac{w_1 d^2 T}{2L_1} \\ & i_{s2} = -\frac{w_1^2 d^2 T}{2w_2 L_1}. \end{aligned} \tag{48}$$

The function $\mathcal{D}_d^{-1}(w_1, w_2)$ gives an explicit parametrization of the manifold in which the modified switch port variables are constrained to lie. It is possible to obtain a voltage controlled representation for this two-port network by eliminating w_1 and w_2 in (48). This representation takes the form

$$\begin{aligned} i_{s1} &= \frac{v_{s1} d^2 T}{2L_1} \\ i_{s2} &= -\frac{v_{s1}^2 d^2 T}{2v_{s2} L_1}. \end{aligned} \tag{49}$$

With this type of representation for a resistive two-port network that replaces the modified switch network in Figure 9, we readily obtain the averaged circuit representation shown in Figure 10.

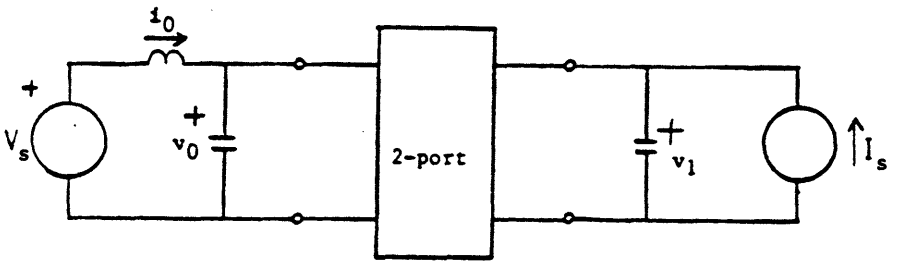

Figure 10: Averaged Circuit Model for Discontinuous Conduction Mode

It is of interest that the resistive two-port model (49) is an incrementally passive model. This can be seen by evaluating the Jacobian matrix for this model, i.e.

$$\left[\frac{di_s}{dv_s}\right] = \begin{bmatrix} \frac{d^2T}{2L_1} & 0 \\ -\frac{v_{s1}d^2T}{v_{s2}L_1} & \frac{v_{s1}^2 d^2T}{2v_{s2}^2 L_1} \end{bmatrix}. \tag{50}$$

This Jacobian matrix is evidently positive semi-definite (where it is well defined), leading to the conclusion that the two-port is incrementally passive. •

5 Summary and Suggestions for Future Research

Summary We have illustrated a systematic approach for synthesizing an averaged circuit model for a switching converter. The averaged circuit models that are obtained are realizations of the state-space averaged models for the underlying circuits, and further, resemble very closely the underlying circuits. None of the methods for averaged circuit synthesis that are presently available in the literature offers as systematic an approach to averaged circuit synthesis. Further, our approach to averaged circuit synthesis is applicable to circuits whose non-switch elements may be nonlinear. This feature is not shared by any previous work on averaged circuit models.

Future Work The results on averaged circuit models in this paper and elsewhere in the literature are applicable only to the class of switching power converters that have well defined state-space averaged models. These converters have switching frequencies that are significantly higher than the bandwidth of the averaged circuit dynamics. The class of resonant converters [2,16] can be modeled with neither the usual state-space averaging techniques nor the available averaged circuit representations. It is of interest to develop an averaged circuit modeling technique for resonant converter circuits. This development might possibly follow along the lines of the in-place averaging scheme used here and in [14]. In this case, it would be necessary to replace not only the switch network, but also the $L-C$ resonant tank elements. Because the resonant tank exhibits nontrivial low frequency dynamical behavior [2], it would be necessary to replace the tank and switch elements with a dynamical network, rather than a resistive network. This topic remains as a subject for future research.

There are many other related areas for future study. One such topic of interest is the characterization of limit cycles of in periodically switched converter circuits. We would like to investigate the relationship between the existence of an unique equilibrium for an averaged circuit model and the existence of an unique limit cycle for the underlying periodically switched circuit. This will be the subject of a future publication. Note that there has been considerable interest in this topic with some results available in [26,27].

A Proof of Theorem 4.1

Define the controlling port variables of the reactive multiport to be the inductor currents and the capacitor voltages (elements of vector x_1), the controlling port variables of the source multiport to be voltages for voltage sources and currents for current sources (elements of vector x_3), and select one of the two ports of the switch network to be current-controlled and the other to be voltage-controlled, as shown in Figure 3.

Partition H_R to reflect the three sets of ports to which it is connected, i.e.

$$H_R = \begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} \tag{51}$$

where the first set of ports are those connected to the reactive network, the second set consists of the ports connected to the switch network, and the third set corresponds to the ports connected to the source network. For the two-port switch network, with the controlling variables and switch

positions ($u = 0, 1$) indicated in Figure 3, we obtain for $u = 0$

$$H_s(0) = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}. \tag{52}$$

For $u = 1$, the hybrid representation is not well defined, but it is clear that the controlling port variables are constrained to be zero, i.e. $x_2 = 0$.

A first step in deriving the required constitutive relation is to determine the explicit solution for the vector of switch port variables for each switch configuration, i.e.

$$\begin{bmatrix} x_2|_u \\ y_2|_u \end{bmatrix},$$

where $x_2|_u$ is the vector of controlling port variables and $y_2|_u$ is the vector of complementary non-controlling port variables. (The subscript u indicates which switch configuration is present.) For this purpose, consider the application of the network constraints (KCL and KVL) at the switch ports. i.e.

$$H_{21}x_1 \quad + \quad [H_s(u) + H_{22}]x_2|_u \quad + \quad H_{23}x_3 \quad = \quad 0. \tag{53}$$

With (53) and the relations imposed by the hybrid model H_R for the resistive subnetwork in Figure 3, it is possible to solve for $x_2|_u$ and $y_2|_u$. In particular, for $u = 0$ we have

$$\begin{aligned} x_2|_{u=0} &= -H_{22}^{-1}[H_{21}x_1 + H_{23}x_3] \\ y_2|_{u=0} &= 0. \end{aligned} \tag{54}$$

The first line in (54) is obtained by noting that $H_s(0) = 0$ in (53), and that H_{22}^{-1} must exist, or else there would not exist an unique solution $x_2|_{u=0}$. The second line is a simple consequence of the fact that $H_s(0) = 0$, or equivalently, that $y_2|_{u=0}$ is constrained to be zero by the switch network. For $u = 1$, we obtain

$$\begin{aligned} x_2|_{u=1} &= 0 \\ y_2|_{u=1} &= H_{21}x_1 + H_{23}x_3 \end{aligned} \tag{55}$$

The first line in (55) is a consequence of the constraint imposed by the switch network, and the second line is obtained by considering the hybrid relationship for the resistive subnetwork.

With the above formulas for the switch port variables in each switch configuration, it is possible to determine the one-cycle averaged values for the switch port variables, i.e.

$$\begin{aligned} \overline{x}_2 &= (1-d)x_2|_{u=0} + (d)x_2|_{u=1} = -(1-d)H_{22}^{-1}w \\ \overline{y}_2 &= (1-d)y_2|_{u=0} + (d)y_2|_{u=1} = (d)w. \end{aligned} \tag{56}$$

where $w = [H_{21}x_1 + H_{23}x_3]$. Note that (56) gives an explicit parametrization of the subspace of $\mathcal{R}^4$ that contains the vector of one-cycle averaged switch port variables. This subspace is parametrized by the vector $w \in \mathcal{R}^2$. (This type of parametrization is essential in the case where nonlinear resistive elements are present in the switched circuit. See Subsection 4.2.) In the actual operation of the circuit, the port variables may not attain any arbitrary point in the subspace parametrized by w in (56), since evidently w may not assume any arbitrary value in $\mathcal{R}^2$. For our purposes, it is

adequate to characterize a two-port resistive network that constrains its port variables to lie in the defined subspace. Such a characterization is sufficient because it constrains the averaged switch port variables as required in the averaged circuit. It will be demonstrated that such a characterization will result in an averaged circuit that realizes the state-space averaged model.

A more familiar functional relationship can be obtained by elimination of w in (56), i.e.

$$\overline{y}_2 = -\frac{d}{1-d} H_{22} \overline{x}_2 \tag{57}$$

for $d \neq 1$. The relationship (57) suggests that the two-port switch network should be replaced in the averaged circuit by a resistive two-port with hybrid representation given by (19), i.e.

$$H_s(d) = \frac{d}{1-d} H_{22} \tag{58}$$

for $d \neq 1$. (A sign reversal is required to account for the opposing polarities of the non-controlling port variables of the switch and resistive subnetworks in the original switched circuit.)

To see that the resulting averaged circuit model is a realization of the state-space averaged model, consider the following explicit solution for $\overline{y}_1$, the negative of the averaged vector of inductor voltages and capacitor currents (the non-controlling reactive port variables):

$$\begin{aligned} \overline{y}_1 &= H_{11}\overline{x}_1 + H_{12}\overline{x}_2 + H_{13}\overline{x}_3 \\ &= H_{11}\overline{x}_1 - (1-d)H_{12}H_{22}^{-1}[H_{21}\overline{x}_1 + H_{23}\overline{x}_3] + H_{13}\overline{x}_3 \end{aligned} \tag{59}$$

where the form of $\overline{x}_2$ in the second line of (59) is obtained from (56). The state-space averaged model can be obtained from (59) by simply writing

$$\overline{q}_1' = -\overline{y}_1 \tag{60}$$

since $\overline{y}_1$ can in turn be written in terms of $\overline{x}_1 = Q^{-1}(\overline{q}_1)$ and $\overline{x}_3$ using (59). This is readily verified to be the form of the state-space averaged model, by noting that it varies with d on the chord connecting the two extreme state-space models obtained by solving the network equations under $u = 0$ and $u = 1$. •

B Constraint Relations

A constraint relation is a rather general way to characterize a nonlinear (or linear) resistive multiport network. As an example, consider a two-terminal resistive element whose branch variables v and i are constrained by the element to lie on the unit circle in the $v-i$ plane, i.e. $v^2+i^2 = 1$. Obviously, this element has neither a global current-controlled representation, nor a global voltage-controlled representation, and therefore illustrates the possible utility of the constraint representation. Constraint relations are also useful for LTI resistive multiport networks since it can be rather difficult to determine which subset of the port variables can serve as the controlling variables in a hybrid representation (see [15]). In general, the constraint relation for an n-port network takes the form

$$C(x) = 0. \tag{61}$$

In this paper, we consider only the where the constraint relation (61) is continuous and possesses at least first partial derivatives, i.e. $\mathcal{C}(\bullet)$ is C^1. The constraint relation (61) is termed *regular* [21] if it imposes n independent constraints on the $2n$ components of x. That is, the Jacobian matrix

$$\left[\frac{d\mathcal{C}}{dx}\right]_{x_0}$$

has rank n at every x_0 that satisfies (61). The regularity condition essentially eliminates the possible presence of unusual network types such as norators and nullators. An equivalent way to characterize a nonlinear resistive network is with an explicitly parametrized manifold embedded in $\mathcal{R}^{2n}$ that contains the port variables. For the example above (with constraint $v^2 + i^2 = 1$), such a parametrization takes the form

$$\begin{aligned} v &= sin(\sigma) \\ i &= cos(\sigma) \end{aligned} \tag{62}$$

where $\sigma \in [0, 2\pi)$. See [21] for more on this. This type of characterization is also of use in our development.

C Necessity of Separability Condition

In the case where the resistive subnetwork obtained by extracting the reactive and switch multiports is reciprocal, the separability condition given in Theorem 4.2 is necessary as well as sufficent for the existence of a constraint manifold in which the vector of averaged switch port variables must lie. This is demonstrated here. We begin by obtaining a simple necessary condition on the first constraint of the composite constraint relation (24), i.e. $-y = \mathcal{C}_1(v, x)$.

It turns out that $\mathcal{C}_1(\bullet, \bullet)$ must be linear in its second argument. This is a consequence of the fact that the state-space averaged model for duty ratio d can be expressed in terms of the variable y via

$$\overline{q}' = \overline{y} = -(1-d)\mathcal{C}_1\{\overline{v}, g_0(\overline{v})\} - (d)\mathcal{C}_1\{\overline{v}, g_1(\overline{v})\} \tag{63}$$

and equivalently by

$$\overline{q}' = \overline{y} = -\mathcal{C}_1\{\overline{v}, (1-d)g_0(\overline{v}) + (d)g_1(\overline{v})\} \tag{64}$$

where q is the vector of inductor fluxes and capacitor charges. Equation (63) results by forming a convex combination of the two extreme state-space models, while (64) is obtained by substituting the form of the averaged switch port vector $\overline{x}$ into the first line of (24). Since $g_0(\bullet)$ and $g_1(\bullet)$ are general functions and (63,64) hold for all $d \in [0,1]$, $\mathcal{C}_1(\bullet, \bullet)$ is evidently linear in its second argument. The separability condition on the second constraint of (24) is a consequence of this condition and the reciprocity of the resistive network modeled by the first two lines of (24).

To see this, consider the manifold determined by the second constraint of the constraint relation (24). Recall that this is the manifold to which the vector of switch port variables is constrained by the resistive subnetwork, with the vector v of controlling reactive port variables viewed as a constant parameter. At any given point in the configuration space, such a manifold must locally have at least one hybrid description of the form

$$x_2 = h(v, x_1) \tag{65}$$

where the dependence on the parameter vector v is noted explicitly. (This follows from the analogous property of linear resistive networks [22,23]. The tangent space of the constraint manifold at the point (x_1, x_2) is a local approximation to this manifold.) With these coordinates, we can obtain a hybrid representation (at least locally) for the resistive network described by the first two constraints in (24). Such a representation takes the form

$$\begin{aligned} -y &= \tilde{C}_1(v, x_1) = C_1\{v, (x_1, x_2)\} \\ x_2 &= h(v, x_1). \end{aligned} \tag{66}$$

Now the hybrid relation (66) must retain the property that the first line involving the variable y is linear in x, or x_1 in this case. The reciprocity of the resistive network implies that the Jacobian matrix for this hybrid representation must satisfy

$$H\Sigma = \Sigma H^* \tag{67}$$

where Σ is a diagonal (signature) matrix with all its diagonal elements either $+1$ or -1. Consider partitioning the relationship (67) commensurately with the two sets of ports, i.e.

$$\begin{bmatrix} \tilde{C}_{1v} & \tilde{C}_{1x} \\ h_v & h_x \end{bmatrix} \begin{bmatrix} \Sigma_1 & 0 \\ 0 & \Sigma_2 \end{bmatrix} = \begin{bmatrix} \Sigma_1 & 0 \\ 0 & \Sigma_2 \end{bmatrix} \begin{bmatrix} \tilde{C}^*_{1v} & h^*_v \\ \tilde{C}^*_{1x} & h^*_x \end{bmatrix}. \tag{68}$$

An implication of this symmetry constraint is that

$$\tilde{C}_{1x}\Sigma_2 = \Sigma_1 h^*_v. \tag{69}$$

Because of the linearity of $\tilde{C}_1(\bullet, \bullet)$ in its second argument, the corresponding entry of the Jacobian matrix, i.e. $\tilde{C}_{1x}$, is not dependent on x_1 (or x). The symmetry constraint (69) guarantees that h_v is also independent of x_1, i.e.

$$\frac{d}{dx_1} h_v = 0.$$

A consequence of this is that $h(v, x_1)$ which appears in (66) can be expressed as the sum of two additive terms, namely as

$$h(v, x_1) = h^v(v) + h^x(x_1).$$

(This can be seen by considering the first two terms in a Taylor series expansion for $h(v, x_1)$.) The result is the separability condition of Theorem 4.2. •

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