Synthesis Strategies for Sub-V_{T} Systems

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***Abstract*—Various synthesis strategies relying on conventional standard-cell libraries (SCLs) are evaluated in order to minimize the energy dissipation per operation in sub-threshold (sub-V_{T}) systems. First, two sub-V_{T} analysis methods are reviewed, both of which allow to evaluate the energy dissipation and performance in the sub-V_{T} regime for designs which have been synthesized using a 65-nm CMOS SCL, characterized at nominal supply voltage. Both analysis methods are able to predict the energy minimum supply voltage (EMV) of any given design. Next, the results of a sub-V_{T} synthesis at EMV using re-characterized SCLs are compared to the initial synthesis results. Finally, the results of timing-driven synthesis in both the above-V_{T} and the sub-V_{T} domain are compared to the results of power-driven synthesis.**

I. Introduction

Battery-powered devices such as hearing aids, medical implants [1], and remote sensors impose severe constraints on energy dissipation. Supply voltage scaling reduces both active energy dissipation and leakage power. When applied aggressively, voltage scaling leads to sub-threshold (sub-V_{T}) operation [2]. As an alternative to full-custom sub-V_{T} circuit design, [3–5] promote the design of sub-V_{T} circuits based on conventional standard-cell libraries (SCLs).

However, most commercial SCLs are designed for the above-V_{T} domain, meaning that a) they are mainly optimized for performance, as performance has been the main concern for above-V_{T} circuit design over the last few decades, and that b) physical models describing the timing and the power consumption of the standard-cells are readily available only for the nominal supply voltage. Instead of using commercial SCLs optimized for above-V_{T} operation, standard-cell based sub-V_{T} design would ideally rely on SCLs which are especially optimized for sub-V_{T} operation [6,7], meaning that more emphasis is given to leakage reduction than to performance while designing the standard-cells. If the development of a dedicated sub-V_{T} SCL is not economic—which corresponds to the viewpoint adopted in this paper—, a commercial SCL, optimized for above-V_{T} operation, can still be re-characterized to at least generate the physical timing and power models valid for sub-V_{T} supply voltages. Beside SCLs, virtually all logic synthesis tools as well as place-and-route (P&R) tools have been developed for regular digital VLSI design in the above-V_{T} domain, and therefore use sophisticated timing-driven optimization algorithms, whereas they hardly allow to directly optimize a design for minimum energy dissipation per operation, which is an important metric for energy-constrained systems.

Contribution: This paper shows different synthesis and analysis strategies for sub-V_{T} system design using commercial SCLs and commercial logic synthesis as well as P&R tools. The focus is on energy-constrained sub-V_{T} systems, which are optimized to perform a given operation with the lowest possible energy dissipation, assuming that the system might be power-gated or turned off after task completion. Sec. II reviews and compares two methods to analyze the sub-V_{T} energy dissipation and timing of designs which have previously been synthesized in the above-V_{T} domain, before focusing on a direct sub-V_{T} synthesis and analysis flow. Sec. III discusses and compares various strategies to minimize the energy per operation: above-V_{T}-only synthesis with different power and timing constraints, and above-V_{T} synthesis (to determine EMV) followed by an incremental sub-V_{T} synthesis at EMV, again with different constraints. Sec. IV concludes the paper.

II. Synthesis and Analysis Methods

A. Above-V_{T} Synthesis with Sub-V_{T} Analysis

Due to the predominance of SCLs and design tools developed for regular above-V_{T} synthesis, it might be convenient to synthesize different architectural variants of a system, with different constraints on timing and power, in the above-V_{T} domain, and subsequently analyze and compare the energy dissipation and throughput of the various resulting designs in the sub-V_{T} domain. In this section, two methods to analyze the sub-V_{T} behaviour of designs which have previoulsy been synthesized in the above-V_{T} domain are presented and compared.

1) Analytical Sub-V_{T} Model: As shown in Fig. 1(a), the first method starts from a regular static timing analysis (STA) and voltage-change dump (VCD)-based power analysis of a fully placed, routed, and back-annotated netlist in the above-V_{T} domain. An analytical model [8,9] is then used to scale timing and power quantities to the sub-V_{T} domain. A main advantage of this analytical model is the ability to immediatly find the EMV.

The analytical sub-V_{T} frequency model in [8,9] makes the assumption that the propagation delay(s) d_{cell} of all standard-cells slow down at the same pace as the propagation delay d_{inv} of a basic inverter when the supply voltage V_{DD} is gradually scaled down. In other words, the ratio $d_{\mathrm{cell}}/d_{\mathrm{inv}}$ is assumed to be independent of V_{DD}. In order to study the accuracy of this assumption, consider the propagation delay(s) of various standard-cells, extracted from analog circuit simulation for

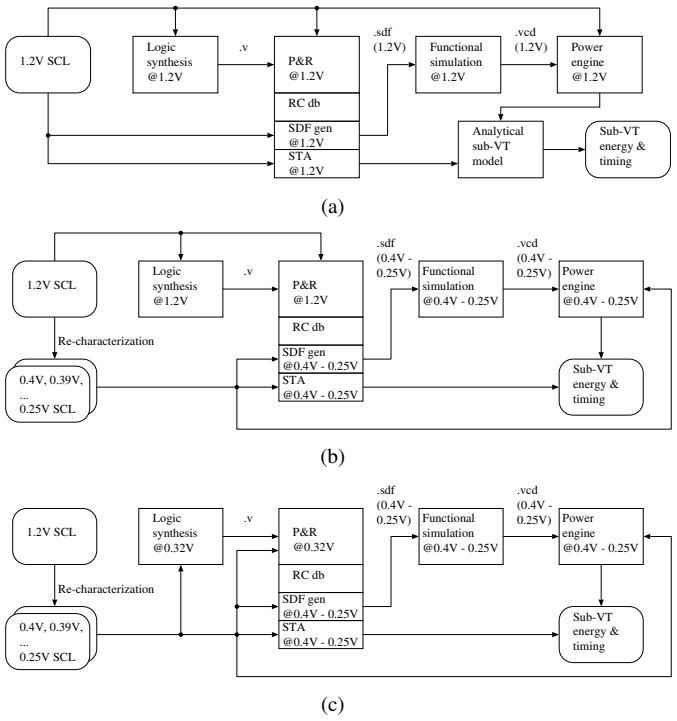


Fig. 1. Sub-V_{T} design and analysis flows: (a) Above-V_{T} synthesis, STA, and power analysis. Analytical sub-V_{T} model. (b) Above-V_{T} synthesis. Sub-V_{T} STA and power analysis. (c) Sub-V_{T} synthesis, STA, and power analysis.

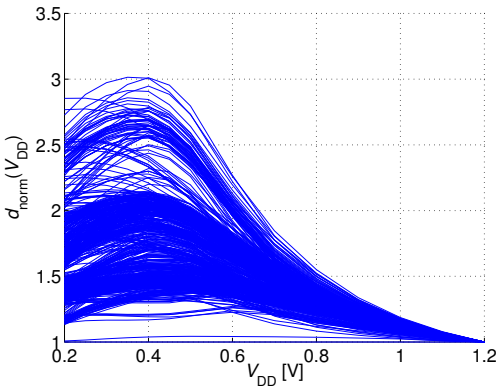


Fig. 2. Normalized delay of standard-cells.

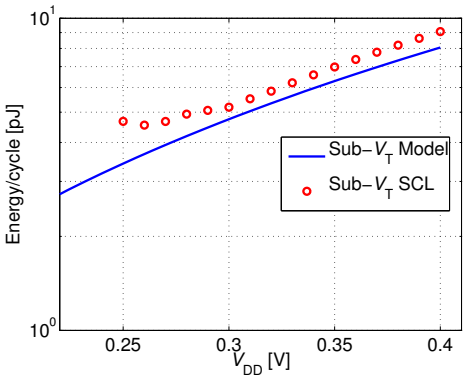


Fig. 3. Comparison of two sub-V_{T} analysis methods (analytical sub-V_{T} model and evaluation using sub-V_{T} SCLs): energy dissipation for operation at a constant frequency of 1kHz.

many different above-V_{T} and sub-V_{T} supply voltages. To better visualize a potential change of cell delays compared to the inverter delay, the *normalized cell delay* is defined as

$$d_{\mathrm{norm}}(V_{\mathrm{DD}}) = \frac{\left(\frac{d_{\mathrm{cell}}(V_{\mathrm{DD}})}{d_{\mathrm{cell}}(V_{\mathrm{DD}}=V_{\mathrm{DD}}^{(0)})}\right)}{\left(\frac{d_{\mathrm{inv}}(V_{\mathrm{DD}})}{d_{\mathrm{inv}}(V_{\mathrm{DD}}=V_{\mathrm{DD}}^{(0)})}\right)}, \qquad (1)$$

where $V_{\mathrm{DD}}^{(0)}$ is the nominal supply voltage ($V_{\mathrm{DD}}^{(0)} = 1.2\,V$ in the current case).

Fig. 2 shows $d_{\mathrm{norm}}(V_{\mathrm{DD}})$ for all timing arcs of all standard-cells in a reference design [9]. In contrast to the basic assumption of the sub-V_{T} frequency model in [8,9], we find that $d_{\mathrm{norm}}(V_{\mathrm{DD}})$ can be significantly larger than one and increases notably for most standard-cells when scaling down V_{DD}. Consequenty, the analytical model [8,9] underestimates the critical path delay in the sub-V_{T} domain for the considered 65-nm CMOS SCL. A more time-consuming but more precise (in terms of timing) sub-V_{T} analysis method is discussed next.

2) Evaluation Using Sub-V_{T} SCLs: The second method, shown in Fig. 1(b), consists of re-characterizing the original SCL for many different supply voltages in the sub-V_{T} domain (from 250 mV to 400 mV in steps of 10 mV in the current case), and then repeating the STA and the VCD-based power analysis using these re-characterized SCLs. The considered low-power (LP) high threshold-voltage (HVT) nMOS and pMOS transistors in a 65-nm CMOS technology have absolute threshold-voltage values above 450 mV. For an accurate VCD-based power analysis, the standard delay format (SDF) file generation from the RC-annotated netlist, and the VCD dump from the gate-level simulation must be repeated for each supply voltage.

3) Comparison of Sub-V_{T} Analysis Methods: The results of the two sub-V_{T} analysis methods (analytical sub-V_{T} model and evaluation using re-characterized sub-V_{T} SCLs) are compared by applying them to a reference design [9] which has previously been synthesized, placed, and routed at nominal supply voltage using a 65-nm CMOS SCL.

Concerning the estimation of the energy dissipation per clock cycle for operation at a constant clock frequency, both sub-V_{T} analysis methods coincide fairly well, as shown in Fig. 3. This means that the sub-V_{T} model [8,9] does accurately predict the active energy and the leakage power.

The analytical sub-V_{T} model is thus very convenient to quickly and reasonably precisely estimate the leakage power consumption and the active energy dissipation in the sub-V_{T} domain, and to quickly have a reasonable guess of EMV. For a more precise maximum frequency and EMV estimation, it is important to re-characterize the SCL and repeat the STA in the sub-V_{T} domain.

The more precise flow, shown in Fig. 1(b), using re-characterized SCLs is used for all above-V_{T} synthesis runs

with subsequent sub-V_T analysis in the reminder of this paper.

B. Direct Sub-V_T Synthesis

For voltage-constrained sub-V_T systems, or if the approximate EMV is already known from a previous above-V_T synthesis, it might be desirable to directly synthesize in the sub-V_T domain, which allows to specify meaningful timing constraints, and to directly obtain timing and power figures for the considered supply voltage from STA and the power engine, respectively. Fig. 1(c) shows a direct sub-V_T synthesis and analysis flow, which, in addition to the supply voltage at which the logic synthesis and P&R are performed, gives the energy dissipation and timing metrics of the resulting design for the entire sub-V_T range, allowing to find the true EMV. This flow is used for all sub-V_T synthesis runs in the remainder of this paper.

III. Design Strategies

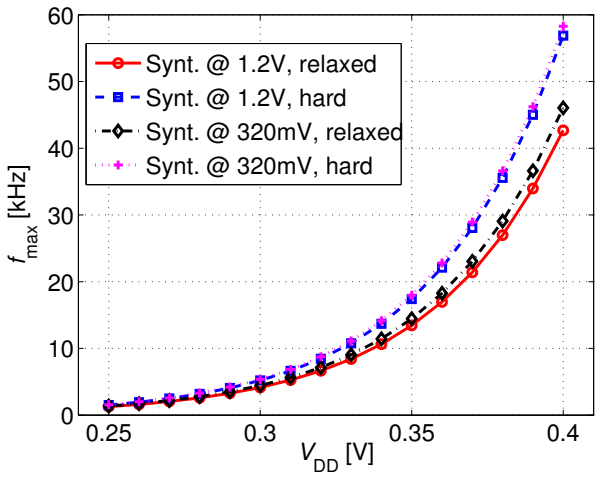
In this section, various synthesis approaches, including synthesis in the above-V_T and in the sub-V_T domain, both with different constraints on timing and power, are compared in terms of energy-efficiency.

A. Power-Driven Above-V_T Synthesis

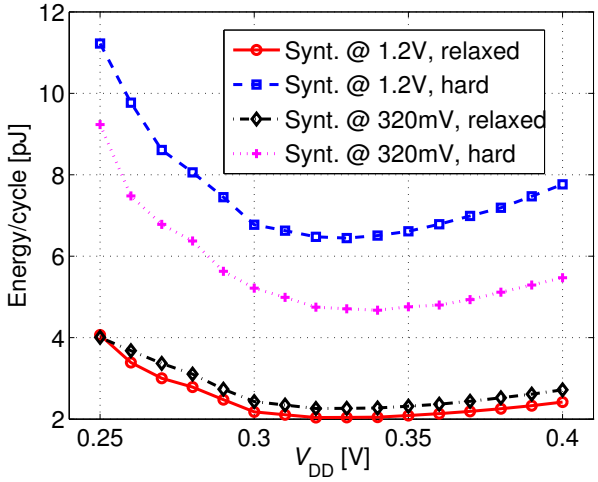
In a first approach, the logic synthesis and backend design are performed at nominal supply voltage ($V_{DD} = 1.2$ V), using commercial SCLs characterized at this voltage. Synthesis constraints are set to minimize the leakage power (and area), as leakage currents are expected to considerably contribute to the total energy dissipation for sub-V_T operation, while timing is virtually unconstrained. This relaxed timing constraint guarantees that mostly minimum-drive cells with minimum leakage current are infered during synthesis. In Fig. 4 the circle (○) markers show a) the maximum operating frequency, b) the energy dissipation per clock cycle when operating at this frequency, and c) the energy dissipation per clock cycle when operating at 1kHz, always as a function of V_{DD}, of the design resulting from this synthesis approach. As shown in Fig. 4(b), there is an EMV at 320 mV for maximum-speed operation.

B. Power-Driven Sub-V_T Synthesis

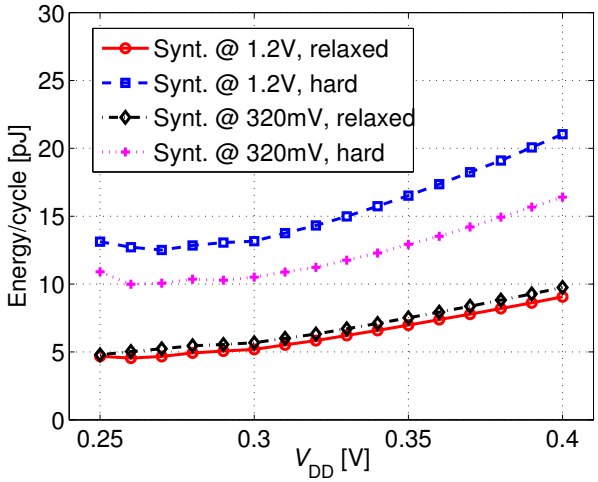
With the knowledge of EMV of the initial design synthesized in the above-V_T domain with a very relaxed timing constraint, an incremental synthesis directly in the sub-V_T domain at EMV is performed in order to see if the synthesizer can leverage the accurate physical information of the standard-cells (power consumption and timing), valid for EMV, to yield a more energy-efficient design. Notice that EMV is a property of a design and might vary for each new design synthesized at a different supply voltage or with a different timing constraint. However, for all synthesis conditions considered in this work, EMV deviates by only 20 mV at maximum from the original 320 mV. Also, the energy at maximum speed starts to increase only very slowly when moving away from the EMV of the various designs, as shown in Fig. 4(b). Consequently, for the



(a)



(b)



(c)

Fig. 4. Comparison of above-V_T synthesis at nominal supply voltage of 1.2 V and sub-V_T synthesis at 320 mV, which corresponds to the EMV of the initial design synthesized in the above-V_T domain. For both above-V_T and sub-V_T synthesis, a very relaxed and a very hard timing constraint are chosen. (a) Maximum operating frequency, (b) energy dissipation per clock cycle for maximum speed operation, and (c) energy dissipation for operation at a constant frequency of 1kHz.

endaveour of finding the most energy-efficient design without the need of synthesizing at many different sub-V_{T} supply voltages, it is reasonable to synthesize at 320 mV. Following the reasoning for the initial above-V_{T} synthesis, the synthesis at 320 mV is driven by a leakage power and an area constraint, while there is a very relaxed timing constraint. The diamond ($\diamond$) markers in Fig. 4 show that the design becomes slightly faster, but also dissipates more energy per cycle compared to the initial synthesis. Apparently, in a leakage- and area-driven flow, sub-V_{T} synthesis has no advantage over above-V_{T} synthesis.

C. Timing-Driven Above-V_{T} Synthesis

The main metric in energy-constrained sub-V_{T} systems being the energy dissipation per operation/task, and assuming that the system is power-gated or turned off after task completion, a faster design might be more energy-efficient, even though it might require more and/or stronger cells and consequently exhibit higher leakage power. In fact, for higher energy-efficiency, a shorter clock cycle over which leakage power is integrated needs to overcompensate the increase in leakage power and the potential increase in the total switched capacitance/active energy dissipation. Energy reduction is given priority over area-increase for the considered energy-constrained sub-V_{T} systems.

The initial above-V_{T} synthesis is thus repeated with a very hard timing constraint. The square ($\square$) markers in Fig. 4 show that the resulting design is indeed significantly faster than all previous designs, which is clearly payed for by a higher energy dissipation for operation at a constant frequency. Also for operation at maximum speed, this design clearly exhibits more energy per cycle compared to all previous designs, as shown in Fig. 4(b), which means that the relatively small decrease in the critical path delay does not sufficiently compensate for the increase in leakage power and active energy dissipation.

D. Timing-Driven Sub-V_{T} Synthesis

In order to investigate if the synthesizer can leverage the knowledge of the power consumption valid for EMV, the sub-V_{T} synthesis at 320 mV is also repeated with a hard timing constraint. The plus sign (+) markers in Fig. 4 indicate that the timing-driven sub-V_{T} synthesis results in a similar speed enhancement as the timing-driven above-V_{T} synthesis. However, the timing-driven sub-V_{T} synthesis clearly leads to less energy dissiation per cycle than the timing-driven above-V_{T} synthesis, showing that the logic synthesizer can indeed benefit from the knowledge of the physical information valid for sub-V_{T} supply voltages. For timing-critical designs, it is thus beneficial to synthesize in the sub-V_{T} domain, in order to improve the energy-efficiency.

However, if timing is not critical, it is sufficient to conveniently synthesize in the above-V_{T} domain with commercial SCLs characterized at the nominal supply voltage in order to get the most energy-efficient sub-V_{T} design, if only the synthesis is driven by a tight power and area constraint, while the timing constraint is very relaxed.

For the timing-driven synthesis runs, the standard-cell area increases by a similar factor as the energy in Fig. 4(c), compared to the power-driven synthesis runs.

IV. Conclusions

Different synthesis strategies relying on commercial standard-cell libraries (SCLs) and commercial synthesis tools are compared for building an optimum energy-constrained sub-V_{T} system in the sense of lowest energy dissipation per operation performed at maximum speed.

The most energy-efficient sub-V_{T} system in the current study is obtained by above-V_{T} synthesis with a hard power and area constraint, merely using commercial SCLs which are readily available, without the need for synthesis in the sub-V_{T} domain and the associated effort to re-characterize a commercial SCL for sub-V_{T} supply voltages. However, if the design is timing-critical, it is beneficial to perform a sub-V_{T} synthesis in order to improve the energy-efficiency, compared to an above-V_{T} synthesis.

A previously developed analytical model precisely predicts the leakage power consumption and the active energy dissipation in the sub-V_{T} domain for a design which has been synthesized in the above-V_{T} domain, while for the estimation of the maximum achievable operating frequency in the sub-V_{T} domain, re-characterizing the SCL and repeating the static timing analysis in the sub-V_{T} domain is more precise.

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