

System Analysis and Implementation of Delta-Sigma Modulator Topologies with Low Gain Amplifiers in 90nm CMOS



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Declaration

Herewith I, Bilal Shahzad, affirm that this thesis titled as “System Analysis and Implementation of Delta-Sigma Modulator Topologies with Low Gain Amplifiers in 90nm CMOS” presents my own research work at Fraunhofer IIS, Germany in candidature of Master’s Degree in System on Chip Design at Royal Institute of Technology (KTH), Sweden. I confirm that this thesis is my own work, any other source wherever used are properly marked in text and listed at the end of the thesis. No information is given that violates the pledge of secrecy signed for work at Fraunhofer IIS.

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Abstract

Data converters are one of the key components in many applications ranging from wireless communication to data acquisitions system, sensors, audio electronics, video display electronics and analog microcontrollers. All of these use some type of data converter to perform the task of signal processing/condition for example in RF transceivers the received analog signal after passing through filters is converted to digital signal for further processing.

The use of delta-sigma modulators nowadays are gaining popularity over the other A/D converters because of sampling and noise shaping. Also the architecture of delta sigma modulator is a mixed system, and digital filters are present (to remove noise in case of MASH architecture) so because of these reason many programmable features can be used in the applications employing delta sigma modulator.

This thesis presents a type of delta sigma modulator which focuses on using of low gain operational amplifier and hence to operate at low voltage technologies and be more power efficient. Two topologies were presented, one having a single loop architecture but with a very highly aggressive NTF and other using multi-stage architecture with no additional digital filter to achieve the required specifications. The thesis presents the complete system analysis of the topologies, and the non-idealities modeling at system level. Then the transistor level design of the designed topologies was done in Cadence in 90nm CMOS. Each component of the designed modulator was tested individually at circuit level. The complete system was analyzed using the Verilog-A model.

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I would also like to thank my friends who are always there to listen to me and lighten up my burden.

This thesis would not have been possible if I didn't have the constant support of my parents and family. Their encouragement, belief in me is the driving force right through my educational career. Though far, their prayers have always been with me.

Dedication

*To my Mother, my Father and my Siblings, for
their everlasting Love, Sacrifices & Prayers*

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Chapter 1

Introduction

1. Introduction

Data converters are the most important part of the electronic devices, ranging from the telecommunication transceivers, data acquisition boards signal conditionings, bio medical and sensor applications. Indeed where ever there is need of interaction between analog and digital signals we need analog-to-digital (A/D) and digital-to-analog (D/A) converters.

The data converters can be classified into two main categories namely as under based on the operating frequency.

1. Nyquist-Rate Converters
2. Oversampling Converters

1. Nyquist-Rate Converters

The Nyquist-rate data converter generates a series of output values in which each output value has one to one correspondence with the input value. Mostly Nyquist rate converters operate at 3 to 20 times the input signal bandwidth (1.5 to 10 times Nyquist rate) [1]. These converters are seldom run at Nyquist rate because of difficulty in realizing the practical aliasing and reconstruction filters.

2. Oversampling Converters

In Oversampling converters, the speed of operation is greater than the Nyquist rate counterparts. They run much faster than input signals Nyquist rate (typically 20 – 512 times faster) [1]. This type of converter filters out the quantization noise that is present in the signal bandwidth and hence increases the output signal to noise (SNR). Much of the quantization noise is placed outside the band of interest by using noise shaping.

There are two main types of oversampling converters namely as

- Delta Modulators
- Delta-Sigma Modulators

The Delta modulators are not used any more on the other hand the delta sigma modulators are very popular nowadays. The delta-sigma ($\Delta\Sigma$) modulator contains a loop filter, a Quantizer (ADC) in forward path and a DAC in a feedback loop as shown in figure 1.1.

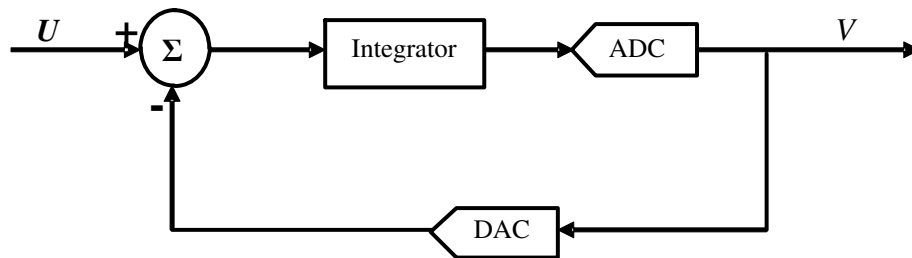


Figure 1.1: The Delta-Sigma ($\Delta\Sigma$) modulator [2]

The delta-sigma ($\Delta\Sigma$) modulators (DSMs) are usually employed in applications requiring high accuracy and low-to-medium speed and bandwidth. The reason for this is the employed oversampling operation, which eases out the requirement of the high accuracy analog circuitry at the expense of complex digital circuitry and the high sampling frequency (determined by oversampling ratio).

1.1. Motivation

With modern submicron technologies the digital circuitry can be realized very efficiently in small area with a very good performance. However the design of analog circuitry is much more complex and has to meet tough design constraints. A example of such constraint is the low supply voltages ranging to 1.2V and even below in present day technologies. Another example of tough constraint is when wide band applications come, the sampling frequency become very high (>200 MHz) for such application large power is required for amplifiers and speed of amplifiers may cross the frequency limit of technology [3, 4]. So in analog design there are trade-offs in between different design constraint the best solution.

The main motivation behind this thesis is to design a high order Delta-Sigma ($\Delta\Sigma$) modulator that uses low gain operational amplifiers. The high order modulators can be designed by using following two architectures of the Delta-Sigma ($\Delta\Sigma$) modulator.

- Single Loop High Order Modulator.
- Multistage Noise Shaping (MASH) Architecture.

Both of the above mentioned architectures have their own advantages and disadvantages. The single loop high order structure can fulfil the need of high SNR with relax requirement on circuit component i.e. low gain Op-Amps can be used. As the order increases these structures face the issue of stability. One of the reasons of instability is that all the quantization noise is to be processed in the single loop and may causes the system to go unstable.

The MASH architecture however is more stable than the single loop counterpart. MASH is made by cascading low order modulators in stages. One major drawback of MASH architectures is that we need digital filters at the output to cancel the quantization noise this increases the circuit components and face the issue of matching requirements in analog filters in the loop and digital cancelation filters at the output of individual stages [1-4].

The basic motivation of the thesis is to design new topologies that are suitable for implementation in low voltage technologies. At the same time we have to keep the circuit requirements as relaxed as possible i.e. using low gain Op-Amps to reduce the power consumption and maximum tolerance to the inaccuracies in analog circuitry components and digital filters if used.

1.2. Overview

The writing style of the report is just the explanations of the method adopted to perform the required tasks without the rigorous theory that is available in many references. The design procedure of the components is presented in detail, and the results and simulation of the individual components is also attached both at the transistor level and complete system at system level in the report.

In Chapter 1 the general use of data converters and delta sigma modulator is discussed then the motivation behind this thesis is given.

In Chapter 2, there is a short introduction about the previous work and the methodologies adopted to obtain the same goals are discussed and then three new topologies are presented.

In Chapter 3, the three new topologies proposed are modelled in Matlab/Simulink, and complete system analysis is done for these models. Also non-idealities were modelled to come close to practical scenarios.

In Chapter 4, two new topologies for implementation at circuit level are selected, that is followed by the details of circuit level implementations in Chapter 5, along with the different tradeoffs, made in selection of various components for the design of the modulator and the complete system is presented at the end of chapter.

In Chapter 6, the Verilog-A level design is done for Operational amplifier and the quantizer.

In Chapter 7, conclusion of the overall work is presented with some suggestion for the future work.

Chapter 2

Proposed Topologies

2. Proposed Topologies

The designed Delta-Sigma ($\Delta\Sigma$) Modulator should meet the specifications listed in table 2.1. The design is done in 90 nm CMOS technology with power supply voltage of 1.2V. Also the designed modulator should take care of using operational amplifier with as low gain as possible, because it would give the advantage of less power consumption.

Design Specifications	
Sampling Frequency	100MHz
Bandwidth	2.5 MHz
Oversampling Ratio	20
Order of the modulator	4
Eff. No. Of bits	>10

Table 2.1: Desired Specifications of the modulator

To achieve above specification, we can either choose a single loop delta sigma modulator, or MASH architecture, as described in previous chapter. If the new topology is single loop architecture, then the Noise Transfer Function (NTF) should be high. On the other hand if we MASH architecture is used we aim to design a topology such that matching requirement on

the analog and digital filter is relaxed or completely removed to achieve better performance and less power consumption.

Keeping these specification in mind the following three new topologies were proposed, based on the structures and techniques presented in the previous papers [3-12].

1. A Sturdy MASH (SMASH) architecture with both stages having 2nd order noise shaping using quantization noise coupling concept.
2. Sturdy MASH architecture with one stage having 2nd order noise shaping using quantization noise coupling concept and the other stage using the conventional 2nd order structure.
3. The single loop feed forward structure with quantization noise coupling.

Before going in detail of the designed topology the Sturdy MASH (SMASH) architecture that was presented first in [5] and different versions in [3,4 6]and Quantization Noise Coupling [7-9] in the modulator.

Sturdy MASH Architecture:

The basic difference between the traditional MASH and the sturdy MASH structure is that in MASH architecture we need digital filter cancellation at the output of each stage to cancel the noise of the first stage. However the Sturdy MASH (SMASH) presented in [5] removes the need of the digital cancelation filters.

The traditional MASH architecture is shown in figure 2.1. There are two digital filters H_1 and H_2 at each of the output to nullify the effect of quantization noise. There is strict requirement of matching between digital cancelation and analog loop filters. If these are not matched, which is the case in practical situations; there is some leakage of the quantization noise to the output that causes overall deterioration in the performance.

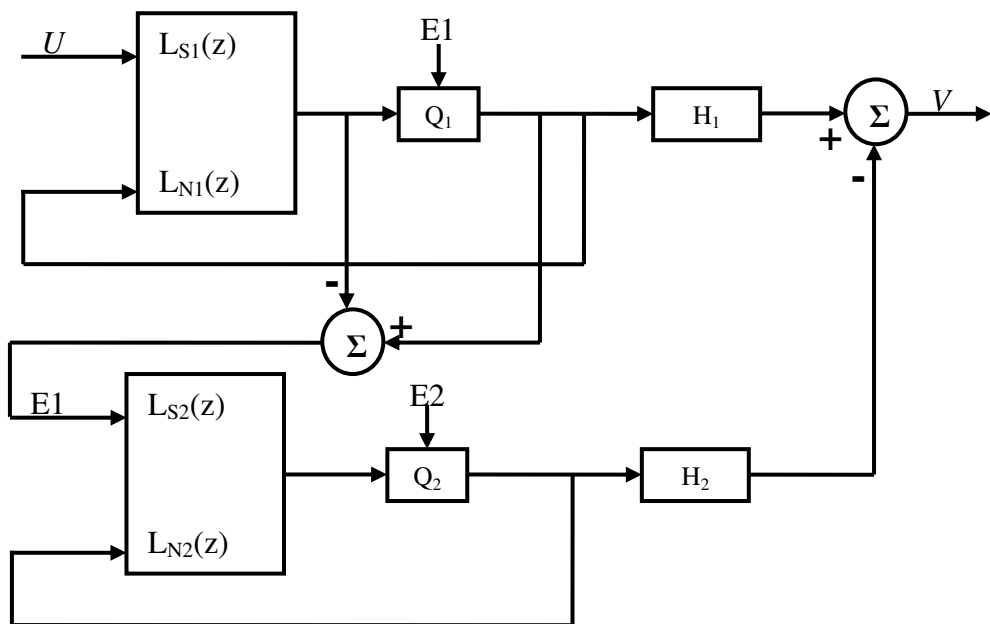


Figure 2.1: Traditional MASH architecture [5]

The effect of the leakage of quantization noise of stage 1, E_1 , can be seen more clearly if we write the equations for the output of the whole modulator [4].

$$V = STF_1U + (NTF_1H_1 - STF_2H_2) E_1 + NTF_2H_2E_2 \quad (2.1)$$

In equation 2.1 E_1 can be completely cancelled by setting digital cancelation filter response to the other stage STF and NTF as follows

$$H_1 = STF_2 \quad \text{and} \quad H_2 = NTF_1 \quad (2.2)$$

And then the output just has the quantization noise of second stage shaped by the product of both the NTF, i.e. $NTF_1.NTF_2$, since the quantization noise of the first is been completely cancelled as shown below in equation,

$$V = STF_1U + NTF_2NTF_1E_2 \quad (2.3)$$

However, if H_1 and H_2 are not perfectly match and suppose they varies as under,

$$H_1 = STF_{2a} \quad \text{and} \quad H_2 = NTF_{1a} \quad (2.4)$$

Then the output contains quantization noises from both stages and the whole output is as under [5].

$$V = STF_1U + (NTF_1STF_{2a} - STF_2NTF_{1a}) E_1 + NTF_2H_2E_2 \quad (2.5)$$

The sturdy MASH differs as it has no digital filters at its outputs as mentioned before. The sturdy MASH is shown in the figure 2.2.

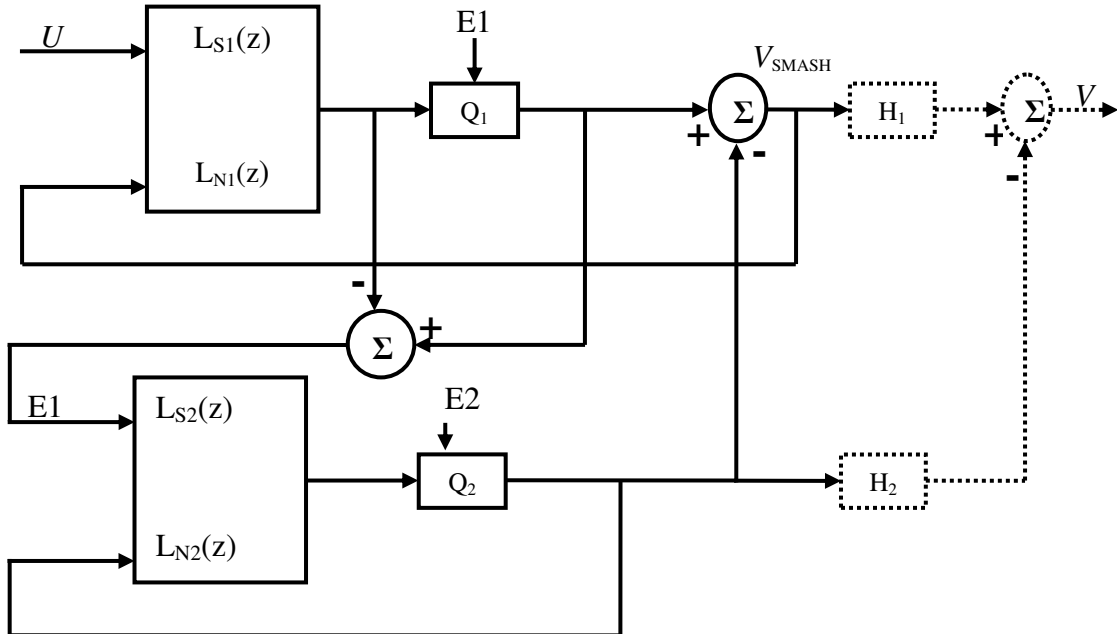


Figure 2.2: The SMASH architecture and differences (dotted blocks) from traditional MASH [5]

The quantization noise of the first stage is fed to the second stage and the output of the second stage is directly subtracted from the output of the first stage quantizer in digital domain [5].

So by using SMASH we can have advantage of no digital filters at the output and also the quantization noise E_1 is additionally noise shaped. If we write the equation of the output V_{SMASH} of the system we can see E_1 is present shown in equation 2.6.

$$V_{SMASH} = STF_1 U + NTF_1 (1 - STF_2) E_1 - NTF_1 NTF_2 E_2 \quad (2.6)$$

Now in equation 2.6, we can see that the quantization noise of both stages can be shaped to the same order if we set following condition

$$NTF_2 = (1 - STF_2) \quad (2.7)$$

Also if the second stage has unity Signal Transfer Function then the quantization noise of the systems is completely eliminated, which however has some practical limitation. In one of the new proposed topology in this thesis, it has been tried to achieve complete cancellation of quantization noise.

Quantization Noise Coupling:

The other concept behind the designed topologies is Quantization Noise coupling. The coupling of quantization noise called as noise shaping enhancement was introduced in split architecture $\Delta\Sigma$ ADC in [7]. It was shown there that a higher order noise shaping is achieved with the stability condition of one order less structure. This idea of mutual noise coupling in split architecture $\Delta\Sigma$ ADC was extended to single stage $\Delta\Sigma$ loops and split architecture with self enhancement in [8]. The scheme proposed there just replaces NTF to $(1 - z^{-1})$ times NTF hence increasing the effective order by one.

Based on these proposed architectures, instead of introducing a white quantization noise, a high-pass-filtered quantization noise (shaped quantization noise) is injected in the system as proposed in [9]. This increases the noise shaping of the modulator by the same order.

In the modulator the shaped quantization noise “ $(1 - z^{-1}).Q(z)$ ” is obtained by introduction of an extra branch , where the quantization noise $Q(z)$ is delayed by a clock cycle and subtracted by the summing node before the quantizer as shown in figure 2.3 [9] .

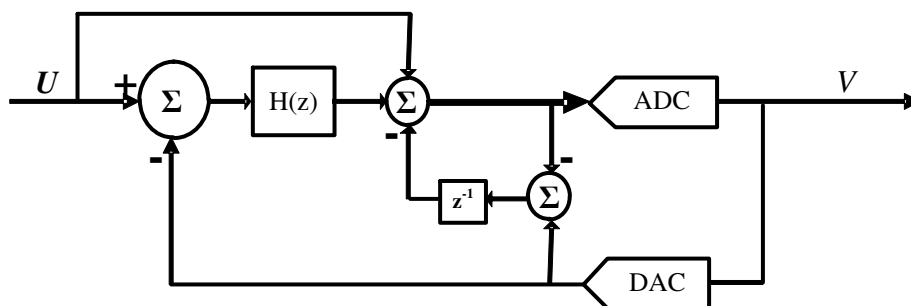


Figure 2.3: Introducing Shape Quantization Noise in the modulator using Noise Coupling. [9]

If we see the block diagram of $\Delta\Sigma$ modulator as shown in figure 2.4[9] on next page we can see how actually Quantization Noise coupling is achieved at system level. It introduces

delaying integrating function in signal path with an extra delayed output branch is added in the summing node.

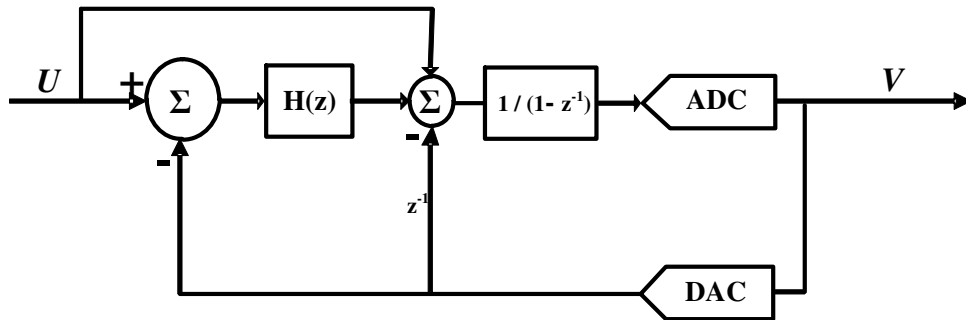


Figure 2.4: Equivalent block level representation of the Shape Quantization Noise [9].

The Quantization Noise coupling is used by all three new proposed $\Delta\Sigma$ modulator. In first two architectures, the second stage has the quantization noise coupling whereas the third structure that is single loop also uses the quantization noise coupling.

2.1 SMASH with both stages as 2nd order Noise Coupled Δ - Σ ADC

This architecture, from here on will be referred as Proposed Topology –I, as name indicates, has no digital cancellation filter at its output as in SMASH architecture [5]. Thus the condition of having a very perfect matching, accurate analog circuitry and digital cancellation filters at output implied by the traditional MASH architecture is removed. The other feature in this proposed topology is the use of Noise Coupled low distortion Δ - Σ ADC [9, 13] in each stage. By doing this we attain the added benefit of using less no. of Op-amps and that are required by the actual fourth order delta-sigma modulator (DSM) structure and hence saves power[13]. The new proposed topology is shown in the figure 2.5 where $H(z)$ is a delaying integrating function.

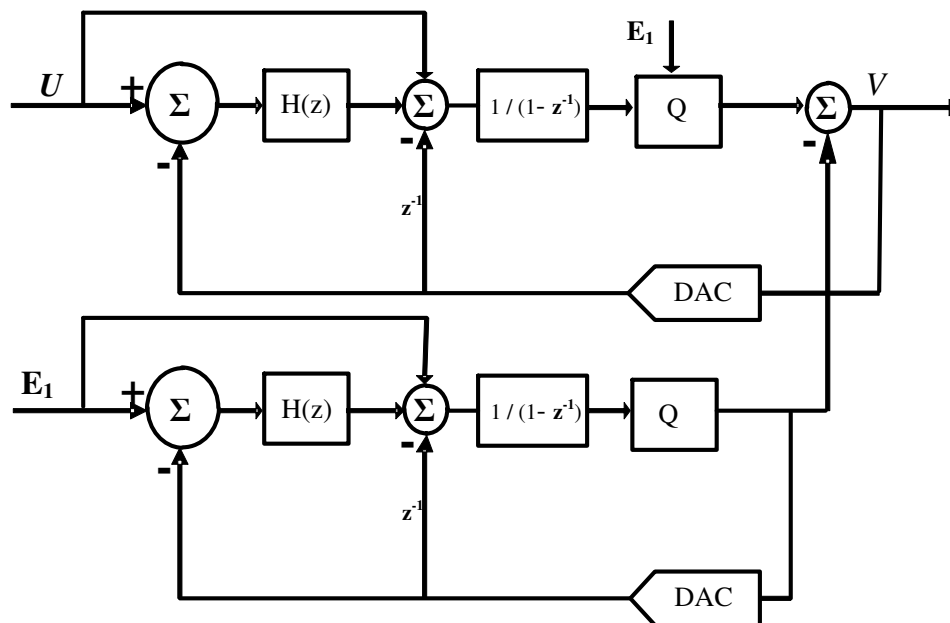


Figure 2.5: Proposed Topology-I

This topology differs from the basic SMASH structure presented in [4, 5]. In proposed topology I, second stage has a unity STF to completely remove the first order quantization noise. The quantization noise of first stage is passed through a second stage having unity STF and subtracting this processed quantization noise from first stage output as in [10]. The limiting performance factor in the SMASH performance is the first stage quantization noise [3], so if there is no first stage quantization noise we will have a very good performance.

2.2 SMASH with one stage as 2nd order Noise Coupled Δ - Σ ADC and other as conventional 2nd order Δ - Σ ADC

This architecture, from here on will be referred as Proposed Topology –II, and is based on SMASH architecture. One of its stages is the conventional 2nd order Δ - Σ ADC presented in [14] and the other as noise coupled low distortion Δ - Σ ADC presented in [9, 13]. This causes an improvement in performance and makes it more feasible from implementation point of view. The proposed topology II is shown in figure 2.6, where $H(z)$ is the delaying integrating function.

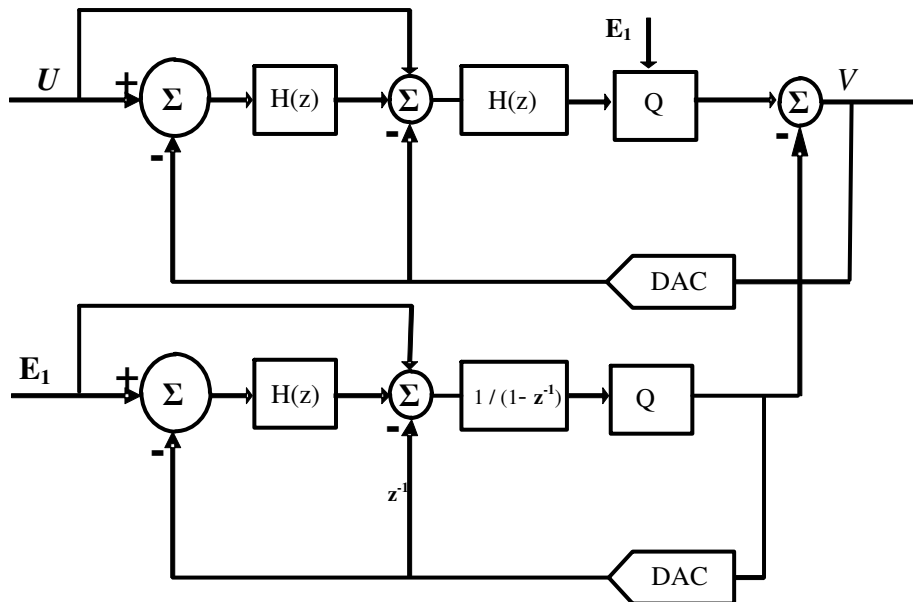


Figure 2.6: Proposed Topology-II

The only difference between the proposed topology I and II is the difference between first stages but the second stage is identical in both. The first stage in proposed topology II has both integrators as delaying, where the proposed topology I has alternate of delaying and non-delaying integrators.

2.3 Single Loop feed forward structure and the quantization noise coupling

The last possibility is to use the single loop structure with multibit quantization to achieve the required SNR. The preferable choice in single loop architectures is feed forward structure. The Feedforward delta sigma modulator requires only one feedback DAC path, and also design requirements on integrators are much relaxed than the feedback structure.

The proposed topology III, shown in the figure 2.7 on next page, is constructed by using the Feedforward architecture presented in [12], with a third order noise shaping. With enhanced noise shaping using the Quantization Noise coupling presented in [9]. The alternating delaying and non-delaying integrators are used that helps to reduce the noise peaking and hence the stability of the modulator is improved [12]. The new proposed modulator use the same number of op-amps as used by the modulator presented in the paper however provides a fourth order noise shaping. In the figure 2.7 $H_1(z)$ and $H_2(z)$ are delaying and non-delaying integration functions.

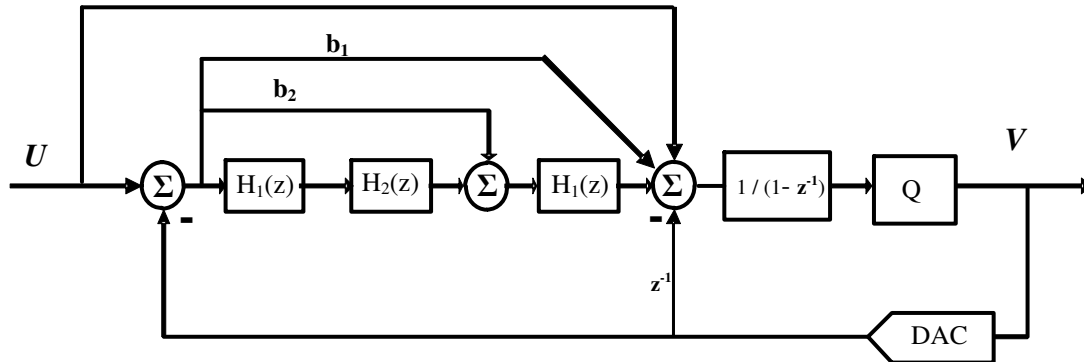


Figure 2.7: Proposed Topology-III

Chapter 3

System Analysis

3. System Analysis

As a starting point, the proposed topologies were implemented in Simulink to estimate the basic response of the modulators. The modulators were modelled by already designed Simulink blocks and some models were also written to model non ideal behaviour of the system. The models at start only used ideal delaying and non-delaying integrators and quantizer. The feedback DAC was modelled only by a zero order hold.

To run the system analysis, whole system was given a sine input, the no of quantizer bits were selected to be four (4). The required SNDR was calculated and plotted by doing the FFT of the modulator output. Each modulator was excited from full scale voltage to the about 80dB lower to the full scale value and also a plot of SNDR vs. Input Amplitude was obtained.

The simulation parameters used in the Matlab are as under

```
SR = 20;           %Oversampling ratio
bw = 2500e3;       %ADC bandwidth in Hz
ftest = 2500e3/3; %test tone frequency in Hz
fs = OSR*2*fbw;    %Sampling frequency in Hz
k = 13;           %Number of bits of the FFT
Afs = 0.45;        %Full scale value of input tone
AdB = -8;          %Tone amplitude in dBFS
A = 10AdB/20 * Afs; %Test tone amplitude in volt
```

3.1 Simulation Results of Proposed Topology-I

The Proposed Topology-I was drawn in Simulink using different pre-designed blocks and this is shown in figure 3.1 on next page.

The Proposed Topology-I was simulated in Matlab/Simulink with the parameters listed above and the Power Spectral Density plot obtained below is simulated at input amplitude of -8dB as shown in figure 3.2 on next page

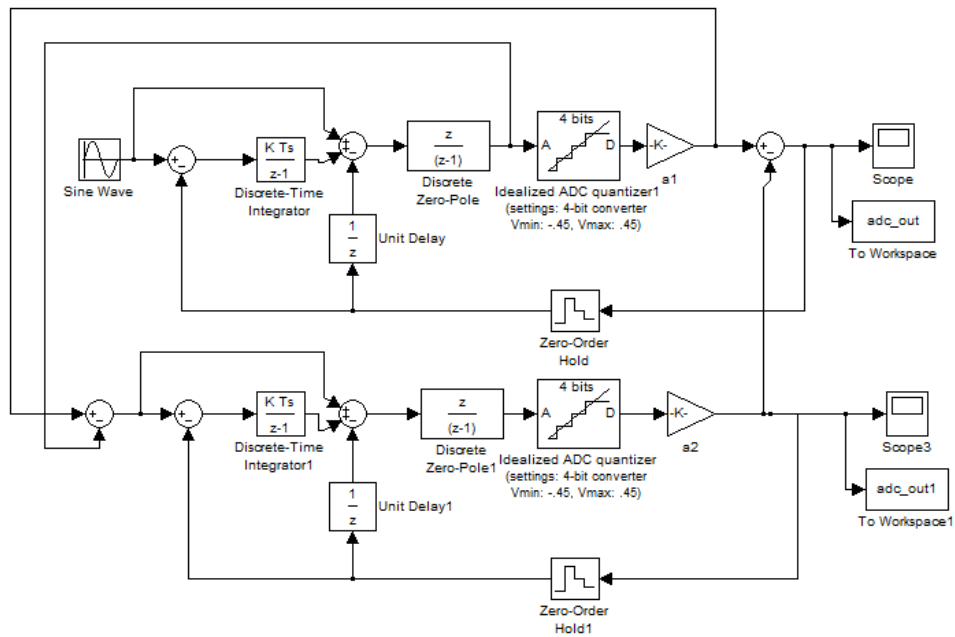


Figure 3.1: Simulink Model of Proposed Topology-I

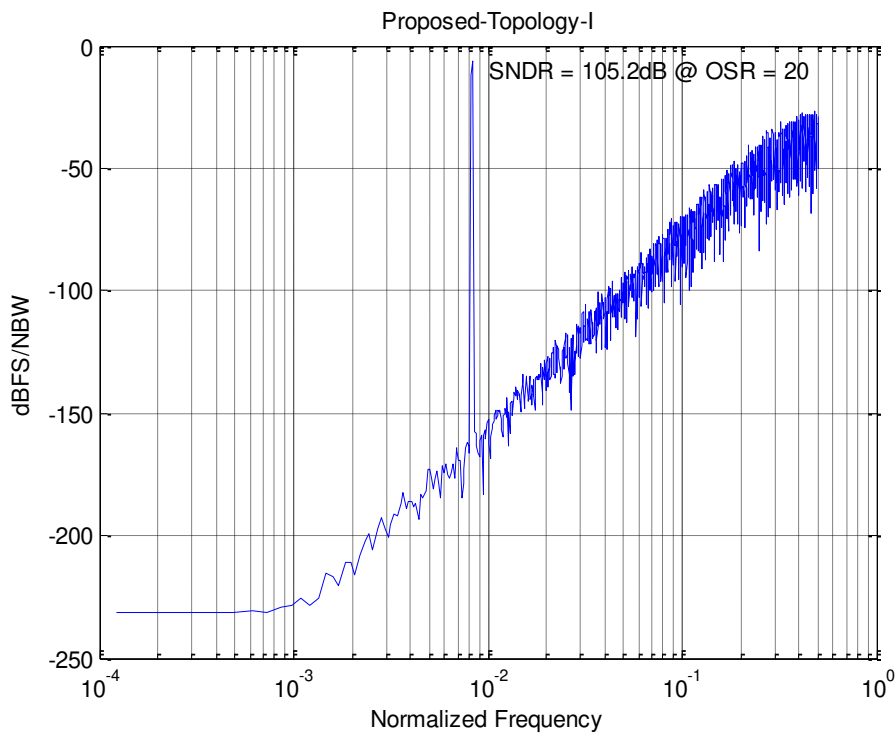


Figure 3.2: PSD of the Proposed Topology-I @ input amplitude = -8dB

In another simulation the modulator was swept from full scale value till 80dB lower than the full-scale, the result is shown in figure 3.3 on next page.

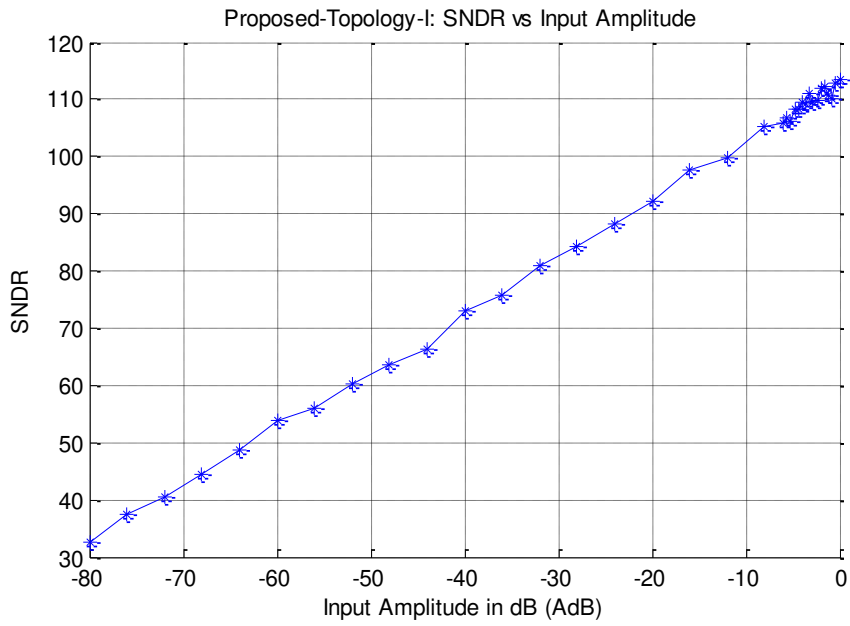


Figure 3.3: SNDR of the Proposed Topology-I for input amplitude swept from 0 to -80dB

3.2 Simulation Results of Proposed Topology-II

The figure 3.4 below shows the Simulink model of the proposed topology II.

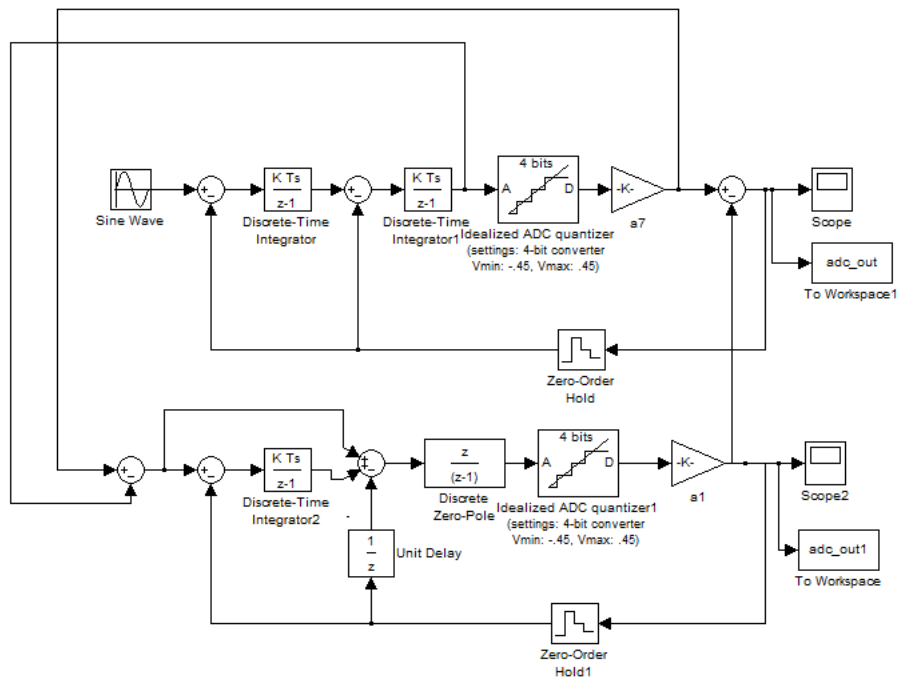


Figure 3.4: Simulink model of Proposed Topology-II

The proposed topology-II was simulated in Matlab/Simulink with the parameters listed in section 3. The Power Spectral Density plot shown in figure 3.5 is obtained with system simulation at input amplitude of -8dB.

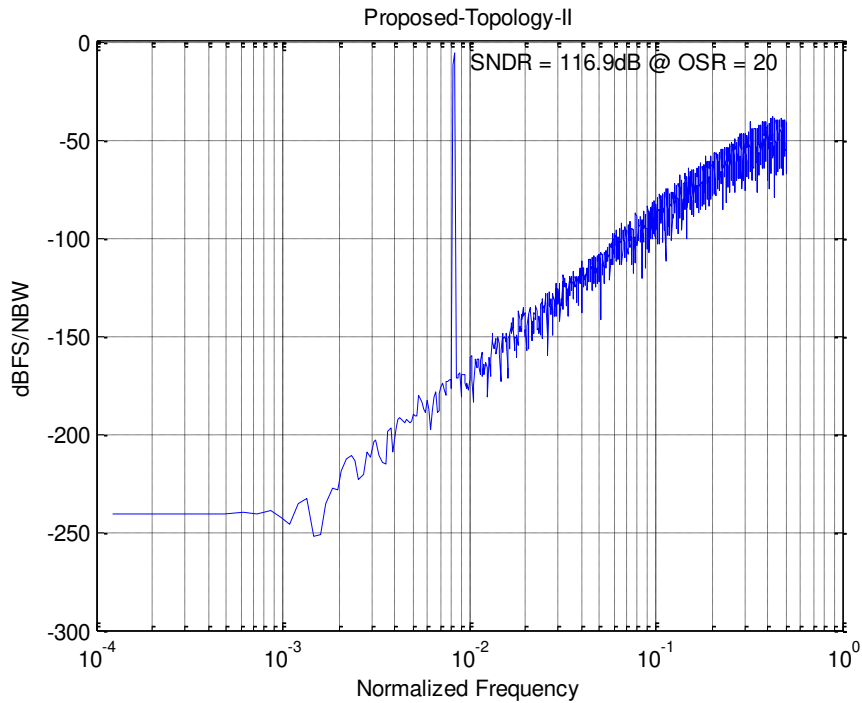


Figure 3.5: PSD of the Proposed Topology-II @ input amplitude = -8dB

In another simulation the modulator was swept from full scale value till 80dB lower than the full-scale, the result is shown below in figure 3.6.

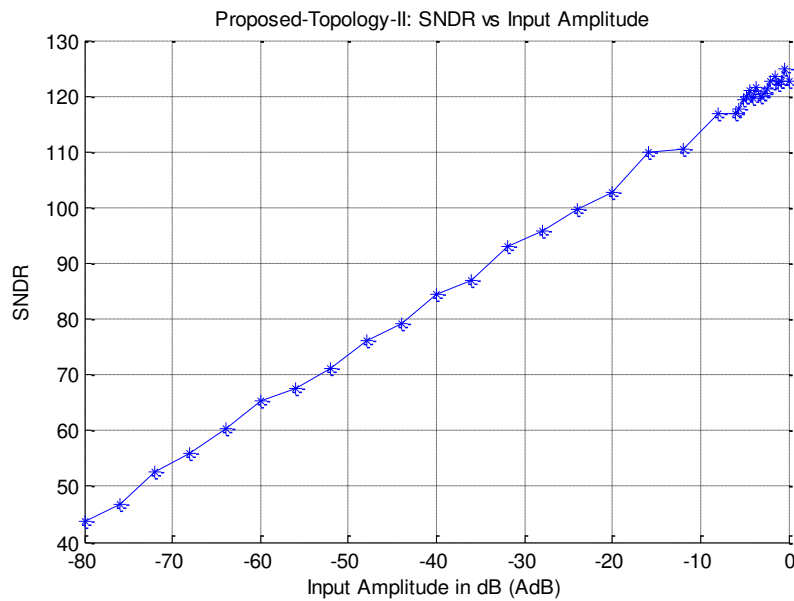


Figure 3.6: SNDR of the Proposed Topology-II for input amplitude swept from 0 to -80dB

3.3 Simulation Results of Proposed Topology-III

The Proposed Topology-III modelled in Simulink is shown in figure 3.7.

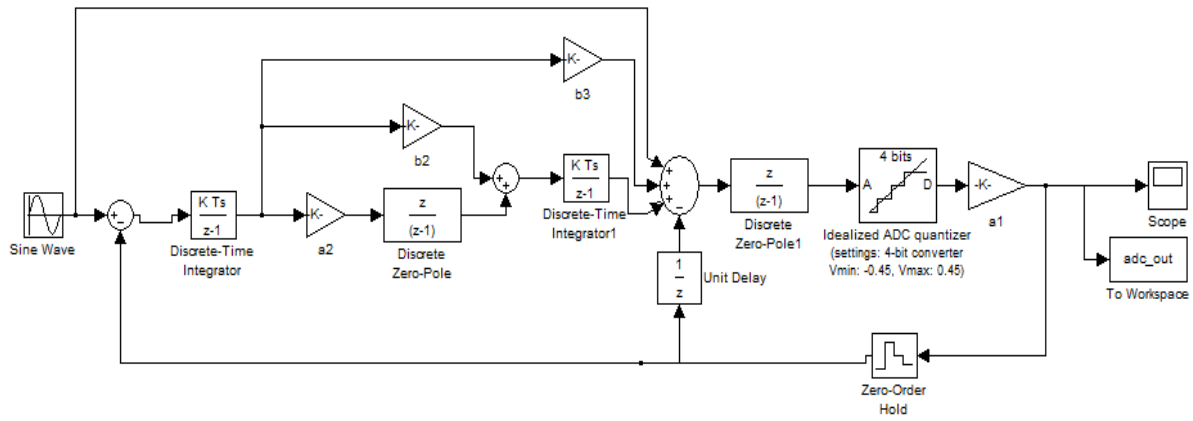


Figure 3.7: Simulink model of Proposed Topology-III

The proposed topology-III was simulated in Matlab/Simulink with the parameters listed in start of the chapter and the Power Spectral Density plot obtained below is simulated at input amplitude of -8dB shown in figure 3.8.

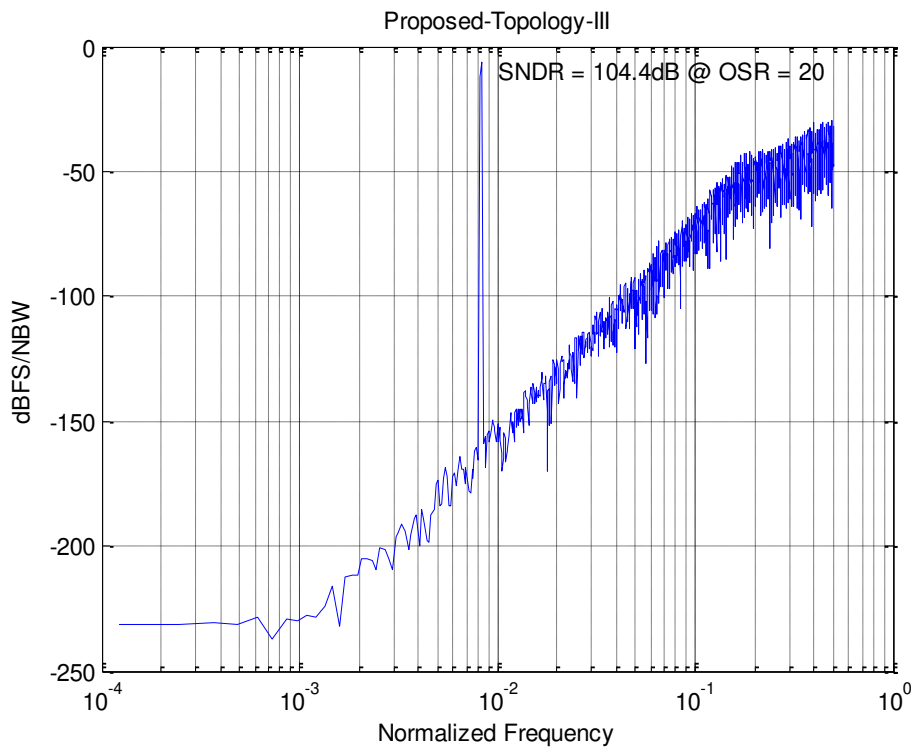


Figure 3.8: SNDR of the proposed Topology-III @ input amplitude = -8dB

In another simulation the modulator was swept from full scale value till 80dB lower than the full-scale, the result is shown below in figure 3.9.

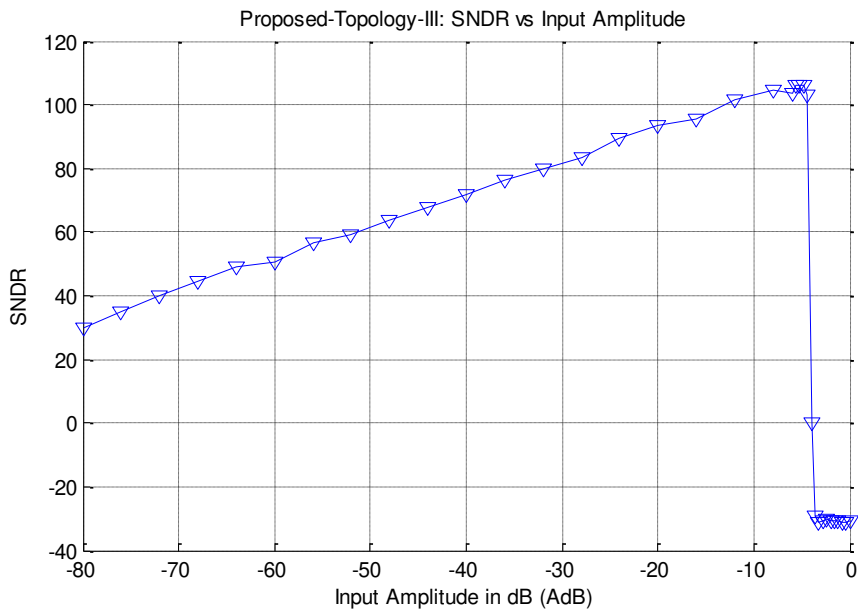


Figure 3.9: SNDR of the Proposed Topology-III for input amplitude swept from 0 to -80dB

3.4 Modelling of Non-Idealities in Proposed Topology

As the scope of the topic is to investigate the effect of use of low op-amp gain in the modulator topology, so the main concern was to see the effect, of the non-idealities associated with the op-amp. So it was important to see the performance when the ideal integrators are replaced with the model of integrators that take in account the effect of finite gain and saturation effect.

The structure that is used to model the real finite gain and saturation is presented [15] and are shown below in figure 3.10 and figure 3.11 for the delaying and non-delaying integrator respectively.

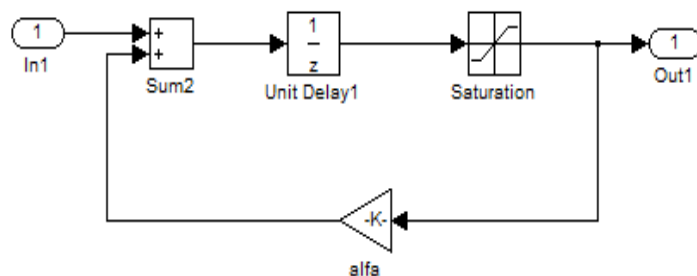


Figure 3.10: A Delaying Integrator with finite gain modelled by alpha (α) [15].

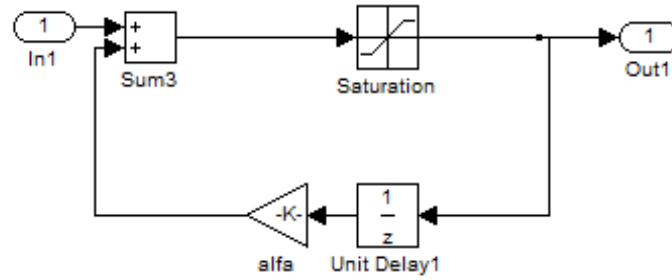


Figure 3.11: A Non-Delaying Integrator with finite gain modelled by alpha (α) [15].

The ‘alfa’ factors in different integrators are also taken different to maximize the mismatch between integrators that is present in practical scenarios. The ‘alfa’ factor is given by the equation 4.1.

$$\text{Alfa} = 1 - 1 / (10. ^ (A / 20)) \tag{3.1}$$

Where in the above equation “A” is the DC gain in db of the operational amplifier.

With ignoring the slew rate effect for the moment and the non-linearity of the operational amplifier and all topologies were simulated again, with replacing the delaying and non-delaying integrators of the proposed topology with the models of delaying and non-delaying integrators presented in [15].

The following figures 3.12-3.14 depict the SNDR once the effect of finite gain and saturation are taken into effect.

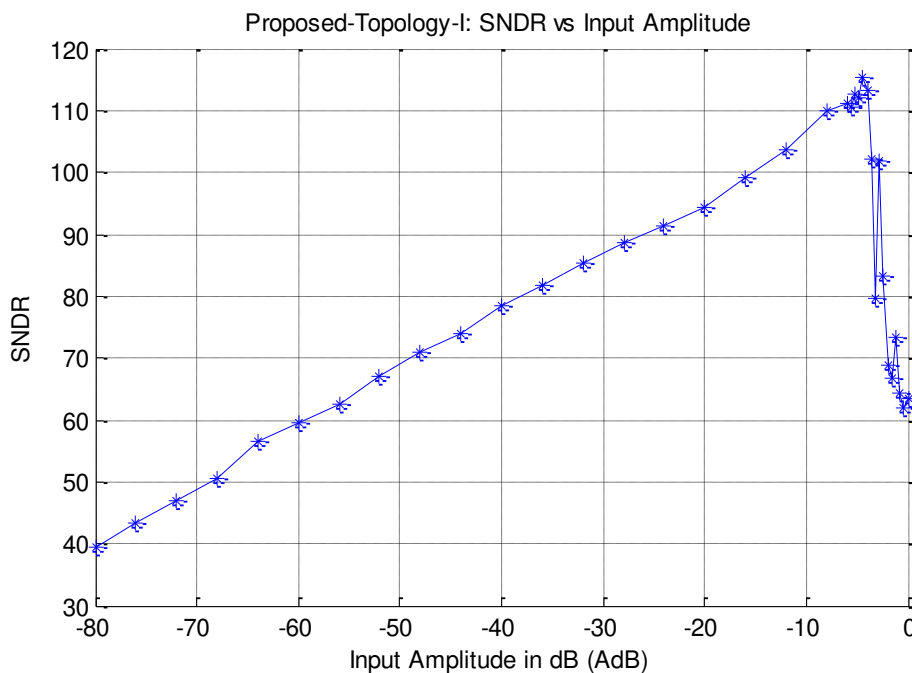


Figure 3.12: Effect on SNDR of Proposed Topology–I when Finite DC gain of Integrators considered

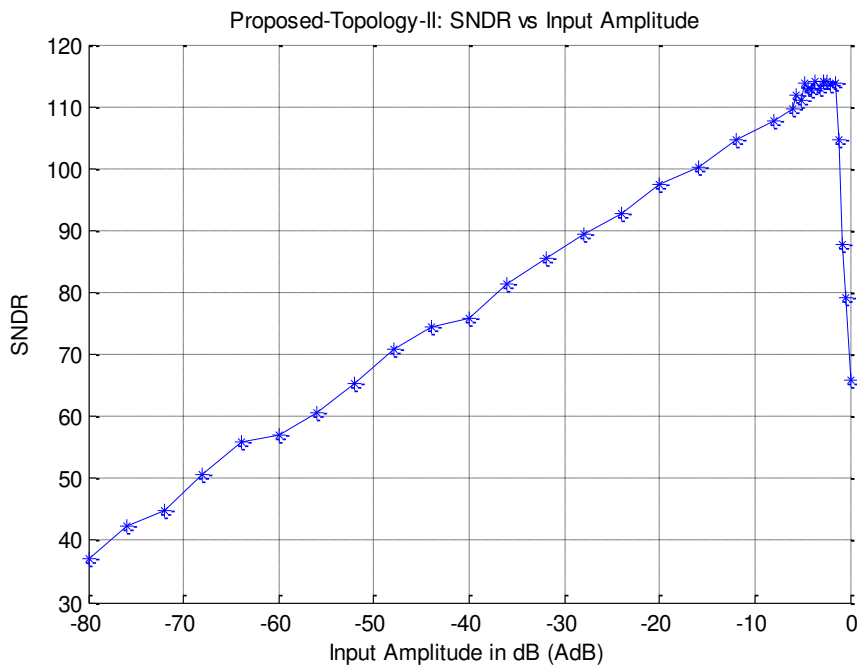


Figure 3.13: Effect on SNDR of Proposed Topology–II when Finite DC gain of Integrators considered

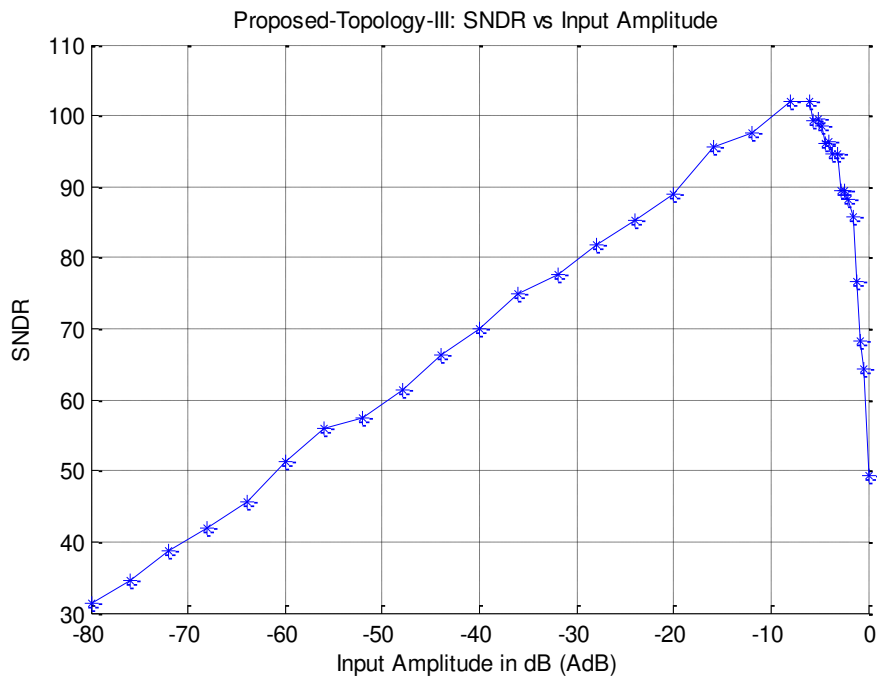


Figure 3.14: Effect on SNDR of Proposed Topology–III when Finite DC gain of Integrators considered

We can observe that the SNDR for each topology has been decreased when the non ideal effects are modelled.

Chapter 4

Selection of Topology

4. Selection of Topology

To select topologies for further investigation, figure 4.1 below shows the SNDR of all the proposed topologies. In figure it's clearly shown that Proposed Topology I and II had very similar results of the output SNDRs. Both the topologies follow each other's curve almost exactly at the higher input values however there is difference at values close to 0 db.

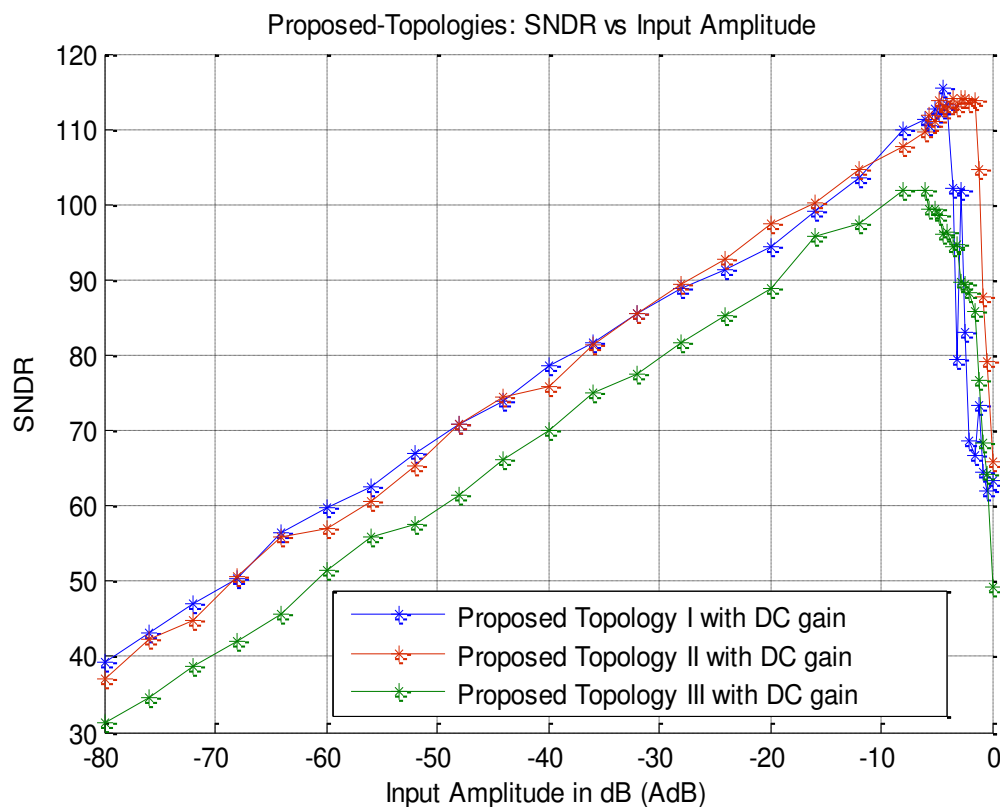


Figure 4.1: SNDR of the Proposed Topologies-I, II and III

However the timing requirements on both of these topologies from actual circuit level implementation point of view are very hard, with the Proposed Topology-I having just a single delay in signal path in both stages, hence it is difficult to fit the operation of modulator in two clock cycles, however both the topologies has the best SNDRs with a bit of disadvantage of a bit complex circuit level implementation. Also at db range around -6 db the performance of the Proposed Topology-I is not as good as the proposed topology-II.

On the other hand the proposed topology III has the most advantage of easier implementation at circuit level because of single loop structure, and also has lenient timing requirements but has bit less SNDR as compared to the other topologies but still fulfil the requirements.

Keeping these points in mind mentioned above, the last two topologies namely Proposed Topology II and III were selected for further investigation at circuit and behavioural level, giving both the options of achieving particular level of performances either using a single loop architecture or multi stage noise shaping.

However one key point is that the proposed topology-II was further modified to make it a Low-distortion that will further enhance the performance of the modulator, as know the signal transfer function is equal to one and the loop only have to process the quantization noise [7]. This change can be easily seen as a marked “X” in a circle at the two adders, where there is cancellation of the input signal at the two adders to make the Signal Transfer function as unity. The block diagram of the modified Proposed Topology -II is shown in figure 4.2.

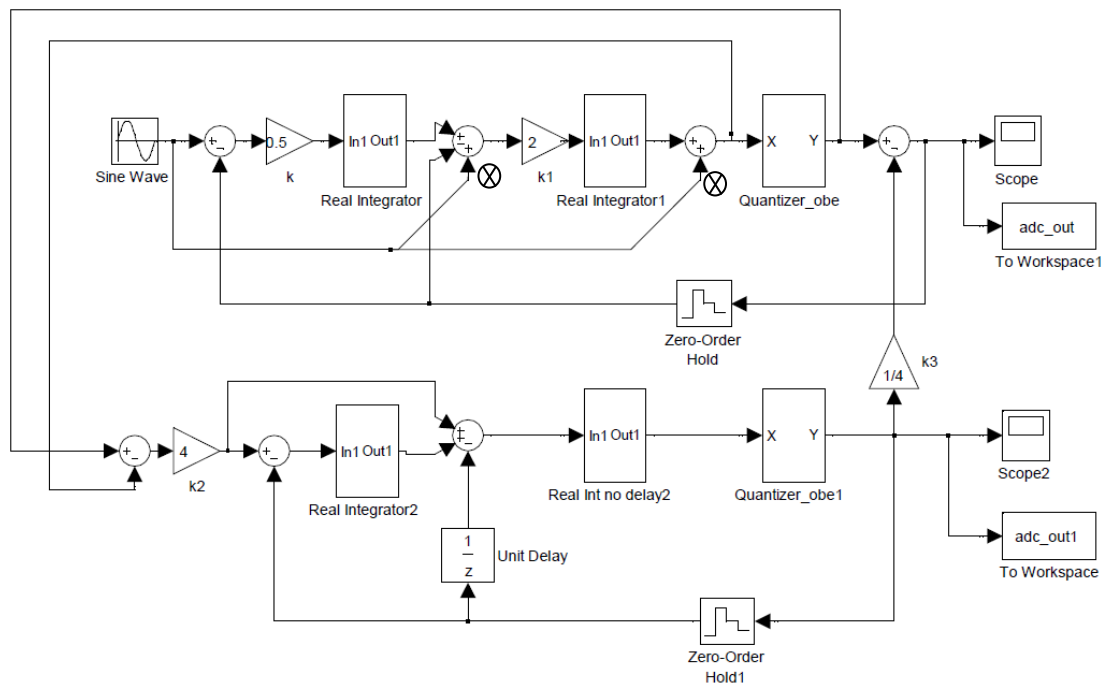


Figure 4.2: Modified Proposed Topology-II, with modification marked by X

After this modification there was an improvement seen in the SNDR at the values of input amplitude close to full scale value, however the performance at values away from the full

scale value is almost the same as before without modification. The difference in performance of the Proposed Topology II and modified Proposed Topology-II, which is pretty much evident at the zoom in near the values of full scale shown in figure 4.3 by the circle inside-

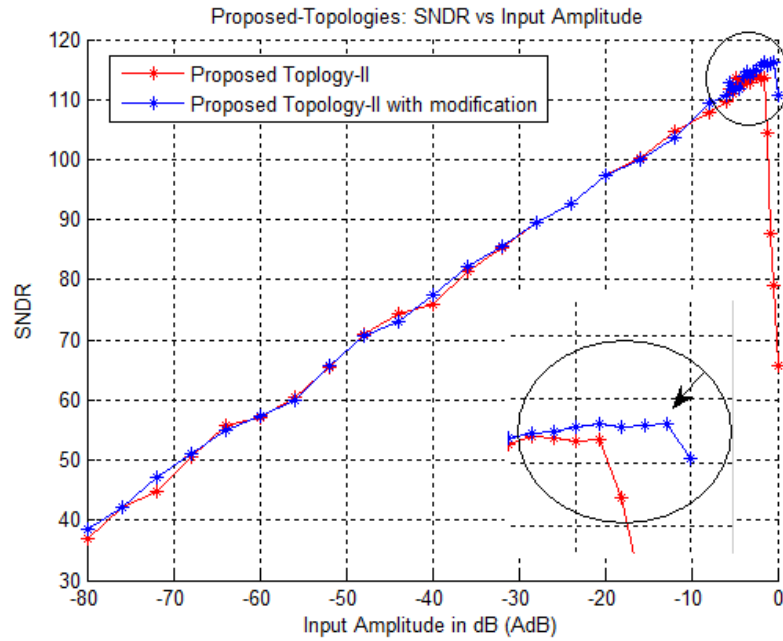


Figure 4.3: Improvement in SNDR for Higher Input Amplitudes

Chapter 5

Circuit Level Implementation

5. Circuit Level Implementation

After the topologies have been selected the next step is to have the switched capacitor implementations of the different components of the delta-sigma modulator.

The circuit level implementation starts with the design of following components

1. Selection and Design of the OTA.
2. Selection of the Capacitances (Sampling & Integration).
3. Design of Switch.
4. Design of multi-bit Quantizer.
5. Design of feedback DAC.
6. Complete System.

Another point worth mentioning from implementation point of view is that implementation is kept to a very simple level. All the four integrators are modelled with the same designed OTA of the first integrator for first hand approximation, and to keep the circuit level implementation simple.

Separate switches used for both sampling and feedback i.e. avoided switch sharing, and also separate capacitances, for the DAC and input are used.

5.1 Selection and Design of OTA

The basic requirements on the selection of topology were determined by the behavioural level simulation in Matlab and the specifications of the desired modulator. Next step is to use the circuit elements in the sigma delta modulator to meet the required specification at the expense of minimum power dissipation. In case of OTA, we need to use the one with gains as small as we can but enough to meet our specification and performance requirement. The next subsections discuss in detail about the topology of OTA used and design procedure.

5.1.1 Selection of Topology

For an Operational Amplifiers (Op-Amp) with low gain and lesser power consumption, one of the better choices is the single stage OTA's, without any gain boosting technique. The following two OTAs can be good choices for low voltage/power operation.

1. Folded Cascode Single Stage OTA
2. Telescopic Cascode OTA.

The selection among above two OTAs mostly depends on the performance requirements: It is difficult selection choice as both the topologies have gain in medium ranges and somewhat similar characteristics. The following table summarizes the characteristics of both the topologies.

Topology	Power Consumption	Output Swing	Noise
Telescopic	Low	Small	Low
Folded	Medium	Avg.	Medium

Table 5.1: Comparison between Folded and Telescopic Cascode Topologies [16]

The overall voltage output swing of the folded cascode is just a bit high as compared to the telescopic configuration as shown in table 5.1. This fact is also evident from the schematic of both the op-amps as shown in figure 5.1 because of less no. of transistors stacked in the output branch of Folded cascode (figure 5.1 (b)) as compared to Telescopic OTA (figure 5.1(a)). The tail current transistor in the telescopic cascode topology causes at least one more V_{ds} drop and hence reducing the voltage swing.

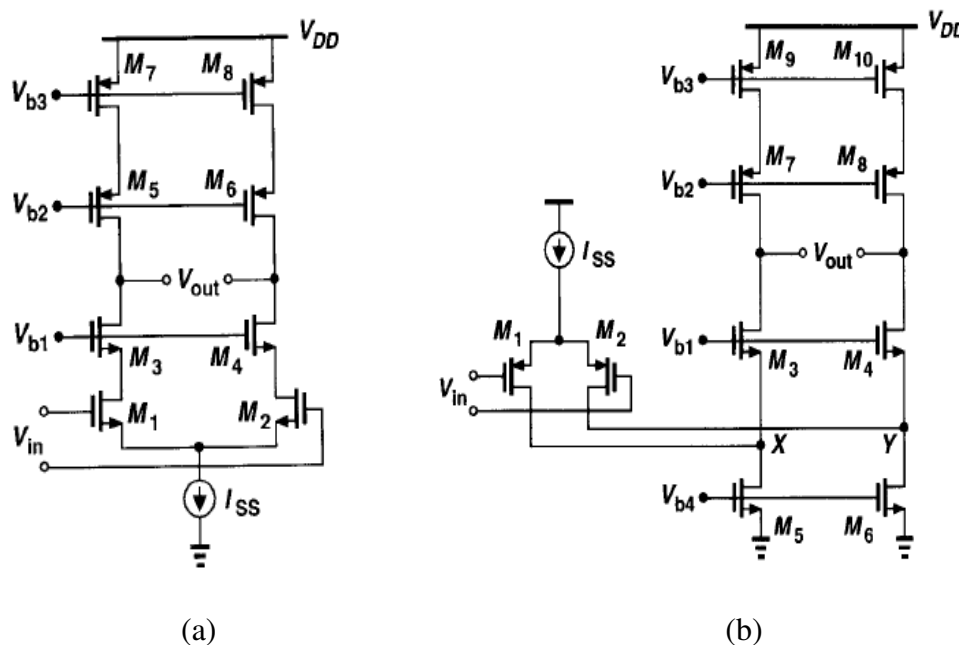


Figure 5.1: (a). Telescopic Cascode OTA, (b).Folded Cascode OTA [14]

However the improvement in the voltage swing comes at the added power consumption, and the high noise in folded cascode topology. Since we can short the input and output together, the choice of input common mode is much easier, and folded cascode are used more than telescopic cascode topology [16]

The Folded cascode was chosen based on low gain requirements with high voltage swing as it seems the optimal among two topologies.

5.1.2 Single Ended Output Vs Fully Differential Output:

After the topology selection is finalized, next is the implementation of the topology either as a single ended or fully differential OTA. In practice, the fully differential is used because of the following advantages over the single ended implementation [17, 18].

- Fully Differential Op-Amps provide a larger output voltage swing, as compared to the single ended output ones. The output voltage swing is almost twice in magnitude as to the single ended Op-Amps.
- Since the output voltages wing is large we get a higher Signal to Noise Ratio (SNR). We get four times increase in the signal output power because of twice the output voltage also the noise power is doubled, hence we get a overall 3 dB improvements in signal to noise ratio(SNR).
- Another advantage is the less susceptibility to common mode noise, which is mostly generated by the digital circuit, integrated on the same substrate.

There are some other advantages, along the above mentioned one but these all comes at the cost of extra power consumption because of the additional circuit required, to keep the output common mode level stable ; i.e. a Common Mode Feedback Circuit . It requires more current, and so the value of this current becomes important [16].

There are two types of CMFB circuits, continuous CMFB circuits and Switched Capacitor CMFB circuits. For switch capacitor delta sigma modulator, SC CMFBs are preferred, because they provide a larger output signal swing and are not limited by their common Mode sensing circuit, as it only consists of passive elements, capacitors and switches [1, 18].

So, the best choice for OTA was to be a fully differential folded cascode OTA with a SC CMFB. However for ease of simulation purposes the continuous CMFB circuit was used. The design procedure for Folded Cascode OTA and CMFB circuit is explained in section to follow.

5.1.3 Design Procedure for Folded Cascode OTA

The design procedure of the folded cascode was started with the setting of the goals of the Gain bandwidth; where GBW is usually selected greater than 5-7 times the sampling frequency; and speed/slew rate requirements.

From the Slew rate and predetermined load capacitance, the current in the differential current bias transistor marked as I_1 , I_2 and I_3 in figure 5.2 on next page was determined.

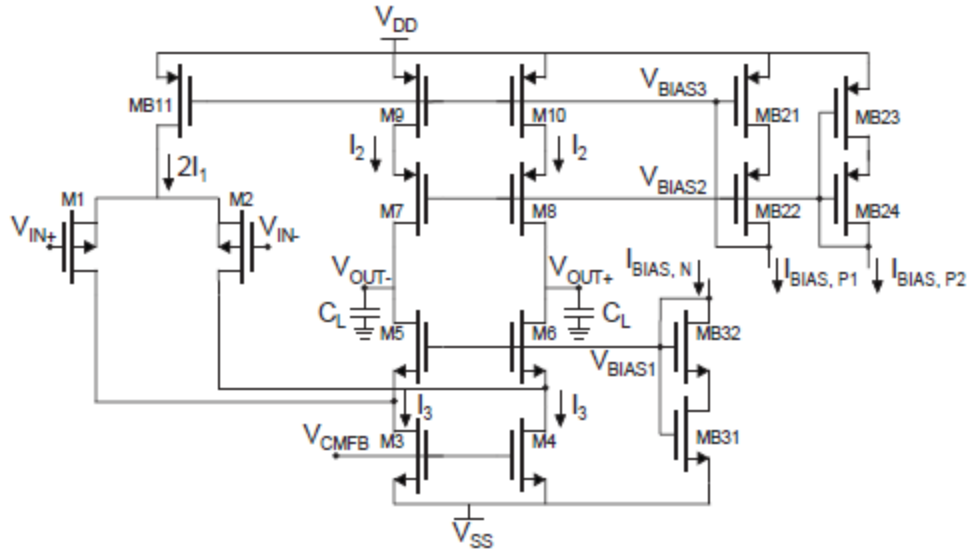


Figure 5.2: Folded Cascode Topology with the currents I_1 , I_2 and I_3 flowing in different branches [19]

current I_1 , in the input differential pairs (M_1 and M_2 in figure 5.2) is determined using the following relation

$$I_1 > SR * C_L \quad (5.1)$$

As a rule of thumb, the current in the load branch (I_2) shown in figure 5.2 should be

$$1.2I_1 < I_2 < 2I_1 \quad (5.2)$$

Then from the value of GBW, the trans-conductance, g_m , is calculated using the following relation;

$$GBW = g_m / 2 * \pi * C_L \quad (5.3)$$

And then using the relation of g_m and (W/L) ratio of the input differential transistor M_1 and M_2 in figure can be determined by the following relation

$$g_m = (2 * K * (W/L) * I_1)^{1/2} \quad (5.4)$$

Where;

$$K = \mu * C_{ox}$$

For other transistors, M_3 to M_{10} , in the output branch, a minimum V_{dssat} was assigned across each transistor, and then using the current flowing in the branch (I_2 and I_3), the (W/L) of the corresponding transistors was calculated using the following relation

$$I_{ds} = 1/2 * K * (W/L) * (V_{dssat})^2 \quad (5.5)$$

Once the sizes were found, transistors were fine tuned around these calculated values get the required results and achieved the required specifications.

5.1.4 Designed OTA

The OTA used in the delta sigma modulator is bit changed from the normal folded cascode. There are four transistors stacked up in the output branch, since in our case the gain of the OTA can be about 25 ~30dB, so from the cascode load one of the PMOS transistor pair was removed as shown by the figure 5.3. In figure 5.3 all the substrate connections of transistors are to the V_{dd} in case of PMOS and to V_{ss} in case of NMOS if not shown explicitly.

As one pair of PMOS was removed from output branch, the voltage swing is improved as there will be one less ‘ V_{dssat} ’ drop in between rails.

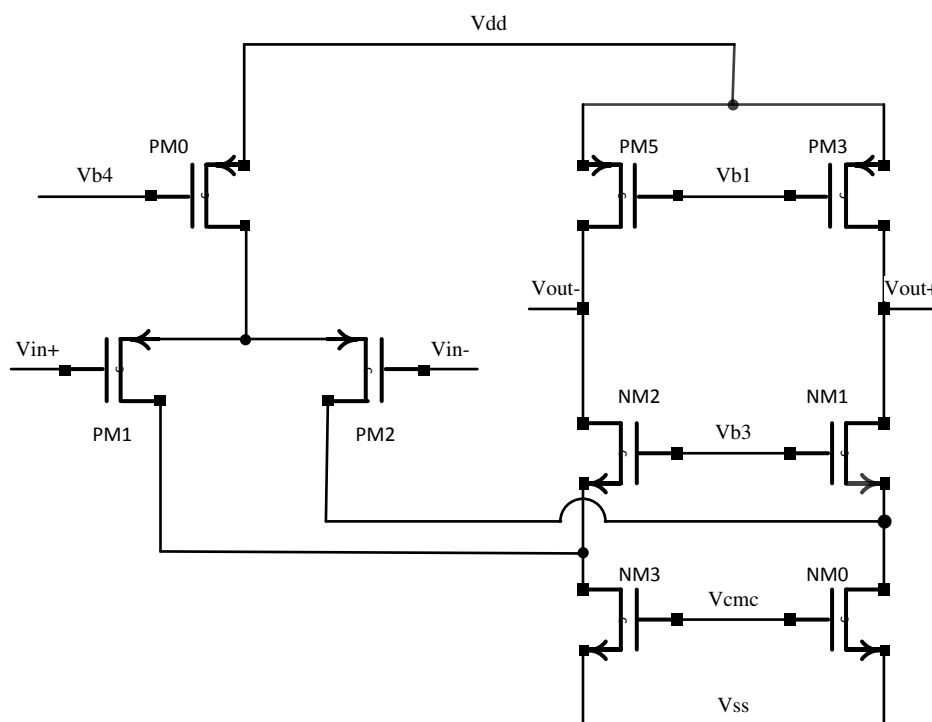


Figure 5.3: Folded cascode OTA with improved Voltage Swing

The input pair is a PMOS differential pair. Advantage of the PMOS input pair is, it helps to increase the slew rate. As the PMOS transistor has greater overdrive voltage and hence the slew rate which is proportional to overdrive voltage of the input transistors, however this depends on the value of trans-conductance. The other benefit is the less flicker noise due to PMOS input pair as the PMOS has a lower mobility.

The points Vb1, Vb3, and Vb4 show the biasing of the Op-Amp, and Vcmc, controls the common mode output of the Op-Amp. The current through the tail transistor at input side is equally divided in the input branches and then summed with the current from PMOS load. The functionality of this OTA is the same as that of a nominal folded cascode OTA. The CMFB circuit will be discussed in the section to follow, however the complete biased OTA is shown in figure 5.7 in section 5.1.6.

5.1.5 CMFB for the Designed Folded Cascode OTA

Along many advantages of the fully differential OTAs, one big disadvantage is that the common mode output if not controlled can either go to positive or negative rails, and causes some of transistor to not operate in saturation region. Hence a circuit is required to keep track, of the common mode and set it to the required level.

The CMFB circuit just measures the common mode voltage of the OTA, and then compares it with the desired common mode voltage, changes the control voltage to set the common voltage. This three step process can be described by the figure 5.4 based on [16].

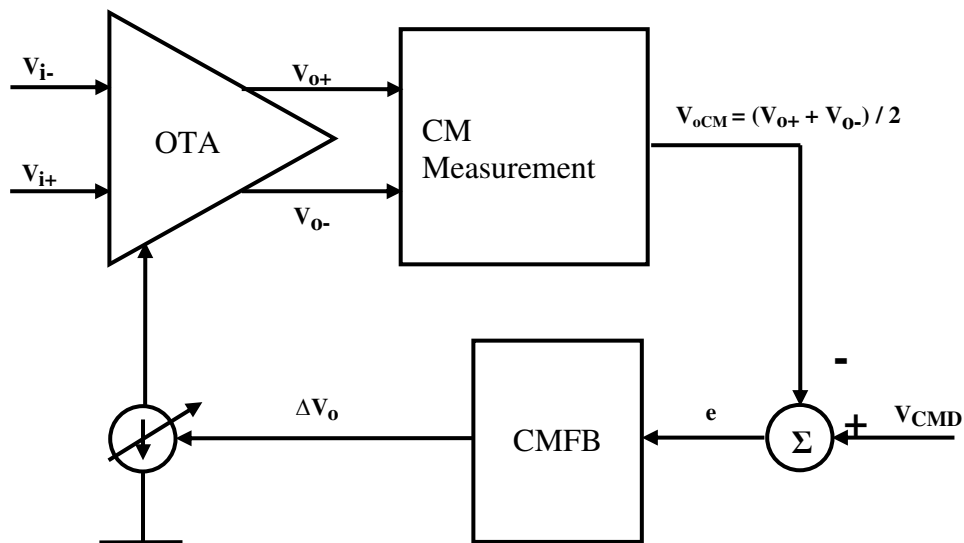


Figure 5.4: Basic concept behind the CMFB in a fully differential OTA.

The CMFB circuit used is shown in figure 5.5 and is based on a circuit presented in [18] and is called as Differential Difference Amplifier (DDA). The CMFB in figure 5.5 has two inputs

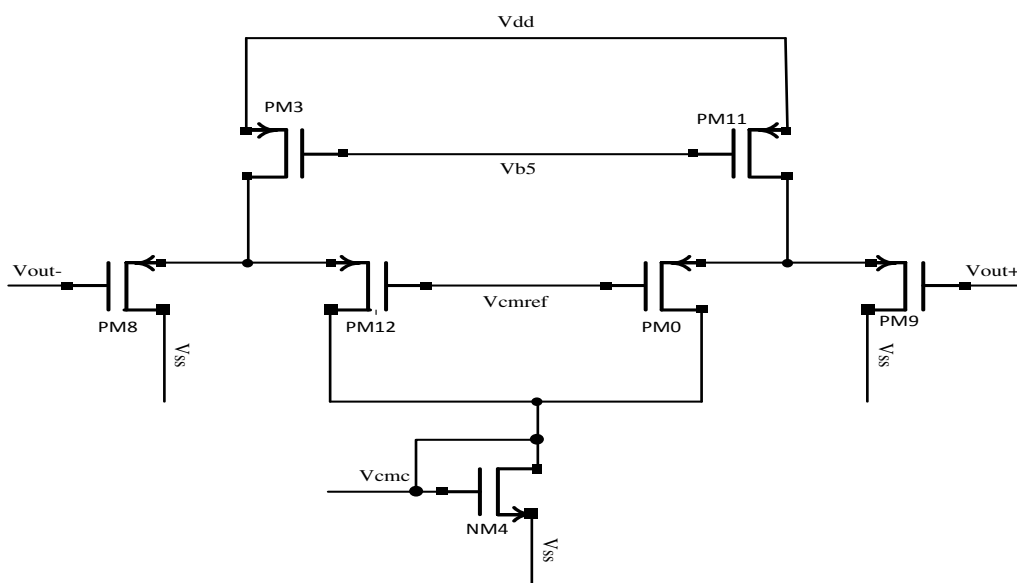


Figure 5.5: Common Mode Feedback Circuit.

differential pairs of PMOS transistors, a diode connected NMOS NM4 to carry tail current and then PMOS PM11 and PM13 is used to bias the whole circuit, where Vb5 is externally set by a biasing circuit. The PMOS transistors, PM8, 12 and PM 0, 9 are all matched transistors.

These source couple transistors sense the output common mode V_{OCM} and then produces an output that is proportional to the difference between the reference/desired common mode voltage, which is set externally to a desired value, and referred as V_{cmref} in the circuit in figure 5.5.

The analysis in [16] shows that the current through the tail transistor NM4, carries a current that is proportional to the voltage difference in between the desired common voltage (V_{cmref} in the circuit below) and the common mode voltage V_{OCM} . This current is then mirrored that controls then the current in the NMOS transistors in the OTA.

5.1.6 DC and AC Analysis of the Designed OTA:

The designed DDA CMFB was connected and tested to get the performance analysis of the operational amplifier in presence of the common feedback circuit. The test setup is shown in figure 5.6.

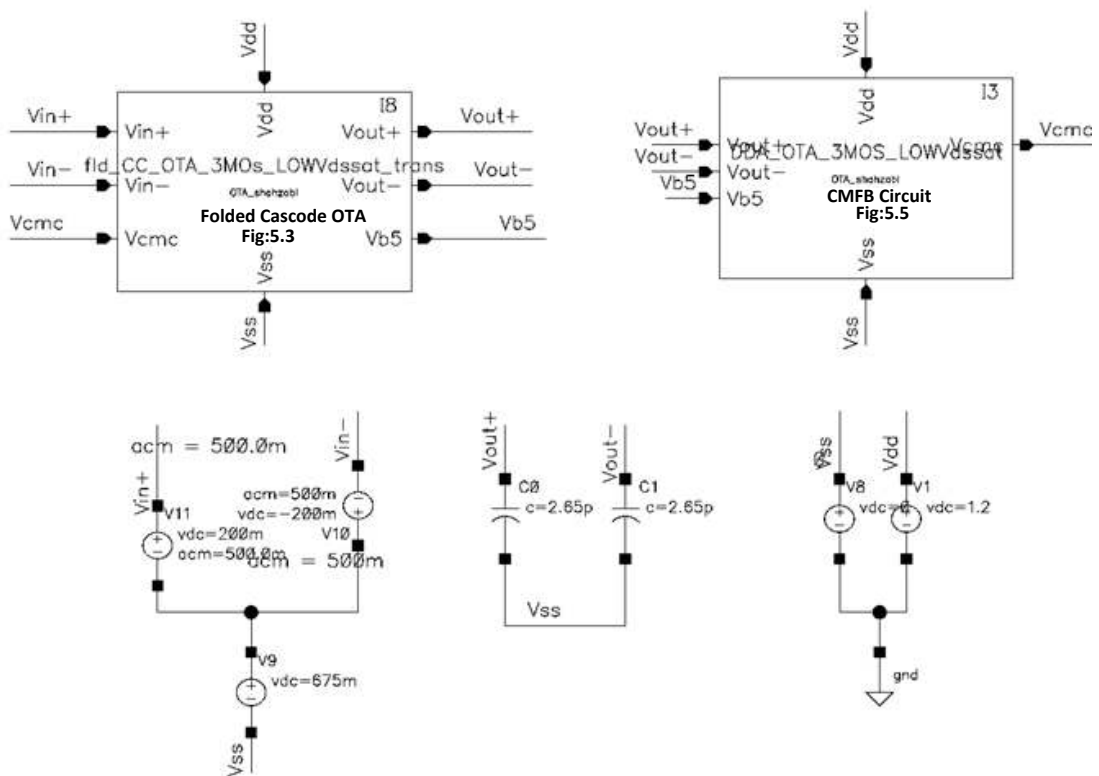


Figure 5.6: Test bench of the Folded Cascode OTA

The DC analysis was done and then the DC point was saved, the DC analysis is shown in figure 5.7. The DC voltages across nodes are marked on each transistor and we can see that a common mode output voltage of about 670mV is there at output.

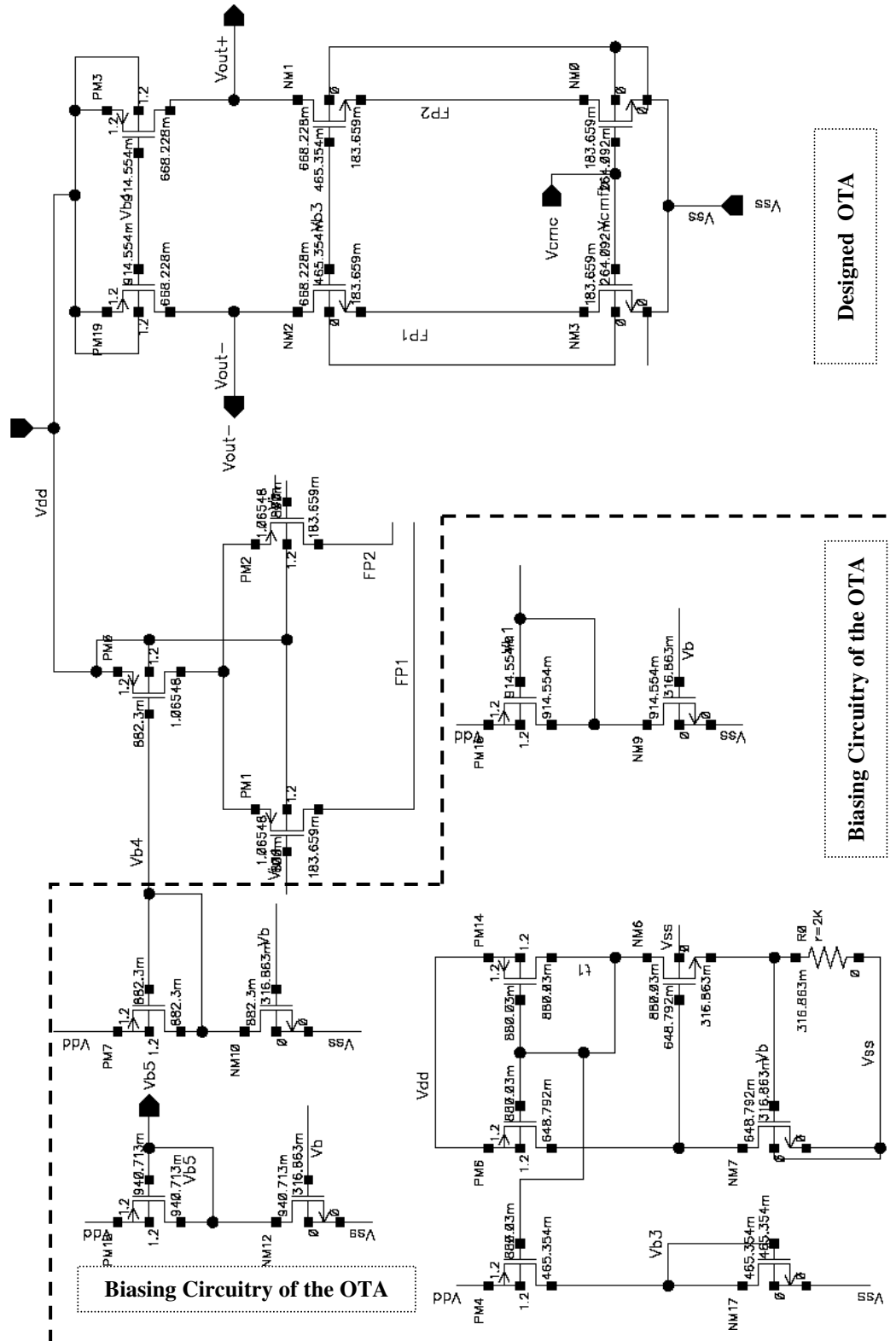


Figure 5.7: Illustrating Bias of the OTA (In the Dashed Block) and DC node Voltages at output of OTA

The AC analysis of the system is done and response is shown in figure 5.9 and a gain of about 30 dB is achieved, with a very good voltage swing of around 0.9 Volts with a supply of $V_{dd} = 1.2$ Volts and $V_{ss} = 0$ Volts.

The Gain bandwidth and Phase margin are calculated and are about 303 MHz and 86 degrees respectively. The figure shows the AC response of the, designed OTA.

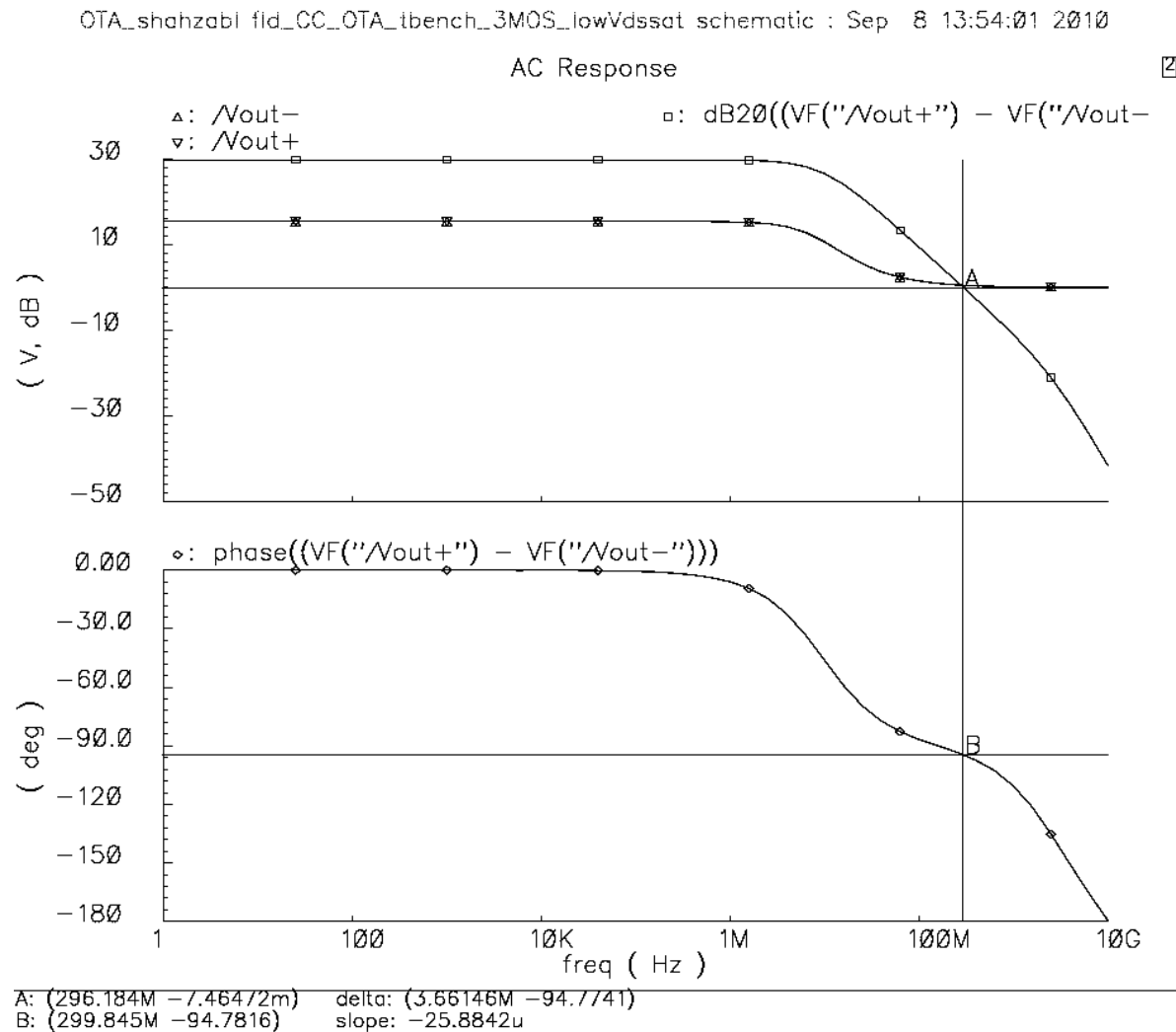


Figure 5.8: Gain and Phase Response of the OTA.

5.2 Selection of Capacitances

A big factor in the overall noise of the system is the noise contribution of the switch thermal noise and the thermal noise of Op-Amp. This makes the selection of the values of capacitances attached to these switches very important.

The switch noise is basically because of the on resistance, R_{on} , inherent in the switch. This R_{on} with the sampling capacitance makes a RC circuit and dominates the noise performance within the band of interest and careful selection of this capacitance can cause the performance of the overall system better. It is actually the thermal noise of the switch resistance R_{on}

which is sampled by the sampling capacitance hence the value of the sampling capacitance directly controls the amount of noise sampled. The relation of noise power P_{noise} to the sampling capacitance C_s is given in [15] rewritten in equation 5.6.

$$P_{\text{noise}} = S_n(t) = kT/C_s \quad (5.6)$$

Where;

- k = Boltzmann Constant
- T = Temperature
- C_s = Sampling Capacitance

So from equation 5.6, it can be seen noise power and sampling capacitance are inversely related i.e. larger the C_s the smaller noise will be coupled into the system. However there is a limitation on the value of the capacitance that can be used set by a mix of constraint like the area requirements, performance requirements and the settling time.

The value of the sampling capacitance is selected by modelling this switch noise into the model of proposed topology. It simply adds the noise to the input signal and can be analysed by the following equations [15].

$$y(t) = [x(t) + S_n(t)] * b \quad (5.7)$$

$$= [x(t) + (kT/C_s)^{-1/2}] * b \quad (5.8)$$

Where;

- b = C_s/C_f , the coefficient of integrator.
- C_f = the feedback capacitance.

The above equation can be modelled using the following block diagram [15] in the Simulink as shown in figure 5.9.

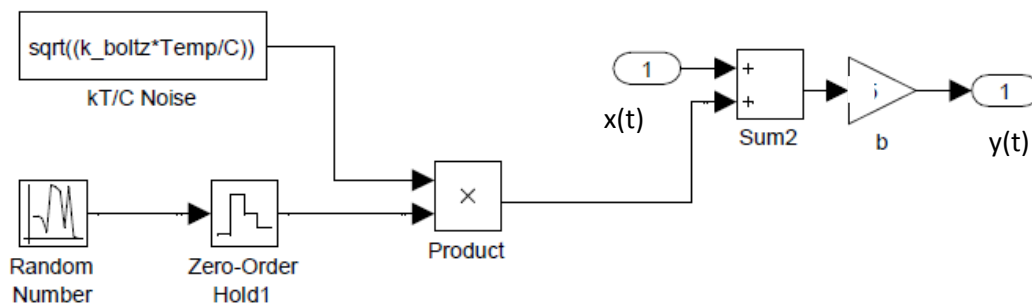


Figure 5.9: Modelling of Switch Thermal Noise

The following subsections explain the modelling of the noise of switch and op-amp models in the proposed topologies model with real integrators.

5.2.1 Modelling the noise model in Proposed Topology II

The switch thermal noise was modelled in Simulink as shown in figure 5.9, and then proposed topology II was remodelled as shown in figure 5.10 with non-idealities. The op-amp noise is just simply RMS input referred noise of operational amplifier. It is modelled simply by adding some random noise into the system.

These noises were integrated into the proposed topology as shown by the dashed red rectangles in the figure 5.10.

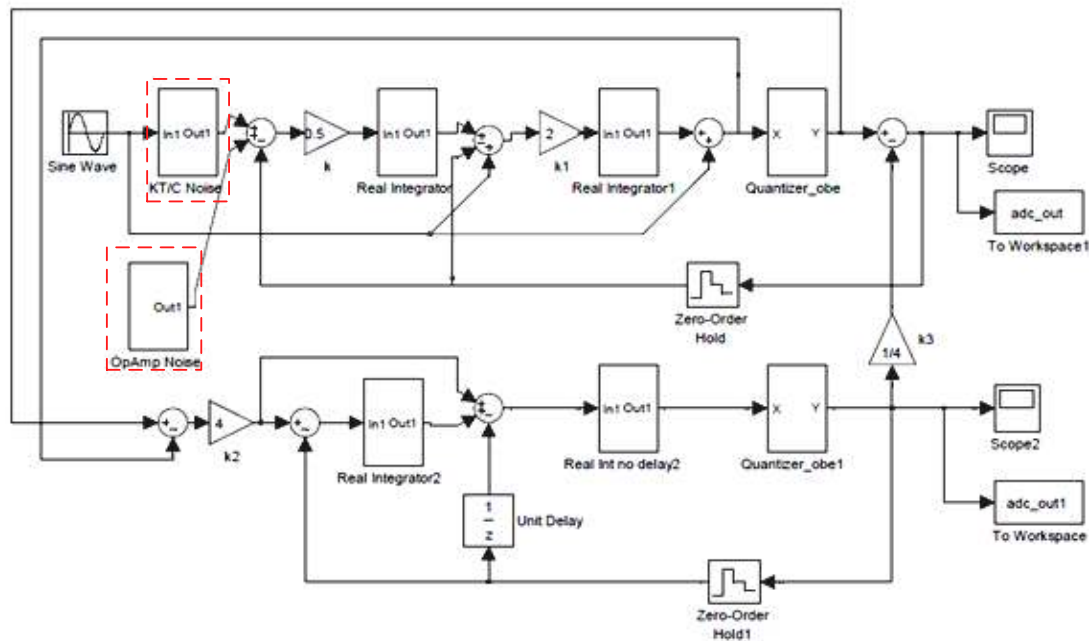


Figure 5.10: The kT/C Noise and Integrator noise in PTII.

The performance of the system was checked for the different values of the sampling capacitances and the results are shown below for Proposed Topology II in figure 5.11.

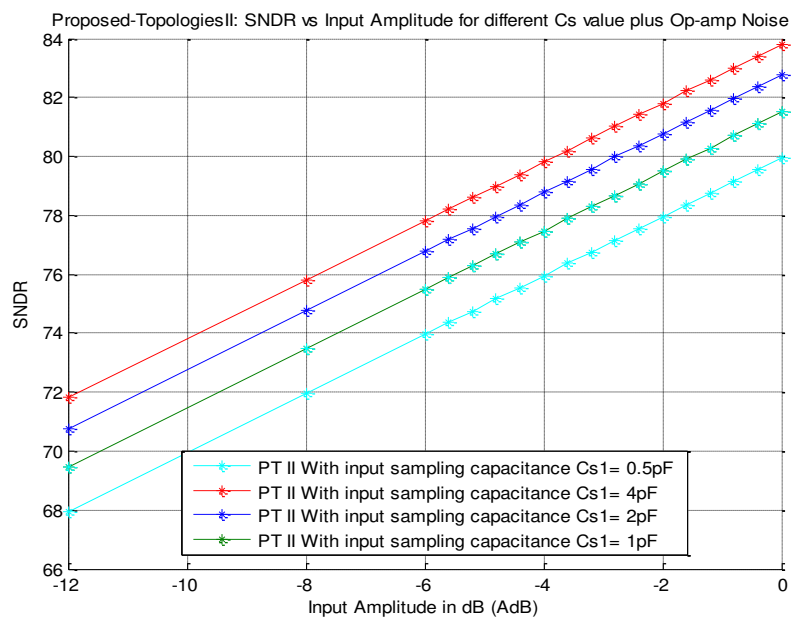


Figure 5.11: Effect of sampling capacitance and op-amp noises on the SNDR in PTII.

In figure 5.11 it is evident that, the values of the input capacitance, effects the signal to noise ratio, the larger the C_s value the larger is the signal to noise ratio. However an important design process is to choose an intermediate value of the capacitor that is feasible from the physical area used by the capacitor and the performance requirement. From figure 5.11 it can be seen that a value of around 2 pF for C_{s1} is an optimal choice in between power and area constraints as the larger the value of the sampling capacitance the more area is taken up.

The value of the capacitances and the DC gain of Op-Amps can be relaxed for following integrators in the same stage or next stage, because of the oversampling nature of the modulators. This is because contribution to the kT/C noise from the sampling capacitance of these integrator are attenuated within the signal band by the gain of the previous integrators and same is the case with the DC gains whose contribution to noise leakage go on decreasing [19]. Based on the above argument, the capacitors in the next integrators and or stage can be considerably relaxed however then the matching requirements in between the first and 2nd integrator is very important [19].

To see the overall system performance in presence of noise contribution from both integrators, a simulation was run modelling the kT/C noise contribution of the second integrator as shown by the figure 5.12 in which another kT/C block (marked by blue rectangle), before the second integrator, is added. By doing this we can see the combined effect of the capacitors of both integrator on the system and choose a value that is well within range of area limits and help to save area by choosing a smaller value of the sampling capacitances in the next stage.

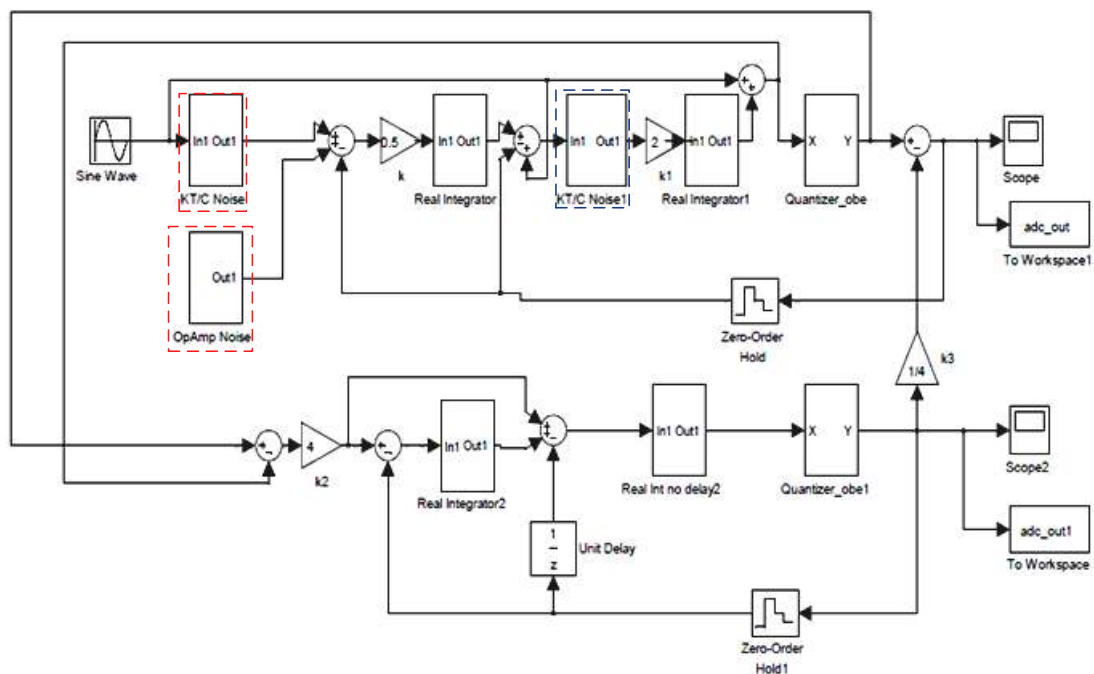


Figure 5.12: Modelling the kT/C Noise in 1st and 2nd integrator.

When the sampling capacitances of first and second integrators were modelled in Simulink, there is performance degradation in overall response of system as shown in figure 5.13 on next page. We can see that if we choose a value of 0.5pF for C_{s2} and 2pF for C_{s1} we get very

good performance and with this pair of values of capacitances there will be less area covered in implementation.

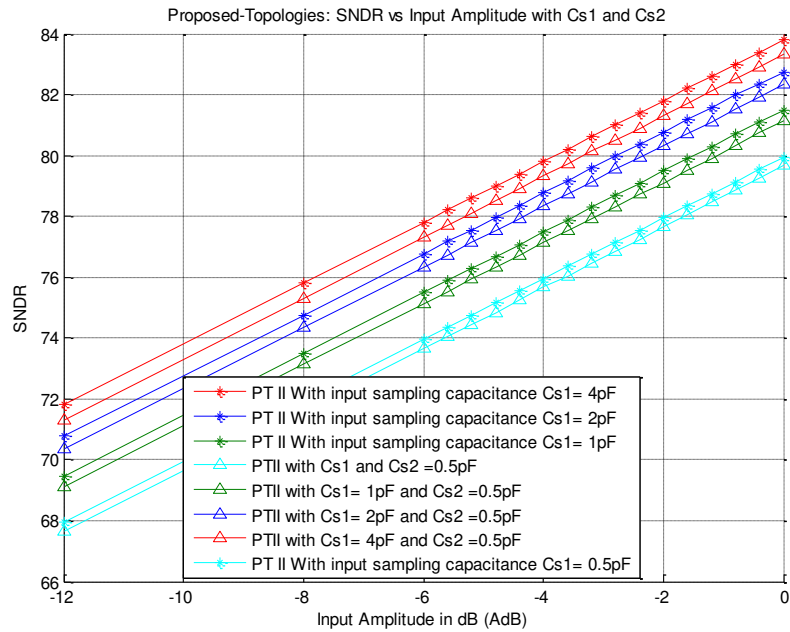


Figure 5.13: Effect of sampling capacitances Cs1 and Cs2 in PT II.

5.2.2 Modelling the noise model in Proposed Topology III

The Simulink model of the proposed topology III with non-idealities is shown in figure 5.14. The same simulation was run for this topology as proposed topology II, and the red dashed rectangles in figure shows the inclusion of the op-amp noise block, and the sampling capacitance effect for the first integrator.

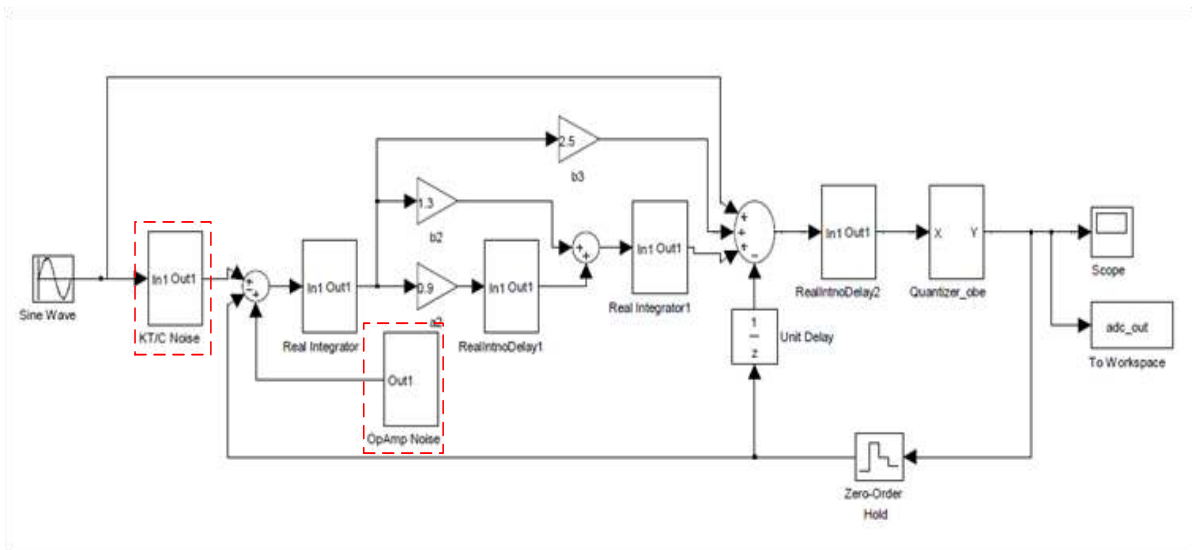


Figure 5.14: The kT/C Noise and Integrator Noise in PT III

The figure 5.15 on next page show the simulation of the propose topology III run for different values of capacitances in presence of Op-Amp noise in first integrator. From figure it can be clearly seen that the value of 2 pF is good compromise between the performance and area.

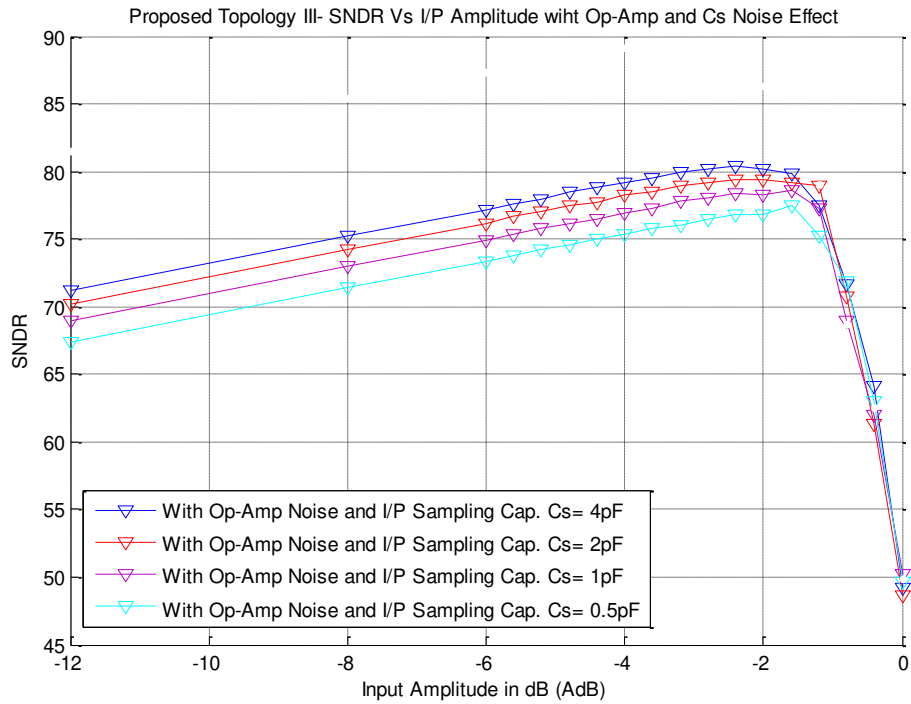


Figure 5.15: Effect of sampling capacitance and op-amp noises on the SNR in PT III.

To find the values of C_{s2} and to see the relation between the first and second integrator noise contribution and the matching between these values propose topology was remodelled as shown in figure 5.16. The kT/C noise block, inside the blue coloured rectangle, was added before 2nd integrator.

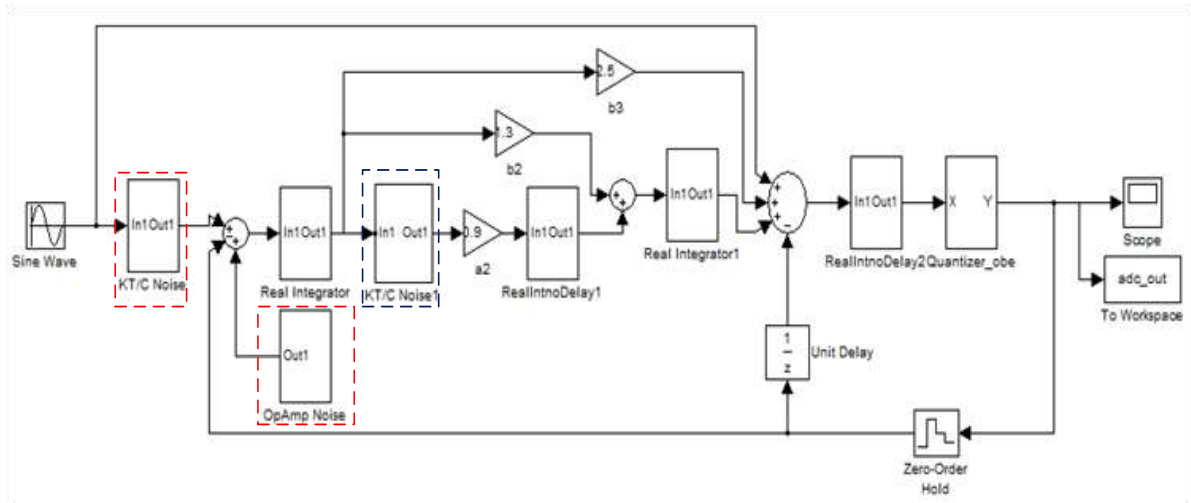


Figure 5.16: Modelling of the kT/C Noise in 1st and 2nd integrator.

After the running of the simulation, figure 5.17 on next page shows how the overall system response is affected. It is observed that as for the previous topology, the high capacitance values have the best performance at the expense of larger physical area, whereas the less values of capacitances gives low system performance but saves area. Thus C_s value pair of 2 pF for the first capacitor and the 0.5pF for the second capacitor is an optimal solution that is acceptable from system performance and as well as saves physical area in implementation.

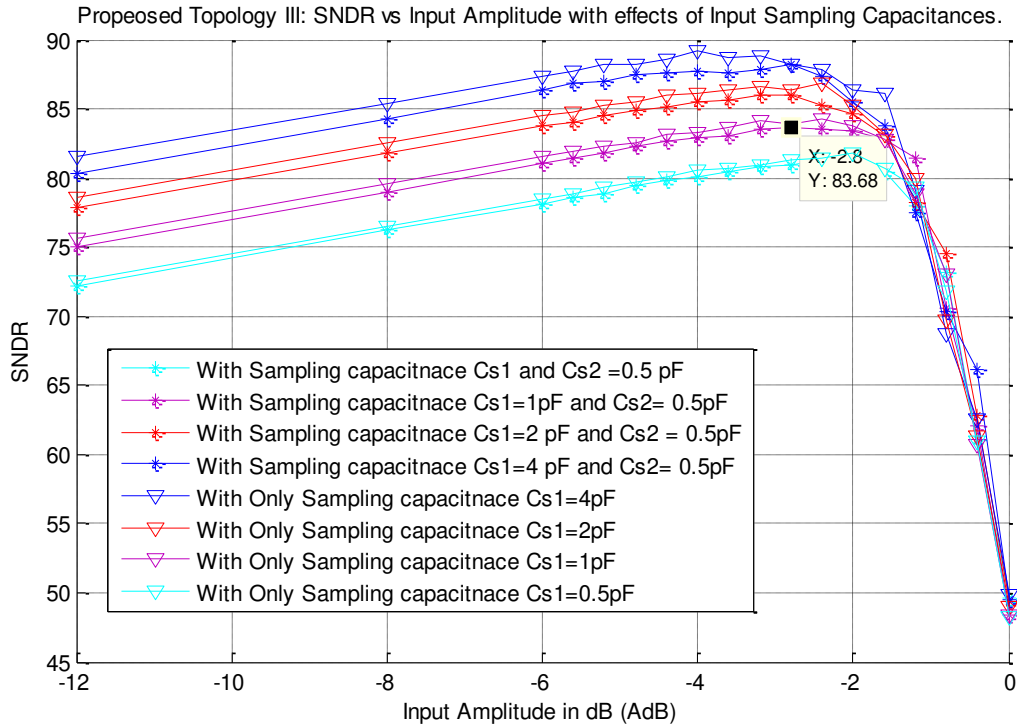


Figure 5.17: Illustrating the effect of sampling capacitances Cs1 and Cs2 in PT III.

5.3 Design of the Switch

After the differential OTA has been designed and the values of the sampling capacitances have been selected, the next step is the selection of the switches. The switch will turn these capacitances on and off in different clock timing cycles in the circuit and form the basis of the switch capacitor delta sigma modulator.

An ideal switch is just short circuit when ON and an open circuit when it is in OFF state. In simple words when the switch is in ON state there should be zero resistance and the value of the resistance in OFF state is infinity. However the real practical switch cannot have these ideal values there will be some resistance between the two points connected by the switch, called as on resistance R_{on} (value in very few ohms) in ON state and an off resistance R_{off} (values in several mega ohms) in OFF state.

The advantage of the MOS technology is the use of the simple MOS transistor as a switch; the following figure 5.18 [21] shows the use of a MOS transistor as switch.

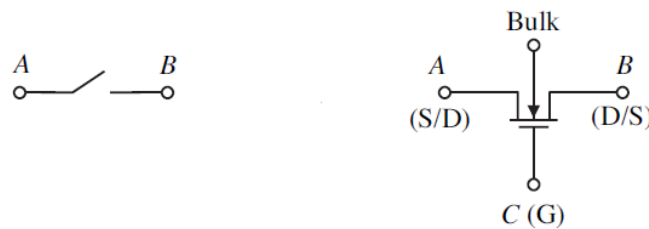


Figure 5.18: A MOS switch.

The voltage application at the gate (point C in figure 5.18) allows the flow of current through the transistor from point A to point B, where the bulk/body of the MOS connected according to the type of the transistor.

Assume a nMOS switch operating in active region, if there is a high voltage at the gate, and a small V_{DS} present across drain and source, then the current will flow from point A to B (figure 5.18) and there will be a resistance that is a series combination of the drain, source and the resistance of the channel between the drain and source this is of the most concern. An expression for the on resistance based on above description given in [21] is rewritten in equation 5.9.

$$R_{ON} = 1 / \mu C_{ox} WL^{-1} (V_{GS} - V_T) \quad (5.9)$$

The MOS transistor switches are the best for use as switches in the integrated circuits, from physical implementation point of view and gives sufficient value of the on and off resistances.

5.3.1 Channel Charge Injection

The use of a single MOS as a switch in the circuits is not a good choice because of the many non-ideal effects associated with it such as the clock feed through or channel charge injection. The channel charge injection or clock feed through is the flow of the unnecessary charge from the transistor to the circuit when transistor goes in OFF state [1].

This charge error occurs because of two main charge flows, one is the channel charge in between drain and source and other is the charge stored in the gate and overlap capacitances. These charges must leave to the drain and source when the transistor goes in off mode. The charge error because of the channel charge can be estimated as in [1] when the transistor has a zero V_{DS} .

$$Q_{CH} = WLC_{ox}(V_{GS} - V_T) \quad (5.10)$$

The figure 5.19 tells the flow of charge from the channel to drain and source terminals. When CLK goes low there is a small change ΔV at the output across C_L . At the C_L end there is a change at the output because of this charge transfer, so this node is a sensitive node, the charge also flows towards the voltage source however since it's a voltage source the charge transfer doesn't affect this node.

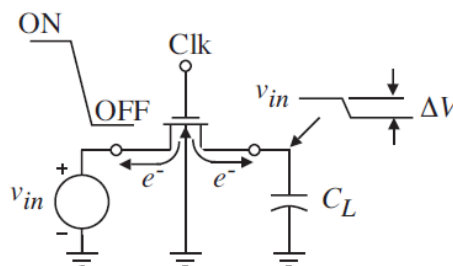


Figure 5.19: Channel charge flow in a MOS switch. [21]

The channel charge injection can be reduced if we use large values of the holding/sampling capacitances which is not good from the physical implementation point of view. The effect of channel charge injection can be cancelled by using a transistor with its source and drain shorted, called as a dummy transistor, to nullify the effect of the channel charge flow. A dummy switch cancelling the effect of channel charge injection is shown in figure 5.20 [21].

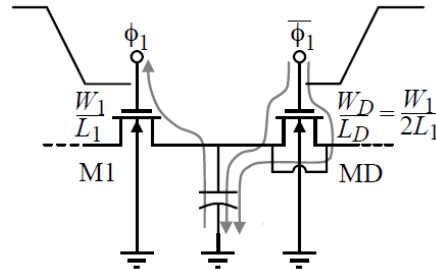


Figure 5.20: MOS switch with a dummy transistor to cancel channel charge flow.

The biggest disadvantage of this is the use of complementary clock. However this dummy transistor method does not completely cancel the charge feed injection. The dummy transistors can be on the sensitive nodes only or on both sides, as in previous circuit the only sensitive node was at the capacitor side, because the other side was a voltage source.

5.3.2 The Designed Switch

A single nMOS transistor passes a '0' i.e a low voltage near V_{ss} easily and a pMOS transistor passes a '1' high voltage near V_{dd} easily. We use CMOS technology to build a transmission switch or transmission gate in which nMOS and pMOS are connected in parallel. This has advantage of passing both the voltages strongly and also the dynamic analog signal range in the ON range is increased.

A transmission gate was designed and to cancel out the effect of charge injection dummy transmission gates were added on both sides of the transmission gates. The designed transmission gate is shown in the figure 5.21.

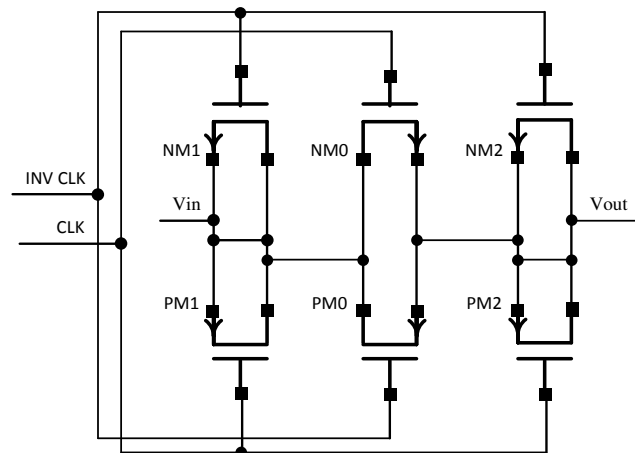


Figure 5.21: Transmission Gate with a dummy Transmission gate to cancel channel charge flow.

5.4 Design of Quantizer

The conversion of analog to digital is a two operation process. First analog signal is sampled at some specific instant of time periodically and then assigning these sampled values some particular finite value i.e. the process of quantization. The component doing the process of quantization is called the Quantizer [2].

The Quantizer shown in figure 5.22 is assumed to be memory less non-linear device, and it can be defined completely by its static input/output characteristics for example by a y-v curve.

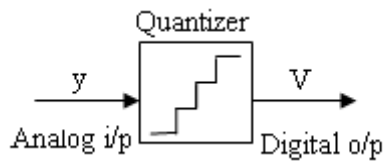


Figure 5.22: A block representation of the Quantizer.

Often it's desirable to approximated the input output transfer characteristics by a straight line curve

$$v = k y \quad (5.11)$$

Where, 'k' is the gain of the equivalent gain of the quantizer. The deviation of the actual characteristics from the approximate ones is the source of the quantization noise or error, which is of fundamental importance [2]. Quantizer in the delta sigma modulator can be a single bit and/or multibit depending upon the performance requirement. An M- bit quantizer has 2^M levels, to which the previously sampled values are mapped.

The procedure of the design of the quantizer starts with the selection of the no of bits for the quantizer. After the no of bits have been finalized, then the single bit quantizer is designed and this single bit designed quantizer is reused to design the full multi bit quantizer, by having each single bit quantizer for each of the total number of levels.

A single bit/ binary quantizer has only one threshold, so a single bit quantizer is just a comparator with some threshold. The design of the single bit quantizer thus is essentially the design of the comparator. The next section carries out the details of the design of the comparator.

5.4.1 Comparator

The comparator is the second most widely used building block after operational amplifiers. A voltage comparator is just a device that compares the input voltage with the reference voltage and produces the output voltage accordingly.

The comparators are very important part in the delta sigma modulator because of the comparison operation in the quantizer. The block diagram of a simple high speed comparator

is shown in figure 5.23[22].

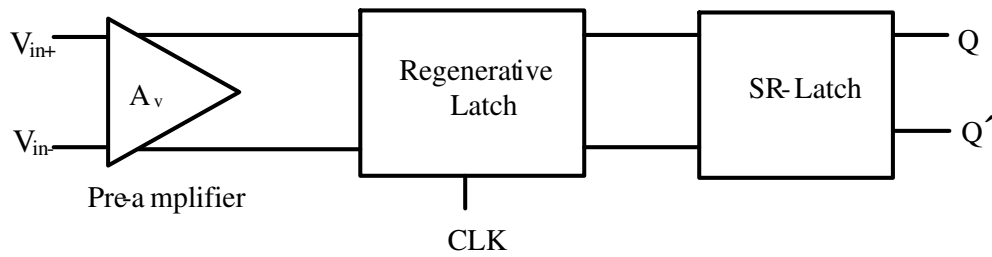


Figure 5.23: Block representation of the High Voltage Comparator

So the design of the comparator is basically the design of the regenerative latch, and preamplifier and then finally the SR-latch. The following section explains the design of the each block.

5.4.1.1 Regenerative Latch

A Regenerative Latch uses back to back cross coupled inverters that convert the input signal to a full scale signal value. It uses the mechanism of positive feedback, to accomplish the comparison of the signals.

A simple current sense latch amplifier presented in [22] was used as the regenerative latch and is shown in figure 5.24. This latch comparator is variation of the latch comparator presented in [23], with two additional MOS transistors M10 and M11 added in parallel that charges the node $Di+$ and $Di-$.

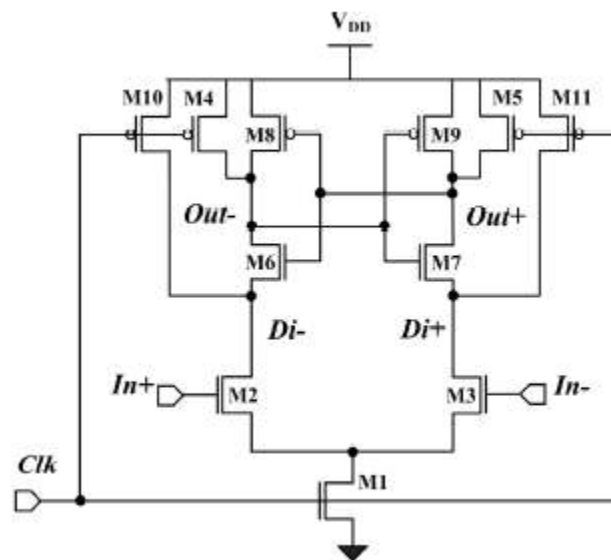


Figure 5.24: A Current Sense Latch amplifier. [22]

The latch in figure 5.24 is simply a differential amplifier which has coupled back to back inverters as loads. The operation of the above circuit is very simple when clock (CLK) is high, i.e. evaluation phase, there is a current flow through M2 and M3 to the tail transistor M1. The current flowing through the M2 and M3 controls the latch formed by the

inverters M7-9 and drives each of the output accordingly to difference in the currents in the branches to either high voltage or a low voltage using serially connected latch.

When the clock is low the M1 is off, and the input transistors are cut off from the lower supply and also, the M10 and M11 charges the Di nodes to Vdd. The transistors M4 and M5, causes the output nodes to pre-charge to Vdd.

The latch shown in figure 5.24 was drawn in 90 nm CMOS, the sizes of PMOS transistor were sized twice as the size of NMOS transistors; the schematic of the latch is shown in figure 5.25.

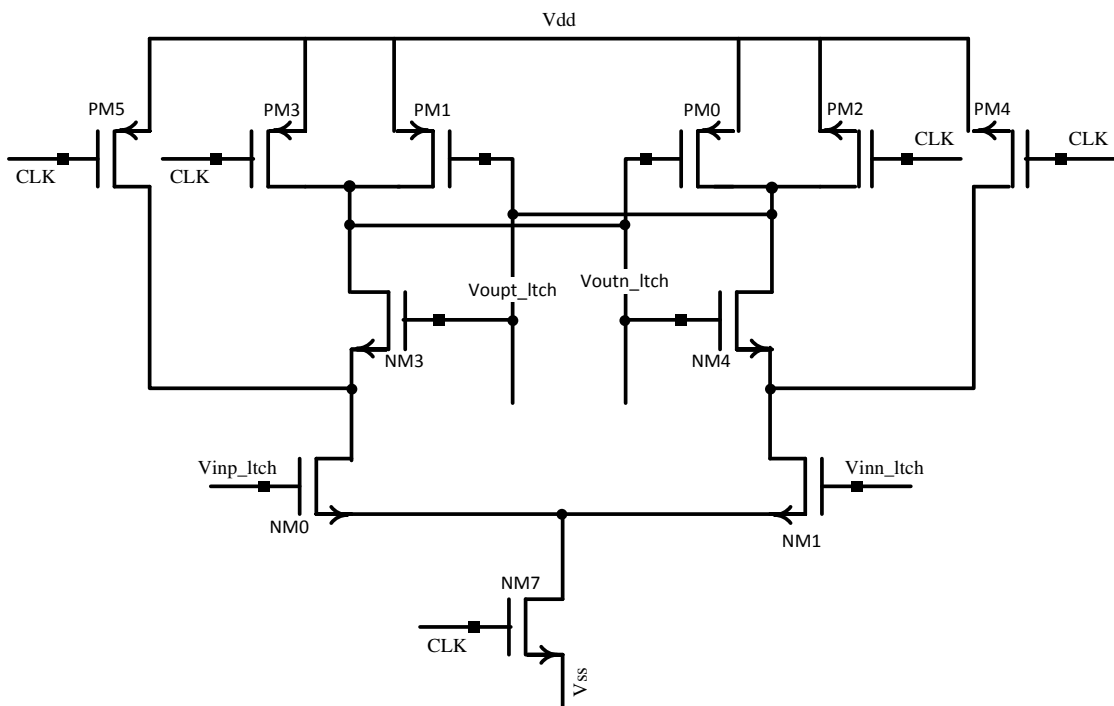


Figure 5.25: The Designed Current Sense Latch amplifier

5.4.1.2 Pre Amplifier

The pre amplification is done to minimize the charge transfer in or out of the input side of the latch, when it goes from evaluation mode to latch mode.

In the latch of figure 5.25 if the output current is to increase, the size of the tail transistor NM7 should increase and the current through the input transistor during the evaluation phase also increases. This high current causes these input transistors to operate in saturation region for a short time as the drain of the input transistors discharges from Vdd to ground and cause the lower amplification of the input voltage difference. So to avoid lower amplification we need some pre-amplification before the latch. A high input referred offset will also be there, because of a small V_{th} of NM3 and NM4, so the pre-amplifier is used to circumvent these drawbacks.

The Pre-Amplifier circuit designed is just cross coupled NMOS differential pair with a pair of

differential diode- connected MOS as load as shown in the figure 5.26.

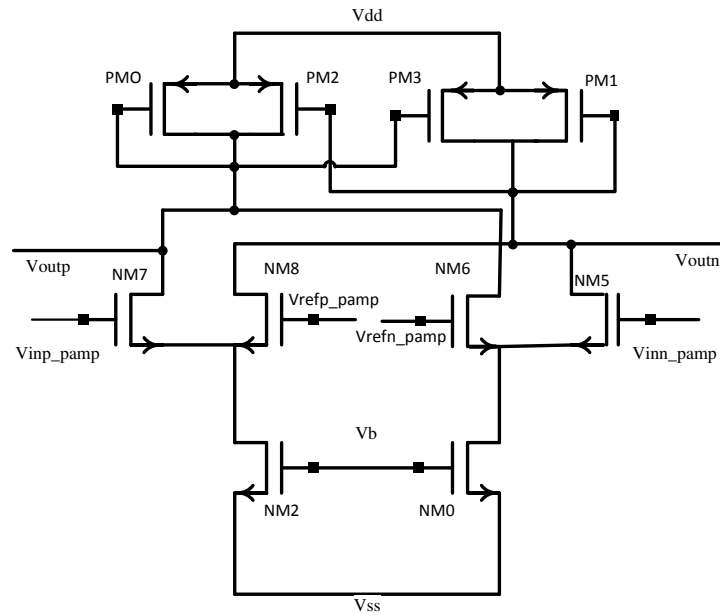


Figure 5.26: The Pre-Amplifier.

The differential diode connected load in the pre-amplifier of figure 5.26 is redrawn in figure 5.27[17]. This load is an ideal load for a differential amplifier. It can realize any resistance from $1/g_m$ to infinity. This can be understood simply as the simple pair of diode connected MOS has a positive resistance of $2/g_m$ whereas the cross coupled diode connected MOS has a negative resistance of $-2/g_m$ and creates a positive feedback.

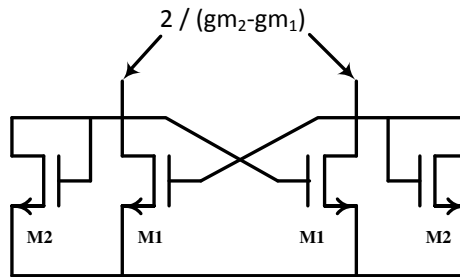


Figure 5.27: The differential diode connected load

When these two diode connected MOS transistor pairs are connected in parallel as shown in figure 5.27, assume M1 and M2 MOS transistors pair have trans-conductance g_{m1} and g_{m2} respectively, it causes the total resistance to be seen $2 / (g_{m2} - g_{m1})$, the parallel combination of the positive and negative resistance, and thus can realize a resistance of $1/g_m$ when $(g_m = g_{m2} = 2g_{m1})$ and infinity when $(g_m = g_{m2} = g_{m1})$.

The biasing of the preamplifier is similar to that of the OTA. The circuit in figure 5.26 just causes the flow of current from transistors NM6-9 corresponding to the difference between the input and reference voltage, and the circuit amplifies the voltages at drains of these transistors re -generatively.

The SR-Latch is simply built from the NAND gates, already provided and hence is not discussed here.

5.4.2 The 4-bit Quantizer

As mentioned before a M-bit Quantizer has 2^M levels, so for a 4-bit quantizer it will be 16 levels and there will be 15 1-bit quantizer, each with a different input reference voltage, to compare it with the input and set the corresponding bit of the quantizer. The hierarchical structure of a 4-bit Quantizer is shown in figure 5.28.

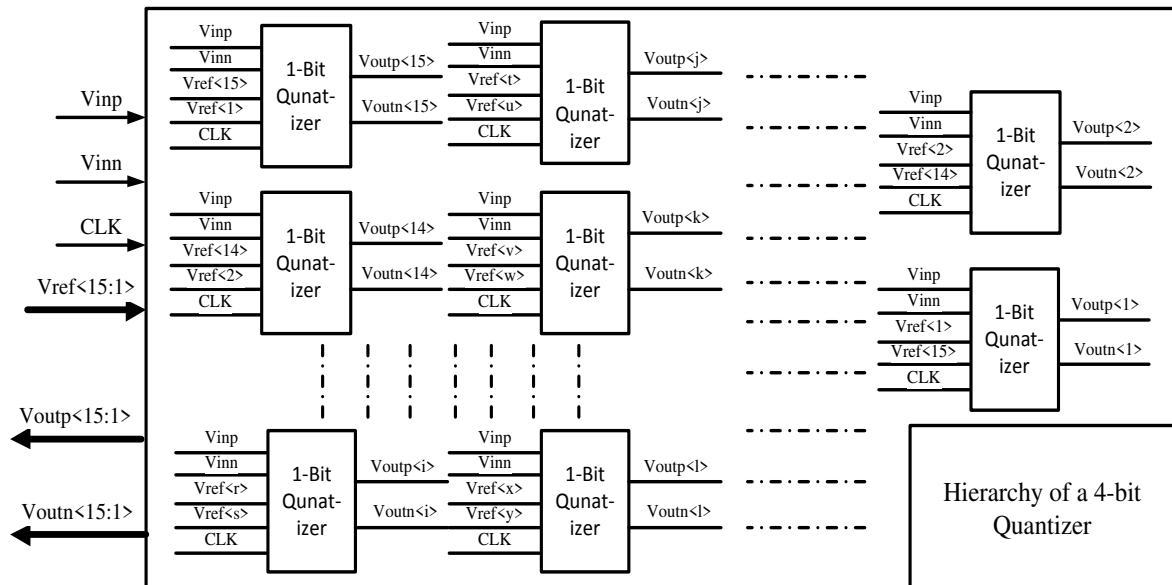


Figure 5.28: Hierarchical structure of 4-bit Quantizer.

From figure 5.28, it can be seen that every single bit quantizer needs reference voltage, hence we need a reference circuit that divides the whole full scale swing into levels corresponding to which the input will be compared.

The best and the easiest way is the use of a resistive ladder circuit as shown in figure 5.29. It is just the combination of RC segments, from which voltage references are tapped out.

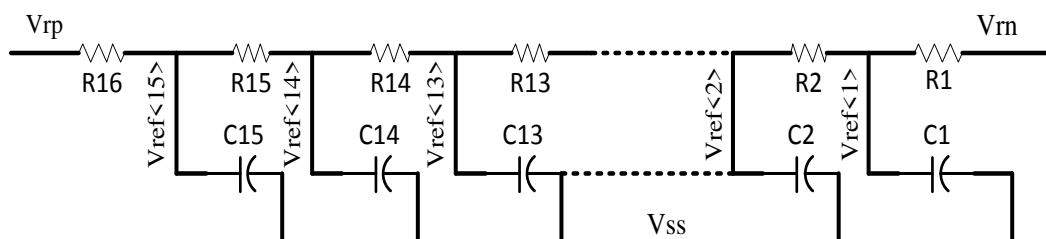


Figure 5.29: Reference Voltage Generation Circuit

In the figure it can be seen that to each resistor a capacitor has been added to smooth the response and remove the fluctuations of the voltage levels. Also the voltage range of 0.9 V (from 1.05(Vrp) to 0.3(Vrn) Volts) is divided into equal 15 levels by using fifteen such RC-sections.

5.5 Design of feedback DAC

The DAC is the component that completes the feedback as shown by the figure 1.1 in chapter 1. It just reconstructs the signal from the quantized version and then subtracts it from the input and thus completes the delta (difference) operation of a delta sigma modulator.

In our system we had actually a thermometer based output for a four bit quantizer, because we have used 2^N-1 bits to represent 2^N different levels of N-bit quantizer. In our case numerically speaking, we have a 15 bit output of a 4-bit data converter. So taking advantage of this, we can use thermometer based charge redistribution DAC shown in figure 5.30[1].

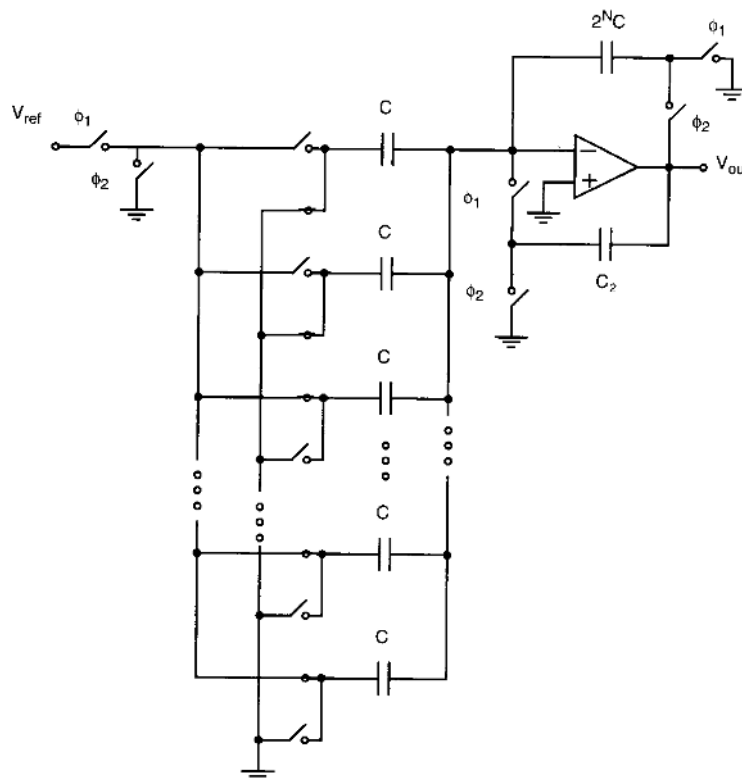


Figure 5.30: A charge redistributing Digital to Analog converter [1]

In the above figure the switches attached to each of the capacitors are controlled by the digital output of the quantizer, according to a proper timing circuitry and moreover the top of the capacitance is connected to ground and the bottom to reference voltage.

One of the advantages of this type of converter is that we don't have glitches, and also the analog area implementation of this type of converters is not more than the binary weighted data converters, and also since in each branch we can use the same size of a switch as it has the same size of capacitance [1].

5.6 Complete System

Once each individual component was designed and tested separately, each of them was connected to check the overall response, of the system. The figure 5.32 on next page shows the complete system diagrams

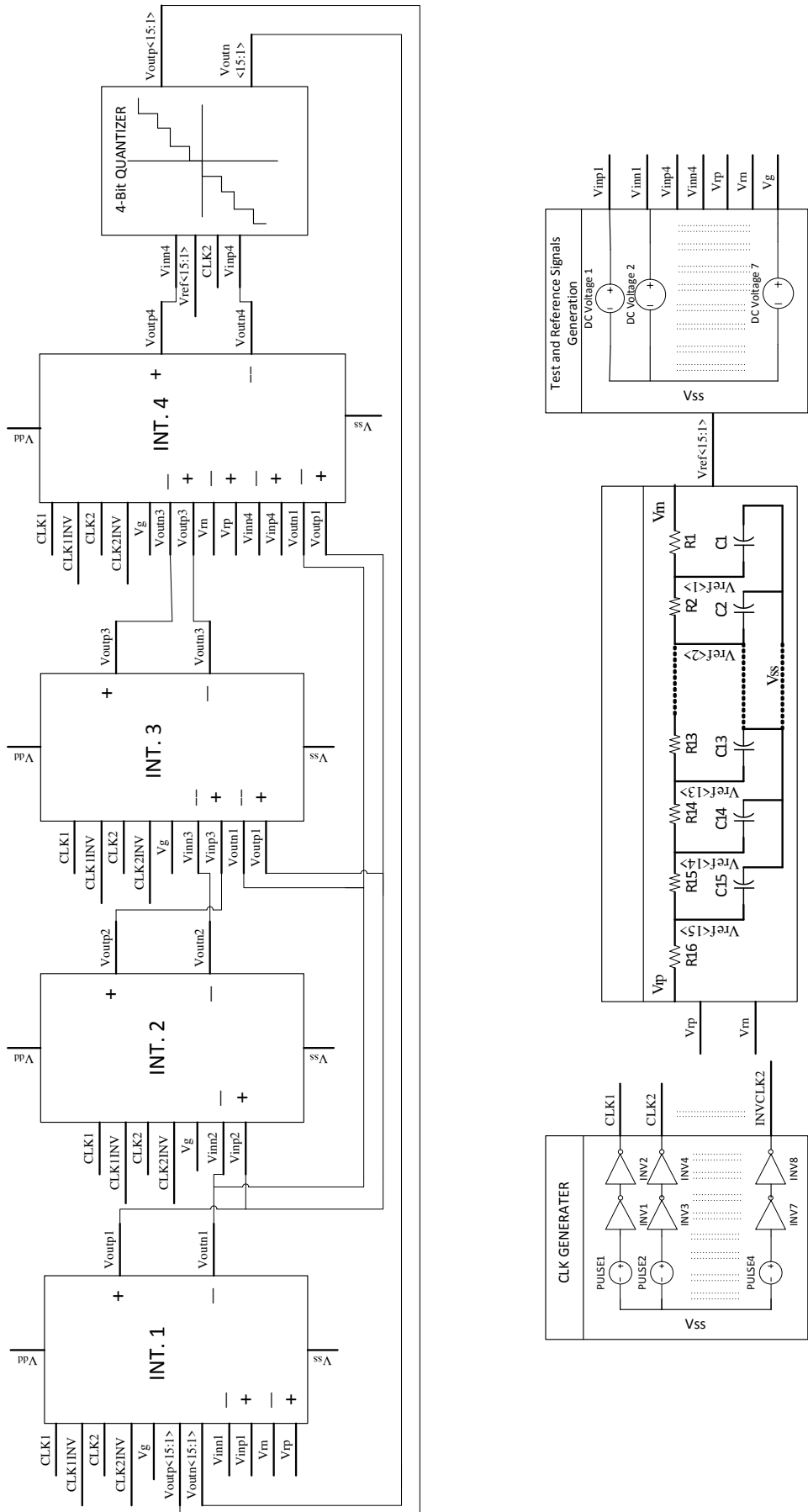


Figure 5.31: Hierarchy Overview of Proposed Topology III

The figure 5.31 on previous page show the complete system along with the clock generation circuitry and the four integrators (INT.1, INT.2, INT.3 and INT.4) connected together along with the supply voltages and the reference voltages levels generation circuit and 4-bit quantizer. Each of the integrator blocks along with the switch capacitor circuit is attached as Appendix B.

Chapter6

Behavioural Implementation in Verilog- A

6. Behavioural Implementation in Verilog- A

As simulation of a delta sigma modulator at transistor level is very time taking and difficult it is far more easier to check the system and debug it at behavioural level. The behavioural level implementation of the complete system is to be done by use of the hardware descriptive language, in this case Verilog-A, in Cadence environment.

Another advantage of the behavioural implementation is that it gives us with the reusable building blocks, that imitates the behaviour of the component at transistor level, but however this way of simulation of mixed signal circuits is closer to logic simulation, and is much more time saving and feasible solution [24].

For this a behavioural model of the following component was designed

1. Verilog -A model of Op-Amp.
2. Verilog -A model of Quantizer.

The following sections discuss in detail the behavioural models of above components.

6.1 Verilog-A model of Op-Amp

The behavioural model of the Op-amp was based on the small signal model of the differential amplifier. The characteristics of the op-amp were based on the relations given in [24].

The most important characteristics of the operational amplifier that affects the delta sigma modulator are the finite DC gain, slew rate, and the gain bandwidth. These were taken into account. The small signal model that was used for the basis of the behavioural model is shown in figure 6.1 on next page. It shows all the input and output pins of the implemented operational amplifier along with some internal nodes.

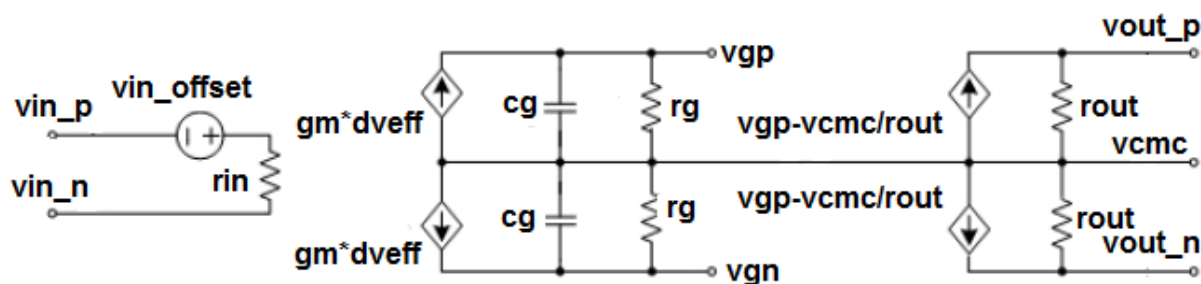


Figure 6.1: Complete small signal model of Op-Amp for Verilog-A implementation

The pins, parameters of the op-amp and the internal variables used in the code of the above op-amp model, of which some are self-explanatory, are shown in table 6.1.

Explanation of Pins, Parameters and Internal variables of the Verilog-A model of Op-Amp	
Pins	
vin_p	Positive input voltage
vin_n	Negative input voltage
vout_p	Positive output voltage
vout_n	Negative output voltage
vcmc	Common mode output voltage
vsupply_p	Positive input voltage
vssupply_n	Negative input voltage
Parameters	
gain	DC gain of the op-amp
gbw	Gain bandwidth of the op-amp
imax	Max. input current of the op-amp
Sr	Slew rate of the op-amp
vin_offset	Input offset voltage of the op-amp
Rin	Input Resistance of the op-amp
rout	Output Resistance of the op-amp
Internal Variables	
Cg	capacitance modelling dominant pole
Rg	resistance modelling dominant pole
dveff	effective input voltage
Gm	trans-conductance

Table 6.1: Explanation of Pins, Parameters and Internal variables of the Verilog-A model of Op-Amp

The complete code of the Verilog-A model of Op-amp is attached as an appendix and the performance of operational amplifier is i.e the DC and AC analysis is done in the next section.

6.1.1 DC and AC Analysis of the Verilog-A model of Op-Amp

The DC and AC analysis of the model was done. In the figure 6.2 the test bench for the op-amp is shown along with the DC response. The Op-Amp is loaded with the same load, and given the same test input voltage as for the transistor level operational amplifier

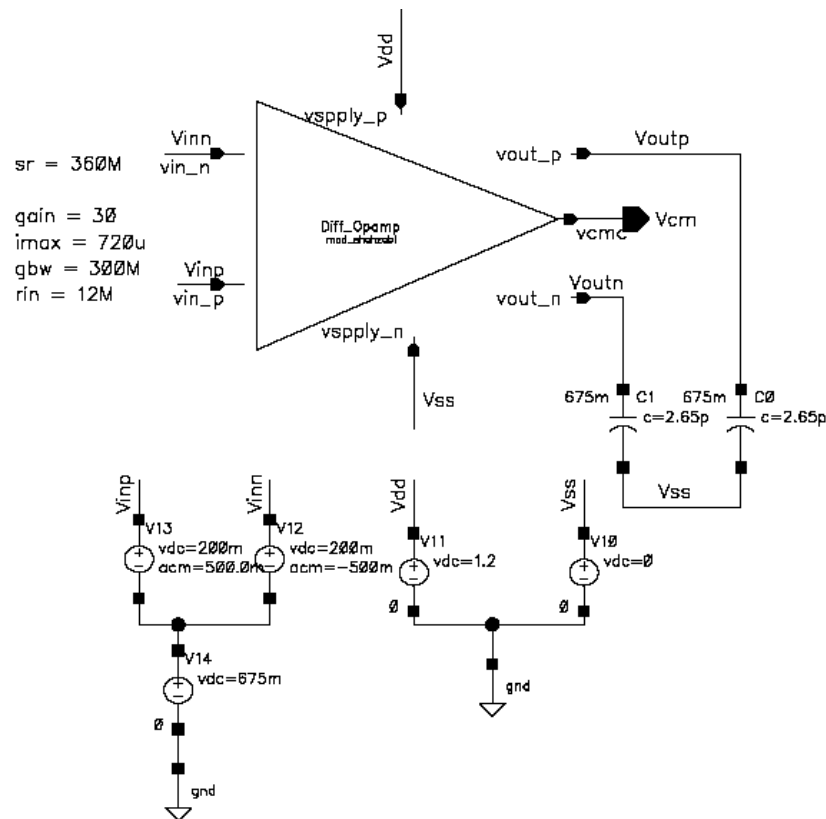


Figure 6.2: The DC-Response of the Verilog-A model of Op-Amp

The DC response in above figure clearly states the common mode voltage at the common mode output voltage node Vcm equals to 675 mV when there is a load of about 2.65pF. The other parameters such as slew rate, gain bandwidth and gain are also stated.

The operational amplifiers Verilog-A model was also simulated to find the gain and phase response, as shown by the figure 6.3 on next page The gain plot shows a DC gain of 30 db and the phase of about 90 degrees.

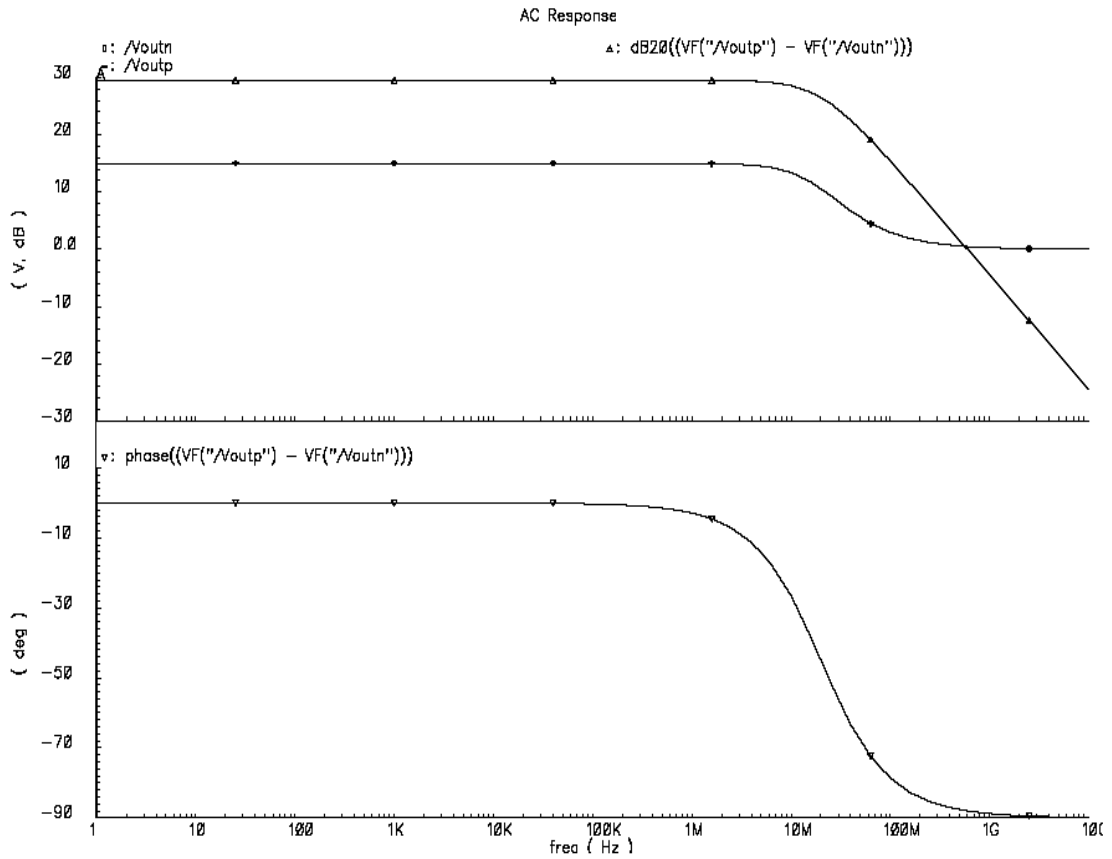


Figure 6.3: AC-Response of the Verilog-A model of Op-Amp

6.2 Verilog-A model of Quantizer

The quantizer was also modelled in Verilog-A. The Verilog-A model of Quantizer just implement the basic function of quantization. In a Verilog-A code, the full-scale voltage range is given as a parameter, and then divided into different voltages level according to the number of bits of quantizer i.e. the full scale range was divided into 16 levels for a 4-bit quantizer. Then the input voltage is compared with the levels, and the output bits are set equal to that voltage level in which the input falls. The figure 6.4 shows the symbol of the quantizer

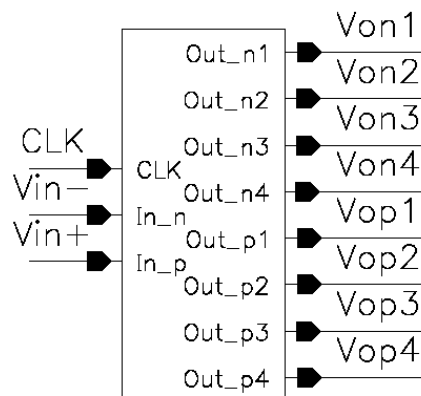


Figure 6.4: Verilog-A model of Quantizer

The quantizer was simulated in Cadence Spectre, with the input voltage spanning over the complete full scale and then the output was checked. The variation of the output bits is clearly shown in the response of the quantizer in figure 6.5.

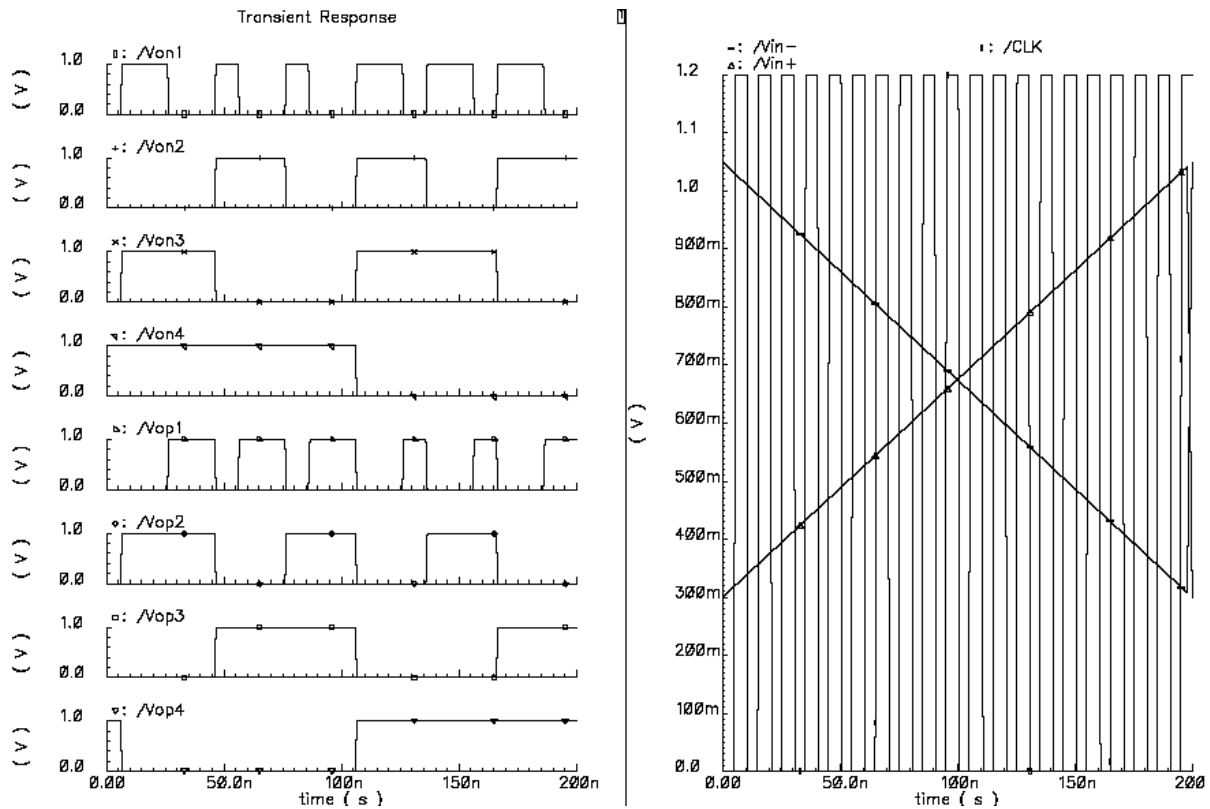


Figure 6.5: Response of the Verilog-A model of Quantizer

The complete code of the quantizer is attached as an appendix. Also the switch was designed in Verilog-A which is just simple behavioural implementation of a resistance R_{on} or R_{off} depending upon the control voltage. The complete code of switch is also a part of appendix.

Chapter 7

Conclusion and Future Work

7. Conclusion and Future Work

In this work the investigations of the use of low gain operational amplifier, in high order delta sigma modulator was made. The new topologies were designed to achieve the high SNR. For this, two structures were chosen one with multistage noise shaping architecture and the other single loop higher order delta sigma modulator.

One of the key aspects of the work was using the idea of quantization noise coupling of the system because of this both the structure saves one extra operational amplifier, which would be necessary if implemented otherwise.

The behavioural implementation in Matlab/Simulink, suggest a very high SNR, and high dynamic range.

At circuit level, the folded cascode topology was used to build the OTA, however it was different from the conventional one because of less transistor in the output branch that helps improve increase of the voltage swing.

The each component at the transistor level was tested individually and the simulations were also run for Verilog-A model. However the complete system performance wasn't checked because of the time limitations.

Further work can be done to complete the behavioural model in Verilog-A for the complete system and then running the simulations over the complete delta sigma modulator and checking the performance of the system. Then after each Verilog-A model being replaced by its transistor level counterpart and checking the system performance. The future work will be layout, tape out and then the testing of the chip.

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Appendix

Appendix A: Matlab Code for the test bench of ADC

Test Bench Code:

```
%% Set global variables

Nbits =4;                %Number of bits of the quantizer
OSR = 20;                %Oversampling ratio
ftest = 2500e3/3;        %test tone frequency in Hz
fbw = 2500e3;            %ADC bandwidth in Hz
fs= OSR*2*fbw;
Ts= 1;
k = 13;                  %Suggested number of bits of the fft

% signal conditioning
[fTone fB Nfft] = stestcondition(ftest,OSR,fbw,0,k,3);

Afs=0.45;                %Full scale value of the input tone
AdB =-8;                  %Tone amplitude in dBFS
A = 10.^(AdB/20) *Afs;    % Test tone amplitude in volt

% Parameters modelling the non-idealities
k_boltz=1.38*10^-23;
Temp=298;
C= 2*10^-12;
rms_noise= 73*10^-6;

A1= 23;
A2= 21;
A3= 20;
A4= 19;
alfa= 0.999;
alfa1= 1-1/(10.^(A1/20));
alfa2= 1-1/(10.^(A2/20));
alfa3= 1-1/(10.^(A3/20));
alfa4=1-1/(10.^(A4/20));
sr= 0.1*10^6;
GBW=100000;

% Launch Simulink simulation

sim('proposed_topology_I');

% Compute power spectral density (PSD)

% apply hann window to data
```

```

[w,w0,signalBinsQty,NBW] = window(transpose(adc_out),'hann');
psd_simulink = sd_psd(w,A,w0);

%Plot PSD

figure(3);
clf;
f = linspace(0,0.5,Nfft/2+1);    % x axis normalized w.r.t. Fs (Fs norm. w.r.t Nfft)

semilogx(f, dbv(psd_simulink(1:Nfft/2+1)), 'b')
xlabel('Normalized Frequency');
ylabel('dBFS/NBW');
title('Proposed-Topology-I');
grid on
getslopeintercept

% Calculate SNDR

% Index of fTone to account for matlab indexing conventions (index 0 not allowed)

fToneIdx = fTone + 1;

% Index of fB to account for matlab indexing conventions (index 0 not allowed)
fBidx = fB + 1;

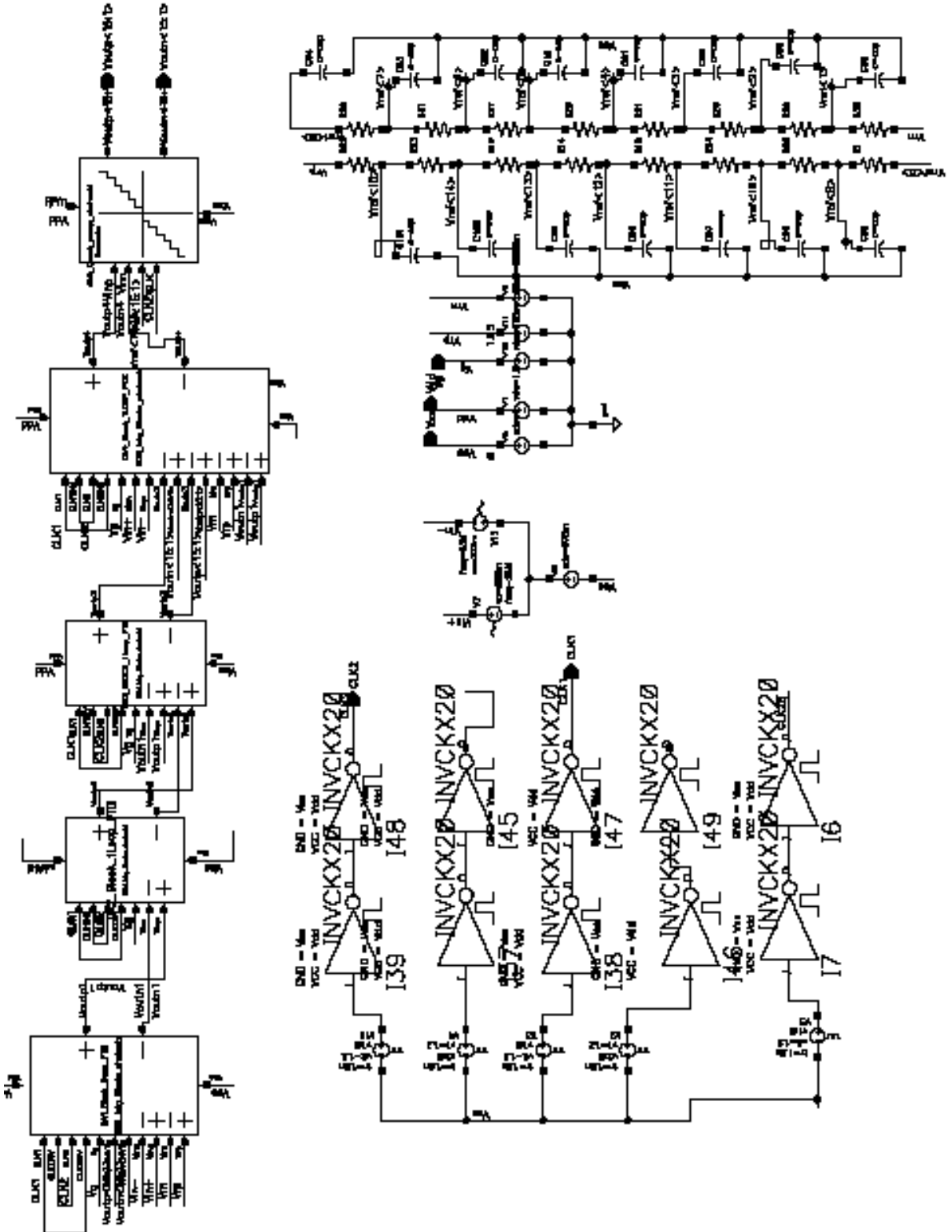
% Exclude DC and adjacent bin for SNDR in the calculation
inBandBins = psd_simulink(3:fBidx);

snr = sd_snr(inBandBins,fToneIdx-2,signalBinsQty);
text(0.01,-10, sprintf('SNDR = %4.1fdB @ OSR = %d',snr,OSR),'vert','middle');

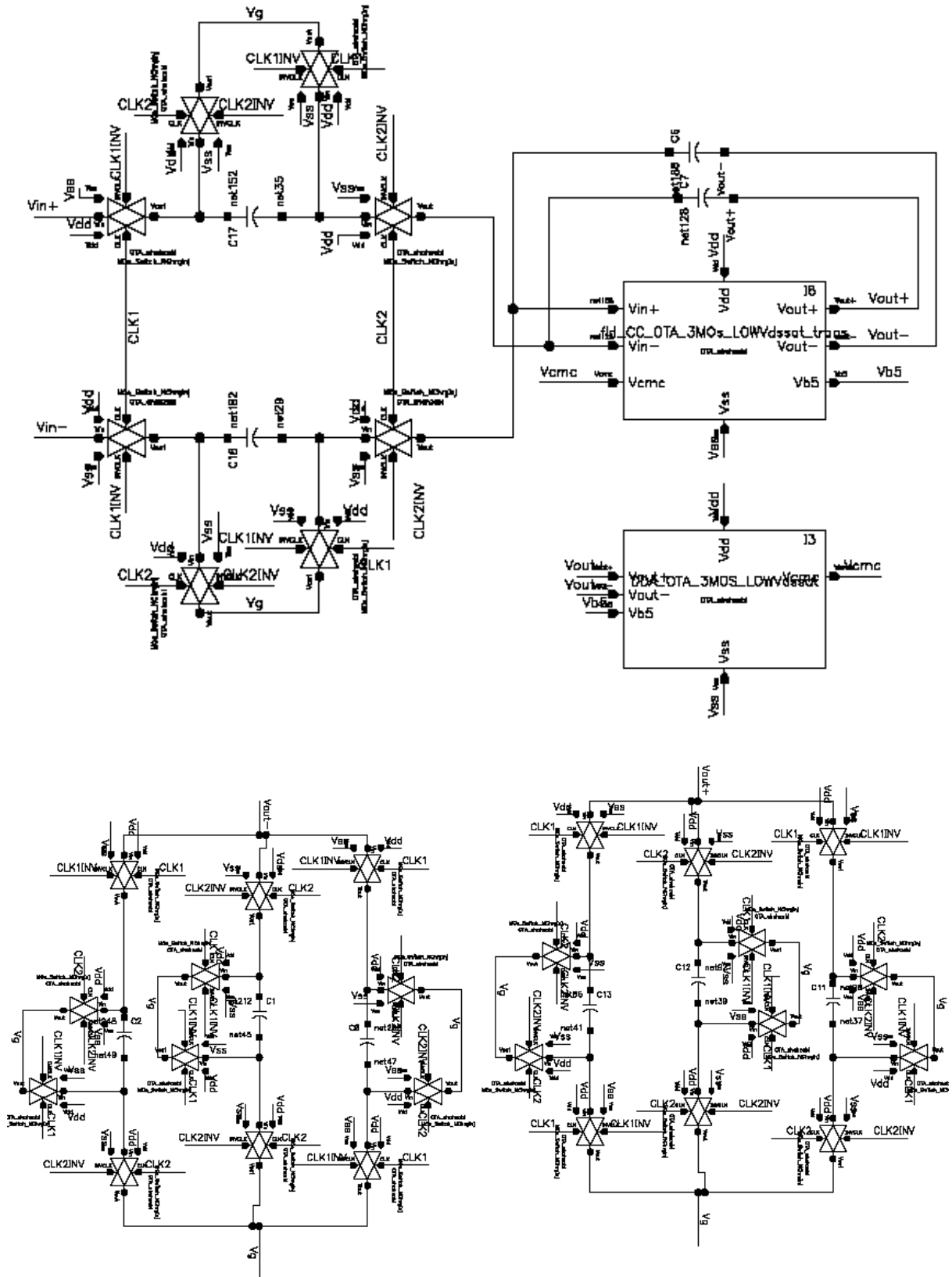
```

Appendix B: Full System Diagrams

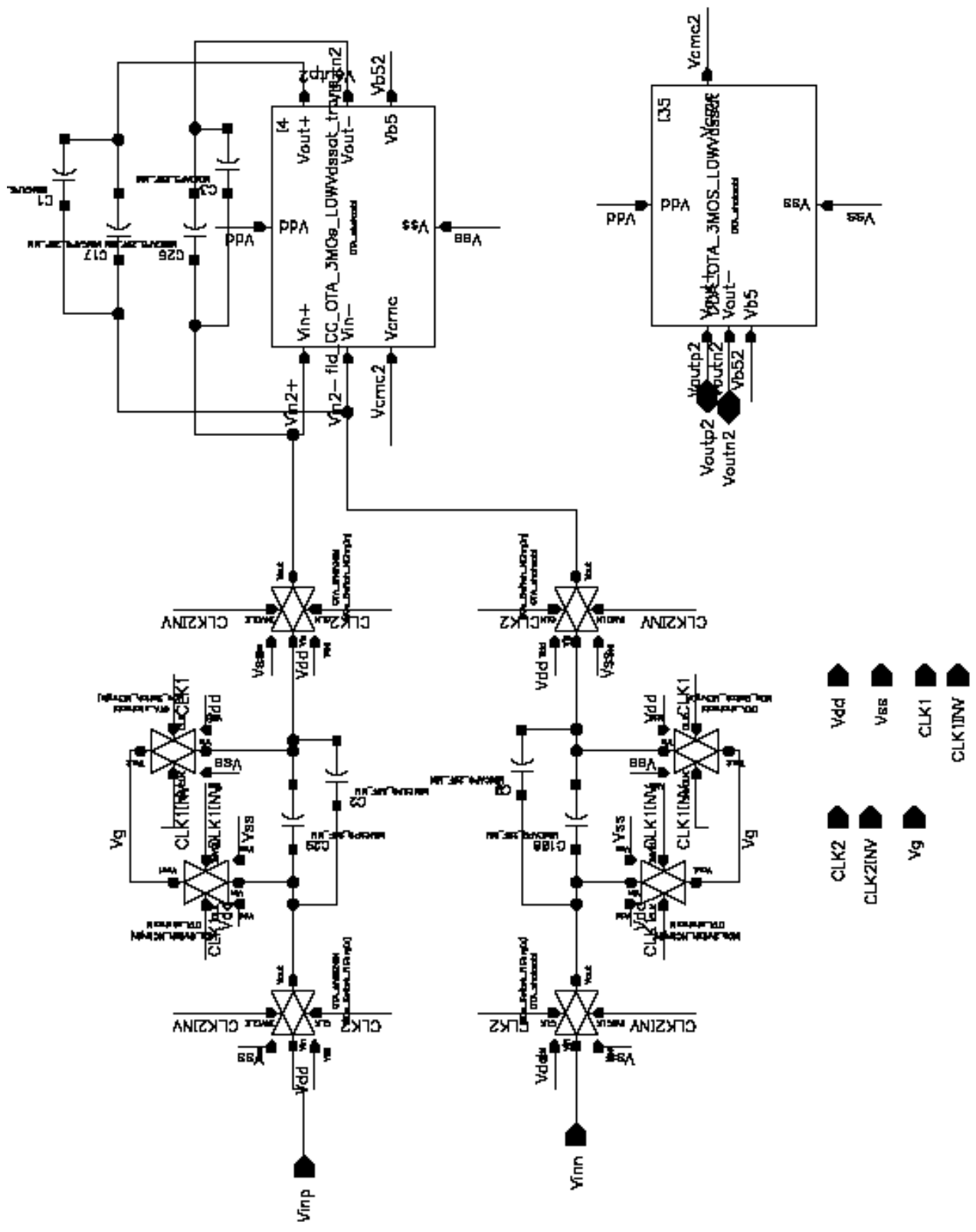
B1: Proposed Topology III



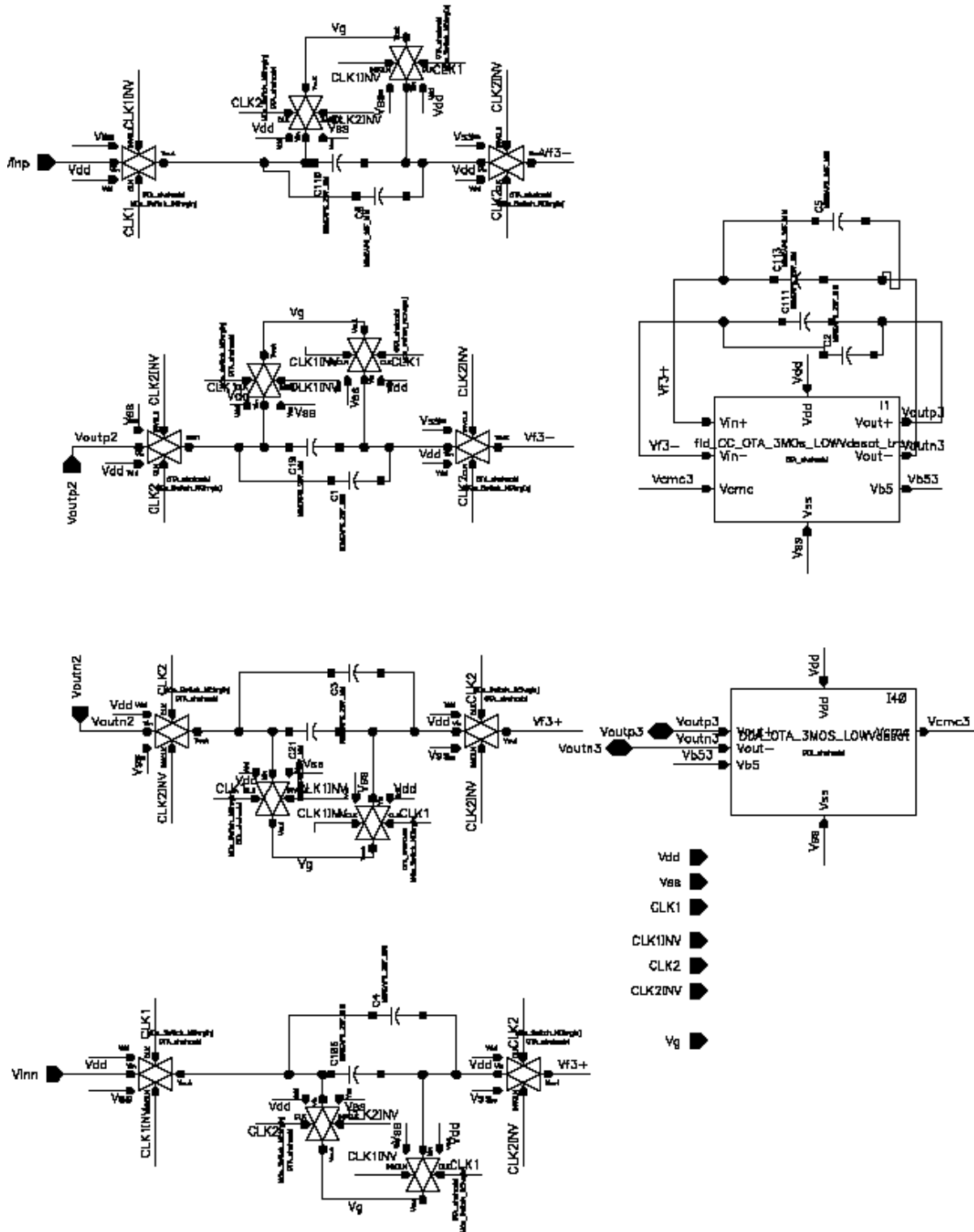
B2: Proposed Topology-III First integrator



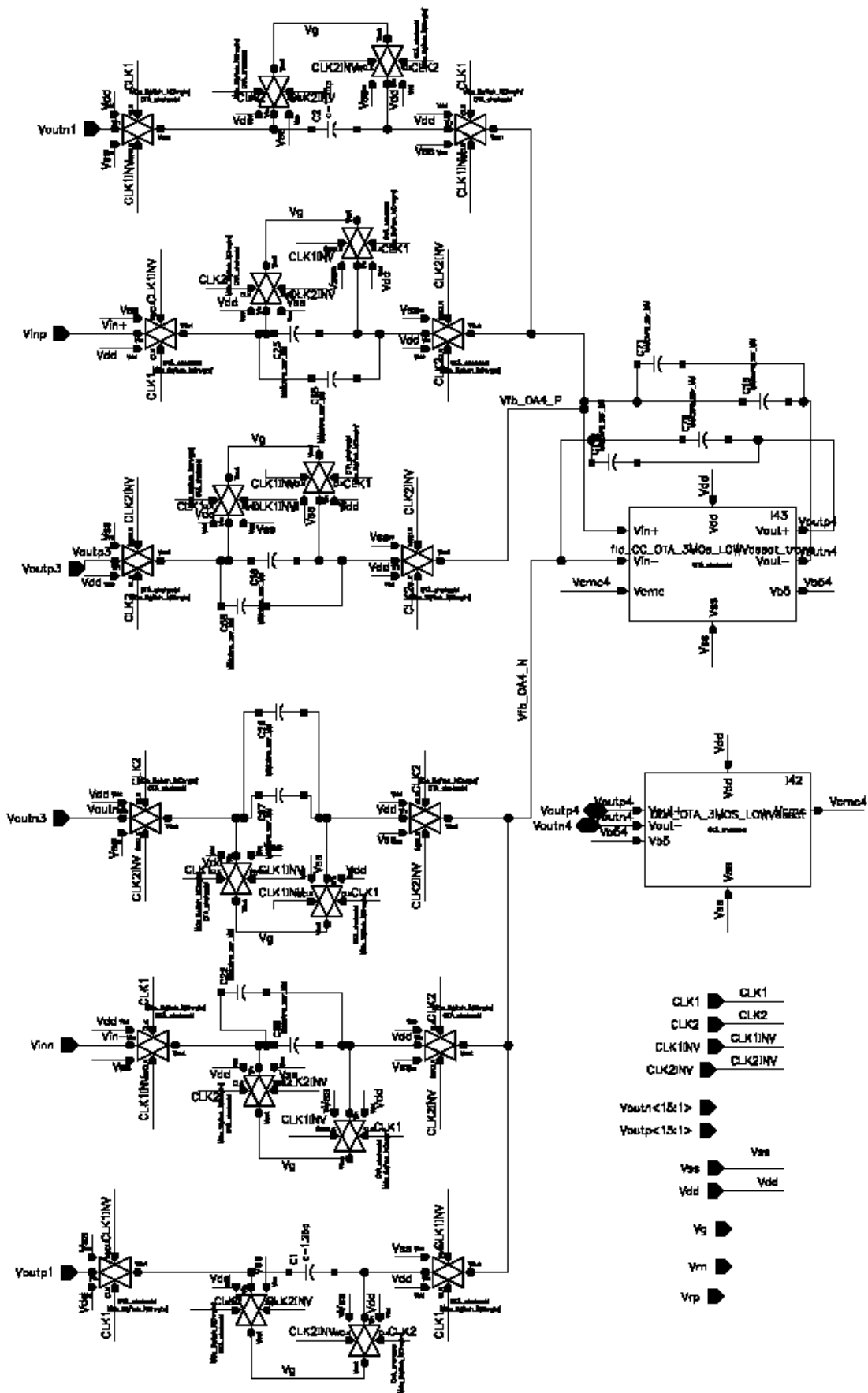
B3: Proposed Topology- III Second integrator



B3: Proposed Topology-III Third integrator



B4: Proposed Topology-III Fourth integrator



Appendix C: Verilog-A codes

C1: Verilog-A code for Operational Amplifier

```
// VerilogA for mod_shahzabl, Diff_Opamp, veriloga

//from different examples provided in AHDL labopf Cadence and paper: Behav.mod fo Op-Amp dsm
with verilog-A

`include "discipline.h"
`include "constants.h"

`define PI 2.141592653589
//=====

module Diff_Opamp(vout_p, vout_n, vcmc, vin_p, vin_n, vspply_p, vspply_n );
// PINS
input vin_p, vin_n;
// vin_p - differntial positive or non-inverting input pin
// vin_n - differntial negative or inverting input pin

input vspply_p, vspply_n; // pos and neg power supplies

output vout_p, vout_n;
output vcmc;

electrical vin_p, vin_n, vout_p, vout_n, vcmc, vspply_p, vspply_n;

// INSTANCE PARAMETERS:

parameter real gain = 1000.0 exclude 0.0; // gain = Open loop voltage gain, or DC voltage
gain

parameter real imax = 1000u exclude 0.0; // imax = Input Tail bias current [A]

parameter real gbw = 1000M exclude 1.0; // GBW = Gain bandwidth/unity gainfrequency
[Hz]

parameter real rin = 12.0M exclude 0.0; // rin = Differential input resistance, or resistance
measured // between both inputs [ohms]

parameter real sr = 500.0M exclude 0.0; // sr= Slew rate of the op Amp

parameter real rout = 6000.0; // rout = output resistance
[ohms]
```



```

    parameter real vin_offset = 0.0u;      // vin_offset = Input offset voltage, the voltage
required for                             //volts output [V]

// vsoft = Output soft clipping point, measured from the
// supply rails [V]

    parameter real vsoftn = 0.3;
    parameter real vsoftp = 0.15;

// LOCAL VARIABLES

    real cg, rg;                          // components of the dominant pole
    real vmax_in;                          // input diff voltage
    real dveff;                            // differential effective input voltage and offset factor (vinp-
//vinn+ voffset)

    //real r_out;                          // output resistance

    real gm;                               // circuits transconductance

// INTERNAL NODES
electrical vgp, vgn, cmc;

//=====
analog begin

    @(initial_step)
    begin                                  // by default ALL analyses

        cg = imax/(sr);

        gm = 2 * 2.141592653589 * gbw * cg;
        rg = gain/gm;

        vmax_in = imax/gm;

    end

    dveff = V(vin_p, vin_n) + vin_offset; //it will be zero because the op-amp is considered with no
offset

    V(cmc, vspply_n) <+ 0.5 * (V(vspply_p)+ V(vspply_n)- vsoftp + vsoftn);

    V(vcmc) <+ V(cmc);

    // ----- Input Stage

```

```

I(vin_p, vin_n) <+ dveff / rin;
I(cmc, vin_p) <+ imax;
I(cmc, vin_n) <+ imax;

I(cmc, vgp) <+ gm * dveff ;
I(cmc, vgn) <+ -gm * dveff ;

// ----- Dominant Pole and Output Stage.

I(vgp, cmc) <+ 2*V(vgp, cmc)/rg;

I(vgn, cmc) <+ 2*V(vgn, cmc)/rg;

I(cmc, vout_p) <+ 2*V(vgp, cmc)/rout;
I(vout_p, cmc) <+ 2*V(vout_p, cmc)/rout;
I(cmc, vout_n) <+ 2*V(vgn, cmc)/rout;
I(vout_n, cmc) <+ 2*V(vout_n, cmc)/rout;

end
endmodule

```

C2: Verilog-A code for Quantizer

```
// VerilogA for mod_shahzabl, Qunatizer_4bit, veriloga

`include "constants.h"
`include "disciplines.h"

module Qunatizer_4bit(In_p, In_n , CLK, Out_p1, Out_p2, Out_p3, Out_p4, Out_n1, Out_n2, Out_n3,
Out_n4);

input In_p, In_n, CLK;
output Out_p1, Out_p2, Out_p3, Out_p4, Out_n1, Out_n2, Out_n3, Out_n4;

parameter real fs = 1.0 from (0:1) ;
parameter real delay = 0 from [0:inf];
electrical In_p,In_n, CLK;

real In;
//p , Inn ;

electrical Out_p1, Out_p2, Out_p3, Out_p4, Out_n1, Out_n2, Out_n3, Out_n4;

real Outp1, Outp2, Outp3, Outp4, Outn1, Outn2, Outn3, Outn4;

analog begin

    @(initial_step)
    begin

        Outp1 = 0;
        Outp2 = 0;
        Outp3 = 0;
        Outp4 = 1;

        Outn1 = 0;
        Outn2 = 0;
        Outn3 = 0;
        Outn4 = 1;

    end

    @(cross(V(CLK)-0.005, +1)) begin

        In = V(In_p) - V(In_n);

        if((In > 14.0/15* fs )) begin
            Outp1 = 1;
            Outp2 = 1;
        end
    end
end
```

```

    Outp3 = 1;
    Outp4 = 1;

    Outn1 = 0;
    Outn2 = 0;
    Outn3 = 0;
    Outn4 = 0;

end
else if(((In <= 14.0/15*fs) && (In > 12.0/15*fs))) begin
    Outp1 = 0;
    Outp2 = 1;
    Outp3 = 1;
    Outp4 = 1;

    Outn1 = 1;
    Outn2 = 0;
    Outn3 = 0;
    Outn4 = 0;
end

else if(((In <= 12.0/15*fs) && (In > 10.0/15*fs))) begin
    Outp1 = 1;
    Outp2 = 0;
    Outp3 = 1;
    Outp4 = 1;

    Outn1 = 0;
    Outn2 = 1;
    Outn3 = 0;
    Outn4 = 0;
end

else if(((In <= 10.0/15*fs) && (In > 8.0/15*fs))) begin
    Outp1 = 0;
    Outp2 = 0;
    Outp3 = 1;
    Outp4 = 1;

    Outn1 = 1;
    Outn2 = 1;
    Outn3 = 0;
    Outn4 = 0;
end

else if(((In <= 8.0/15*fs) && (In > 6.0/15*fs))) begin
    Outp1 = 1;
    Outp2 = 1;
    Outp3 = 0;
    Outp4 = 1;

```

```

    Outn1 = 0;
    Outn2 = 0;
    Outn3 = 1;
    Outn4 = 0;
end

else if(((In <= 6.0/15*fs) && (In > 4.0/15*fs))) begin
    Outp1 = 0;
    Outp2 = 1;
    Outp3 = 0;
    Outp4 = 1;

    Outn1 = 1;
    Outn2 = 0;
    Outn3 = 1;
    Outn4 = 0;

end

else if(((In <= 4.0/15*fs) && (In > 2.0/15*fs))) begin

    Outp1 = 1;
    Outp2 = 0;
    Outp3 = 0;
    Outp4 = 1;

    Outn1 = 0;
    Outn2 = 1;
    Outn3 = 1;
    Outn4 = 0;

end

else if(((In <= 2.0/15*fs) && (In > 0))) begin

    Outp1 = 0;
    Outp2 = 0;
    Outp3 = 0;
    Outp4 = 1;

    Outn1 = 1;
    Outn2 = 1;
    Outn3 = 1;
    Outn4 = 0;

end

else if(((In <= 0) && (In > -2.0/15*fs))) begin
    Outp1 = 1;
    Outp2 = 1;
    Outp3 = 1;

```

```

    Outp4 = 0;

    Outn1 = 0;
    Outn2 = 0;
    Outn3 = 0;
    Outn4 = 1;
end

else if(((ln <= -2.0/15*fs) && (ln > -4.0/15*fs))) begin
    Outp1 = 0;
    Outp2 = 1;
    Outp3 = 1;
    Outp4 = 0;

    Outn1 = 1;
    Outn2 = 0;
    Outn3 = 0;
    Outn4 = 1;

end

else if(((ln <= -4.0/15*fs) && (ln > -6.0/15*fs))) begin
    Outp1 = 1;
    Outp2 = 0;
    Outp3 = 1;
    Outp4 = 0;

    Outn1 = 0;
    Outn2 = 1;
    Outn3 = 0;
    Outn4 = 1;

end

else if(((ln <= -6.0/15*fs) && (ln > -8.0/15*fs))) begin
    Outp1 = 0;
    Outp2 = 0;
    Outp3 = 1;
    Outp4 = 0;

    Outn1 = 1;
    Outn2 = 1;
    Outn3 = 0;
    Outn4 = 1;

end

else if( ((ln <= -8.0/15*fs) && (ln > -10.0/15*fs))) begin
    Outp1 = 1;
    Outp2 = 1;
    Outp3 = 0;

```

```

    Outp4 = 0;

    Outn1 = 0;
    Outn2 = 0;
    Outn3 = 1;
    Outn4 = 1;
end

else if( ((In <= -10.0/15*fs) && (In > -12.0/15*fs))) begin

    Outp1 = 0;
    Outp2 = 1;
    Outp3 = 0;
    Outp4 = 0;

    Outn1 = 1;
    Outn2 = 0;
    Outn3 = 1;
    Outn4 = 1;

end

else if( ((In <= -12.0/15*fs) && (In > -14.0/15*fs))) begin

    Outp1 = 1;
    Outp2 = 0;
    Outp3 = 0;
    Outp4 = 0;

    Outn1 = 0;
    Outn2 = 1;
    Outn3 = 1;
    Outn4 = 1;

end

else begin
    Outp1 = 0;
    Outp2 = 0;
    Outp3 = 0;
    Outp4 = 0;

    Outn1 = 1;
    Outn2 = 1;
    Outn3 = 1;
    Outn4 = 1;
end

end

//Assigning the ouputs

```

```
V(Out_p1) <+ transition(Outp1,delay);  
V(Out_p2) <+ transition(Outp2,delay);  
V(Out_p3) <+ transition(Outp3,delay);  
V(Out_p4) <+ transition(Outp4,delay);
```

```
V(Out_n1) <+ transition(Outn1,delay);  
V(Out_n2) <+ transition(Outn2,delay);  
V(Out_n3) <+ transition(Outn3,delay);  
V(Out_n4) <+ transition(Outn4,delay);
```

```
end  
endmodule
```


C3: Verilog-A code for Switch

```
// VerilogA for OTA_shahzabl, Switch_NonIdeal_VerilogA, veriloga
// Based on Code from Praveen Gujjala
```

```
`include "constants.h"
`include "disciplines.h"
```

```
module Switch_NonIdeal_VerilogA (vin, control, vout);
```

```
    inout  vin, vout;
    input  control;
    electrical control;
    electrical vin, vout;
    parameter real vth = 0.5;
    parameter real ron = 10.0 from (0:inf);
    parameter real roff = 10.0M from (ron:inf);
    parameter real tconv = 2.0p from (0:inf);
    parameter real trise = 1.0p from (0:inf);
    parameter real tfall = 1.0p from (0:inf);
    parameter real slack = 0.1p from (0:inf);
```

```
    real rstate, rout;
```

```
    analog begin
```

```
        @(initial_step("ac","dc","tran","xf" )) begin
            rout = roff;
            rstate=roff;
        end
```

```
        @(cross (V(control)- vth, 0,
            slack, control.potential.abstol)) begin
```

```
            if( V(control) >= vth )
                rstate=ron ;
            else
                rstate=roff ;
```

```
        end
```

```
        rout = transition( rstate, tconv, trise, tfall);
        I(vin,vout) <+ V(vin,vout)/rout;
```

```
    end
```

```
endmodule
```

