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System Level Design of a Continuous-Time $\Delta\Sigma$ Modulator for Portable Ultrasound Scanners

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***Abstract*—In this paper the system level design of a continuous-time $\Delta\Sigma$ modulator for portable ultrasound scanners is presented. The overall required signal-to-noise ratio (SNR) is derived to be 42 dB and the sampling frequency used is 320 MHz for an oversampling ratio of 16. In order to match these requirements, a fourth order, 1-bit modulator with optimal zero placing is used. An analysis shows that the thermal noise from the resistors and operational transconductance amplifier is not a limiting factor due to the low required SNR, leading to an inherently very low-power implementation. Furthermore, based on high-level VerilogA simulations, the performance of the $\Delta\Sigma$ modulator versus various block performance parameters is presented as trade-off curves. Based on these results, the block specifications are derived.**

I. Introduction

Ultrasound systems are widely used in medical applications as a diagnosis technique. It has many advantages such as non-invasing scanning, live imaging and no long-term effect on the patient. Furthermore, the scanning equipment to perform ultrasound imaging is easily accessible and inexpensive compared to other diagnosis techniques like x-ray. However, ultrasound scanners are static devices with a significant size and high power consuming, which limits the amount of diagnosis that can be performed per unit of time. For the purpose of lowering the cost and increasing the amount of diagnosis per unit of time, portable ultrasound devices are being developed. Nonetheless, portable ultrasound scanners have a size limitation and are supplied with a battery which imposes another limitation on the maximum power consumption of the electronics inside. In order to maximize the quality of the picture with a fixed power budget, the electronics need to be custom designed, hence an application specific integrated circuit (ASIC) solution is required.

Ultrasound scanners consist of a transmitting circuit (Tx) [1], [2], a receiving circuit (Rx) and a transducer. In transmitting mode the transducer gets excited by the high-voltage Tx generating ultrasonic waves. In receiving mode the low-voltage Rx amplifies, delays and digitizes the waves received by the transducer. The Rx is usually the most power consuming circuitry due to the high receiving duty cycle of ultrasound scanners. One of the highest power consuming block of the receiving circuitry is typically the ADC, hence it is a very critical design for portable ultrasound scanners.

This paper presents the design of a fully-differential continuous-time delta-sigma modulator (CTDSM) for a receiving channel of a portable ultrasound scanners using capacitive ultrasonic micromachined transducers (CMUTs).

II. System level ADC requirements

The CTDSM in this paper is designed specifically for the 64-channel ultrasound Rx system in Fig. 1. Each channel contains a CMUT, a low noise amplifier (LNA), a time-gain control (TGC), an analog to digital converter (ADC) and a digital delay (DD). All channels are digitally summed using beamforming in order to reduce the amount of data that needs to be transferred from the portable device to the digital signal processing unit. The signal to noise ratio (SNR) of this data dictates the maximum image quality achievable, however, the higher the SNR the more power consuming the electronics are. The design target is to achieve the lowest power consumption with an acceptable level of image quality, which is estimated to be obtained with a minimum of 60 dB SNR at the output (SNR_{out}). Nonetheless, the signals received by the CMUT are uncorrelated, hence the SNR after summing 2^N channels is N·3 dB higher than the single channel SNR. In this particular ultrasound receiving system, if a SNR_{out} of 60 dB wants to be achieved, SNR of each ADCs needs to be 42 dB.

The supply rails of the electronics in the Rx system are specified at V_{ss} = 0 V and V_{dd} = 1.2 V with a common mode level of V_{cm} = 0.6 V. The input signal of the fully-differential ADC, which is defined by the output signal of the TGC, is a differential signal with a 10 MHz bandwidth (BW) and peak-to-peak voltage of V_{pp} = 1.2 V.

Another important specification of the Rx system is the delay resolution in the DD, which determines the precision of the beamforming. Increasing the resolution of the delay improves the image resolution but it also increases the power consumption and area of the digital circuitry. A study performed showed that the minimum delay resolution that provides a sufficient image quality is 3 ns. This result has a large impact on the ADC topology selection.

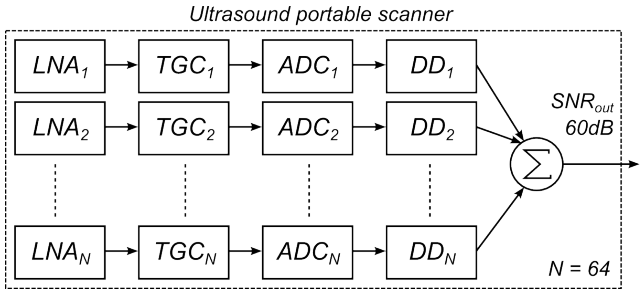

Fig. 1. 64-channel ultrasonic portable device structure.

TABLE I. CONTINUOUS-TIME ΔΣ MODULATOR SPECIFICATIONS

SNR [dB]	BW [MHz]	V_{pp} [V]	V_{cm} [V]	OSR	Quant. bits
42	10	1.2	0.6	16	1

After determining the specifications of the ADC, a topology must be chosen. Traditionally a nyquist-rate ADC running at two times the BW (20 MHz) is used. However, the delay resolution achievable is only 50 ns hence there is a need for an interpolation filter. These filters are complex, area demanding and power consuming. An alternative approach is to use a delta-sigma modulator with an oversampling ratio (OSR) of 16 running at a sampling frequency f_s = 320 MHz, which inherently provides enough delay resolution. A continuous-time delta-sigma modulator is selected over a discrete-time due to its lower power and higher frequency operation range [3], [4]. In order to simplify the digital circuitry the number of bits in the output of the delta-sigma modulator is chosen to be 1. In this case, the DD block becomes a simple 1-bit delay line running at 320 MHz which can be easily be accessed at any intermediate point, and can be custom designed to achieve high efficiency. A summary of the specifications of the CTDSM is shown in Table I.

III. CONTINUOUS-TIME ΔΣ MODULATOR DESIGN

The first step of designing a CTDSM is to split total noise budget, SNR_{tot}, into quantization and thermal noise. Typically, the signal to quantization noise ratio (SQNR) is designed to be 10-12dB higher than the target SNR_{tot}, allowing for the thermal noise to spend most of the noise budget. This margin is used later in the implementation in order to accommodate for circuitry with non ideal specifications. In this design, for a total SNR_{tot} of 42 dB, the SQNR targeted is 54 dB, which leads to a maximum spectral density of the thermal noise of 3.3 mV/$\sqrt{\text{Hz}}$.

The following step is to determine the order (M) and output of band gain of the loop filter (H_{inf}) of the CTDSM. For that purpose a discrete-time model of the CTDSM is used. In Fig. 2 the SQNR and the maximum stable amplitude (MSA) are plotted versus the H_{inf} for different orders. The OSR is set to 16 and number of output bits is set to 1-bit for all the plots. Optimal placing of zeros is used for all the orders to obtain a

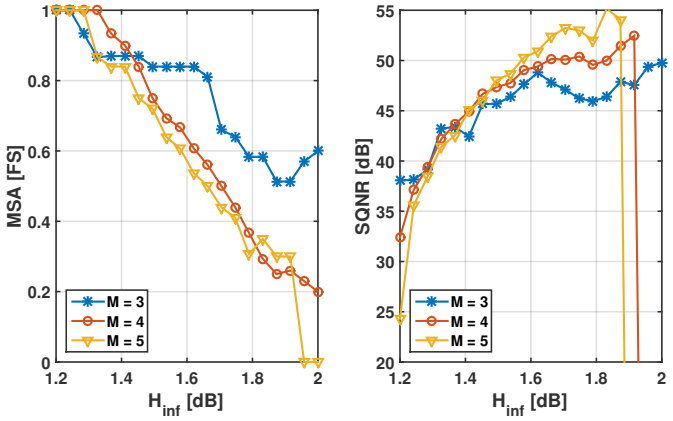

Fig. 2. MSA and SQNR at MSA-6 dB versus H_{inf} for different M.

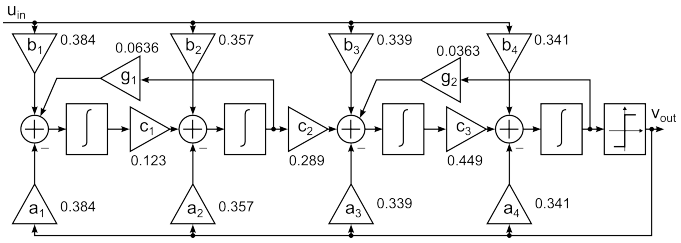

Fig. 3. Structure of the continuous-time delta-sigma modulator.

higher SQNR [3]. As it can be seen from Fig. 2 the minimum order that can achieve a sufficient peak SQNR is M = 4, and H_{inf} = 1.7 dB leads to the best compromise between SQNR and MSA. A low MSA can be chosen due to the high thermal noise allowed in the circuitry.

The structure chosen to implement the CTDSM is the cascade-of-resonators feedback structure (CRFB) shown in Fig. 3. It consists of four feedforward paths, a_1-a_4, four feedback paths b_1-b_4, three scaling coefficients c_1-c_3 and two resonators g_1-g_2. Feedforward was used so that the integrators only have to process the noise and not the input signal, hence their output swing is reduced. The two resonator coefficients realize the optimal placing of the zeros of the system. The value of the continuous-time coefficients of this CRFB structure can also be seen in Fig. 3. Using this structure and coefficients, the frequency spectrum of the continuous time model of the CTDSM is shown in Fig. 4. The MSA is 0.7 full-scale and the peak SQNR obtained is 55.5 dB.

IV. BLOCK IMPLEMENTATION

The next step is to implemented the integrators, the coefficients, the quantizer and the feedback digital to analog converter (DAC). All the circuitry is designed to be implemented in a 65 nm process. The full CTDSM on circuitry level is shown in Fig. 5. The next subsections describe the topology selection of each block, and how are they realized.

A. Integrators and coefficients

For the implementation of the integrators an RC-integrator topology is used and it was designed accordingly to [5].

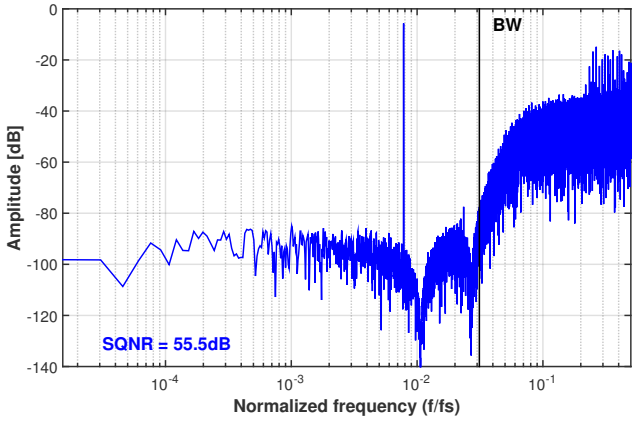

Fig. 4. Frequency spectrum of the continuous-time ΔΣ modulator designed.

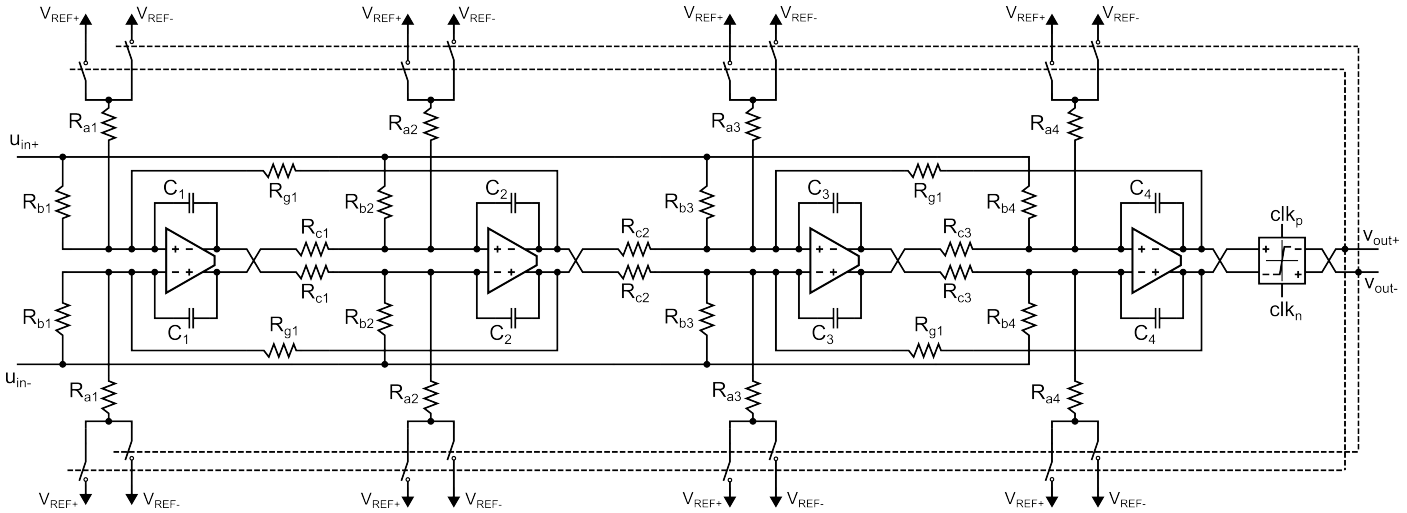

Fig. 5. Continuous-time delta sigma modulator implemented.

It consists of fully-differential operational transconductance amplifier (OTA_i), two integrating capacitors (C_i) and several resistors which implement the coefficients defined in Section III (a_i, b_i, c_i and g_i). The relationship between the coefficients, k_i, and the value of the resistors R_i is dictated by (1). The absolute value of the resistors and capacitor is a trade-off between power consumption and thermal noise which is discussed in Section V-A.

$$k_i = \frac{1}{f_s \cdot C_i \cdot R_i} \tag{1}$$

This type of integrator was chosen due to its simplicity, its high linearity and high parasitic insensitivity. It was also considered to use gmC integrators since they can provide high frequency operation, but the THD performance of these type of integrators is poor and it is a very critical factor for ultrasound imaging signal quality [4].

B. Quantizer and feedback DAC

The CTDSM designed has 1-bit output, hence the quantizer can be implemented with a fully-differential comparator. The DACs are realized as voltage feedbacks which consists of a feedback resistor connected to two reference voltages V_{ref+} V_{ref-} through two switches controlled by the output of the comparator. This topology was chosen since it is low area demanding, easily controllable and has low parasitics. The feedback pulse shape is chosen to be a non-return to zero due to its less sensitivity to jitter, which is critical at the high operating frequency used, and its low circuitry requirements, which translate into area and power consumption savings.

V. Block specifications and trade-offs

Simulations show that the maximum achievable SQNR for this topology is 55.5 dB, however, this number can only be achieved with ideal blocks. The higher the performance of each block the closer the SQNR will be to 55.5 dB. Nonetheless, the circuitry designed is used in portable ultrasound scanners, hence the performance of each block needs to be compromised in favor of reducing the area and power consumption. Furthermore, for a fixed SNR_{tot}, if the SQNR is lowered the maximum thermal noise allowed needs to be reduced, which also affects the power consumption and area of the circuitry. All these trade-offs between the performance of the blocks, SQNR and thermal noise are difficult to assess due to the complexity of the CTDSM. In order to address these trade-offs, a VerilogA model of the OTA, the comparator and the DACs was created, and a testbench was prepared to simulate the full CTDSM on schematic level. Using this testbench with VerilogA models of the blocks, the designer can easily create trade-off curves by sweeping all the different performance parameters to find a good compromise between block specifications and SQNR.

A. Coefficient capacitor/resistor size

The coefficients found in Section III impose a relationship between the integrating capacitors and the resistors (1), however, determining the absolute values is a trade-off. The lower the capacitor value, the lower the current to charge it, however the resistors become bigger, hence the thermal noise introduced also increases. The minimum capacitor size of a 65 nm process is approximately 10 fF, which leads to the maximum resistor size of approximately 8 MΩ. The spectral density of the thermal noise generated by such a resistor is $0.36\,\mu V/\sqrt{Hz}$, which is four orders of magnitude lower compared to the total spectral density of the thermal noise allowed in the circuitry, $3.3\,mV/\sqrt{Hz}$. Consequently, the thermal noise of the resistors is not a limiting factor, hence the integrating capacitors used should be as small as possible. Capacitor sizes of 100 fF are used for matching purposes and also to make the circuitry more robust to parasitic capacitances.

Another relevant consideration regarding the coefficients is the robustness of the CTDSM to R and C process variations. In a 65 nm process, both R and C can vary up to 20%. Using the testbench with the VerilogA model of all the blocks, this variation can be introduced in order to see what effect does it have in the CTDSM. The simulations show that by using a 3-bit capacitor trimmeable array for each of the integrator capacitors the SQNR drop due to process variations is less than 0.8 dB. It is important to realize that the OTA needs to be able to handle the maximum capacitance of the trimmeable array, which costs extra current.

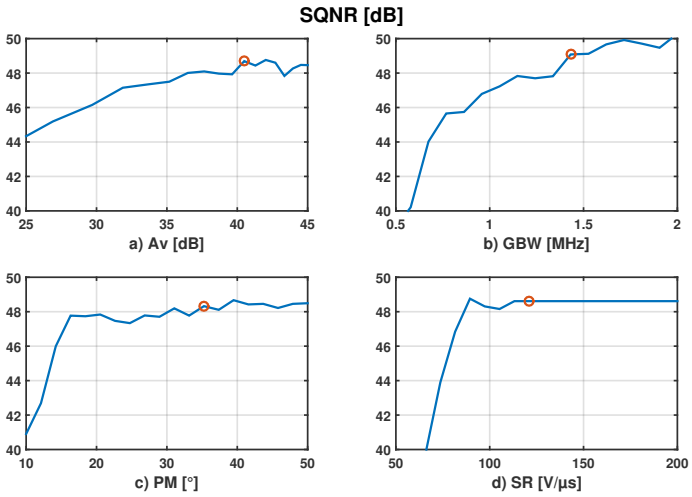

Fig. 6. OTA parameter sweep. SQNR versus: a) A_v b) GBW c) PM d) SR.

B. Operational Transconductance Amplifiers

The OTAs of the CTDSM are the most power consuming parts, hence finding the correct minimum specifications is key to minimize the power consumption of the system. Using the VerilogA model of the fully-differential OTAs, the trade-off curves of the SQNR versus gain (A_v), gain-bandwidth (GBW), phase margin (PM) and slew rate (SR) can be found. The results can be seen in Fig. 6, where an offset of 5 mV is used as a design margin. A good compromise between the OTAs performance parameters and SQNR is found with an A_v of 40 dB, a GBW of 1.4 GHz, a PM of 35° and a SR of 120 V/µs. These first OTA specifications lead to a SQNR of 49.2 dB. Readjusting the noise budget to the new SQNR, the maximum spectral density of thermal noise allowed in the circuitry is now 1.74 mV/$\sqrt{\text{Hz}}$. A simple fully-differential OTA with such specifications was quickly designed to assess the approximate magnitude of the thermal noise. Simulations shown a total input referred spectral density of noise of 50 µV/$\sqrt{\text{Hz}}$ which is negligible compared to the total thermal noise budget. Consequently, the thermal noise of the OTA is not a design limiting factor. In this design, the same OTA is used in all four integrators for simplicity purposes. However, in future designs the second, third and fourth OTAs can be downscaled lowering the specifications and thereby the power consumption.

C. Comparator and DACs

One of the most important factors for the CTDSM stability is the loop delay, which is the time that it takes for the comparator to generate a valid output that can be used as a feedback signal. This loop delay is determined by the speed and transition time of the comparator and DACs. Using the same approach as the OTAs, the VerilogA model of the comparator and DACs are used in order to sweep the total loop delay (ld) and the output transition time (tt). The trade-off plots are shown in Fig. 7, where an offset of 5 mV is used as a design margin. The specifications for the ld and tt are set to 0.3 ns and 55 ps respectively. Similarly to the OTAs the estimated thermal noise generated by the comparator and DACs is negligible compared to the thermal noise budget.

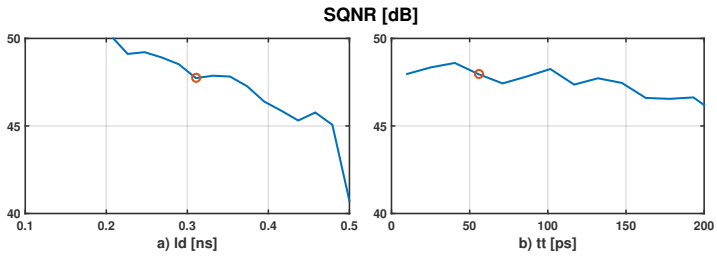

Fig. 7. Comparator and DACs parameter sweep. SQNR versus: a) Loop delay b) Transition time.

VI. Discussion and Future Work

After the trade-off analysis, the values of the resistors and capacitors and also the first specifications for the OTAs, comparator and DACs are defined. The next step is to design the blocks at transistor level using a 65 nm process. During the design, the performance parameters of the blocks might need to be tweaked due to non-idealities, process corners and mismatch. The design of the OTAs, comparator and DACs are mostly complete and the full $\Delta\Sigma$ modulator design will be sent for fabrication in the next months. The first simulation results show a very high correlation between the results obtained with the VerilogA models and the implemented circuitry, and the expected current consumption of the modulator is 0.9 mA.

VII. Conclusions

In this the system level design of a fully-differential continuous-time $\Delta\Sigma$ modulator for portable ultrasound scanners is presented. A fourth order cascade-of-resonators feedback topology with optimal zero placing is used achieving a SNR = 49.2 dB. The modulator has an OSR of 16, 1-bit quantizer and it runs at a f_s of 320 MHz. The thermal noise of the resistors and OTAs is shown to be negligible due to the low SNR requirements, which inherently leads to a very power efficient implementation. VerilogA models of the OTA, comparator and DACs are used to assess the modulator performance versus the performance parameters of each block generating trade-off curves. The specifications derived for the OTAs are A_v = 40 dB, GBW = 1.4 GHz, PM = 35° and SR = 120 V/µs. The comparator and DACs can allow for a maximum loop delay of 0.3 ns and a maximum transition time of 55 ps.

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