SYSTEM LEVEL POLICIES FOR FAULT TOLERANCE ISSUES IN THE FERMI PROJECT

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Abstract

The FERMI system, performing acquisition and DSP of calorimeter data in high energy collision experiments, planned at the LHC collider (CERN, Geneva, CH) is briefly overviewed. The system relies mainly upon the FERMI module, a dedicated VLSI multi-chip device performing most of the above functions, which is to be installed in large quantities (around 10^5) in the immediate neighbourhood of the collider itself, requiring rad-hard features. The issues for a system which absolutely requires fault diagnosis and possibly fault tolerance are described, with regard to the FERMI module itself.

1. Introduction

The FERMI Collaboration [2] is a research group of nine universities and three industrial partners, under the supervision of CERN, cooperating in the RD-16 Project[1], aimed at developing

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[1] Participating institutions are: CERN (Geneva), IMM (Linköping), Manne Siegbahn Institute of Physics, (Stockholm), Politecnico di Milano, University of Linköping, Universities of Paris VI-VII,

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a Front-End Readout MIcrosystem. The FERMI system is designed for *calorimetry* measurement experiments, planned at the LHC, CERN. The whole system must perform *analog* detection, dynamic range compression and digitisation, followed by *digital* triggering, DSP and buffering of large amounts of data (around 10^2 TeraBytes/sec, sampling rate 15 ns, frequency 67 MHz), related to the measurements of the positions and the energies of subatomic particles in collision experiments. The system works by detecting all raw information and then by performing three successive triggering steps, through which the amount of data is greatly reduced. It is intended for replacing the existing data acquisition systems for such calorimetry applications, which are entirely designed and built with analog technologies. The system consists of a *local* part, placed on the shell of the collider, which performs the low level triggering functions, and of a *remote* part, which performs the high level ones and supervises the work of the whole system. Most of the 1st and part of the 2nd level functions of the FERMI system need be executed by a *dedicated VLSI device*, the FERMI module, to be placed in a large number in the neighbourhoods of the experiment area, for reasons of speed and computational power. The experiment area is expected to be exposed to severe radiation stimulation, especially neutronic and high energy ionizing radiation, and to suffer from radiation activation. This requires to design a system capable of granting the completeness and the credibility of the measurements, which in turn imposes self diagnostic capabilities as a minimal working requirement.

The FERMI module is a multi-chip VLSI device implementing a number of acquisition channels, performing the above functions; the whole system is made of a large number of FERMI modules (around 10^5), placed together with the detectors (which are liquid argon calorimeters) on the shell of the collider, and of a set of driving host computers, placed in a separate and protected environment. The FERMI module is up to now the most widely developed part of the FERMI system. Therefore the core of the system, the FERMI module, need absolutely have diagnostic capabilities and possibly also fault tolerance. For this reason, the design of the FERMI module has required to put together physical requirements, related to the nature of the physical experiments to be carried out, environmental/technological constraints and performances, including self diagnosis and fault tolerance.

Section 2 introduces the adopted guidelines for the self diagnosis and for the fault tolerance in the FERMI system and, more specifically, in the FERMI module. Section 3 gives a description of the structure of the FERMI system, focusing onto the FERMI module itself. Section 4 presents the strategies used for the self diagnosis and the fault tolerance of the FERMI module, while Section 5 lists the related testing procedures.

2. System Specifications

The quantity of data to be processed by the FERMI system is extremely large, yet data contain a very large degree of redundancy. However, from physical considerations [1, 2] significant events are expected to occur at a very low frequency and to be mixed with a large number of irrelevant ones as well as to be masked by background noise. This implies that, in spite of the large degree of redundancy, both the *completeness* (no loss of data) and the *credibility* (no corruption, masking or aliasing) of data need absolutely be granted.

The project was started in the absence of definite knowledge about the behaviour of microelectronic digital devices in rad-hard environments, in particular the absence of

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University of Pavia, University of Stockholm. Industrial partners are: ABB-Hafo AB, SiCon AB, Swedish MicroSystems AB.

characterizations of the nature and of the spatial/temporal distributions of faults. This has prevented the possibility of formulating realistic fault models. Due to this high uncertainty degree about possible faults, several technological options have been considered, namely CMOS and SOS (Silicon On Sapphire), for the implementation of the FERMI module: the first one is less expensive, but the second one is hard-rad. No definite choice has however been possible, due to the lack of experimental quantitative data, at the beginning of the project, about the behaviour of the two technologies in conditions of exposure to radiations of various types. Experiments of this type are being carried out at ATOMIKI (Debrecen, Hungary), but definite results are not yet available. Preliminary results show that both transient and permanent faults (in general multiple) are to be expected for both technologies, although SOS seems to be less sensitive than CMOS.

To match the above physical requirements and environmental constraints it has been decided to design the FERMI system giving priority to *self diagnosis* capabilities, in order to grant that data delivered from one level of the system to the next one are *correct*. Should this be no longer true, the related piece of information is better discarded. *Self correction* is implemented whenever possible, compatibly with costs, measured in terms of the overhead of silicon area, of time and of circuital complexity. The indeterminacy of the fault models has suggested to fulfill the following priority list:

- handling both transient and permanent faults;
- handling single and possibly also some multiple faults;
- providing graceful degradation.

As a result, the designed FERMI system and, in particular, the FERMI module provide the following functionalities:

- information is complete and credible (up to physical limitations, of course);
- the system is fault tolerant at least to single faults;
- the system gracefully degrades in the presence of multiple faults.

The information in the FERMI system is partly handled locally (in the FERMI module) and partly remotely. Due to the locality of the extremely large number of FERMI modules and to the amount of data to be processed, self diagnosis is performed for the FERMI module in a highly concurrent and distributed way. This implies that each FERMI module need autonomously perform self diagnosis. On the contrary, not all fault tolerance policies can be performed locally, but need be deferred to a remote monitoring, in particular the fault tolerance functions requiring a large reconfiguration of the system, by excluding/including a number of acquisition channels. This remote control is anyway necessary for the higher level processing of the triggered information, since these computations are too difficult to be performed locally.

3. Structure of the System

The local part of the system consists of a number of acquisition channels (up to 5×10^5). Each acquisition channel is tied to one detector. The channels perform data acquisition and the 1st level triggering functions. They output filtered and partially processed data for the 2nd and 3rd level triggering functions, which are performed by the remote part of the system; output data are associated with a temporal frame. Optical fibres connect the local and the remote parts of the system.

The system is redundant at the level of acquisition channels: one channel is spare every group of four channels. To support dynamic redundancy two groups of switches have been introduced for each acquisition channel, in order to guarantee a proper routing of data flow through the working channels. Additional circuits, the validators, are required to validate the data processed by the channels, with respect to their relevance, from the point of view of the physical meaning, in the collision experiments. Figure 1 shows the general structure of the local part of the system at this level. The reconfiguration policies are handled by the remote hosts; a validation circuit allows to periodically calibrate and test each channel.

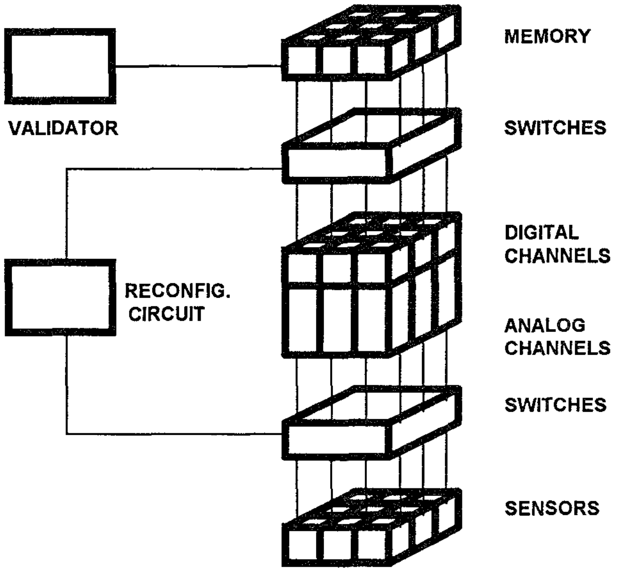

Figure 1: General structure of the local part of the FREMI system.

A FERMI module is composed by 12 such acquisition channels, integrated in groups of 4 channels, one of which is spare. It includes also one service chip, which performs DSP and support functions for the 9 active channels. These functions are: digital FIR filtering of the samples, by means of convolvers, and initialisation, calibration and monitoring of the channels, by means of microcontrollers. The chips inside a FERMI module are connected by means of electrical wires. The chips are programmable: each register is assigned an address and therefore it can be read or, in some cases, written by the microcontrollers and/or by the remote hosts.

Each acquisition channel consists of an analog part, an ADC, followed by a digital part, a look-up table (LUT), that linearizes and expands the outputs of the ADC, and a storage buffer, shared by all channels in a group of three active channels. The sampling period is 15 ns and the samples are represented over 10 bits, which are expanded to 15 bits in the LUT.

First level triggering is obtained in each FERMI module by summing the outputs of the nine active channels and then by thresholding the result. Filters in the service chip extract a rough estimation of the timing and of the energy of the triggered event. Triggered data are stored in the storage buffer, together with their timing/energy reference, and are passed to the 2nd and to the 3rd level triggering functions. Other filters in the service chip process the stored data before broadcasting them to the remote hosts, in order to extract more accurate timing and energy information. Figure 2 shows the structure of an acquisition channel and of the service chip in the FERMI module.

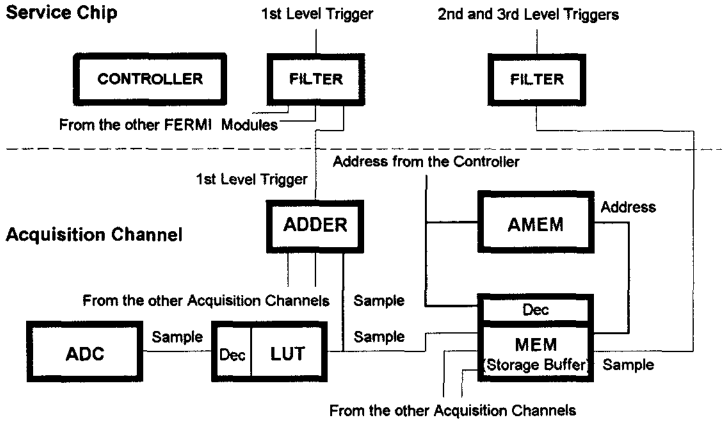

Figure 2: The structure of the FERMI module.

A FERMI board contains three channel chips plus one service chip; the whole system consists of a high number of such boards, placed in the immediate neighbourhood of the collider (thus being exposed to radiation). The module is integrated as a silicon-on-silicon multi-chip microsystem; the silicon substrate contains all the connection wires among the chips as well as a built-in support circuitry. It must be noted that the dimensioning of the intrinsic redundancy of the FERMI module and the partitioning of the module itself into four chips derive from a tradeoff between costs, measured in terms of silicon surface, given the technologies, from technological limitations and from the necessity of protecting the most critical parts of the module, which are the acquisition channels, because of the relevance of the processed physical information. Moreover, since the service chip is unique for every FERMI module, it must be designed with particular care, in order to make it as robust as possible.

4. Strategies for System Fault Tolerance

Given the lack of definite information on the fault model (in particular, on the distribution of faults), for the protection of the digital part of the FERMI module, it was decided to adopt techniques capable of:

- detecting single or multiple faults within individual subsystems of each acquisition channel (see also Figure 2), by means of ECC. These are linear cyclic redundancy codes, e.g. the extended Hamming code, for busses and memory elements, or residue arithmetic codes, e.g. the 3N code, for adders, threshold comparators and digital filters, respectively;
- providing survival to single faults within the individual subsystems of each acquisition channel (see also Figure 2), by means of hardware redundancy: triple modular redundancy for the most critical and otherwise unrecoverable functional units of each acquisition channel (the redundancy of acquisition channels themselves must also be taken into account);
- providing diagnostic information and reconfiguration hardware for the host-driven reconfiguration of acquisition channels (see also Figure 1).

The analog part of the FERMI module is inherently safer then the digital part. In fact, the liquid argon calorimeter is fault resistant and the ADC is an analog device, designed by means of robust technologies. The possible degradation of the ADC can be adequately corrected by reprogramming the look-up table and, moreover, it is possible to rely upon the intrinsic redundancy of the system. For this reason, the analog part is not protected to the extents of the digital part. Periodical testing of the analog part is foreseen, by means of a validation circuit that allows to calibrate and test the channels; in case of degradation, the redundancy of acquisition channels is exploited to exclude the faulty ones. In the sequel, we give a brief overview of the fault detection and tolerance techniques adopted in the FERMI module.

5. Application of Testing Techniques in the FERMI Module

Following the guidelines presented in Section 4, fault diagnosis and possibly fault tolerance have been implemented in the functional units composing the FERMI module, as follows.

- *Sensors:* the nature of the sensors in the FERMI system is very simple (see [1]). We can assume that they are always fault-free. Possibly low-periodicity testing could be adopted to recheck their behaviour.
- *Input switches and analog part* (ADC): switches are used both for reconfiguration and for testing; they must be designed by adopting a robust, self-checking technique suited for analog data. A fault occurring in this structure is critical since it may prevent the nominal behavior. The sensor itself and the ADC are assumed to be fault-free (see [3, 4, 5]).

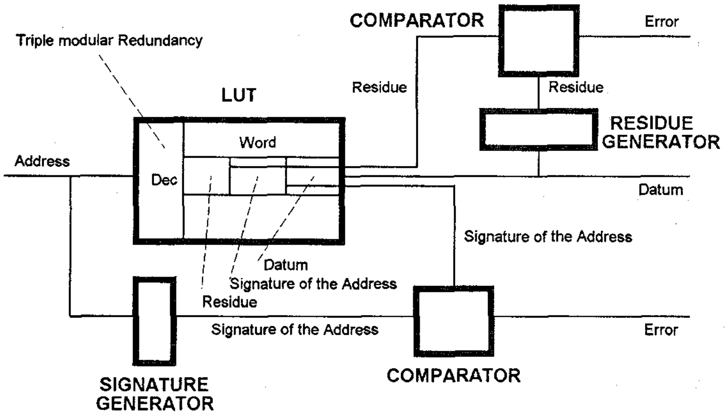

Figure 3: Protection scheme for the concurrent checking of the look-up table.

- *Look-up table* (LUT): two levels of fault management are provided for this device (see[2]).
  1. *Concurrent testing:* it is split into two further levels.
     - *1a. Memory word*: single ECC, e.g. the Hamming code, is adopted, possibly extended to provide double error detection.
     - *1b. Address decoder*: triple modular redundancy with a current voting scheme is adopted, for single fault survival, in the address decoding section. To provide detection of more complex fault distributions, as well as of bridging faults, each word is associated with the signature of its address and a signature checking is performed at readout, as it is shown in Figure 3.
  2. *Periodical testing:* it may be performed through a memory checksum operation, involving not only the data part of the word, but also the signature part. The structure shown in

Figure 4 supports such a scheme, by means of the adoption of an address counter and of a functional unit for the evaluation of the checksum. Some degree of host-driven testing will be required, to handle the testing procedure.

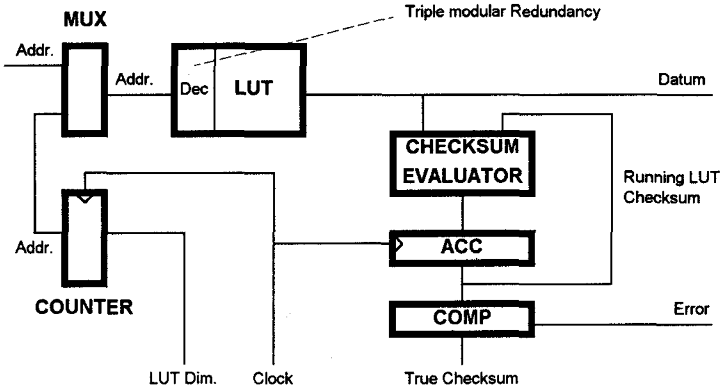

Figure 4: Protection scheme for the periodical checking of the look-up table.

- *Output switches*: these switches must be designed by adopting a robust, self-checking technique suited for digital data. A fault occurring in this structure is critical since it may prevent the nominal behavior of the acquisition channels.
- *Storage buffer:* the same technique adopted to protect the look-up table (concurrent and periodical testing) is suited to the protection of the data part of the storage buffer, with some modifications to take writing into account. The decoder of the storage buffer is protected by means of triple modular redundancy, similarly to the LUT. Since the samples registered in the storage buffers are already validated by the 1st level triggering function, it is important to grant their credibility. For this reason, the addressing of the storage buffer is further protected: an associative memory keeps track of the faulty locations in the storage buffer, as the scheme of Figure 2 shows. The associative memory itself is protected similarly to the LUT.
- *Reconfiguration circuits*: these circuits must store the information related to the working state of each channel and must generate the suited control signals for the input and output switches. A robust implementation technique should be adopted, due to the criticality of the switching control signals (e.g. two-rail logic).
- *Digital filters*: 3N residue arithmetic codes are used for fault diagnosis in digital filters; modular redundancy is employed for achieving fault tolerance (see [6, 7]).
- *Busses*: they are protected by means of EEC codes, which are 3N residue arithmetic codes for the busses connecting the arithmetic functional units and cyclic redundancy codes, in particular the (extended) Hamming code, for the busses connecting the remaining functional units. All encoders/decoders are protected by means of triple modular redundancy.

6. Conclusions

The main choices concerning fault detection and fault tolerance have been devised and a prototype of the FERMI module is currently being designed, which will undergo testing by 1994 (see [1, 2]). The analog part is being developed in full-custom rad-hard SOS-4 technology, by

ABB-Hafo AB; the design of the channel and service chips is being developed on programmable gate array, to be moved to full-custom rad-hard SOS-5 in the next future.

As a result of the effort of the project, the detailed design of an acquisition system (the FERMI module) has been developed, to be placed in an hostile environment, exposed to severe radiation stimulation, yet capable of processing information according to the following specifications.

- Corrupted data, provided by faulty elements, are *immediately* discarded.
- Correct data, provided by working elements, are *safely broadcast* to the remote hosts, which are placed in a less hostile environment.
- The nature of the fault, i.e. whether it is transient or permanent, can be determined.
- The structure can be reconfigurated, wherever it is possible; this can be always done at least at the level of acquisition channels.

The remote part of the FERMI system, i.e. the hosts that perform the 2nd and 3rd level triggering functions and provide a remote control for the FERMI modules, is currently in a preliminary phase of design. However, the design of this part of the system is fairly less critical, since it is placed in a controlled environment. Moreover, the 1st level triggering function and the DSP functions provided by the FERMI modules themselves greatly reduce the amount of data which are broadcast to the remote hosts, relaxing their performance requirements.

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