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System Level Power Optimization of Digital Audio Back End for Hearing Aids

Peter Pracný, Ivan H. H. Jørgensen, and Erik Bruun

Abstract—This work deals with power optimization of the audio processing back end for hearing aids - the interpolation filter (IF), the sigma-delta (ΣΔ) modulator and the Class D power amplifier (PA) as a whole. Specifications are derived and insight into the tradeoffs involved is used to optimize the interpolation filter and the ΣΔ modulator on the system level so that the switching frequency of the Class D PA – the main power consumer in the back end – is minimized. A figure-of-merit (FOM) which allows judging the power consumption of the digital part of the back end early in the design process is used to track the hardware and power demands as the tradeoffs of the system level parameters are investigated. The result is the digital part of the back end optimized with respect to power which provides audio performance comparable to state-of-the-art. A combination of system level parameters leading to the lowest switching frequency of the Class D power amplifier reported in literature for the ΣΔ modulator-based back end is derived using this approach.

Index Terms—audio, hearing aid, low voltage, low power, digital, system level, power optimization, interpolation filter, ΣΔ modulator, digital-to-analog converter, Class D, power amplifier, figure-of-merit.

1. Introduction

High audio quality, longer operation time and small device size are parameters demanded in hearing aids today. Optimum balance between the design parameters in every part of a hearing aid device is therefore of vital importance, making the power consumption one of the crucial requirements for the design. This is also the case for the audio signal processing path which requires a digital-to-analog conversion and a power amplifier at the back end to drive the speaker (see Fig.1). In order to ensure high efficiency in the output stage, it is normally operated in class D mode by using a push-pull configuration (basically two large inverters) controlled by two 1-bit signals [1,4,6,12,16,17]. Apart from having a high efficiency, this also eliminates problems with device matching compared to using a Class AB output stage as in [14,26,30]. The Class D output stage is usually implemented as an H-bridge (schematic in Fig.1 is simplified, showing single ended operation). Compared to [14,26,30] which use Class AB power stage, the Class D allows to perform all the signal processing before the output

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filter in digital domain. Digital design provides the advantage of low voltage, low power and cost effective implementation and scales down with integrated circuit (IC) technologies of today.

As the output stage operates using a single bit input, the resolution of the input signal (16 bits) must be converted to a 1-bit signal. A wide spread solution to this is using oversampled noise shaping modulators, also called ΣΔ modulators [1,12,16,17]. These modulators trade off the number of bits versus sampling frequency by suppressing the quantization noise at low frequencies at the expense of a drastic increase in high frequency noise. The high frequency noise is in this application filtered in the speaker (and placed outside the audible frequencies). Due to the oversampling nature of the oversampled ΣΔ modulator, an interpolation filter (IF) is needed prior to the modulator. The purpose of the interpolation filter is to upscale the sampling frequency of the incoming signal from fs_{in} to a new signal with a sampling rate ($OSR \times fs_{in}$) that equals the sampling rate of the ΣΔ modulator. Basically, the interpolation filter is simply a filter which ensures that extra sampling points (interpolation points) are added to the input signal without deteriorating the quality of the signal. However, the complexity of the interpolation filter depends on the upscaled sampling rate and thus the power consumption of the interpolation filter must be taken into account when evaluating the performance of the entire output stage. This will be treated in this paper. When using a multibit ΣΔ modulator, a digital pulse width modulation (DPWM) block that turns the ΣΔ signal into a symmetrical 1 bit pulse width modulation is needed.

This paper deals with the power optimization of the system in Fig. 1 and provides an overview of results obtained during a PhD study presented in [18]. The paper summarizes and elaborates the partial conclusions derived during the course of the PhD project. In Section 2, the design specifications and the figure-of-merit for the ΣΔ modulator and the interpolation filter are discussed. The figure-of-merit is used to judge the power consumption of the digital part early in the design process. In Section 3, an initial design is described. This design is used as the starting point for the optimization described in this section. Various approaches to optimize the initial ΣΔ modulator design are investigated using the tradeoffs of basic system level parameters and summarized. The resulting designs are then compared using the figure-of-merit which is introduced in section 2. A

trendline for the digital part of the system of Fig. 1 is derived based on the summary of results in Section 4, and a comparison with other state-of-the-art works in this topic is presented. In the conclusion of Section 5, it is discussed which approach leads to optimized audio back end with respect to power consumption.

2. Design Specifications and Figure-of-merit

A thorough discussion on hearing aid audio back end system specification and the ΣΔ modulator is provided in [19]. Taking into account that a hearing aid is intended for people with hearing problems, the bandwidth (BW) of the audio signal is a tradeoff between ensuring sufficient sound quality and the limited power available and is normally around 10 kHz. While it is possible to design a hearing aid with a signal bandwidth of 4 kHz to keep the current consumption even lower and still ensure some speech intelligibility, the bandwidth of BW = 10 kHz ensures good speech intelligibility as well as good localization of sound sources. In order to fulfill the Nyquist criterion, the input sampling frequency fs_{in} must be larger than 2×BW = 20 kHz. As the bandwidth for the hearing aid application is half of the bandwidth in high fidelity audio, the sampling frequency at the input of the system for this design was chosen to be half of the standard high fidelity audio sampling frequency 44.1 kHz/2=22.05 kHz. Also, in this work ideal 16 bit quantization of the input signal to the back end system is assumed. This results in the signal-to-quantization-noise ratio SQNR =98 dB. The input signal of the back end is then up-sampled using a multistage IF and passed to the ΣΔ modulator [15,24,27].

Investigating the hearing aids in the market today does not bring much information about the requirements for the electronics as this is considered confidential information. However, from [1] and [6] the peak signal-to-noise-ratio varies between 70 dB and 92dB, and in this work, the target is a signal-to-noise-and-distortion ratio (SNDR) of 90 dB at the total output. The IF and the ΣΔ modulator are designed to keep the quality of the audio signal close to SNDR = 98 dB so that a margin of approximately 8 dB is left for the performance reduction introduced by the output stage. Higher order ΣΔ-modulators inherently become unstable when the input exceeds a certain signal amplitude. This amplitude is called the maximum stable amplitude (MSA) and varies for all ΣΔ-modulators

depending on the design. Therefore, the higher the MSA, the more the requirement for the noise can be relaxed to achieve a certain SNR. However, when the MSA approaches full scale, the quantization noise tends to increase drastically for ΣΔ-modulators, yielding a very poor SNR, and thus a design requirement of an MSA as close to -1 dBFS as possible is chosen as a compromise. A maximum system clock frequency was initially specified by a hearing aid company to be 5.6 MHz but as the work in this paper shows significant improvements can be achieved by exceeding this number.

Both the IF and the ΣΔ modulator are digital designs in this work. A digital ΣΔ modulator can be looked at as a digital filter with two transfer functions: a signal transfer function (STF) and a noise transfer function (NTF). Hence, a figure of merit (FOM) developed for digital filters [2,28,35] can be applied. In this work, the FOM is used to judge the complexity of the IF and the ΣΔ modulator by counting the number and complexity of adders [11, 20-23]. This leads to

$$FOM = (\Sigma_i \, b_i \times OSR_i) \,/\, 64 \qquad (1)$$

where i is the number of adders in the block of interest, b_i is the number of bits used in individual adders and OSR_i is the oversampling used for the individual adders. The factor of 64 in (1) is included since this is the OSR for the ΣΔ modulator in the first design presented in this paper and thus we normalized the FOM to this. In the case of the ΣΔ modulator block, OSR_i is the same for all the adders. Since this FOM accounts for the majority of the cells needed to implement the IF and the ΣΔ modulator, it is roughly proportional to the power consumption of the design and is a valuable tool when choosing between designs in an early design phase. The lower the FOM, the less hardware and power demanding the design is. There are more precise figures of merit for ΣΔ modulators used in other works [27]. However, these figures of merit can be used only after the design has been completed and possibly measured. The advantage of the figure of merit of (1) is that it makes it possible to decide early in the design process whether or not an optimization approach is reasonable. The above mentioned specifications and FOM will be used in this work for comparison when optimizing the back end system. For the sake of comparison, all the FOMs in this work are normalized to $64 \times fs_{in}$ = 64×22.05 kHz = 1.4 MHz, the sampling rate used for the first design presented in section 3.

3. Optimization

A simplified general schematic for all the ΣΔ modulators in this work is shown in Fig. 2. The basic cascade of resonators with feedback (CRFB) structure is used. This converter type has been chosen for two reasons. First, the order can be scaled arbitrarily simply by adding more feedback loops. Second, as the study focuses on the system level design parameters (sampling rate, modulator order, etc.), only one topology is treated to limit the study. There are other architectures also suited for digital implementation, such as MASH [32], using the bus splitting and frequency masking methods to save hardware and current consumption [7,33,34]. Since this work covers the initial design phase, it discusses simple tradeoffs of system level parameters to arrive at a conclusion of how the choice of these parameters affects the hardware and power demands of the system. Inclusion of the above mentioned advanced design techniques would introduce complexity and make the effect of a simple parameter tradeoff less readable. For this reason, the ΣΔ modulator architecture is kept to be the basic CRFB. The advanced design techniques can be introduced at a later phase in a project. Moreover, feedback (FB) can be used around the whole back end to improve the performance, but in this case an analog-to-digital converter (ADC) has to be included in the FB, and the system is not fully digital. In this case, the FOM of (1) would become more complex to account for the hardware and power consumption of the analog blocks. Such investigation is left as future work.

A model using fixed-point arithmetic was designed and simulated in Matlab for all the ΣΔ modulator and IF designs of this work. The coefficients of these designs can be found in [18]. Since all the designs have the same SQNR performance at the output and the fixed-point model performs computations exactly as a VHDL code does (there is one-to-one correspondence of the output bit stream of the Matlab model and the VHDL code), the fixed-point model can be used for judging the complexity of the design with the FOM.

Typical state-of-the-art designs use a combination of system level parameters as shown in Table 1 [5,8,13,31]. The starting point for the ΣΔ modulator design in this work was to design a modulator using a low number of bits at the output and a maximum sampling rate of 5.6Mhz. This resulted in a 3rd order modulator with an oversampling ratio OSR = 64 and a 3 bit quantizer [19].

The maximum modulator NTF gain is H_{inf} = 1.5 as advised in [27]. Since the ΣΔ modulator of the initial design works with OSR = 64, the IF has to increase the input sampling frequency fs_{in} by a factor of 64. To reduce the hardware demands and power consumption, the state-of-the-art DAC designs implement the IF as a multi stage filter [15,24,27]. The IF that is used for the initial ΣΔ modulator design consists of 4 stages and is shown in Fig. 3. In order to investigate the impact of the first stage of the interpolation filter on the FOM there are two versions of the initial design. The details of the first version are provided in [19] and [24]. This design uses an FIR filter as the first stage of the IF and it turns out that the FOM is too high for a hearing aid application. The second version with an IIR filter as the first stage of the IF [11] is inspired by [25,29,36] and is denoted in Table 2 and 3 as the 'Initial design'.

Rather than using the suggestion in [27] that the IF should suppress the frequency images below the ΣΔ modulator NTF, this work uses suppression of around 60 dB for the closest image in the frequency spectrum. This is sufficient to reach the hearing threshold of a normal hearing person to make sure the image is not hearable [24] and [10].

Normally, plots such as the one shown in Fig. 4 are used to understand the system level parameter tradeoffs and their impact on peak SQNR performance [27]. Fig. 4 shows the peak SQNR of the ΣΔ modulator plotted as a function of the OSR parameter for modulator orders of M = 1 to 8. For the case of the 'Initial design', the peak SQNR = 106 dB. Since peak SQNR = 98 dB is sufficient according to the specification, the margin left is used for coarse coefficient quantization to reduce the FOM [20]. The resulting peak SQNR of the modulator is then 98 dB.

For hearing aid application, the power consumption is a critical parameter. But the information about the power consumption is not included in plots such as Fig. 4. Therefore, the tradeoffs of the system level parameters and the power consumption will be investigated in the following sections of this article. To optimize the 'Initial design' with respect to power, various approaches were investigated in this work:

3.1 ΣΔ Modulator Order versus OSR tradeoff

The idea behind the optimization of the ΣΔ modulator and the entire back end compared to the initial design (order = 3, OSR = 64, 3bit, max. NTF gain = 1.5) is to decrease the OSR of the modulator from 64 to 32 and increase its order from 3 to 6. This keeps the ideal peak SQNR = 106 dB so that coefficients can again be coarsely quantized and give resulting SQNR = 98 dB after coefficient quantization with low FOM [20]. By performing these changes in the ΣΔ modulator, the aim is to reduce the switching frequency of the Class D output stage [3] and the DPWM block by 50% as this frequency is the same as the operating frequency of the ΣΔ modulator (see Fig. 1). With the Class D output stage being the main power consumer in the back end system due to switching losses of the output transistors, this will result in considerable power savings. Moreover, these changes will have positive impact on the IF too as oversampling by 32 only is needed compared to oversampling by 64 in the initial design. This saves part of the last stage, performing oversampling by a factor of 2 in the IF of the initial design. Using the FOM of (1), a FOM = 86.8 is calculated for the whole IF, out of which FOM = 36 goes for the part that will be saved by this optimization. This is a reduction in power consumption by more than 40% in the IF. With savings in the PA and the IF, the only block of the back end system that remains to be investigated to see whether or not this optimization approach is reasonable is the ΣΔ modulator. This investigation was performed in [20]. Taking the Matlab fixed-point models and calculating the FOM according to (1) gives the data and FOM in Table 2 and 3, clearly showing that the FOM of the 6^{th} order modulator with OSR = 32 compared to 3rd order modulator with OSR = 64 of the initial design remains approximately the same after the back end system optimization. This can be predicted by looking at Fig. 2. The OSR of the 6th order modulator is halved compared to the 3rd order modulator but the area is doubled. To have lower power consumption in the Class D output stage and have larger area of the ΣΔ modulator is a reasonable tradeoff since the ΣΔ modulator is implemented using only digital standard cells and thus easily scales with technology. The same cannot be said about the Class D output stage. The current consumption of the back end can be calculated as the sum of the currents needed in each block:

$$I_{total} = I_{int} + I_{SDM} + I_{DPWM} + I_{dr} \quad (2)$$

where I_{int} is the current needed in the IF, I_{SDM} is the current of the ΣΔ modulator, I_{DPWM} is the current of the DPWM block and I_{dr} is the current of the Class D PA. It was found that I_{dr} and I_{DPWM} will be reduced by 50% and I_{int} by 41.5% by the optimization. Comparing the 'Section 3.1' design with the 'Initial design' in Table 3, it can be seen that I_{SDM} will remain approximately the same. Thus, in total there are considerable power savings achieved by this optimization approach.

3.2 Very High Order Modulators

The same optimization approach as in Section 3.1 is used again. Again, the OSR of the ΣΔ modulator is halved and the order is doubled compared to the ΣΔ modulator of Section 3.1 (order = 6, OSR = 32, 3bits) while the audio quality is kept within the specification. Thus the OSR is 32/2 = 16 and the order is 6×2 = 12.

To reach the required SQNR at the modulator output and for stability reasons, the number of bits in the quantizer has to be increased from 3 bits to 5 bits. Again, a model using fixed-point arithmetic was built and simulated in Matlab. A comparison with the previous design iterations is shown in Table 2 and Table 3. Table 3 shows that the FOM of the 12th order ΣΔ modulator design is much higher than the FOM of previous design iterations. The reasons are described in detail in [18]. The trade-off between modulator order and OSR is shown graphically in Fig. 5 assuming a ΣΔ modulator with 3 or 5 bits quantization.

In conclusion, further attempts to continue with the approach of trading higher modulator order for lower OSR result in higher FOM. This leads the optimization of the DAC away from the optimum design and parameter choice. The idea of trading lower OSR for higher modulator order to obtain better FOM has its limits and a different approach has to be tried in further optimization steps.

3.3 Using Interpolation Factor of 3

The DAC can be optimized with respect to power by reducing the OSR of the ΣΔ modulator. If the OSR is restricted to be a factor of integer power of two, the only option is to reduce the OSR from 32 down to 16. Such an optimization would reduce the switching frequency of the Class D PA by 50% and thus save 50% of power compared to the design of Section 3.1. Moreover, the power

consumption of the DPWM block would also be reduced by 50% as its operating frequency fs_{DPWM} depends directly on OSR (see Fig. 1). Power consumption would also be saved in the IF because the part of the last stage that increases the frequency from $16\times fs_{in}$ to $32\times fs_{in}$ would not be needed. Table 2 shows that this stage has the highest FOM of all stages for the design of Section 3.1 because it operates at highest frequency and thus consumes the largest amount of power in the IF. The only block of the DAC that remains to be investigated is the ΣΔ modulator. This has been done in [22-23], and the investigation shows that in order to achieve the necessary performance of SQNR and MSA, the maximum gain of NTF, $H_{inf,}$ of the ΣΔ modulator must be increased significantly above the recommendations in [27].

Alternatively, the OSR can be selected to 24 as a compromise between the values of 32 and 16. The resulting ΣΔ modulator design is included in Table 3. In order to achieve OSR = 24, one of the stages of the IF has to perform sample rate increase by a factor of 3. In [22-23], two cases are investigated. The sampling frequency increase by a factor of 3 can be performed either by the first stage of the IF or by the last stage of the IF. The IF options investigated in [22-23] are summarized in Table 4. Table 4 shows that a lower FOM is achieved if the sampling frequency increase is implemented with the first stage as an IIR filter. Further improvement of the FOM of the IF without significantly compromising the performance can be achieved by implementing the second stage of the IF as a CIC (Cascaded Integrator Comb) filter instead of IIR. The IF option with the lowest FOM is then included in Table 3 for total FOM comparison.

3.4 Increasing the Number of Quantizer Bits

With a higher number of bits, the OSR may be further reduced without compromising the peak SQNR. Also, Section 3.3 shows that increase of the maximum NTF gain of the ΣΔ modulator should be investigated as a way to achieve better performance. In this section, these two approaches are combined in order to reduce the OSR of the ΣΔ modulator while keeping its order, peak SQNR and MSA. The maximum clock frequency is defined by the DPWM block to be

$$fs_{DPWM} = 2^{Q}\times \mathrm{OSR}\times fs_{in} \tag{3}$$

For the design of Section 3.1, this results in $fs_{DPWM} = 2^3 \times 32 \times 22.05$ kHz = 5.65 MHz. The same maximum system frequency can be obtained if the number of bits in the ΣΔ modulator quantizer is increased to 5 and the OSR is decreased to 8. In this case, $f_{DPWM} = 2^Q \times$ OSR$\times fs_{in} = 2^5 \times 8 \times 22.05$ kHz = 5.65 MHz. Thus, the power consumption of the DPWM block remains unchanged by such change. Again, since the switching frequency of the Class D stage is the same as the operating frequency of the ΣΔ modulator (see Fig. 1), it would be reduced by 75% compared to the design of Section 3.1 (order = 6, OSR = 32, 3 bit). To have lower power consumption in the Class D output stage and have more bits in the quantizer of the ΣΔ modulator is a reasonable tradeoff since the ΣΔ modulator is completely digital.

However, a 6th order modulator with OSR = 8 and a 5 bit quantizer does not provide the required peak SQNR = 98 dB at the output of the modulator if maximum NTF gain $H_{inf} = 1.5$ is used as recommended in [27]. As in section 3.3, maximum NTF gain H_{inf} can be increased to obtain the required peak SQNR performance [21]. A detailed investigation in [21] shows that a maximum NTF gain $H_{inf} = 5$ is sufficient to achieve the required SQNR, and further increase of this parameter decreases MSA of the ΣΔ modulator below the specification of -1.2 dBFS. Thus, $H_{inf} = 5$ is chosen for this design.

With this modification, the operating frequency of the ΣΔ modulator and thus the switching frequency of the Class D output stage is reduced by a factor of 8 compared to the initial design (order = 3, OSR = 64, 3 bits) and by a factor of 4 compared to the design of Section 3.1 (order = 6, OSR = 32, 3 bits). This will result in considerable power savings. Again, these changes will have a positive impact on the IF too as only an oversampling by 8 is needed compared to oversampling by 64 in [8, 13, 31] and by 32 in Section 3.1. This saves the entire last stage in the IF operating at high frequency. Using the FOM of (1) for the IF of the 'Initial design' and Section 3.1 results in FOM = 86.8 and FOM = 51 respectively (see Table 2). After the reduction of OSR down to 8, the FOM of the IF is 16.3. This is an improvement of hardware/power saving by more that 80% in the IF compared to the 'Initial design' and by more than 65% compared to the design of Section 3.1. With the same maximum clock frequency of the DPWM block as in Section 3.1, and with power savings in the IF and in the Class D output stage, also the ΣΔ modulator must be investigated. This investigation was

performed in [21], and the result is included as the ΣΔ FOM in Table 3. From this, a reduction of the current consumption of the ΣΔ modulator of more than 60% is estimated. Thus, in (2), I_{int}, I_{SDM} and I_{dr} are reduced substantially, resulting in considerable power savings from the proposed optimization approach.

3.5 Relaxing the Specification for Maximum Clock Frequency

In Section 3.1, the Class D PA has been identified as the main power consumer in the back end system. The switching frequency (and thus the power consumption) of the PA directly depends on the OSR of the ΣΔ modulator. Therefore, it makes sense to reduce the OSR in order to save power. In a state-of-the-art work on hearing aid audio back end design, [1] and [9], the Class D PA switching frequency is as low as 96 kHz. In order to achieve such a low Class D PA switching frequency, a hybrid PWM-ΣΔ modulator is used. The disadvantage is that without a clock doubler [1], this back end requires 24 MHz system clock. In this section, it is shown that if the maximum clock frequency specification of 5.6 MHz given in Section 2 is relaxed, the ΣΔ modulator and IF can be designed for OSR = 4 with Q = 8 bits in the quantizer and still deliver SQNR = 98 dB at the ΣΔ modulator output and MSA = -1 dBFS. With this specification, (3) results in $fs_{DPWM} = 2^8 \times 4 \times 22.05$ kHz = 22.6 MHz. Using the same design approach as in Section 3.4 and [21], the maximum NTF gain is found by the simulation to be H_{inf} = 20. Thus, the ΣΔ modulator uses order = 6, OSR = 4 and 8 bits in the quantizer. This results in switching frequency of the PA of $fs_{PA} = OSR \times fs_{in} = 4 \times 22.05$ kHz = 88.2 kHz, which, to the best knowledge of the authors, is the lowest switching frequency of a Class D PA reported in the literature for a digital audio back end.

The disadvantage of this design is that a maximum NTF gain of H_{inf} = 20 allows high frequency content at the input of the ΣΔ modulator quantizer which limits the amplitude at the output of the ΣΔ modulator and thus the power that can be delivered to the load (e.g. the STF DC gain of the ΣΔ modulator drops to -2.3 dB [18]). However, the same problem would be experienced in [1].

Again, a model using fixed-point arithmetic was built and simulated in Matlab. The FOM of the ΣΔ modulator is 36.4 and the FOM of the IF is 11.8. With OSR = 4 and an 8 bit quantizer in the ΣΔ modulator, the operating frequency of the DPWM block is 22.6 MHz. Moreover, with an 8 bit quantizer, the DPWM block becomes complex, and for a poor design, it might consume more power

than the Class D PA itself [9]. An ASIC implementation is needed to properly measure the power consumption of the DPWM block and the Class D PA and arrive at a proper conclusion which of these two blocks would be the main power consumer. Still, the tradeoff of higher number of bits in the quantizer for a lower OSR is of interest as, unlike the Class D PA, the digital blocks of the back end (the IF, the ΣΔ modulator and the DPWM block) scale with technology.

The results of section 3.3 to 3.5 show that a trade-off between OSR and number of bits can be made with a significant effect on the FOM. This is also illustrated in Fig. 6.

The real penalty is the -2.3 dB DC gain of the ΣΔ modulator STF which limits the amount of signal power that can be delivered to the load. This problem is solved by including the feedforward coefficients in the ΣΔ modulator to have STF = 1 (e.g. 0 dB). The feedforward coefficients require additional adders, but, unlike in Section 3.2, with OSR = 4, these adders do not increase the FOM significantly due to the low sampling frequency. Further investigation is left as future work.

3.6 Comparison to State-of-the-art

The design developed in Section 3.5 is compared with other state-of-the-art designs for hearing aid back ends in Table 4. In the end, the aim of all the digital modulator types for Class D PA mentioned in this work is to provide a 1 bit (or 1.5 bit) signal to drive the Class D PA. Ten years back, designers and researchers argued whether to use a pulse width modulation (PWM) to obtain the 1 bit signal or a pulse density modulation (PDM) (e.g. 1 bit ΣΔ modulator). It can be concluded that the state-of-the-art development and research of the past decade show that optimization of both - the PWM modulator and the PDM modulator - leads to a similar result. This result is one of the types of hybrid between ΣΔ modulation and PWM modulation such as this work (ΣΔ modulator combined with DPWM stage) or [1].

One of the disadvantages of the ΣΔ modulation when compared to PWM, often mentioned in the state-of-the-art is the high switching frequency of the Class D PA [1, 3,9]. Table 6 shows that the design proposed in this work is an example that a back end based on digital ΣΔ modulator can be designed with Class D PA

switching frequency comparable (or even lower) than a back end based on digital PWM.

4. Conclusion

The design of a digital audio back end is a task with a considerable number of design variables. An optimization at system level has been investigated in order to determine the optimum configuration of the interpolation filter and the ΣΔ modulator while achieving minimal power consumption for a system. The optimization is performed at system level, and the power consumption is estimated by considering the number and complexity of adders in combination with the clock frequencies for the digital pulse width modulator and the Class D output stage.

For the ΣΔ modulator, a cascade of resonators with feedback (CRFB) is assumed. It is found that both the order of the modulator, the oversampling ratio and the number of bits in the quantizer influence the overall power consumption significantly. This is partly due to the power consumption of the modulator itself, but occurs also because the number of bits and the sampling rate greatly influence the complexity of the interpolation filter. An optimum configuration is found to be a 6th order modulator with an oversampling ratio of 4 and 8 bits in the quantizer. This configuration requires a maximum system clock frequency of 22.6 MHz and results in a switching frequency for the digital output stage of only 88.2 kHz. Also, the interpolation filter becomes very simple. If such a high frequency system clock is not available, a higher oversampling ratio and a lower number of bits in the quantizer is required.

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Fig. 1. Block schematic of a back end used in hearing aid audio application.

Fig. 2. Simplified schematic of N-th order CRFB ΣΔ modulator with Q bit quantizer (in the case of this schematic, N is an odd number. In general, N can be an odd or an even number. In the case N is an even number, the 'g' coefficient would be wrapped around the 1st and 2nd stage of the modulator).

Fig. 3. Multi-stage IF with 4 stages performing sample-rate increase by 64.

Fig. 4. Peak SQNR of the 3 bit ΣΔ modulator output signal as a function of OSR for modulator orders 1 to 8.

Fig. 5. Trading lower OSR for higher order of the ΣΔ modulator. The ΣΔ modulator gives the larger contribution to the combined FOM (blue plot), especially at high ΣΔ modulator orders. The optimum when trading lower OSR for higher order of the ΣΔ modulator is order = 6 and OSR = 32.

Fig. 6. Trading lower OSR for higher number of bits in the ΣΔ modulator quantizer and higher maximum NTF gain.

Table 1. State-of-the-art hearing-aid audio DAC designs and DACs intended for mobile phones using Class D power amplifier.

Table 2. IF FOM comparison

Table 3. Back end design comparison including all the blocks of the system, with completed design in Matlab.

Table 4. IFs using a stage performing interpolation by a factor of 3.

Table 5. Maximum clock defined by the DPWM block

Table 6. Comparison of state-of-the-art hearing aid back end designs.

Figure

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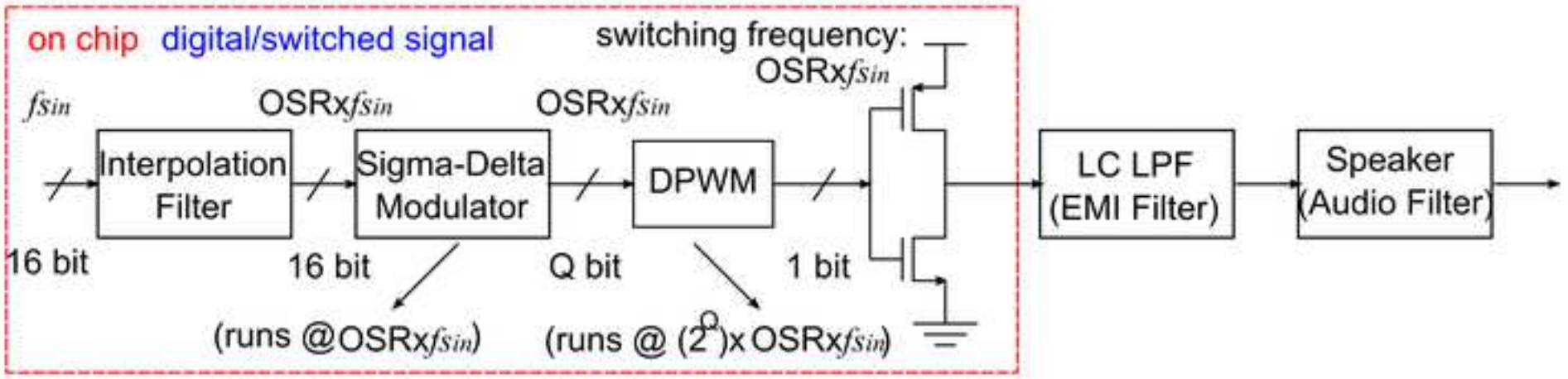

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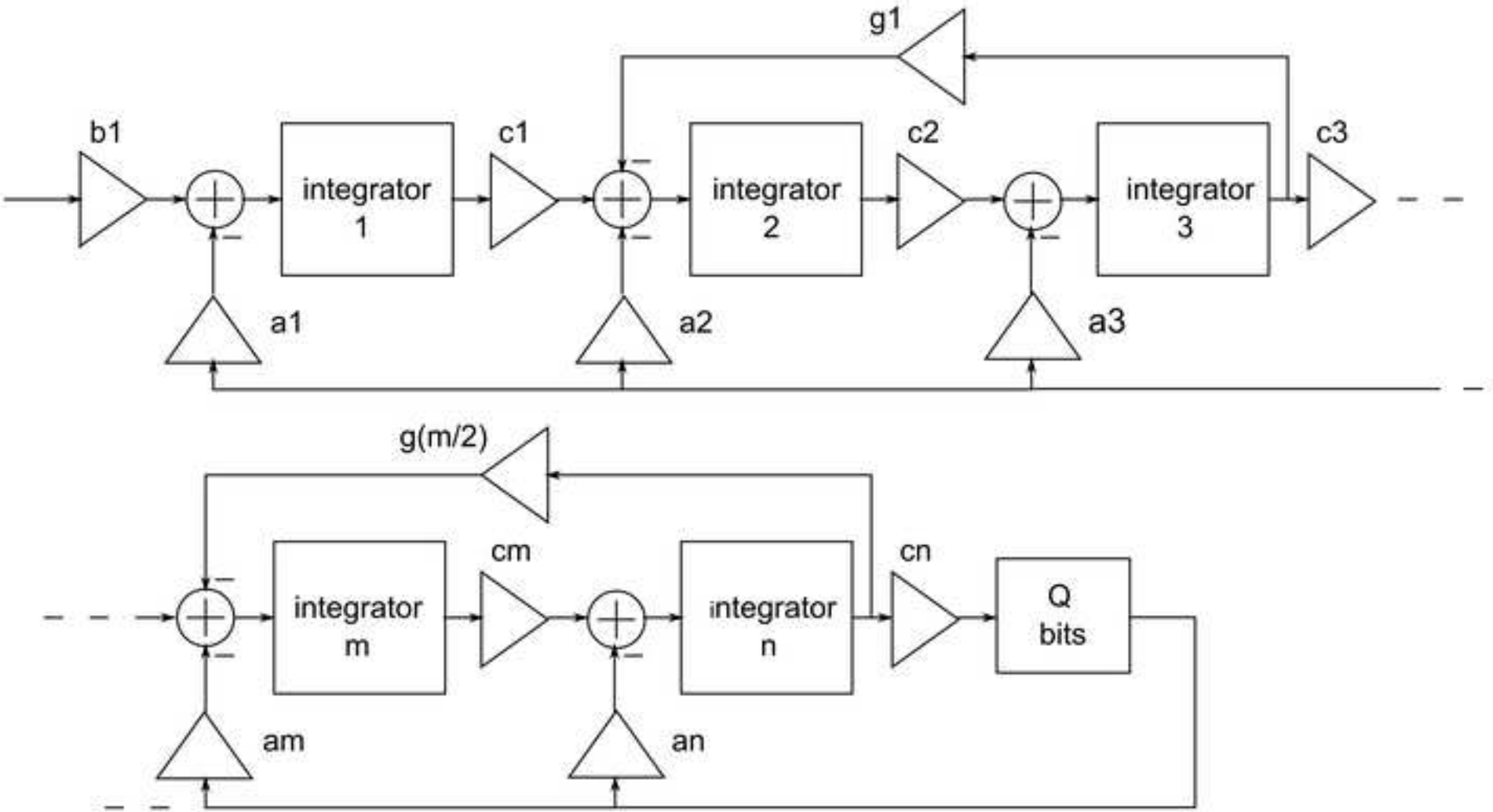

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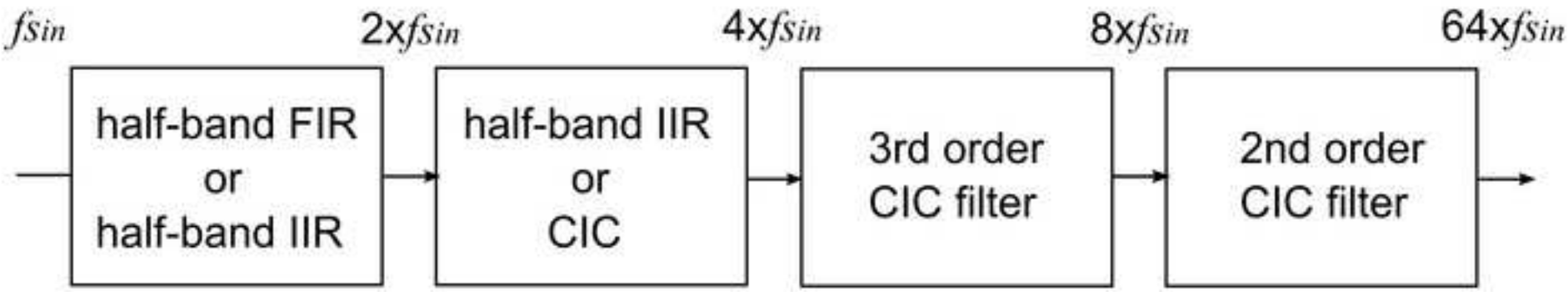

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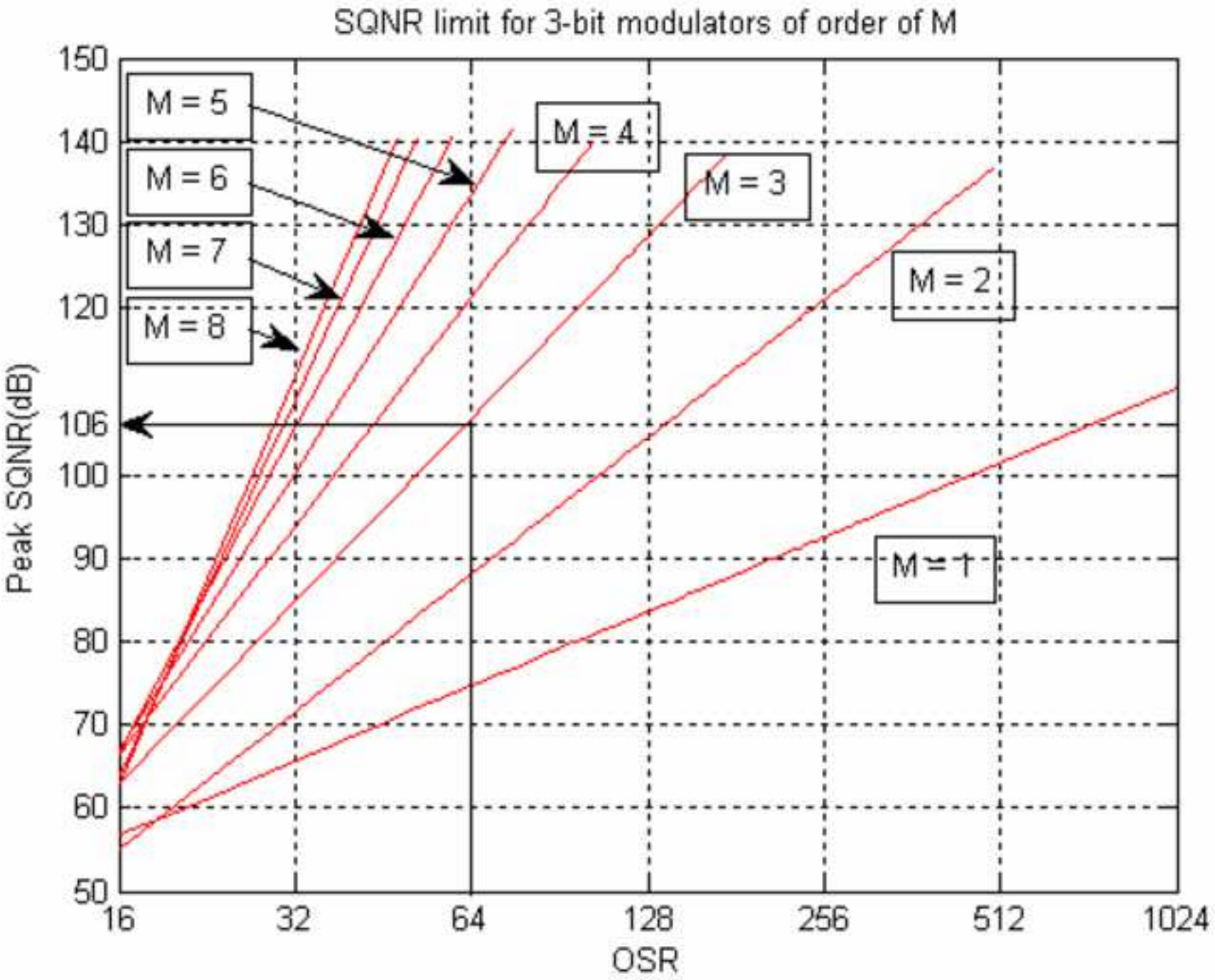

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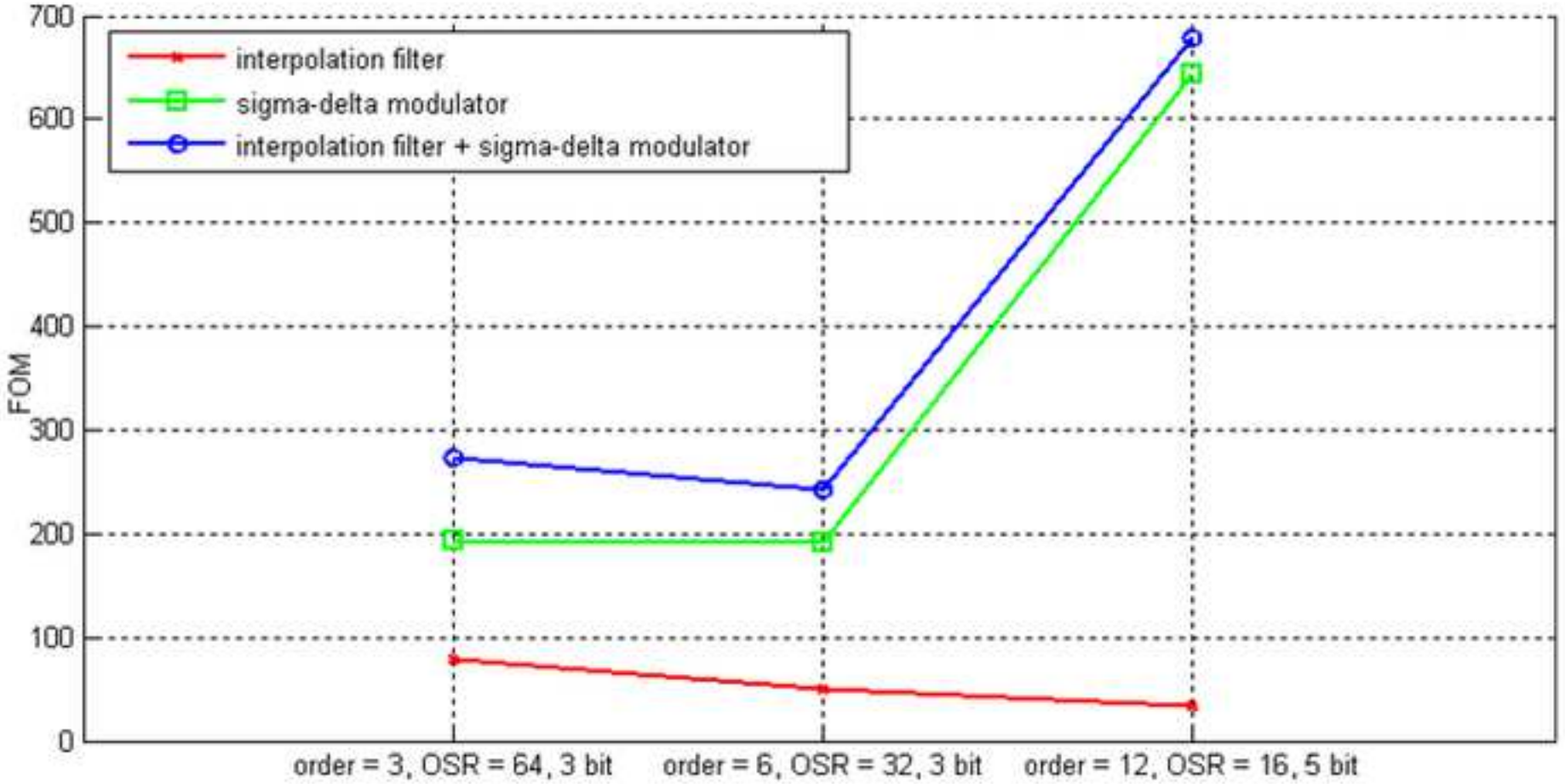

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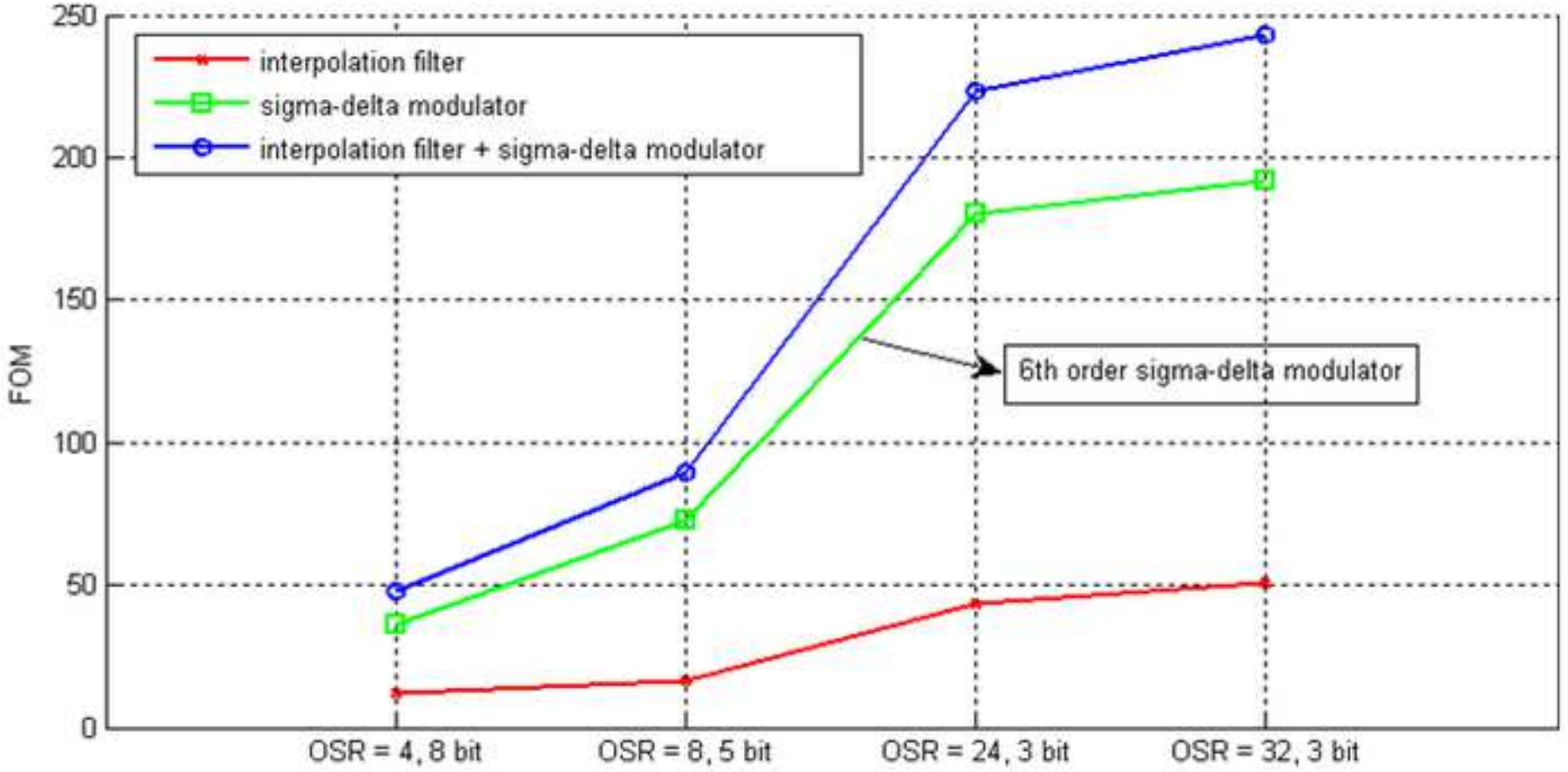

Table 1.

[Ref.] 'year	Application	Vdd [V]	Input signal		Modulator				System output	
			Bits	fs_{in} [kHz]	OSR	Order	Bits	SNDR [dB]	PA	SNDR [dB]
[13] '07	Hearing aid	0.9	16	32	64	4	1	N/A	onchip	79
[8] '09	Mobile phone	1.2	16	44.1	64	3	3	106.7	offchip	90
[5] '09	Mobile phone	3.6	24	48	48	3	7	122	onchip	N/A
[31] '10	Hearing aid	1.8	16	22.05	64	4	1	105.7	onchip	85.6

Table 2.

ΣΔ Modulator	Order = 3, OSR = 64, 3bit (Initial design)				Order = 6, OSR = 32, 3 bit (Section 3A)				Order = 12, OSR = 16, 5 bit (Section 3B)			
	Filter	OSRin	OSR	FOM	Filter	OSRin	OSR	FOM	Filter	OSRin	OSR	FOM
IF stage 1	IIR	fs_{in}	2	9.5	IIR	fs_{in}	2	9.5	IIR	fs_{in}	2	9.5
IF stage 2	IIR	$2\times fs_{in}$	2	7.2	IIR	$2\times fs_{in}$	2	7.2	IIR	$2\times fs_{in}$	2	7.2
IF stage 3	CIC	$4\times fs_{in}$	2	8.6	CIC	$4\times fs_{in}$	2	8.6	CIC	$4\times fs_{in}$	2	8.6
IF stage 4	CIC	$8\times fs_{in}$	8	61.5	CIC	$8\times fs_{in}$	4	25.5	CIC	$8\times fs_{in}$	2	9
IF total			64	86.8			32	51			16	34.3

ΣΔ Modulator	Order = 6, OSR = 24, 3bit (Section 3C)				Order = 6, OSR = 8, 5 bit (Section 3D)				Order = 6, OSR = 4, 8 bit (Section 3E)			
	Filter	OSRin	OSR	FOM	Filter	OSRin	OSR	FOM	Filter	OSRin	OSR	FOM
IF stage 1	IIR	fs_{in}	3	19.9	IIR	fs_{in}	2	9.5	IIR	fs_{in}	2	9.5
IF stage 2	CIC	$3\times fs_{in}$	2	3.4	CIC	$2\times fs_{in}$	2	2.3	CIC	$2\times fs_{in}$	2	2.3
IF stage 3	CIC	$6\times fs_{in}$	2	6.7	CIC	$4\times fs_{in}$	2	4.5	-	-	-	-
IF stage 4	CIC	$12\times fs_{in}$	2	13.5	-	-	-	-	-	-	-	-
IF total			24	43.5			8	16.3			4	11.8

Table 3.

	Design	Initial design	Section 3.1	Section 3.2	Section 3.3	Section 3.4	Section 3.5
ΣΔ Modulator	Order	3	6	12	6	6	6
	OSR	64	32	16	24	8	4
	Quantizer bits	3	3	5	3	5	8
	Max. NTF gain	1.5	1.5	1.5	1.7	5	20
	MSA	-0.5 dBFS	-0.9 dBFS	-1 dBFS	-1.2 dBFS	-1.2 dBFS	-0.1 dBFS
	SNDR @ MSA	98.2 dB	96 dB	97.7 dB	99.3 dB	98.7 dB	98.4 dB
	STF DC gain	-0.16 dB	-0.81 dB	0.61 dB	-0.84 dB	-0.65 dB	0 dB
	Feedforward coeffs.	no	no	yes	no	no	no
	ΣΔ FOM	193	192	644	180	73	36.4
Interpolation filter (IF)	SNDR @ MSA	97.7 dB	101.2 dB	101.2 dB	97.4 dB	98.7 dB	98.2 dB
	pass-band ripple	0.5 dB	0.5 dB	0.5 dB	0.6 dB	0.6 dB	0.6 dB
	1st stage FOM	9.5	9.5	9.5	19.9	9.5	9.5
	2nd stage FOM	7.2	7.2	7.2	3.4	2.3	2.3
	3rd stage FOM	8.6	8.6	8.6	6.7	4.5	-
	4th stage FOM	61.5	25.5	8.3	13.5	-	-
	IF total FOM	86.8	51	33.6	43.5	16.3	11.8
Total FOM (IF + ΣΔ)		273	243	677.6	223.5	89.3	48.2
DPWM clock freq.		11.3 MHz	5.6 MHz	11.3 MHz	4.2 MHz	5.6 MHz	22.6 MHz
PA switching freq.		1.4 MHz	706 kHz	353 kHz	529 kHz	176 kHz	88.2 kHz

Table 4.

ΣΔ Modulator	order = 6, OSR = 24, 3 bit (Section 3.3) (a)				order = 6, OSR = 24, 3 bit (Section 3.3) (b)				order = 6, OSR = 24, 3 bit (Section 3.3) (c)			
	Filter	OSRin	OSR	FOM	Filter	OSRin	OSR	FOM	Filter	OSRin	OSR	FOM
IF stage 1	IIR	fs_{in}	2	9.5	IIR	fs_{in}	3	19.9	IIR	fs_{in}	3	19.9
IF stage 2	IIR	$2\times fs_{in}$	2	7.2	IIR	$3\times fs_{in}$	2	10.8	CIC	$3\times fs_{in}$	2	3.4
IF stage 3	CIC	$4\times fs_{in}$	2	4.5	CIC	$6\times fs_{in}$	2	6.7	CIC	$6\times fs_{in}$	2	6.7
IF stage 4	CIC	$8\times fs_{in}$	3	53	CIC	$12\times fs_{in}$	2	13.5	CIC	$12\times fs_{in}$	2	13.5
IF total			24	74			24	51			24	43.5

Table 5.

Design	ΣΔ Modulator		DPWM clock ($OSR \times 2^{Q} \times 22.05$ kHz)
	OSR	Q bits	
Section 3.1	32	3	5.6 MHz
Section 3.4	8	5	5.6 MHz

Table 6.

[Ref] ‘year	Analog / Digital	Modulator	BW/fs_{in} [kHz]	ΣΔ modulator			System clock	Class D freq.	FB
				order	OSR	bits			
[9] ‘05	Digital	PWM	4/48	-	-	-	100 MHz	96 kHz	no
[12] ‘06	Analog	PWM	-	-	-	-	-	75 kHz	no
[13] ‘07	Digital	ΣΔ	4/32	4	16	1	2 MHz	2 MHz	no
[1] ‘09	Digital	ΣΔ+PWM	8/48	3	2	8	24.6 MHz	96 kHz	no
[17] ‘10	Analog	PWM	-	-	-	-	-	200 kHz	no
[31] ‘10	Digital	ΣΔ	10/22.05	4	64	1	1.28 MHz	1.28 MHz	no
[16] ‘13	Analog +Digital	ΣΔ	-	6	-	3 level	5 MHz	5 MHz	yes
this work	Digital	ΣΔ+PWM	10/22.05	6	4	8	22.6 MHz	88.2 kHz	no