System-Level Test Synthesis for Mixed-Signal Designs

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***Abstract*—Hierarchical test approaches are a must for large designs due to the computational complexity and tight time-to-market requirements. In hierarchical test synthesis, test design is conducted at a subsystem level where the design complexity is manageable. For analog systems, tests are generally designed at the basic block level. This paper outlines a tool for translating basic block-level tests into system-level tests for large analog systems. Computational effectiveness is achieved by the use of high level models and by a pre-analysis of the system to identify feasible translation paths. A method to compute the fault and yield coverages of the resultant system-level tests is also provided in order to evaluate the translation. Experimental results show that test translation reduces design for testability overhead significantly while satisfying coverage requirements.**

***Index Terms*—Mixed-signal systems, parameter tolerances, probabilistic fault coverage, system-level test.**

I. Introduction

While digital test synthesis and associated design for testability (DFT) tools have a long history, manual approaches have been the norm in the analog domain to date. The main reason for this lag in analog test automation is that basic analog building blocks, such as filters, mixers, and DACs, have been traditionally fabricated as easily tested isolated elements. Yet, recent developments in fabrication technology enable integration of mixed-signal systems composed of several functional blocks onto a single chip. Designers and test engineers have accumulated knowledge as to how individual functional blocks need to be tested so as to obtain adequate coverage. However, a system level composition of this test knowledge as a whole is lacking. Instead, costly DFT methods such as test-point insertion are typically utilized in order to achieve direct test access to each functional block.

As the number of analog basic blocks in a system increases, the overhead of providing test access to each block in terms of I/O, area and performance becomes increasingly unpalatable. The highly limited number of analog sources and digitizers in mixed-signal testers poses an additional problem compared to the digital domain. The limitation in the number of analog ports necessitates frequent switching of analog sources and sinks of the tester. Settling times for analog source relays dominate data acquisition times, and the overhead for initialization is nearly five times larger than test application times if the test input is switched each time. Even though frequent switching can be obviated by multiplexing all the test inputs and outputs to the same port, such approaches in turn result in increased complexity and performance overhead.

In order to decrease the burden of additional pins, the use of analog test buses has been proposed. The IEEE 1149.4 mixed-signal test bus standard is aimed at providing I/O access to each basic block with minimal additional pin requirements, and at standardizing the test access to each IC at the board level [1]. However, with gigahertz range designs and high number of functional blocks in today's systems, bus noise and loading still remain as important issues in terms of signal integrity and performance overhead [2], [3].

Test translation schemes aim instead at minimizing DFT overhead by utilizing existing functional signal paths in the system, in order to obtain access to the inputs and outputs of the modules. The complexity of today's mixed-signal systems, and the need for repetitive application of test translation in case of testability-improving system modifications, necessitate automation of such test translation schemes. The presented work is analogous to test translation attempts in the digital domain. However, not much hope can be drawn from a utilization of these methods in the analog domain, as the concept of a single numeric value associated with a particular time point is not sufficient to capture all the relevant intricacies. The proposed approach differs from the previous test generation approaches by the level of abstraction, and in the use of library-based models for basic blocks in the system so as to avoid time consuming circuit simulations. Parameter tolerances are incorporated through a probabilistic approach. Faults used in this methodology are also of a probabilistic and continuous nature as explained in [4].

In this paper, a tool capable of translating basic block tests into system level tests is outlined. This novel tool constitutes a first attempt at test translation for the analog domain and attempts to answer the needs of the increasingly important requirements of the mixed-signal core-based designs. The stringent requirements of ensuring fidelity of all system parameters is obtained through models of block level analog design and test behavior, while computational effectiveness is achieved through early analysis and identification of feasible paths. The tool also computes fault and yield coverages corresponding to each translated test to provide a quantitative evaluation of the system level tests. The paper starts by providing an overview of previous research activities in the analog test area. Section III presents a brief motivation. Fundamental issues in analog test translation are discussed in Section IV. Section V explains the transla-

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tion methods utilized in the tool. The computation of fault and yield coverages is discussed in Section VI. Section VII presents the architecture of the test translation tool. A sample of experimental results on a two channel signal up-conversion system is presented in Section VIII. The paper concludes with an evaluation of the efficacy of the tool.

II. Previous Work

The need for hierarchical test generation stems from the computational complexity of the test generation problem and the complexity of modern very large scale integration designs. The digital domain has encountered these complexity problems and several hierarchical test generation schemes have been proposed, such as [5]–[7]. In [5], the goal is to identify transparent channels in the modules, through which test vectors and output responses of other modules can be propagated. In [6], the goal is to propagate pre-computed test stimuli and output responses of a module by utilizing only transparency and inverse modes of other modules. In [7], system level constraints are identified on modules before module-level test generation is conducted.

Automation of the analog test generation process is still in the research phase. The continuous feature of the analog domain further complicates modeling and detecting faults and failures [8]. An identification of the effects of manufacturing defects on the output response of the circuit under test using dc input stimuli only is attempted in [9]. In this work, effects of process parameter tolerances are modeled through the sensitivity approach. Output signal sensitivities to process parameters are obtained through circuit simulations.

Automated generation of test stimuli is the aim of approaches outlined in [10]–[12], which employ output signal sensitivity, a concept introduced in [13], to circuit parameters. In [11] and [12], test inputs are defined as single tone sinusoidal signals with frequency as an unknown parameter. The frequency at which the sensitivity of the output voltage (voltage gain) of the circuit is highest to a given component is selected to test it. Sensitivities are determined by manual analysis in [11] and by circuit simulations and the use of the adjoint network method in [12].

Evaluation of a given test set by computing determination accuracies of functional parameters is outlined in [13]. The inaccuracy in determining a parameter stems from the dependency of several system parameters and their tolerances. The work outlined in [14] aims at identifying groups of interdependent parameters in the system to evaluate testability and presents a method to locate an error in the parameters. In [15], analog circuitry is assumed to be placed between an ADC and a DAC, and is tested through a signature analysis, where the random, digital input to the DAC has a noise-like effect and the cross correlation between the input and output patterns is used to approximate the impulse response of the analog circuit. An overview of research activities in the analog and mixed-signal test area, which delineates the traditional analog test emphasis on generating test vectors at the basic block level, can be found in [16].

In most of the aforementioned approaches, circuits are studied at resistor-transistor level and most approaches rely on a detailed circuit simulator, such as SPICE. While such test generation approaches can be utilized at the basic block level, as the complexity of systems increases, their computational complexity precludes the utilization of these detailed approaches. Justification of the generated basic block tests at the system level has not, as of yet, received attention commensurate to its increasing importance in the analog domain.

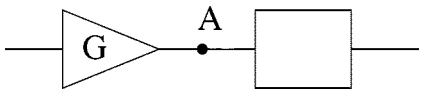


Fig. 1. Effect of parameter tolerances on controllability.

III. Motivation

A technique such as test translation fundamentally attempts to provide an answer to the problem of efficient test generation without resorting to costly and design-altering test additions. It achieves its goals by raising the level of abstraction, thus providing a possible solution in the case of large, complex circuits. Yet its benefits come at the expense, fundamentally, of some information loss that can result in reduced possibilities in setting appropriate controllability and observability characteristics.

Such controllability and observability concerns are not only prevalent, but may possibly be of increased importance in the context of analog test translation. The situation is exacerbated as not only distinct values, but also attributes with complex characteristics need to be modeled in order to ascertain correct primary input and expected primary output behavior. One such characteristic of analog circuits is parameter tolerances. Parameters of a defect-free circuit can vary within a range specified by the system designer. As a result, when only primary inputs are controlled and primary outputs are observed, it is not possible to determine the exact values of signal attributes at any point in the system. As an example, consider a two block system in Fig. 1. Since gain, G, of the amplifier can assume any value in a specified range, the exact value of signal amplitude at point A cannot be determined. Such indeterminism in signals introduces a new and challenging controllability problem in the context of analog test translation. Therefore, parameter tolerances and their resultant effects on controllability and observability of basic blocks must be incorporated into an analog test translation scheme to ensure correctness.

Modeling basic blocks is another important step in signal propagation. Detailed models for basic blocks are often nonlinear. In a test translation scheme, nonlinear models are not desirable as they result in unacceptable computational complexity, especially when backward justification is needed. However, sufficient information must be contained in basic block models in order to relate signals at the inputs and outputs. Moreover, in the test translation context, nonideal responses of a basic block such as noise and spurious response must be included in the models to avoid degeneration of information.

In the analog domain, most tests are defined as a range rather than a single vector. For example, the gain of a filter needs to be tested within the frequency passband and amplitude dynamic range. A subset of a test range may be out of the operation ranges of all possible paths leading to primary inputs and outputs. In case the controllability and observability ranges do not overlap with a test range for a basic block, the test is not translatable to

the system level. A subset of such untranslatable tests may be redundant for the system and therefore may be pruned away. The attributes of a test vector for a particular test must be set within a range where controllability and observability ranges overlap with the given test range for a viable test translation scheme. This requirement necessitates identification of system level constraints on the controllability and observability of a basic block. The problem is further complicated by a variety of factors, such as parameter tolerances and noise, impacting controllability and observability at any point in the system.

IV. Fundamental Issues in Analog Test Translation

In an analog test translation scheme, test input stimuli for a targeted block are propagated from the primary inputs through other functional blocks. Similarly, the test response of the targeted block is propagated through other functional blocks to the primary outputs. Modeling issues related to signals, basic blocks, and parameter tolerances are briefly outlined in [17]. In this section, a detailed explanation of these fundamental concepts related to signal propagation and test translation is provided.

A. Signal Attributes

During propagation, the signals must contain sufficient information to compute circuit parameters. Frequency, amplitude, and phase are basic attributes that define a dynamic analog signal. However, in a realistic signal propagation scheme, additional attributes for signals are needed to model the effects of parameter tolerances, noise, and bias levels as they may degenerate test signals. The following signal attributes are identified to model important aspects of the analog domain.

- *Amplitude:* In most cases, the signal amplitude at the input and output of a basic block is needed for the computation of parameters, such as gain, cutoff frequency, and offset error. One also needs to know the amplitude of a signal that is to be propagated through a basic block to ensure that the operation range of that block is not exceeded.
- *Frequency:* The majority of circuit parameters are defined in the frequency domain. Moreover, the frequency of a signal needs to be known in order to decide on the sampling rate, or to ensure that the operation range of a block on the path is not exceeded.
- *Phase:* Phase information is needed to enable switching between time and frequency domains. In addition, some circuit parameters, such as group delay are given in terms of the phase difference between the input and output signals.
- *DC Level:* The dc component of a signal is important for basic blocks that are input biased and for data converter blocks. In some cases, the dc component of a signal may be up-converted to a dynamic signal, where the dc level becomes the signal amplitude.
- *Noise Floor:* Noise is an undesired, yet always existent attribute of an analog signal. The noise level at any point in the system must be known to determine the minimum detectable signal level and signal-to-noise ratio (SNR).
- *Accuracy:* Inability to identify the exact values of circuit parameters results in indeterminism in signal amplitudes and dc levels. In most cases, the circuit parameters are given in the form of a nominal value, together with some tolerance. In the proposed scheme, the signal attributes are determined using the nominal values of the circuit parameters, together with an accuracy inherited from parameter tolerances.

B. Classification of Block-Level Tests at the System Level

In a test translation context, basic block-level test vectors need to be classified into three categories at the system level so as to enable a reasoning on the methodology of test translation and a pruning away of untranslatable tests.

1) Untranslatable Tests Due to Amplitude and Frequency Range Deficiency: The range defined for a test may completely fall out of the amplitude and frequency operation ranges of all paths leading to primary inputs and outputs. Such tests are untranslatable to the system level through the use of existing signal paths. However, if these tests are within the operation of the targeted basic block, they may be substituted for by a system level test. An example of such redundant tests is the dynamic-range test defined for a basic block. While a certain block may have a wider dynamic range than the path it is serving in, nonetheless, testing for the dynamic range of the path may be adequate in terms of guaranteeing correct operation.

Tests that fall out of the operation range of the signal path indicate a testability problem and are reported by the tool. An example is the test for the cutoff frequency of a filter. If the test range defined for the cutoff frequency is not controllable or observable, no system level test can be applied for testing it.

2) Tests That Are Not Translatable Through Signal Propagation Due to Noise or Inadequate Accuracy: Inaccuracy in basic signal attributes, dc level, frequency and amplitude, are due to tolerances of basic block parameters. Inaccuracy in signal amplitudes, which is caused by tolerances of basic block gains, is the most frequently encountered problem in a test translation scheme that utilizes signal paths through basic blocks. Tests that utilize the ratios of input and output signal amplitudes are targeted at measuring the gain of a basic block. Individual gains of basic blocks with errors within tolerance cannot be determined independent of each other in a signal path. However, a composite variable, the path gain, can be measured with some error. Measuring the path gain alone is not sufficient to ensure correct operation at the edges of the amplitude operation range of the signal path. A large positive gain deviation in a basic block may saturate the succeeding basic block at high signal amplitudes, but may be masked by the gain variations of other basic blocks in the path when signal amplitude is low. Similarly, a large negative gain deviation in a basic block may cause the signal to disappear into the noise floor at low signal amplitudes, but may be masked by gain variations of other basic blocks in the path when the signal amplitude is high. Once the signal is corrupted by saturation or noise, it cannot be recovered in the path. Two additional SNR tests at minimum and maximum signal amplitudes for the path need to be employed to detect such errors.

Signals small in amplitude might disappear in the noise floor if several blocks are cascaded. Such signals are out of the dynamic range of the path and are not of interest during the normal operational mode. However, basic block-level tests may require

signals that are smaller in amplitude than the system noise level. Typical examples are tests that target dynamic range, offset errors and code checks for mixed-signal components, ADCs and DACs. For a subset of such tests, the targeted parameter can be tested at the system level as a composition of individual basic block parameters. Dynamic range is an example of such parameters as its test for a single basic block would require signals close to the noise level of that block. Since cascaded blocks add more noise on top, dynamic range measurement responses are most likely to be buried in the system noise floor. Instead of testing the dynamic range of each block, the SNR of the path with minimum and maximum signal amplitudes might be measured. If the dynamic range of one block deviates from the nominal value, such that it would change the system behavior, the SNR either at the maximum or at the minimum signal level will deviate from the desired value. Maximum and minimum operation signal amplitudes are determined from the given block parameters.

3) Directly Translatable Tests: Among tests targeted for a basic block, a subset which satisfies the following conditions is directly translatable to system level.

- Frequency and amplitude of the desired stimulus and the output response fall into the available signal ranges for the basic block.
- The accuracy of computation is higher than the given threshold.
- Amplitudes of the stimulus and output response are higher than the noise level and within the dynamic range of the path.

If there are multiple paths that can be utilized for translation, the path that results in the highest test accuracy should be selected as the best path to conduct the translation.

C. Controllability and Observability Constraints on Basic Blocks

In the analog domain, test inputs are defined as stimuli satisfying certain conditions. For example, testing the gain of an amplifier requires a test stimulus of an in-band input signal with an amplitude around the midscale. If the test signal attributes are set without the system level knowledge, the resulting test vector may not be propagatable through the neighboring blocks even though there may exist a propagatable test satisfying the same conditions.

During signal propagation, the behavior and parameters of each traversed basic block imposes restrictions on the attainable signal attributes. In forward propagation, such restrictions constitute controllability constraints whereas in backward propagation they constitute observability constraints. As an example, the controllability constraints for $BlockB$ in Fig. 2 are imposed by the operating range and behavior of $BlockA$, whereas constraints for $BlockC$ are determined by $BlocksA$ and B. The whole output range is observable for $BlockC$. However, the output of $BlockB$ is constrained by the operating range and behavior of $BlockC$. Fig. 2 also shows the constraints for $BlockB$.

An analog test translation scheme needs to include a preanalysis that identifies ranges of signals that can be propagated through a path to a basic block in order to reason about controllability and observability constraints. In such an analysis, the noise level at any point in the system also needs to be computed to determine minimum detectable signal levels.

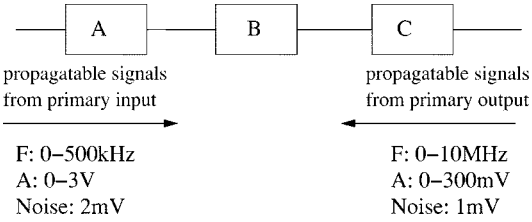
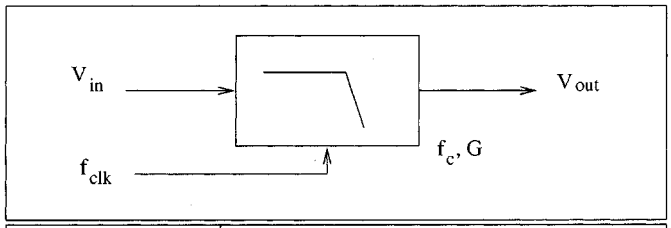


Fig. 2. Observability and controllability constraints.



Model	$V_{out} = G * V_{in}$ if $f < f_c$ and $V_{out} = undefined$ otherwise
Spurious Response	at $k * f_{clk}$
Parameters	$G, f_c, V_{in_{max}}$, $V_{in_{min}}, NF, DR$ and associated tolerances

Fig. 3. Model of a SC low-pass filter.

Such test constraints on the basic blocks may be utilized to evaluate testability of the system and to identify test bottlenecks. If the testability of the system needs to be increased, DFT modifications should concentrate on the identified bottlenecks so that changes to system topology are minimal.

D. Basic Block Models

In order to keep the computational cost manageable during forward and backward propagation, and to ensure applicability of the tool at early design stages, basic block models need to include simple I/O relations that can be expressed with high level parameters.

Even though analog circuits are highly nonlinear, the behavior of most circuits can be expressed with linear relations within a given operating region. The proposed tool takes advantage of this fact and utilizes operating regions of basic blocks for signal propagation. However, the utilized linear I/O relations are approximations of real behavior. Nonlinearity of analog circuits may cause unwanted signals even within the operating range. In order to account for the effect of such nonlinear behavior, the tool keeps track of unwanted signal components such as clock spurs, harmonics or noise during signal propagation. To enable this analysis, expected nonideal behavior of basic blocks also needs to be included in the models.

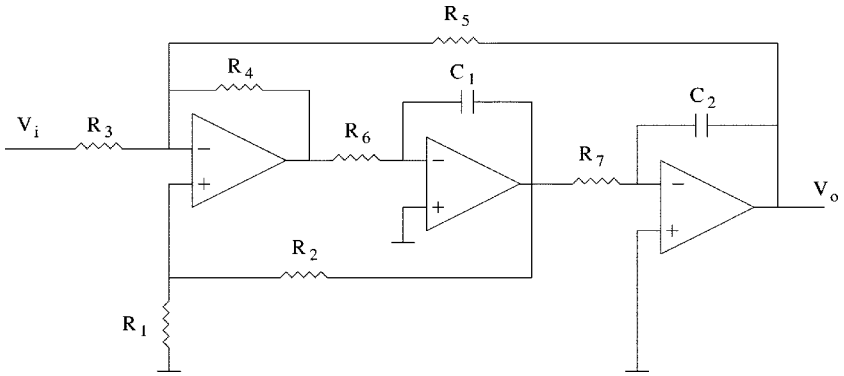


Fig. 4. State variable filter architecture.

In the analog domain, a transition range could exist outside the operating range wherein the circuit behavior is unpredictable. The variations in filter gains are much higher between the cutoff frequency and the stopband region. The output signal attributes are high process and lower level implementation dependent in transition regions. For this reason, the tool assumes that unwanted signal components such as clock spurs or harmonics are not suppressed, whereas desired signals are suppressed in transition regions. This pessimistic approach ensures the correctness of the test translation even though it may result in unnecessary rejection of some tests. As an example, the high level model of a switched capacitor low-pass filter (LPF) is shown in Fig. 3.

Transfer functions are the most commonly used models for basic blocks for behavioral simulation during the design process. A transfer function provides detailed information about the circuit behavior through the complete input spectrum, such as the exact value of gain or phase at any frequency point. However, in the analog domain, the variations in circuit parameters result in variations in the circuit response. A possible way of predicting circuit behavior under parameter variations is to run several circuit simulations with random variations in parameters. The results of Monte Carlo simulations for the state variable filter shown in Fig. 4 is given in Fig. 5(a). Since it is impossible to determine the exact value of circuit components in a high level environment, it is impossible to determine the exact value of gain at a given frequency point. One can only guarantee that the gain of the fault-free filter will be within a given tolerance window as shown in Fig. 5(b). Therefore, some of the information that the transfer function provides will be lost due to process variations.

As another example, consider two different filter responses as given in Figs. 6(a) and 7(a). Monte Carlo simulations which model the effect of parameter variations result in variations in both filter approximations as shown in Figs. 6(b) and 7(b). When the minimum and maximum variations are computed in both responses, the resulting envelopes shown in Figs. 6(c) and 7(c) exhibit similar behavior.

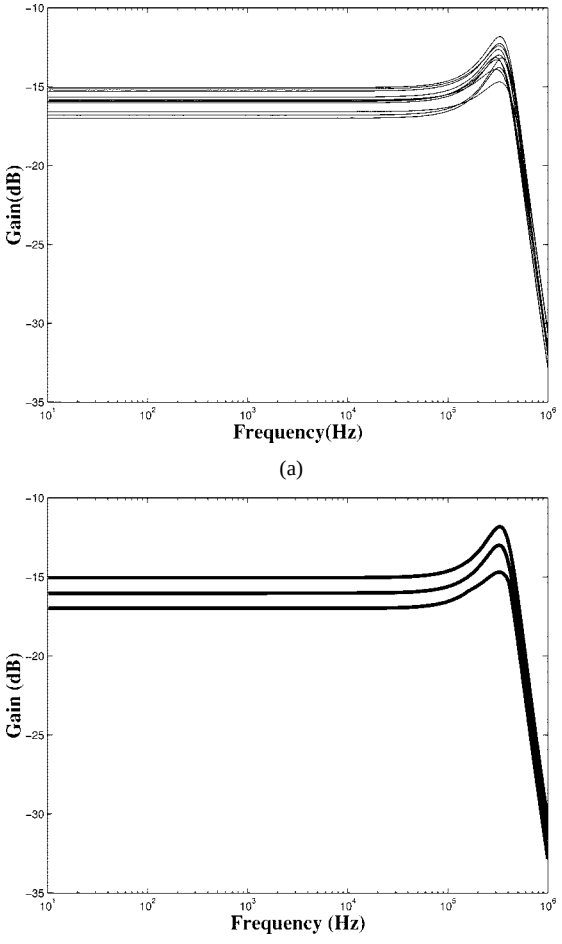
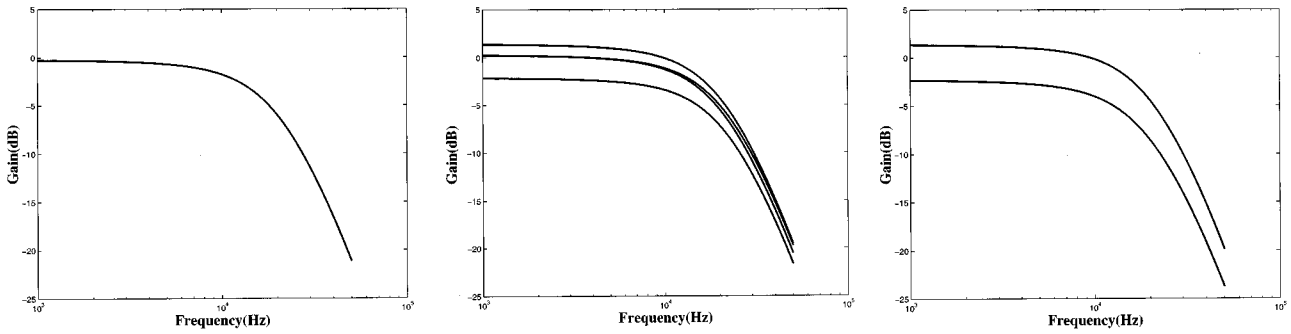


Fig. 5. Response of a state variable filter under process variations. (a) Monte Carlo simulations. (b) Min–Max response.

V. Translation Methods

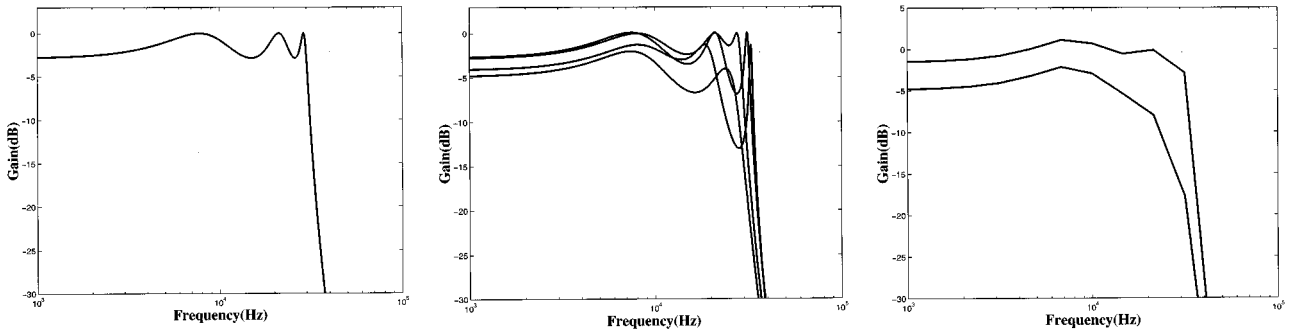
Basic block parameters stem either from direct projections of system level requirements on basic blocks, such as cutoff frequency of a filter, or from partitioning a system level parameter into basic block parameters, such as gain. The tests for the first group need to be conducted individually whereas the tests for partitioned parameters can be composed at the system level.

Basic block parameters that result from partitioning system level parameters can be viewed as a composed parameter. Dynamic range, gain, and noise figure are common examples of such parameters. In a typical system, the tolerances associated with basic block gains are close in value. In such cases, the individual gains of modules cannot be determined with the desired accuracy. However, a composite parameter, the path gain, can be



(a) (b) (c)

Fig. 6. Fourth-order Butterworth response under process variations. (a) Nominal. (b) Monte Carlo simulations. (c) Min–Max response.



(a) (b) (c)

Fig. 7. Fourth-order Chebyshev response under process variations. (a) Nominal. (b) Monte Carlo simulations. (c) Min–Max response.

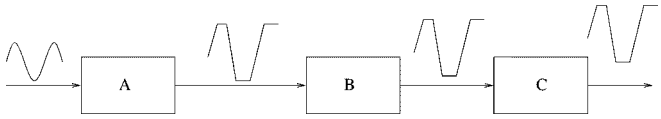


Fig. 8. Gain error resulting in saturation.

measured with a high accuracy. If composed parameters such as path gain are measured, boundary conditions must be checked. Consider a simple system given in Fig. 8. The path gain for this system is typically measured around the mid point of the amplitude operation range. A positive gain error in $BlockA$ may be masked by gain deviation of $BlocksB$ and C. However, when a high signal amplitude is applied, the output of $BlockA$ may saturate $BlockB$. Such a distortion cannot be masked by any other basic block in the path and results in failure. Similarly, a negative gain error in $BlockA$ may be masked by gain deviations of $BlocksB$ and C at the midpoint of the amplitude operation range. In case of small signal amplitudes, this error may result in signal loss, thus resulting in a system failure.

Measurement of signal-to noise ratio at minimum and maximum signal amplitudes is necessary in case the gains of several basic blocks are measured as one composed parameter. In addition to prevention of test point insertion, composition of parameters also decreases the number of required tests in case more than two basic blocks are cascaded.

Translation by Propagation: Some tests are targeted at specific basic block parameters that have no direct or easy-to-extract correspondence at the system level. The third order intercept point (IIP_3) of a mixer, or the cutoff frequency of a filter, are examples of such basic block parameters. In order to test these parameters, required test signals and resultant output responses of corresponding basic blocks must be propagated through other basic blocks in the path.

A. Test Time Impact

If all the tests are translated through signal propagation, the number of system level tests will be the same as the number of block-level tests. Whenever applicable, translation by composition is advantageous in terms of test time since it decreases the number of required tests and keeps the test application methodology constant. This first level of analysis shows that test translation overall cannot result in an increase in test time.

It could be argued that longer signal paths can cause some delay in test application and thus result in longer test times. However, the use of the functional signal path obviates test control delays for the chip and channel switching delays for the tester which are typically much higher than the path delay for analog systems. Savings in test start-up times make up for the path latency; thus, it can be shown, even under this more detailed model, that the overall test time for the system is not increased.

B. Improving Accuracy

Inaccuracy in signal attributes results in error in a measured parameter. In some cases, this inaccuracy can greatly be reduced by adjusting parameter computation with respect to previously computed, more accurate parameters.

As an example, consider the IIP_3 measurement for a mixer in a signal path, as in Fig. 9. When the measurement is converted to system level, IIP_3 of the mixer is computed through measuring the 1st and 3rd order harmonic power at the primary

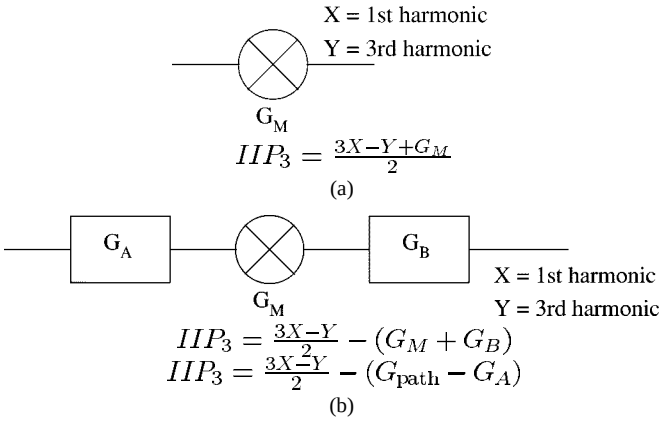


Fig. 9. Improving accuracy of measurements. (a) IIP_3 computation in case of full access. (b) IIP_3 computation in case of no access.

output rather than the output of the mixer. Whereas it is possible to use nominal gains of the mixer and $BlockB$, during the IIP_3 computation, the accuracy of this computation will be affected by the gain tolerances both of $BlockB$ and of the mixer. It is also possible to compute IIP_3 using the path gain and the gain of $BlockA$. Since path gain is a system level parameter, it can be measured with high accuracy and the computation accuracy of IIP_3 is affected by the gain tolerance of $BlockA$ only. Identifying tests that result in increased accuracy helps in reducing yield and fault coverage losses.

VI. Fault and Yield Coverage Computation

Even though the error in parameter computation can be reduced by an adaptive test methodology, as described in the previous section, 100% accuracy cannot be invariably achieved. This error in parameter computation may cause some good parts to fail the test, which results in yield loss, or some bad parts to pass the test, which results in fault coverage loss. If test synthesis results in unacceptable fault coverage and yield loss, a DFT technique needs to be utilized to decrease the amount of error. Therefore, at the end of test translation, yield loss and fault coverage loss need to be computed to evaluate the design in terms of testability.

Testing a parameter consists of computing the parameter and comparing it against pre-defined bounds. Consider the IIP_3 computation in Fig. 9, given by the following equation:

$$IIP_3 = \frac{3X - Y}{2} - (G_{\text{path}} - G_A).$$

The test for this parameter consists of comparing it to a minimum value. If the IIP_3 is higher than this minimum, the part passes the test. The error in the IIP_3 computation stems from the tolerance of G_A. If the actual gain of $BlockA$ is lower than the nominal value, some parts with an unacceptable IIP_3 will be accepted as in Fig. 10. Conversely, if the actual gain of $BlockA$ is higher than its nominal gain, some parts with an acceptable IIP_3 will be rejected.

While translating the test for a particular parameter, additional module-level parameters may be used for computing primary input and output signal attributes. Since the exact values of these parameters are not known, their nominal values are used

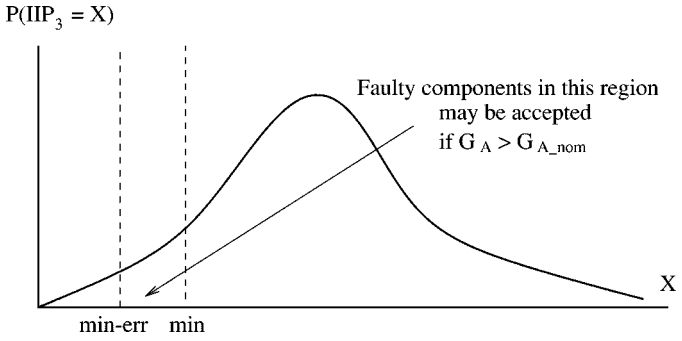


Fig. 10. Impact of error on fault detection.

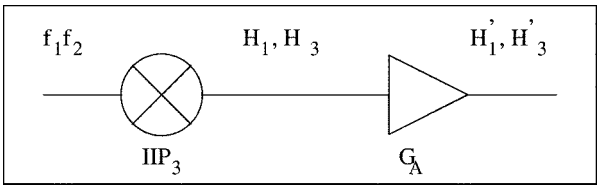


Fig. 11. Propagation of signal attributes.

in the computation and propagation of signal attributes. The difference between the real and nominal values of the parameters that are used in requirement computation causes misclassification. While such misclassification is unavoidable whenever tolerance and noise effects apply, we proceed to show an estimation method for identifying the extent of such misclassification in order to provide an evaluation of the translated tests.

In a test translation scheme, the yield loss (YL) and fault coverage (FC) due to translation can be defined as follows:

$$YL = \frac{\text{number of good circuits that fail the translated test}}{\text{number of good circuits}}$$

$$FC = 1 - \frac{\text{number of faulty circuits that pass the translated test}}{\text{number of faulty circuits}}.$$

The continuity of parameters in the analog domain forces the distinction between good and faulty circuits to be made with respect to the parameter tolerance given by the design specifications.

For fault and yield coverage computation, our goal is to compute the probability of misclassification of the given tests. For a specific parameter, p, a fault-free chip is rejected if the variations in other parameters result in the translated parameter, r, being out of the given tolerance. Therefore the probability of rejecting a chip with a fault free p is

$$\mathcal{P}_R = \frac{\mathcal{P}(p_{\min} < p < p_{\max})}{Y_p} \cdot (\mathcal{P}(r < p_{\min}) + \mathcal{P}(r > p_{\max}))$$

where Y_p is the yield of the parameter, p. Similarly, the probability of accepting a faulty p is

$$\mathcal{P}_A = \frac{\mathcal{P}(p_{\min} > p) + \mathcal{P}(p > p_{\max})}{1 - Y_p} \cdot \mathcal{P}(p_{\min} < r < p_{\max}).$$

In the above equations, P_R corresponds to the loss in yield due to translation (YL), and P_A corresponds to the loss in fault coverage ($1 - FC$).

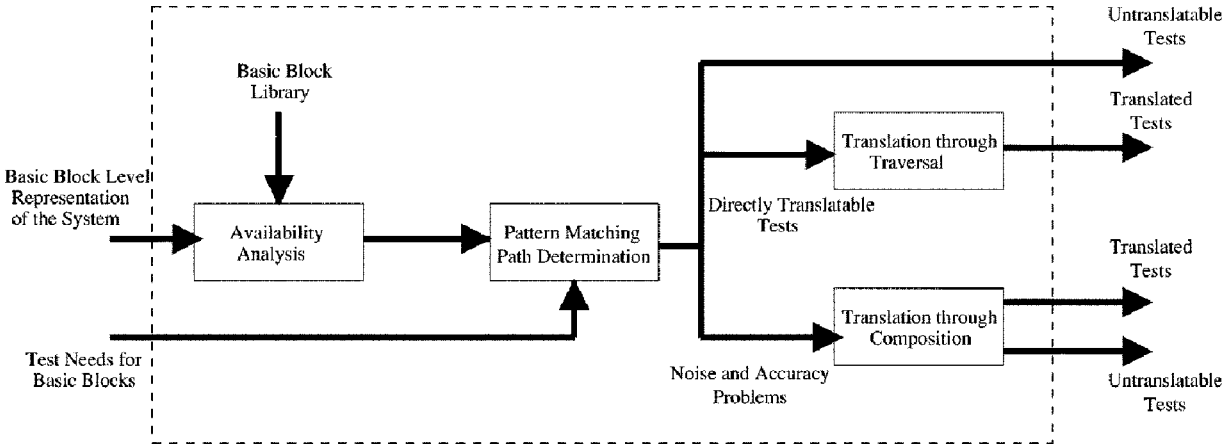


Fig. 12. Implementation overview.

As an example, consider the mixer IIP_3 as in Fig. 11. This parameter is computed at the output of the mixer with

$$IIP_3 = \frac{3H_1 - H_3}{2} - G_M.$$

When this requirement is propagated to the primary output, it becomes

$$IIP_3 = \frac{3H_1' - H_3'}{2} - (G_M + G_A).$$

Due to the variations in G_A and G_M, some faults in IIP_3 will be masked. This loss in fault coverage is given by

$$FC_{\text{Loss}} = \int_0^{\infty} \mathcal{P}(IIP_3 < IIP_{3_{\min}}) \cdot \mathcal{P}(IIP_3' > IIP_{3_{\min}})$$

where IIP_3' denotes the computed IIP_3 at the primary output.

Fault and yield coverages are given by the following relation:

$$FC = 1 - \frac{\int_0^{\infty} \mathcal{P}(IIP_3 = IIP_{3_{\min}} - x) \cdot \mathcal{P}(G > G_{\text{nom}} + x) \cdot dx}{1 - Y_{IIP_3}}$$

$$YC = 1 - \frac{\int_0^{\infty} \mathcal{P}(IIP_3 = IIP_{3_{\min}} + x) \cdot \mathcal{P}(G < G_{\text{nom}} - x) \cdot dx}{Y_{IIP_3}}$$

where:

$$G = G_M + G_A.$$

In the above equations, the third harmonic is assumed to be above the noise level for simplicity. The distribution of the composite parameter, G, is computed out of the given distributions of G_M and G_A

$$\mu_G = \mu_{G_A} + \mu_{G_M}$$
$$\sigma_G = \sigma_{G_A} + \sigma_{G_M}$$

where μ defines the mean and σ the standard deviation of a given distribution.

VII. Implementation Overview

Fig. 12 shows three components that compose the outlined approach and their interactions. The "availability analysis" component consists of computing ranges of signal attributes that can be propagated through the functional blocks in the system, referred to as "available signals." The available signals for a basic block are compared with its test needs by the "pattern matching" engine. The tests for each basic block are classified into three groups: directly translatable tests, untranslatable tests due to range deficiency, and untranslatable tests due to noise or inadequate accuracy. The "test translation" engine computes system level stimuli and output response for directly translatable tests and attempts to identify test sets for tests untranslatable due to noise or inadequate accuracy.

A. Availability Analysis

The availability analysis engine utilizes a forward path traversal algorithm to compute the attributes of signals that can be propagated to the inputs of each basic block through existing paths. At the primary inputs, available signals correspond to the ranges supplied by the tester. If tester information is not available, 100% accuracy and infinite ranges are assumed. As each basic block is traversed, the constraints on signal attributes on its output are computed using the operating range, parameters and the behavior of the basic block. Noise and nonideal behavior such as harmonic components are also included in this analysis. The frequency of the nonideal components will be input frequency dependent and therefore are recorded symbolically.

Backward traversal starts from the primary outputs. The infinite observability range at the primary outputs is degraded as each basic block is traversed, as the observable signals at its input are constrained by the operating range, parameters and behavior. Utilizing this information, signal attribute ranges that can be propagated from the output of each functional block to the primary outputs are computed in addition to harmonic components which are also recorded as observability constraints.

In the analog domain, multiple paths are rarely encountered. However, some components may have control inputs to adjust gain and frequency. These control inputs are modeled as separate paths through the component. If a basic block has multiple paths through it, the ranges for separate paths are recorded

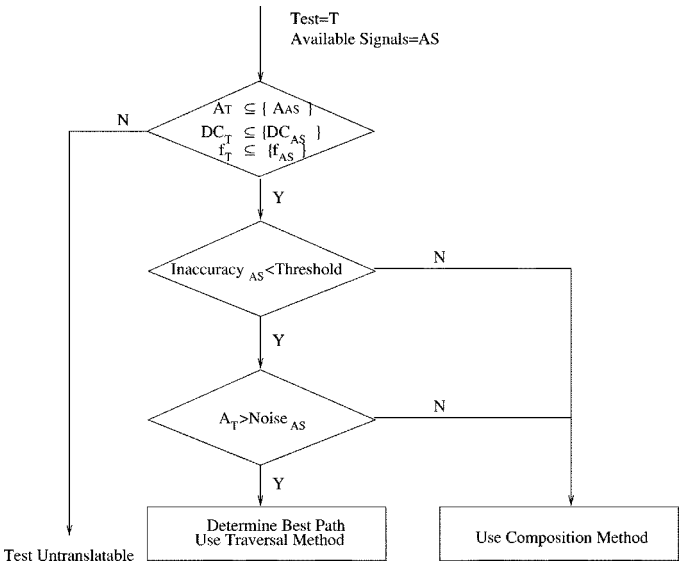


Fig. 13. Classification of tests for a basic block.

together with the path information. This is particularly useful when identifying the test path during translation.

The availability analysis engine traverses all forward and backward paths in the system exactly once, thus providing a computationally effective way of identifying feasible test paths.

B. Test Pattern Matching and Determination of Best Propagation Path

In order to determine the translation method and exclude tests that are untranslatable due to the nature of the analog system, test needs for each basic block are compared with the available signals at its inputs and outputs. The pattern matching engine thus classifies tests for each basic block into three groups. No system level stimuli can be substituted for untranslatable tests due to range deficiency. DFT techniques are required to apply such tests. System level tests corresponding to directly translatable tests are identified by the same path traversal algorithms that are utilized in the availability analysis. If a test can be translated through multiple paths, the path that leads to maximum accuracy is selected.

Inadequate accuracy for translation of some tests is likely to be caused by parameter tolerances, parameter dependencies and noise in the system. Whereas it is not possible to determine the parameters of individual blocks with the required accuracy, it may be possible to combine some tests into a set of system level tests that guarantees correct operation. Such a knowledge-based methodology identifies several parameters such as path gain, dynamic range and noise to be used by the tool. The classification algorithm employed by the pattern matching engine is given in Fig. 13.

C. Translation

The translation engine uses two methods to identify system level tests for the given basic block-level tests. Test stimuli for directly translatable tests are computed by traversing backward the best path identified by the pattern matching engine and utilizing the I/O relations of the basic blocks. Output responses are computed similarly through traversing the identified path forward. For each test, exactly one forward and one backward path need to be traversed.

For directly translatable tests, fault coverage and yield loss need to be computed in order to assess the quality of the translated test. During availability analysis, accuracy of signal attributes is tracked in order to prune away the tests that lead to significantly reduced accuracy. However, this is only a coarse approximation and reflects the worst case scenario. In fact, parameters exhibit a Gaussian-like probability distribution rather than the uniform distribution utilized during availability analysis. In order to enable the computation of fault coverage and yield loss, additional circuit parameters that are used in translation are recorded. The computation of fault coverage and yield loss is the most computationally expensive but essential step in test translation.

A large portion of functional tests requires a measurement of basic block gains. Automated tools that generate tests at the basic block level, such as [12], generate tests targeted at gain measurements at different frequencies. However, as indicated earlier, computation of a basic block gain through a signal path with an error within its tolerance is not possible, because of dependencies of gain parameters in a path. Such gain measurements of individual basic blocks are combined into a set of system level tests that guarantee correct operation throughout the dynamic range. However, the tool also outputs the accuracy of separate basic block gains for evaluation of the translation. The composition of gain and dynamic range tests constitutes an additional method employed by the test translation engine. As composed tests are at the system level, there is no need to compute fault coverage and yield. However, the tool also reports which parameters have composed tests. If the individual parameters of basic blocks need to be tested from a system level perspective, DFT modifications are needed. Therefore, the tool also reports which test translation methodology is utilized for the translated tests.

D. Computational Complexity

In the analog domain, signal paths usually span a large portion of the circuit. Therefore, a large number of traversal paths is unusual. The basic challenge in implementation is keeping track of the necessary information to enable classification of translated tests, path selection and coverage computation. All signal attributes are recorded for controllability and observability at each intermediate point in the system. Noise level is computed for the whole path. A separate list is reserved for harmonic components. During availability analysis, the frequency and the number of tones of the desired test signal are not known. Therefore, harmonics are expressed in terms of input frequencies until the actual test translation step.

Computation of coverages is the most computationally expensive step in the tool. Misclassification probabilities are computed utilizing a Gaussian distribution model for the circuit parameters. 1000 points from each distribution are taken to compute probability levels numerically. A single coverage computation is sufficient for each translated test, resulting in a linear computational complexity of this step in terms of the number of tests.

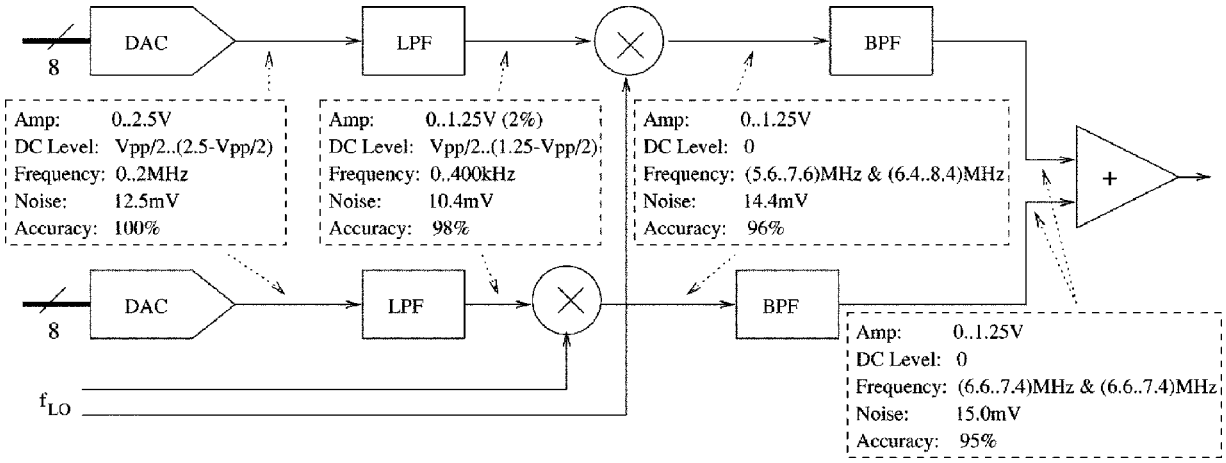


Fig. 14. Mixed-signal up-conversion path.

TABLE I
SET OF PARAMETERS TO BE TESTED

DAC	DNL, Dynamic Range (DR), Full Scale SNR, Offset Error
LPF	$G_{pass-band}, G_{stop-band}, f_c$, DR
Mixer	1-dB Compression Point, IIP_3, NF, G, LO Isolation
BPF	$G_{pass-band}, G_{stop-band}, f_{c_1}, f_{c_2}$, DR
Adder	$G_1, G_2, G_1/G_2, IIP_3$

VIII. EXPERIMENTAL RESULTS

The proposed method has been applied to a typical two-channel up-conversion path shown in Fig. 14, in which two-channel modulated data is up-converted through the mixers that operate 90 degrees out of phase. The outputs are filtered to suppress harmonic components and are added to each other for further up-conversion to the RF frequency that is performed out of this path. Fig. 14 shows the available signals at the inputs of each basic block obtained through availability analysis.

A list of parameters to be tested for each basic block is provided in Table I. Additional parameters for the blocks, such as clock frequencies, and maximum and minimum signal amplitudes, are utilized to conduct the availability analysis. Test vectors for each basic block are determined manually with respect to the functionality and parameters of the basic blocks. In most cases, test vectors are specified as generic vectors with certain properties.

After the availability analysis, the required test stimuli for each block are compared with the available signal ranges at the inputs and outputs of that block. If a match is found, the translation is conducted through paths to the primary input and output. As an example, to measure the third order intercept, (IIP_3), of the mixer, a two-tone waveform is required such that the tones and the third order intermodulation term fall within the passband of the filter with a peak amplitude 3 dB below the full scale. Moreover, with the given specification for the IIP_3, the third order term to be measured must be above the noise floor of the system so that it can be detected at the primary output. Given the availability analysis results, this test can be conducted using the primary input and output only. The input stimulus is propagated through the DAC and the LPF with the same frequency. To prevent any harmonic interference from the second channel, the inputs for that channel are kept at zero.

Table II shows the test requirements for the mixers. The gain test is composed at the system level. The LO Isolation test cannot be translated to the system level through propagation, as the dc level in the signal that propagates through the DAC can exceed 10 mV. Since there is no other component with a similar parameter in the path, the test for this parameter cannot be composed either.

There are 22 module level tests required for each channel, 15 of which were translated to the system level. The remaining seven tests are untranslatable and require application of some DFT technique. The bottlenecks for these untranslatable tests are given in Table III.

For these untranslatable tests, a DFT technique such as test point insertion may need to be applied. In this example, two test points at the outputs of the LPF's are sufficient to translate all the remaining tests.

A. Evaluation of the System Level Tests

In order to evaluate the system level tests, fault and yield coverages corresponding to the propagated tests are computed. Table IV shows the system level tests and corresponding coverages for the mixer parameters. Fault and yield coverages are computed utilizing the probabilistic approach detailed in Section VI. For parameter distributions, the tolerances given to the parameters are assumed to be at the 2σ points, corresponding to a 95% yield. In reality, some parameters have a much better yield which will decrease losses in fault and yield coverages. However, as the distribution data is not available, this pessimistic approach is taken.

The coverage for the IIP_3 is impacted by the gain tolerance and nonlinear distortion of the components in the path. For IIP_3 computation, the path gain and the gain of LPF is used instead of the gains of the BPF and adder. This improves the FC and YC results as the path gain can be measured with a high accuracy and the tolerance of LPF gain is smaller than the combined tolerance of BPF and adder gains. The nonlinear distortion of the mixer is substantially higher compared to the distortion of other components in the path. Therefore, the third order harmonics,

TABLE II
TEST REQUIREMENTS FOR THE MIXER

Parameter	Requirement	Input	Capture	Tol
G	$G = 8$ dB	$f_{in} < 250$kHz, V $< V_{pp} <$ 2V	Amp	2%
IIP_3	$IIP_3 > 6$ dBm	$f_{in_1} < 300$kHz, $f_{in_2} < 300$kHz, $\|2f_{in_1} - f_{in_2}\| < 300$kHz, $V_{in} >$ -12 dBm	FFT	NA
P_{1dB}	$P_{1dB} >$ -3.5 dBm	50mV $< V_{pp} <$ 200mV, f $<$ 200kHz, 300mV pp, f $<$ 200kHz	Amp	NA
NF	$NF <$ 20dB	50mV $< V_{pp} <$ 200mV, f $<$ 200kHz (cold) 50mV $< V_{pp} <$ 200mV, f $<$ 200kHz (hot)	Y-factor	NA
LO Isolation	Isolation $>$ 40 dB	DC $<$ 10mV	FFT	NA

TABLE III
UNTRANSLATABLE TESTS

Test	Bottleneck
Mixer LO Isolation	$A_{response} < Noise$
DAC Offset Error	$A_{response} < Noise$
DAC DNL	$A_{response} < Noise$
LPF G_{sb}	$f \notin f_{available}$
LPF f_c	$f \notin f_{available}$
LPF Group delay	Acc $<$ 1- tol
BPF G_{sb}	$A_{response} < Noise$

TABLE IV
SYSTEM LEVEL TESTS AND CORRESPONDING COVERAGES FOR THE MIXER PARAMETERS

Parameter	Input	FC	YC	Output
IIP_3	700mV (100kHz, 200kHz)	93.2%	96.1%	FFT
P_{1dB}	1Vpp (100kHz) 3Vpp (100kHz)	98.1%	99.3%	Amp
NF	1Vpp (100kHz) (cold) 1Vpp (100kHz) (hot)	95.4%	97.7%	Y-factor

resulting from the filters and the adder in the path, do not degrade the coverage for the mixer IIP_3 measurement.

The coverage for the 1-dB compression point of the mixer, $P_{1\,\mathrm{dB}}$, is impacted only by the nonlinearity in the remaining blocks. Even though the test for this parameter involves gain measurements, the difference between gains measured at two different input powers is dependent mostly on whether the mixer saturates and compresses the gain or not. Therefore, the $P_{1\,\mathrm{dB}}$ measurement for the mixer can be conducted with sufficient accuracy even though the measurement of the mixer gain by itself results in inadequate coverages.

Although the Noise Figure (NF) measurement for the mixer is impacted by the noise added by other components in the path, the NF measurement for the mixer can still be conducted at the system level with adequate accuracy as the mixer is the dominating component in terms of noise figure in the path.

IX. CONCLUSION

The complexity of today's designs and the limitations of test generation methods enforce a hierarchical test generation scheme wherein tests are defined at the basic block level and then translated into system level. In this paper, a tool for translation of basic block-level tests into system level tests is presented. The utilized method aims at applying stimuli at the primary inputs and observing the responses at the primary outputs to avoid test point insertion wherever possible.

To enable the translation, first a set of attributes associated with signals that keep the relevant information is identified. Simplified frequency-domain models for most common basic blocks are defined within an operation range and a translation algorithm that fits with the basic block models and signal attributes is developed. A two-channel signal up-conversion system is utilized to evaluate the efficacy of the tool. The promising experimental results indicate that block-level test translation in the analog domain is not only necessary to meet increasing complexity levels but also sufficiently powerful to meet coverage requirements, and thus constitutes a viable methodology for dealing with the ever increasing mixed-signal test challenge.

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