System-on-a-Package (SOP) Substrate and Module with Digital, RF and Optical Integration

Venky Sundaram*, Rao Tummala, George White, Kyutae Lim, Lixi Wan, Daniel Guidotti, Fuhan Liu, Swapan Bhattacharya, Raj M. Pulugurtha, Isaac Robin Abothu, Ravi Doraiswami, Raghuram V. Pucha, Joy Laskar, Manos Tentzeris, G. K. Chang, Madhavan Swaminathan

Packaging Research Center, Georgia Institute of Technology
* vsunda@ece.gatech.edu, 404-894-9394, 404-894-3842 (Fax)

Abstract

The Packaging Research Center has been developing next generation system-on-a-package (SOP) technology with digital, RF, and optical system integration on a single package. SOP aims to utilize the best of on-chip SOC integration and package integration to achieve highest system performance at the lowest cost. The microminiaturized multifunctional SOP package is highly integrated and fabricated on large area substrates similar to the wafer-to-IC concept. In addition to novel mixed signal design methodologies, SOP research at PRC is targeted at developing enabling technologies for package level integration including ultra-high density wiring, embedded passive components, embedded optical interconnects, wafer level packaging and fine pitch assembly. Several of these enabling technologies have been recently integrated into the first successful system level demonstration of SOP technology using the Intelligent Network Communicator (INC) testbed. This paper reports on the latest INC and SOP testbed results at the PRC and provides an insight into the future SOP integration strategy for convergent microsystems. The focus of this paper is on integration of materials, processes and structures in a single package substrate for System-on-a-Package (SOP) implementation.

I. Introduction

The Packaging Research Center has been developing System on a package (SOP) technology as a high performance, low cost solution for convergent Microsystems [1]. The primary approach to SOP is the integraton of components and functions in the package leading to higher performance, smaller, more reliable full system modules at lower cost. A number of SOP building block technologies have been demonstrated at the PRC and partial integration of digital and RF functionality at the package level has been reported in the past few years [2,3]. A number of SOP technologies have recently been integrated into a mixed signal broadband communication prototype called the Intelligent Network Communicator (INC). The INC testbed integrates digital, RF and optical functionality in a single package fabricated on large area organic substrates using low cost processes.

This paper discusses some of the recent developments in component integration and miniaturization of digital, RF and optical SOP substrates and modules at the PRC. The next section contains a brief description of the INC testbed design, fabrication, assembly and reliability test results. INC system architecture, design and electrical test results are being reported elsewhere [4] and this paper reports on the integration of packaging technologies with specific focus on materials, processes, and reliability.

II. Digital, RF, Optical Integration in a Single Package

The concept of System-On-Package (SOP) can be thought of a conceptual paradigm in which the package, and not the bulky board as the system and the package provides all the system functions in one single module, not as an assemblage of discrete components to be connected together, but as a continuous merging of various integrated thin film technologies to comprise a system solution in a small package. This is accomplished by co-design and fabrication of digital, optical, RF and sensor functions in both IC and the package, thus optimizing functions that are accomplished best at IC level and at package level. An example of a build-up SOP package with integration of three functions is illustrated in Figure 1.

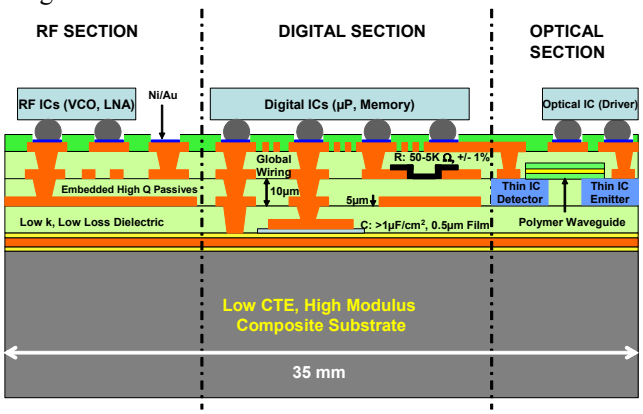

Figure 1: Digital, RF and Optical Function Integration in a Single SOP Package

A typical SOP package will have a size of around 35mm x 35mm and have about four ICs for analog, digital and optical functions. Similar to a wafer-to-IC concept, the SOP packages will be fabricated on 600mm x 600mm panels using low cost processes used in high density organic packages and diced, leading to tremendous size and cost reduction, functionality, performance and reliability.

Digital Integration: The digital functions integrated in the SOP package include (1) impedance matched, multilayer wiring using low loss dielectrics and extremely fine 5µm global wiring; (2) low CTE, high modulus base substrates for multilayer thin film build-up wiring and reliable flip chip assembly without underfill; and (3) embedded high-k thin films with capacitance density >1µF/cm^2 for decoupling and noise suppression below 50mV.

Global Interconnect in Package: With the move to ICs 2cm and larger and multiple GHz speeds, on-chip global

interconnect delay is becoming a serious bottleneck for high speed digital systems. The package wiring provides a unique opportunity to offload global wiring with the availability of 5µm lines and spaces and ultra-thin dielectrics. These dimensions have been demonstrated on low cost build-up FR-4 substrates [5]. Figure 2 illustrates the top view of an extremely fine structure with 5 and 10µm wide lines, 10µm spaces and 4µm copper thickness. Precision photolithography with negative-acting liquid photoresists, glass photomasks and semi additive plating processes were used to form these structures. A novel low cost process for fabricating planar multilayer wiring with stacked microvias without any CMP process has been previously reported [6]. The ultra-fine lines have been integrated with stacked via multilayer structures to route 100-200µm area array pitch flip chip I/Os as shown in Figure 3 [7].

Figure 2. Ultra-fine 5-10 µm Lines and Spaces on Build-up High Tg FR-4.

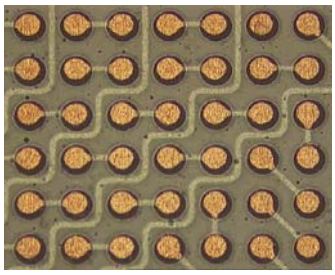

Figure 3. 200µm Pitch Substrate With 15µm Lines and Spaces

Using coplanar transmission lines and 100µm pitch flip chip attach (Figure 4), data rates of 5 GHz have been demonstrated on low loss A-PPE dielectric. The thin films (6-8µm) used as build-up dielectric layers enable the design of 50Ω signals using 10µm lines and spaces, to support 100µm pitch I/Os and global wiring.

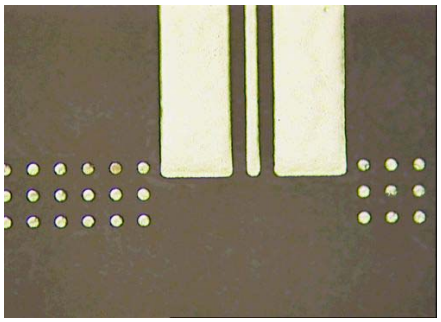

Figure 4. Coplanar Waveguide Transmission Lines and 100µm Pitch I/O pads on A-PPE Dielectric

Low CTE, High Modulus Substrates: Packages for sub-100µm area array pitch, without large capture pads, require substrates with exceptional dimensional stability and high modulus to prevent warpage during multilayer thin film build-up. Novel C-SiC large-area substrates are being developed with CTE as low as 3-5ppm/C and modulus as high as 450GPa [8]. Such a material with exceptional dimensional stability will enable much tighter layer-to-layer registration and higher pad density. The C-SiC substrates have been used to build test vehicles with thin film BCB dielectric (6µm thick) and 30µm thick A-PPE dielectric and 200µm pitch flip chip assembly with and without underfill. The test vehicles with BCB and A-PPE have been subjected to thermal shock testing between -55 and 125°C and no failures were observed after 500 cycles without any underfill [9].

Integration of Decoupling Capacitors: Embedded high-k dielectrics are particularly useful as mid-frequency decoupling capacitors for reducing ground bounce and simultaneous switching noise. Current surface mount discrete components are expected to reach their limit of operation in the few hundred MHz range due to the high lead inductance associated with solder interconnects. Novel polymer-ceramic nanocomposite dielectrics have been used to fabricate thin film capacitors with a thickness of 10µm and ε of 30 to achieve capacitance density up to 10nF/cm^2 [10]. Noise levels below 90mV peak-to-peak have been demonstrated with this approach.

Capacitance densities above 1µF/cm^2 are required to fully integrate SMT capacitors used in mixed signal systems. Nanograined ultrathin crystalline Barium Titanate thin films (Figure 5) were synthesized on laminated titanium foils using a low cost low temperature (<100^{o}C) hydrothermal process [11]. Hydrothermal synthesis of $BaTiO_3$ involves treating a suitable titanium source with Ba^{2+} ions in highly alkaline solution. Titanium foils (12 µm thick) have been used to demonstrate the integration of hydrothermal films on organic packages using lamination and wet etching. The resultant films exhibited a dielectric constant of 350 and loss of 0.07 and a capacitance density greater than 1 µF/cm^2.

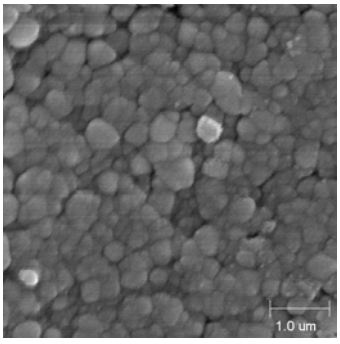

Figure 5. SEM Micrograph of densely packed 0.3µm $BaTiO_3$ grains by Hydrothermal Synthesis

High-K strontium titanate and barium titanate capacitive layers compatible with organic packages have been synthesized using sol-gel process with strontium 2-ethylhexonate and titanium isopropoxide as precursors. Rapid Thermal Process (RTP) was used to lower the process time to 3 minutes as opposed to few hours required for conventional sintering. A capacitance density ranging from 45-700 nF/cm^2 has been achieved by controlling the film thickness from 200 nm to 900 nm and varying the heat treatment conditions. By following the rapid annealing treatment with 1 hr annealing in

N_2 atmosphere, loss was reduced to 0.005 [12]. A SEM micrograph of the thin film cross-section is shown in Fig. 6.

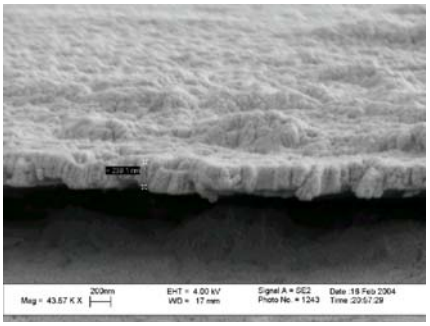

Figure 6: Cross-section of $SrTiO_3$ sol-gel thin film fabricated on nickel foil

RF Integration: The SOP also allows efficient integration of complete passive RF front-end functional building blocks, such as filters and power combiners. Recent development of thin film RF materials and processes makes it possible to integrate RF front ends efficiently in the package to meet stringent wireless communication needs [13-16]. Several low loss and low k polymers including epoxy, A-PPE, Avatrel, BCB, polyimide, and LCP have been evaluated for signal speed and loss at GHz frequencies. The typical electrical properties of these materials are shown in Table 1.

Table 1: Properties of Low Loss Polymers at 1GHz

Thin/Thick Film Dielectric	ε	Tan δ
Polyphenyl Ether (A-PPE)	3.2	0. 005
Liquid Crystal Polymer (LCP)	2.9	<0. 003
Polyimide	3.3-3.5	0. 005
Polynorbornene (Avatrel™)	2.5	<0. 001
Benzocyclobutene (BCB)	2.7	0. 0008

Multilayer build-up wiring has been used to integrate the components found in RF front ends. The 3D design approach using multi-layer topologies leads to high quality components for multi-band, wider-bandwidth and multi-standards in a very compact from factor and low cost. Embedded inductors with Q factors in excess of 150 have been reported [16].

Embedded Filters: Several embedded filters were designed for the SOP process using epoxy materials for the build up layers. The bandpass filter design for C band applications consists of a square patch resonator with inset feed lines, as shown in Figure 7. The inset gaps act as small capacitors and precision lithography with <5% variation in line widths and spaces enables input and output matching. Measurement result shows that bandwidth of 1.5 GHz and a minimum insertion loss of 3 dB at the center frequency of 5.8 GHz.

Integration of Combiners: To overcome the weak coupling at base band and the bandwidth limitation of conventional combiners, coupled lines were implemented as vertical coupling structures in the SOP package as shown in Figure 8.

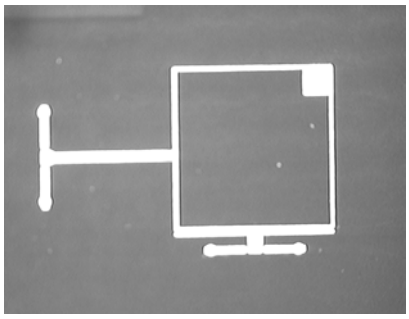

Figure 7. Fabricated Bandpass filter for C-Band using Three Metal Layer Build-up and 75µm microvias.

The output port of the coupled line coupler was used as the input port for the RF signal and the isolation port is shorted to the ground. A ninth order Bessel LPF at the input port for the base band was also integrated to act as a band stop filter for 14 GHz RF signals. An embedded microstrip line was used to interconnect the LPF with the vertical coupling structure. The insertion loss of the RF signal at the output port of the combiner was measured as 1.9dB. The isolation between port 1 and port 2 of the combiner was greater than 10dB in base band and 38dB at 14 Ghz (VNA HP8510). These results satisfy the requirements of 3dB bandwidth of 7 GHz between port 1 and port 3.

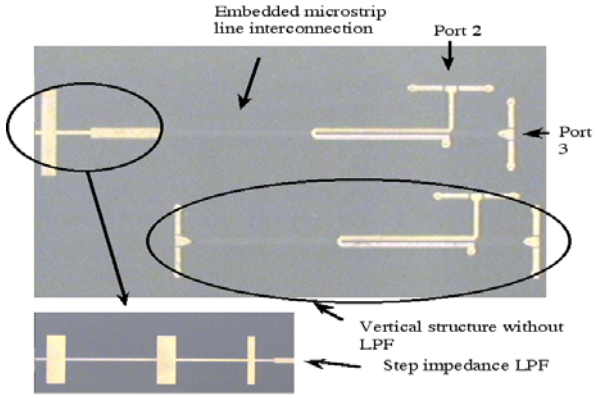

Figure 8. Fabricated Combiner using Multilayer Organic Process

Optical Integration: The objective of optical integration in SOP packages is ultra-high speed chip-to-chip optical interconnects for critical signal paths and clock distribution. Embedded polymer optical waveguides and claddings on FR-4 substrates have been fabricated with embedded thin film MSM photodetectors and commercial pin photodiodes. To minimize waveguide loss, a buffer layer was used to reduce the high frequency roughness and to planarize the undulating surface of typical organic laminates and build-up multilayer wiring. Surface planarity of ±15 nm has been achieved and local roughness as low as 4 nm (Ra) over 500µm has been measured by atomic force microscopy [17].

Embedded Polymer Waveguides: Single mode waveguides on organic packages require waveguide cores of

the order of 9 μm when Δ = 0.02 for indices of refraction around 1.5. Single mode waveguide arrays with 10μm width and spacing have been fabricated using siloxane polymers, with process temperatures below 180°C on high Tg FR-4 substrates, as shown in Figure 9.

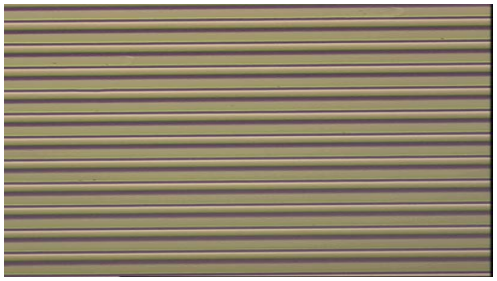

Figure 9. Multi Channel waveguide with 10 μm wide cores on a 20 μm pitch formed on Organic Laminate for single mode applications

Waveguide losses were measured by cut back method for an eight channel S-turn waveguide array having an IPG core 40 μm x 30 μm, 7 μm and 2 μm thick bottom and top cladding, and 1cm radius of curvature. Light was end-coupled into the waveguides using a single mode optical fiber with 8 μm core diameter, and the throughput was collected by a multimode optical fiber having a diameter of 62.5 μm. Measured optical losses were 0.24 dB/cm at 1.322 μm and 0.52 dB/cm at 1.548 μm. The variation in waveguide-to-waveguide insertion loss was ±0.08 dB at 1.32 μm and ±0.11 dB at 1.55 μm.

Embedded Photodetectors: The waveguides have been integrated with embedded thin film I-MSM and commercial PiN photodiode detectors [18]. Figure 10 shows an embedded 10 Gbps PiN detector from AXT. The detector IC was first embedded in a thick polymer, followed by cladding and waveguide core fabrication. Contact pads for electrical connection were opened lithographically in the cladding layers. The detector was evanescently coupled to the waveguide and gratings can be used for greater coupling efficiency.

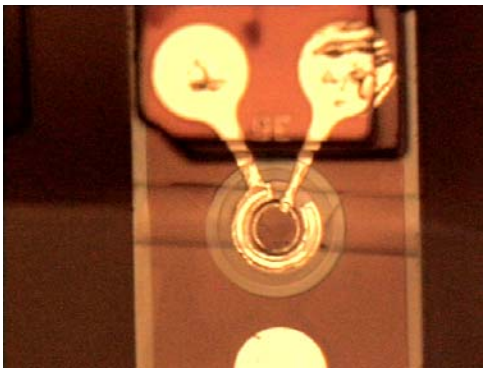

Figure 10. Embedded 10 Gbps PiN detector in polymer waveguide on FR-4 board

Thin films I-MSM detectors, typically 1 μm thick, with a 20 ps response and a large active area have also been embedded in siloxane and BCB waveguides [19]. The MSM thin film detector was attached to thin film gold pads by thermal treatment (Figure 11) and a waveguide core was formed across the detector.

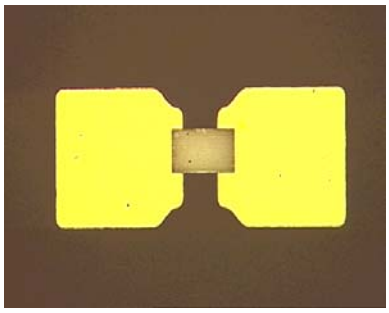

Figure 11. Embedded thin film MSM detector on an FR-4 board prior to waveguide fabrication

III. Intelligent Network Communicator (INC) Module for SOP Demonstration

The previous section described the integration of digital, RF and optical functions in low cost organic substrates. Several of these enabling technologies have been integrated into the first successful system level demonstration of a three function SOP module, referred to as Intelligent Network Communicator (INC). Two implementations of broadband communication INC test vehicles have been designed, fabricated and tested extensively. The INC-1A consisted of a transmit section only, while the INC-1B integrated transmit and receive functions for a complete digital, RF and optical signal path in a compact module.

INC Architecture: In the transmit section, high speed data was input a FPGA (Virtex 50E, Xlinx), programmed as a Digital Signal Processor (DSP). A 16-bit parallel digital signal was serialized by a transceiver (TLK 2701, TI), and fed into the RF block at 2.5Gbps. In the analog block, a 5.8GHz RF signal generated by a VCO was combined with the 2.5Gbps digital data stream, and transferred to the optical block. The combined signal was fed to an external laser driver operating at 10Gbps and 1.55μm wavelength. The optical signal was transmitted through an embedded siloxane waveguide into an external photodetector and converted back to an electrical signal. At the receiver end of the analog block, the electrical signal was separated into the digital and RF signals. The data stream from the RF block was decoded and de-serialized in the transceiver and processed in another FPGA prior to testing. The bandwidth of this testbed was designed at 2.8 Gbps.

Layout: The digital and analog components were located closely on the same organic substrate and the layout was optimized to minimize interference. Split power and ground planes were designed to support three voltage levels: 3.3V, 2.5V and 1.8V. The 2.5V power supply was used by both digital and analog components. To minimize the coupling though a shared power supply, three ferrite beads were used. The split ground plane occupied the second and third metal

layers underneath the signal layer serving digital and RF parts respectively. For high speed transmission, delay lines with 50 ohms impedance zigzag microstrips were designed. Embedded decoupling capacitors were designed to minimize power supply noise and redundancy was ensured with 42 discrete decoupling capacitors in the layout. Single and multi mode optical waveguides were designed as 5 channel U-turns with 50µm width on a 250µm pitch and 4cm length.

INC Testbed Fabrication Process: The INC testbed was designed based on extensive design libraries developed in prior years using the PRC baseline substrate process technology and the INC-1B card measures 4" x 5". The SOP baseline process was developed on 300mm x 300mm panels of high Tg organic laminate using thin film build-up microvia technology. The substrate materials include Hitachi LX-67 and LX-67F low loss laminates, and Nelco N4000-13 high Tg (210°C) laminates of 1mm thickness with 1/4oz copper foil (nominal thickness of 9µm) on each side. The build up dielectric used was negative photoimageable liquid epoxy, Probelec 81/7081^{TM}. This photovia dielectric has a dielectric constant of 3.4 and loss of 0.015 at 1 GHz. The build-up structure consisted of three metal layers with two staggered photovia layers. Embedded capacitors were fabricated using a 10µm thick layer of epoxy-$BaTiO_3$ nanocomposite with capacitance density of 10-15nF/cm^2. After the electrical wiring fabrication, photoimageable polymer waveguides were spin coated and lithographically defined to 50 micron widths. The optical waveguide process consisted of up to seven different layers including planarization, claddings and the core waveguide. The waveguide terminations were end polished to achieve good coupling efficiency from external optical fibers. The polysiloxane was selected based on a cure temperature of 160°C, below the maximum use temperature of both the core laminate and the build-up epoxy dielectric. The ground rules of the process included 25µm lines and spaces, 75-100µm microvias, 10µm thick copper metallization, 30µm dielectric thickness, and 3-8µm thick optical layers. The boards were finished with a layer of Taiyo AUS-5 liquid photoimageable soldermask (15µm thickness) and pad finish used was electroless nickel, immersion gold for assembly of SMT components. Figure 12 shows a fabricated INC-1A substrate and illustrates representative cross-sections of digital, RF and optical blocks.

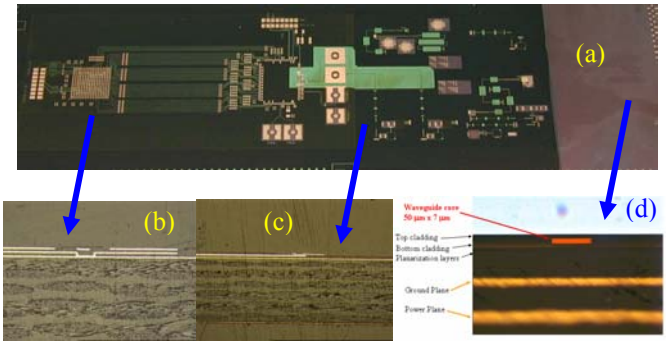

Figure 12. (a) Top View of Fabricated INC-1A Substrate and Cross-sections of (b) Digital Block, (c) RF Combiner, and (c) Optical Waveguides Integrated in INC Module

After initial substrates were fabricated and tested, additional substrates were co-developed with Endicott Interconnect (EI, former IBM Endicott) for reliability testing. *INC Assembly Process:* Digital components including FPGAs, MUX and transceiver chips were then assembled in BGA format and some high value passive components were also assembled using lead-free solder. The chip attach also included wire bonding for VCOs in the RF section. The input and outputs for the Digital and RF signal are through edge connects. The board is reflowed after screen printing solder paste and assembly using a profile having a maximum temperature of 190°C. Care is taken to optimize the profile and the temperature ramp-up is <2°C/min to prevent warpage of the multi-layered substrate. Figure 13 shows the top view of an assembled INC-1B module.

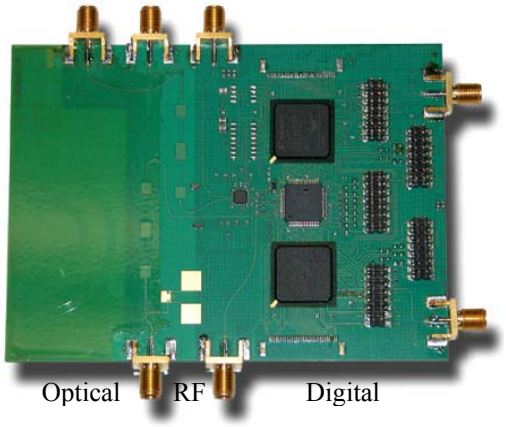

Figure 13. Assembled INC-1B Module with Embedded RF Components and Optical Waveguides

Functional Test: The fully functional SOP modules were subjected to electrical, optical and reliability testing. The results from the first INC testbed met and exceeded the target system specifications for data rates, noise figures and signal integrity. The first implementation of a fully integrated INC system testbed has been demonstrated with digital data rates of 2-3Gbps per channel, 5.8GHz RF signals on board with embedded passives, and 10Gbps optical data rates through embedded waveguides. Figure 14 shows the system link test results and additional details of the INC system design and test can be found elsewhere [4].

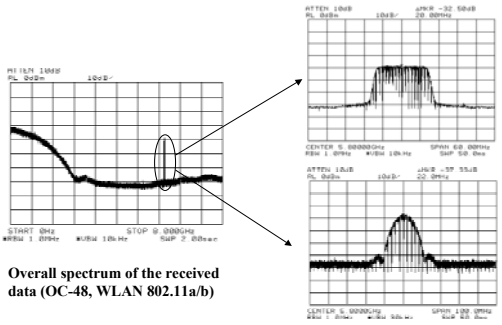

Figure 14. System link test results: frequency response for digital and RF combined signal.

Reliability Testing & Modeling: INC-1A, INC-1B and SOP test vehicles were put through air to air thermal cycling between -55°C to 125°C for 1000 cycles, and temperature/humidity testing at 85°C/85RH for 1000 hours. A 5% change in microvia resistance was observed after 300 cycles. The siloxane polymer waveguides were very stable with <0.02% change in refractive index after 100 cycles.

The reliability research efforts are directed towards understanding various failure mechanisms in digital, RF and Opto functional blocks and their interfaces, and on SOP and system-level reliability. In contrast to the current practices of build-and-test approach the systems approach to reliability at PRC is unique in the following aspects.

1. Use of upfront modeling with physics-based virtual reliability methodology to evaluate various design options and materials selection.
2. Advanced modeling methodologies and algorithms to accommodate materials length scale effects (due to enhanced system integration and miniaturization) in reliability prediction.
3. System-level damage metrics to understand and predict the reliability of digital, RF, and optical functions and their interfaces taking into consideration physics-based failure prediction methodologies as well as statistical aspects.

Using physics-based reliability modeling, prediction of reliability of microvia structures, stress-optical effects in embedded waveguides, and electrical characteristics of embedded capacitors, resistors and inductors has been demonstrated [20, 21].

SOP Integration in INC Testbed: The following technologies have been integrated in the first INC demonstration.

1. Thin film build-up wiring with 20µm lines and spaces and 30µm thick dielectrics
2. Embedded decoupling capacitors using epoxy-BaTiO3 nanocomposite with 10-15nF/cm2 density for noise suppression below 60mV
3. Embedded high Q RF components including inductors (for VCO), combiner and filters for 5.8GHz operation
4. Embedded polymer optical waveguides using siloxane thin films for 10Gbps data rates

IV. Summary

Several enabling technologies for SOP with digital, RF and optical integration in a single, microminiaturized package have been developed. Some of these technologies, including high density interconnect, embedded passives, embedded RF components, and embedded optical waveguides have been integrated into the first demonstration of SOP module using the INC testbed. Future plans for SOP integration include ultra-high density wiring to support 50-100µm pitch flip-chip using low loss dielectrics like BCB; high k, thin film capacitors with >1µF/cm^2 capacitance density; and embedded lasers and photodetectors for optical chip-to-chip interconnects.

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