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Systematic Electromagnetic Interference Filter Design Based on Information From In-Circuit Impedance Measurements

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Abstract—Based on a two-probe measurement approach, the noise source and noise termination impedances of a switched-mode power supply (SMPS) under its normal operating condition are measured. With the accurate noise source and noise termination impedances, an electromagnetic interference (EMI) filter can be optimally designed. A practical example of the design of an EMI filter to comply with a regulatory conducted EMI limit using the proposed procedure is demonstrated and compared with the cases, where the noise source and noise termination impedances are not taken into account, or coarse estimates of them are considered. Although all approaches allow filtered SMPS to pass the regulation limits, designing EMI filters with the accurate noise source and termination impedances leads to optimal component values and avoids overdesign.

Index Terms—Electromagnetic interference (EMI), EMI filter, line impedance stabilization network (LISN), noise source impedance, switched-mode power supply (SMPS).

I. INTRODUCTION

CONDUCTED electromagnetic interference (EMI) is one of the major concerns for switched-mode power supply (SMPS) design [1]. To comply with the international regulatory EMI requirements, an EMI filter is necessary to lower the conducted EMI level of the SMPS below the limit [2]. For filter designs of communications and microwave applications, the source and termination impedances are well defined (usually specified at 50 Ω). However, the impedance levels of the noise source inside an SMPS are not readily available. On the other hand, the impedance level of the filter output, which is conventionally a line impedance stabilization network (LISN), is well defined [3]. One could think of estimating the noise source impedance of an SMPS using the datasheet or typical values, but such estimates are not reliable. In fact, the noise source impedance differs from the nominal impedances of the SMPS and not the SMPS itself (provided by the constructor), due to converter topology, component parasitics, print circuit

board layout, etc. [4]. Also, the complexity of the noise-coupling mechanism makes the generation of adequate models for SMPS a hard task, and engineers prefer to resort to characterization measurements. SMPS may not be easily modeled [5]. Hence, the design of an EMI filter without known noise source impedances can be a challenging task [6]–[8]. In addition, conducted EMI exists in two modes, the common mode (CM) and the differential mode (DM), which further complicates the filter design process as the EMI filter is required to effectively suppress both CM and DM emissions.

Some EMI filter design methods adopt a simplistic approach to design an EMI filter without taking into account the noise source impedance and the noise termination impedance [9]–[11]. Other EMI filter design methods do take into account the noise source and the noise termination impedances but approximate them as purely resistive elements [12], [13]. As there are some approximations being made in these methods, worst case conditions (maximum or minimum possible CM and DM impedances) have to be assumed to design the EMI filter [13]. Although EMI filter design prescriptions of above methods allow the filtered SMPS to pass the regulation limits, they usually lead to overdesign or nonoptimal choice of the filter components. Without precise information (magnitude and phase) of the noise source and noise termination impedances over the frequency range of interest, it is difficult to decide on an appropriate EMI filter configuration and to design an optimal filter for an SMPS to meet a specific conducted EMI limit.

In this paper, based on an in-circuit impedance measurement setup, the amplitude and phase information of the noise source and noise termination impedances can be measured and extracted under actual device operating conditions. The assumption underlying our extraction procedure is that the input impedance of the power supply behaves linearly. This is reasonably true, since, according to [14], the “ON” state impedance prevails during operation and the impedance probing is done by means of small signal perturbations, thus allowing linearization [15]. With the known impedance information, the design limitations of the methods mentioned earlier can be overcome and a systematic EMI filter configuration to achieve the desired filter insertion loss performance becomes possible.

II. IN-CIRCUIT IMPEDANCE MEASUREMENT

In order to extract the noise source impedances, two approaches are available. The passive approach, proposed in [14],

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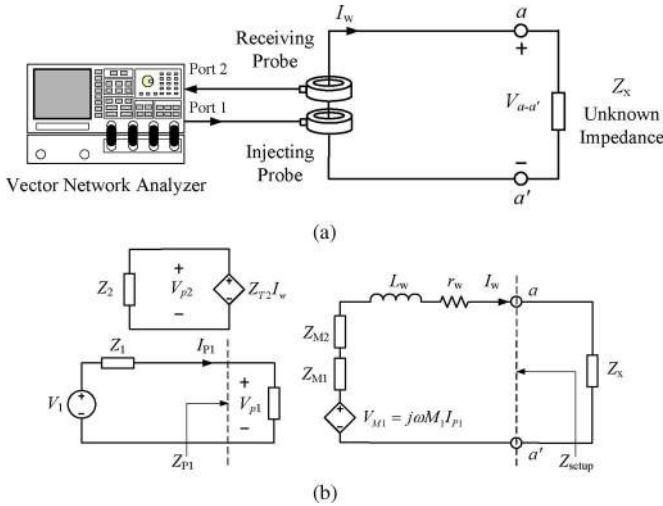


Fig. 1. (a) Conceptual two-probe in-circuit measurement setup. (b) Equivalent circuit of the measurement setup.

amounts to a direct measurements of an SMPS in offline condition; although conceptually simple, this method requires two measurements with a series and shunt load on the SMPS input, and recovers only the impedance magnitude because it relies on insertion loss determination. Alternatively, the active approach, proposed in [16], by means of injecting and receiving current probes extracts the DM and CM impedances of SMPS. However, careful selections of isolating chokes and coupling capacitors are required to measure the noise source impedance. Moreover, only the magnitude of the noise source impedances can be extracted. Unlike the former two-probe method, the proposed method, [17], uses direct clamp-on current probes, and therefore, there is no direct electrical contact to the power line wires between the LISN and the SMPS. Hence, it eliminates the need for the coupling capacitors. Also, no isolating chokes are needed, making the measurement setup simple to implement. With the vector network analyzer (VNA) as a measurement instrument, both the magnitude and the phase information can be extracted accurately.

Fig. 1(a) shows the basic setup to measure the unknown impedance Z_x in a circuit loop, where the loop can be carrying high voltage and/or high current. The setup requires an injecting current probe, a receiving current probe, and a VNA. The two current probes couple to the circuit through inductive couplings without direct connection to the circuit. By transferring the primary circuits of the injecting and receiving probes in the coupled circuit loop, the equivalent circuit of the setup is given in Fig. 1(b). Z_{M1} and Z_{M2} are the equivalent impedances of the injecting and receiving probes, respectively. V_{M1} is the induced signal voltage in the circuit loop from port 1 of the VNA through the injecting probe. L_w and r_w are the loop inductance and resistance, respectively.

Z_x is the impedance to be measured and all the other impedances present in the circuit loop are due to the measurement setup (let us define $Z_{\text{setup}} = Z_{M1} + Z_{M2} + r_w + j\omega L_w$). Also, the current flowing in the circuit loop due to

the injected signal through injecting probe is given by

$$I_w = \frac{V_{M1}}{Z_{\text{setup}} + Z_x}. \quad (1)$$

Finally, the induced voltage in the loop is given by

$$V_{M1} = j\omega M_1 \left(\frac{V_1}{Z_{p1} + Z_1} \right) \quad (2)$$

where M_1 is the mutual inductance between the injecting probe and the coupling loop, V_1 and Z_1 are the Thévenin equivalent voltage source and impedance, respectively, of port 1 of the VNA, and Z_{p1} is the input impedance of the injecting probe.

The received signal at port 2 of the VNA depends on the current I_w measured by the receiving current probe, that is,

$$V_{p2} = Z_{T2} I_w \quad (3)$$

where Z_{T2} is the calibrated transfer impedance of the receiving probe provided by the probe manufacturer.

By substituting (2) and (3) into (1), the unknown impedance to be measured can be determined as follows:

$$Z_x = K \left(\frac{V_{p1}}{V_{p2}} \right) - Z_{\text{setup}} \quad (4)$$

where $K = (j\omega M_1 Z_{T2}) / (Z_{p1})$ is a frequency-dependent coefficient. The premeasurement calibration process to obtain K and Z_{setup} is described in detail in [17] and will not be repeated here.

It is ought to be noted that for the sake of clarity, Fig. 1 is simplified and does not contain the LISN, which powers the active device under test (the SMPS, in our case). The LISN impedance should be considered a part of Z_{setup} without limitations. An additional remark is that the injected signal of the VNA must be much larger than the background noise generated by the device under test in the frequency range of interest so that the background noise does not alter the Z_x value, superimposing on the measured quantities. For most of the low- and medium-power active systems, such a condition can usually be met. However, if the active system is characterized by very high power and generates significant background noise, one could add a power amplifier at the output of port 1 of the VNA to increase the power of the injected signal so that the aforementioned condition could be fulfilled. Moreover, a premeasurement calibration process not properly set jeopardizes the accuracy of the proposed method.

The in-circuit DM and CM impedance measurement setups for the SMPS powered through a LISN are shown in Fig. 2(a) and (b), respectively. The current probes Solar 9144-1N (10 kHz–100 MHz) and the Schaffner CPS-8455 (10 kHz–1000 MHz) are chosen for the noise injection and detection, respectively. The VNA R&S ZVB8 (300 kHz–8 GHz) is selected for the measurement of the voltage ratio, V_{p1}/V_{p2} .

Using the aforementioned setups, the DM and CM impedances of the LISN (acting as a noise sink) and the SMPS (acting as a noise source) can be extracted through the following procedure:

- 1) *Premeasurement calibration process*: The setup impedances ($Z_{\text{setup,DM}}$ and $Z_{\text{setup,CM}}$) and the frequency-dependent coefficients (K_{DM} and K_{CM}) of

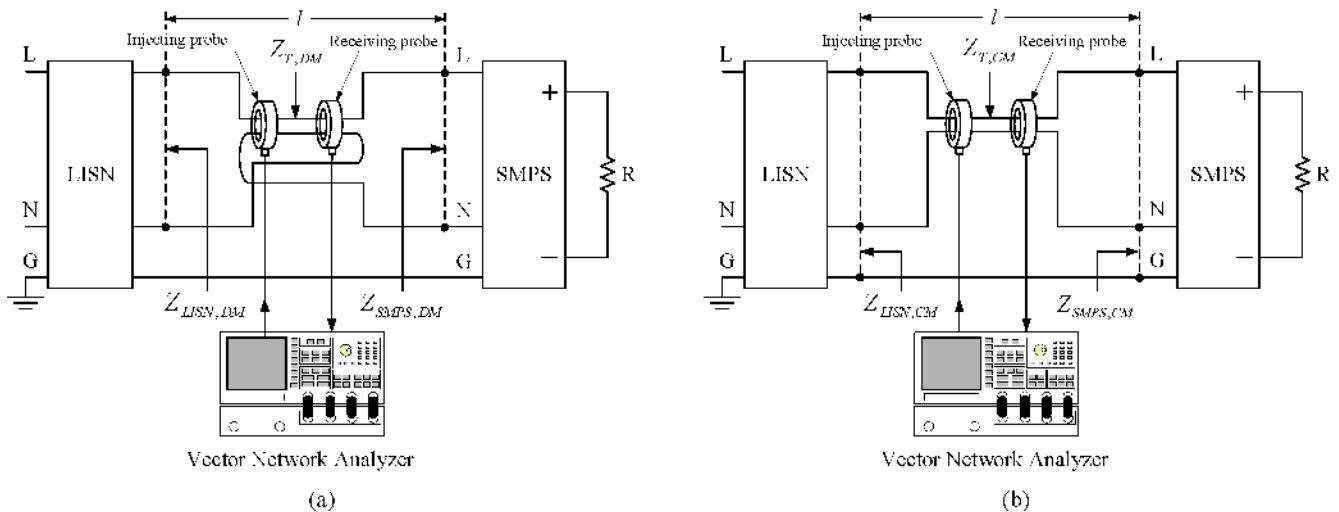


Fig. 2. In-circuit measurement setup. (a) DM. (b) CM.

the measurement setups of Fig. 2(a) and (b) will be determined according to the procedure outlined in [17]. Once these parameters are known, the measurement setup is ready to measure any unknown impedance using (4).

- 2) *Measurement of the noise termination impedances* ($Z_{LISN,DM}$ and $Z_{LISN,CM}$): As the SMPS is powered through the LISN, the LISN acts as a termination for the SMPS noise. To measure the LISN impedance, the SMPS will be replaced by a capacitor, which serves as an ac short at high frequency. In the DM measurement setup, a $1\text{-}\mu\text{F}$ capacitor is connected between line and neutral (nodes L and N in Fig. 2 (a), with SMPS removed). In the CM measurement setup, a $1\text{-}\mu\text{F}$ capacitor is connected between line and ground [nodes L and G in Fig. 2(b)] and another $1\text{-}\mu\text{F}$ capacitor is connected between neutral and ground [nodes N and G in Fig. 2(b)], and the SMPS is removed. The DM and CM impedances of the LISN can be determined by means of (4).
- 3) *Measurement of the noise source impedances* ($Z_{SMPS,DM}$ and $Z_{SMPS,CM}$): In Fig. 2(a) and (b), the measured impedance using the two-probe setup is the total impedance in the circuit loop; we designate such measured impedances as $Z_{T,DM}$ and $Z_{T,CM}$. With the known setup impedance obtained from step 1 and the known LISN impedance from step 2, the respective DM and CM impedances of the noise source (SMPS) can be found as follows:

$$Z_{SMPS,DM} = Z_{T,DM} - Z_{LISN,DM} - Z_{setup,DM} \quad (5)$$

$$Z_{SMPS,CM} = Z_{T,CM} - Z_{LISN,CM} - Z_{setup,CM}. \quad (6)$$

As an example, an SMPS (VTM22WB, 15 W, +12 Vdc/0.75 A, 12 Vdc/0.5 A) is powered through a LISN (Electro-Metrics MIL 5-25/2) and characterized by means of the setups shown in Fig. 2(a) and (b). The DM and CM impedances of the LISN (noise termination) and the SMPS (noise source) are determined with steps 1–3 described earlier.

Since the LISN schematics and component values are provided by the manufacturers or standards, the DM and CM impedances of the LISN can be readily calculated. For comparison purposes, the simulated DM and CM impedances of the LISN using the datasheet provided by manufacturer are also plotted as shown in Fig. 3(a)–(d). Fig. 3(a) and (b) shows the magnitudes and phases of the measured LISN and SMPS impedances for the DM, respectively. Fig. 3(c) and (d) shows the magnitudes and phases of the measured LISN and SMPS impedances for the CM. From Fig. 3(a) and (b), the DM SMPS impedance magnitude is higher than the DM LISN impedance by a few ten Ω to a few hundred Ω , and their phases are spanning approximately 90° over the frequency range of measurements. Fig. 3(c) and (d) shows that the CM SMPS impedance is capacitive and rather regular over the frequency range of measurements, while the CM LISN impedance shows a phase change not easily explainable in terms of elementary circuit equivalents. With the known magnitudes and phases of the noise source (SMPS) and noise termination (LISN) impedances, systematic design of an EMI filter to meet a specific conducted EMI limit becomes possible.

III. EMI FILTER DESIGN PROCEDURE

The same SMPS mentioned earlier is used to guide the reader throughout the design procedure. The intended conducted EMI limit to be met by the SMPS is the CISPR 22 Class B limit [2]. The LISN specified by this standard can only measure the total conducted emissions consisting of the both DM and CM components. Therefore, a discrimination network is needed to separate the DM and CM components from the LISN so that they can be measured separately [18] and used to set the required DM and CM filter insertion losses. The measurement setup is shown in Fig. 4 and a HP 8595E spectrum analyzer (9 kHz–6.5 GHz bandwidth, and peak detection mode) is chosen for the conducted emissions measurement.

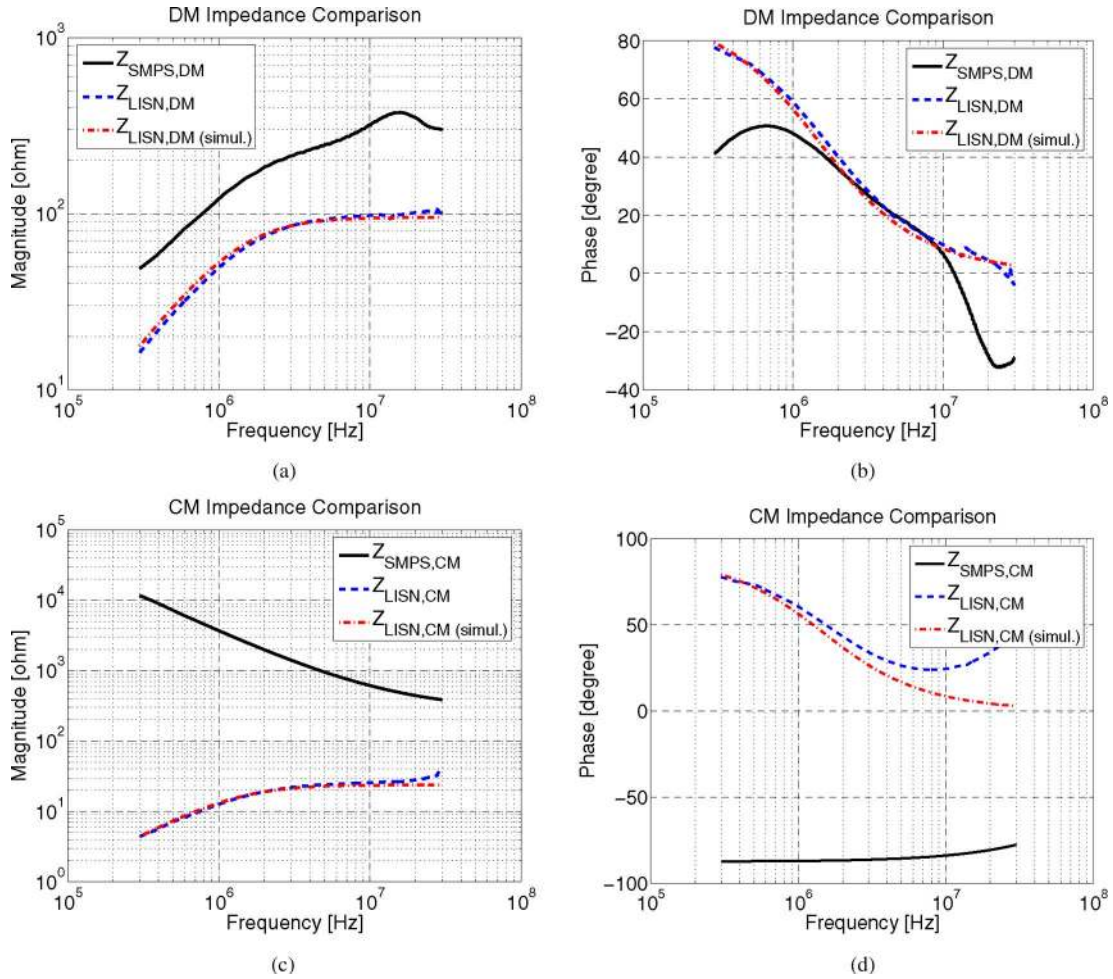


Fig. 3. Measured LISN and SMPS impedances. (a) DM magnitude. (b) DM phase. (c) CM magnitude. (d) CM phase. LISN impedances (dashed lines) are compared with theoretical values (dash-dotted lines) simulated from component values supplied by the manufacturer.

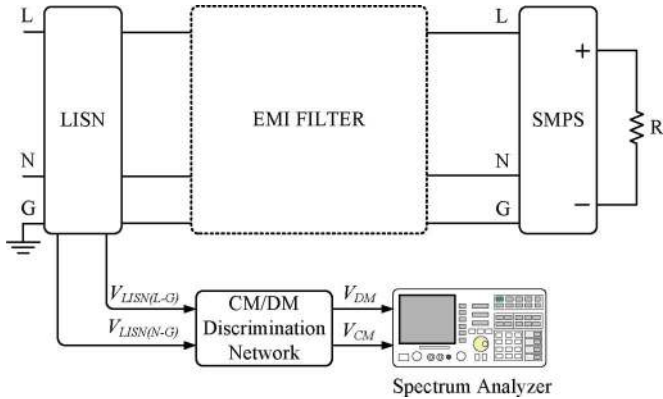


Fig. 4. Conducted EMI measurement scheme with a CM/DM discrimination network.

A. Determination of the Required Insertion Losses

The conducted emissions of the SMPS without the filter are measured with the LISN alone. The line-to-ground and neutral-to-ground conducted emissions are shown in Fig. 5(a) and (b), respectively. Obviously, the SMPS can never meet the required EMI limit without an EMI filter. With the help of the discrimination network proposed in [18], the DM and CM conducted

emissions of the SMPS without the filter are measured and shown in Fig. 5(c) and (d), respectively. Thus, the required DM and CM filter insertion losses can be found by subtracting the standard limit, i.e.,

$$IL_{DM,req} = V_{DM}[dB\mu V] - V_{LIMIT}[dB\mu V] \quad (7)$$

$$IL_{CM,req} = V_{CM}[dB\mu V] - V_{LIMIT}[dB\mu V] \quad (8)$$

where

V_{DM} measured DM emission from SMPS without filter [dB μ V];

V_{CM} measured CM emission from SMPS without filter [dB μ V];

V_{LIMIT} CISPR 22 Class B conducted emission limit [dB μ V].

The required DM and CM filter insertion losses are plotted in Fig. 5(e) and (f), respectively.

B. Selection of the DM/CM Filter Topologies Based on Termination Impedances

The adopted filter configuration is illustrated in Fig. 6(a). The filter is composed of one CM choke (L_C), one DM capacitor (C_X), and two CM capacitors (C_{Y1} and C_{Y2}). Due to the leakage inductance of L_C , it behaves as two DM inductors in the line

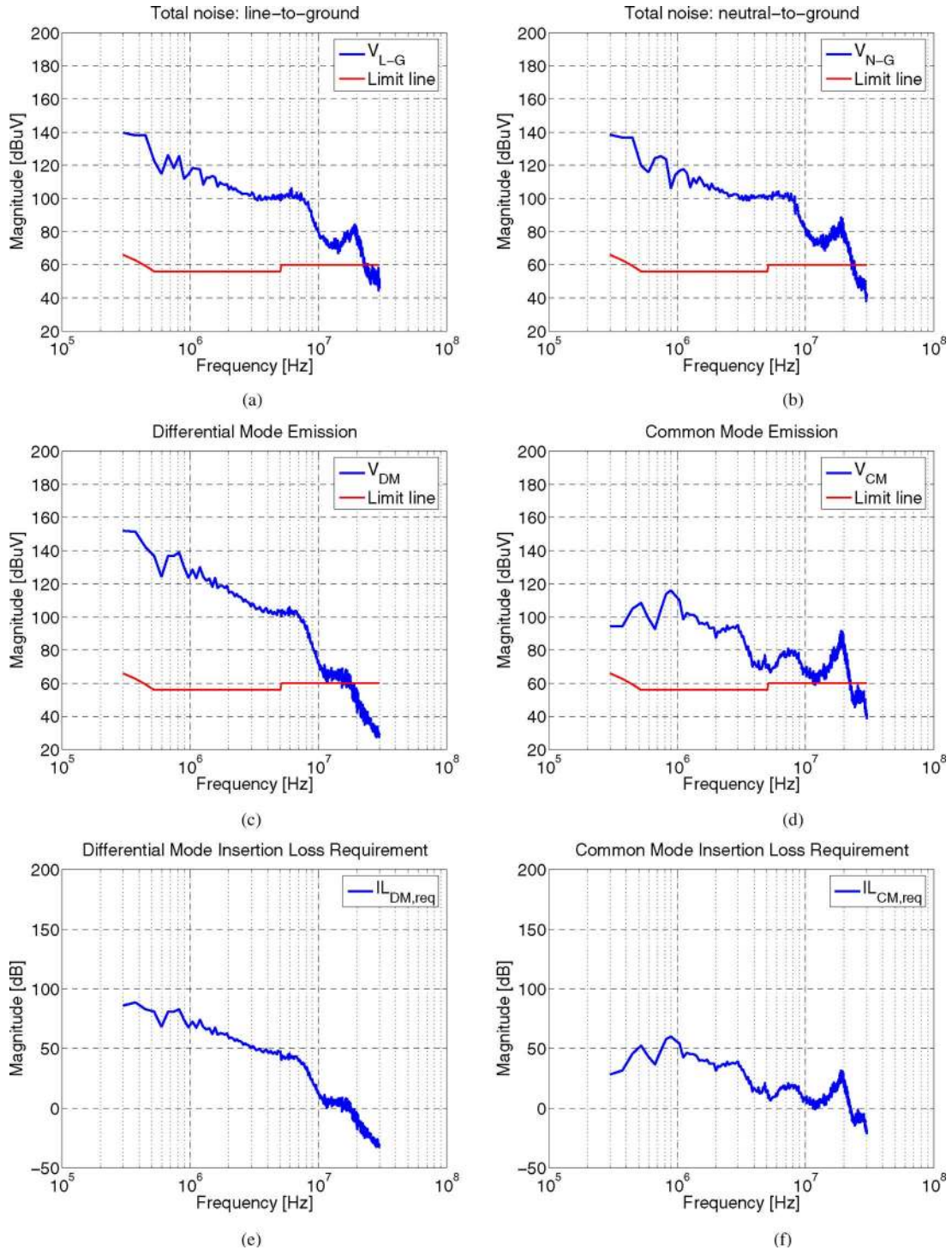


Fig. 5. Measured conducted emissions without filter. (a) Line-to-ground. (b) Neutral-to-ground. (c) DM. (d) CM. (e) Required DM filter insertion loss. (f) Required CM filter insertion loss.

and neutral lines. This particular configuration, with the capacitors facing the SPMS side, is needed in order to achieve the optimal filter attenuation, since the DM and CM SMPS impedances are higher than the corresponding LISN impedances, as clearly documented by Fig. 3(a) and (c). In fact, the capacitor, to be effective, must be placed in parallel to a high impedance and the inductor must be connected in series with a low impedance [19].

The DM and CM interpretation of Fig. 6(a) leads to two separate circuits, shown in Fig. 6(b) and (c), respectively. Fig. 6(b) presents the DM-suppressing part of the filter and is composed of L_{DM} , which is the DM inductance due to L_C , and by C_{XT} , which represents the effective DM capacitor (C_{Y1} and C_{Y2} in series and then in parallel with C_X). Fig. 6(c) presents the CM-suppressing part of the filter and is composed by L_{CM} ,

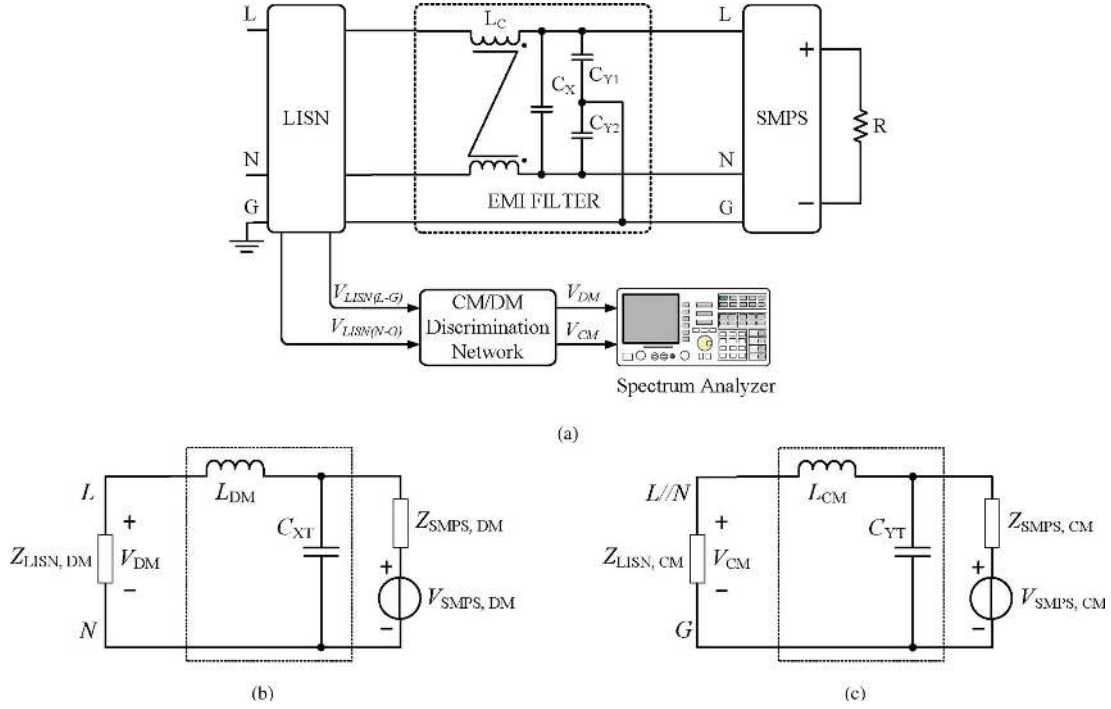


Fig. 6. Conducted EMI measurement in the presence of the EMI filter. (a) Test setup with CM/DM discrimination network. (b) DM part of the filter. (c) CM part of the filter.

which is the CM inductance due to L_C and by C_{YT} , which is the effective CM capacitor (C_{Y1} and C_{Y2} in parallel).

From Fig. 6(b) and (c), the expressions of DM and CM filter insertion losses can be evaluated, according to [7], [8]

$$\begin{aligned} \text{IL}_{\text{DM,estimate}} = 20 \log \left| s^2 \left(\frac{L_{\text{DM}} C_{\text{XT}} Z_{\text{SMPS,DM}}}{Z_{\text{LISN,DM}} + Z_{\text{SMPS,DM}}} \right) \right. \\ \left. + s \left(\frac{L_{\text{DM}} + C_{\text{XT}} Z_{\text{SMPS,DM}} Z_{\text{LISN,DM}}}{Z_{\text{LISN,DM}} + Z_{\text{SMPS,DM}}} \right) + 1 \right| \end{aligned} \quad (9)$$

$$\begin{aligned} \text{IL}_{\text{CM,estimate}} = 20 \log \left| s^2 \left(\frac{L_{\text{CM}} C_{\text{YT}} Z_{\text{SMPS,CM}}}{Z_{\text{LISN,CM}} + Z_{\text{SMPS,CM}}} \right) \right. \\ \left. + s \left(\frac{L_{\text{CM}} + C_{\text{YT}} Z_{\text{SMPS,CM}} Z_{\text{LISN,CM}}}{Z_{\text{LISN,CM}} + Z_{\text{SMPS,CM}}} \right) + 1 \right| \end{aligned} \quad (10)$$

where

$$\begin{aligned} s &= j2\pi f; \\ C_{\text{YT}} &= C_{\text{Y1}} // C_{\text{Y2}} [\text{F}]; \\ C_{\text{XT}} &= C_{\text{X}} / (C_{\text{Y1}} + C_{\text{Y2}}) [\text{F}]; \\ L_{\text{CM}} &\text{CM inductance of CM choke [H]}; \\ L_{\text{DM}} &\text{equivalent DM inductance of CM choke [H]}; \\ Z_{\text{SMPS,DM}} &\text{DM SMPS impedance } [\Omega]; \\ Z_{\text{SMPS,CM}} &\text{CM SMPS impedance } [\Omega]; \\ Z_{\text{LISN,DM}} &\text{DM LISN impedance } [\Omega]; \\ Z_{\text{LISN,CM}} &\text{CM LISN impedance } [\Omega]. \end{aligned}$$

C. CM Filter Design

The CM capacitor is usually constrained by safety requirements, e.g., EN 60335-1 Class I portable, and therefore, the

maximum capacitance connected to ground cannot exceed about 4700 pF on each phase for 250-Vac 50-Hz mains [20]. Hence, C_{Y1} and C_{Y2} are chosen to be 1000 pF each. Substituting the known CM LISN and SMPS impedances and the chosen CM capacitors into (10) and assuming that the filter elements are ideal, the required CM inductance that could provide the CM filter insertion loss higher than $\text{IL}_{\text{CM,req}}$, indicated in Fig. 5(f), is about 2 mH. Hence, two 1000-pF Class Y capacitors and a 2-mH CM choke (NEC/TOKIN SC-02-10A1) are chosen for the CM filter.

In contrast, the conventional design approach [9], not taking into account the SMPS and LISN impedances, leads to a possible overdesign of the CM choke. The $\text{IL}_{\text{CM,req}}$ needs to be 38.85 dB at 300 kHz; the cutoff frequency can be found by $f_{c,CM} = f_{n,CM} / 10^{\text{IL}_{\text{CM,req}} / \beta} = 32 \text{ kHz}$, where $f_{n,CM} = 300 \text{ kHz}$ and $\beta = 40 \text{ dB/decade}$ [10], [21]. Substituting the value $C_{YT} = 2000 \text{ pF}$ and $f_{c,CM} = 32 \text{ kHz}$ into the cutoff frequency formula ($f_{c,CM} = 1 / 2\pi \sqrt{L_{\text{CM}} C_{YT}}$) of the simplistic approach, the needed CM choke results in about 12 mH, which is six times larger than the inductance required by the proposed method. The reduction of the inductance value introduced by the proposed method corresponds to significant size and weight savings.

D. DM Filter Design

Once the CM choke and the CM capacitors are selected, we proceed with the DM filter design. For the DM capacitor, since there is no safety issue, the value can be chosen to be as large as possible but larger capacitors usually exhibit a low self-resonant frequency [22]. Substituting the known DM LISN and SMPS impedances and the measured DM inductance of the CM choke ($L_{\text{DM}} = 17.6 \mu\text{H}$) into (9), the required

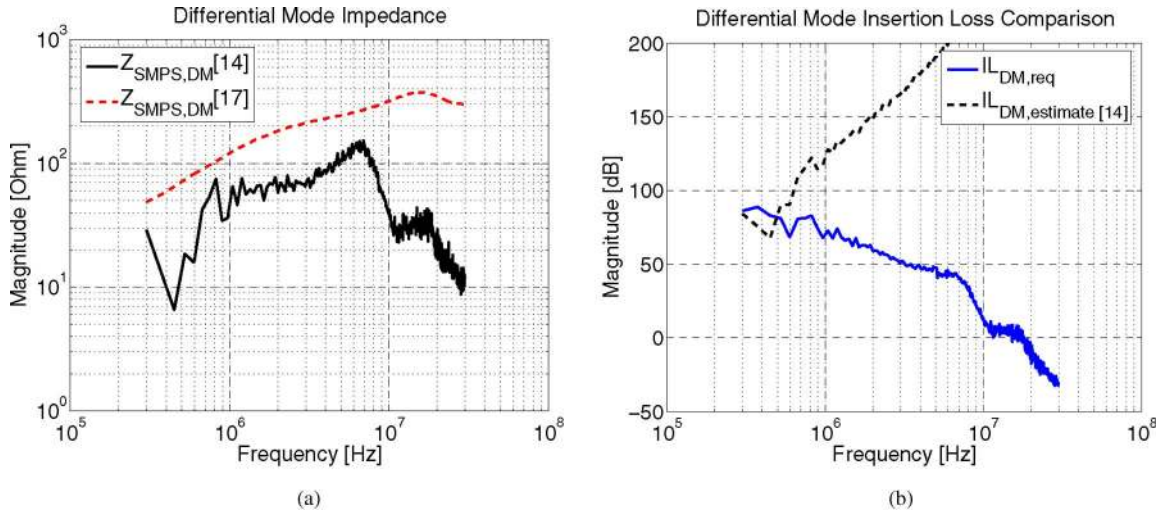


Fig. 7. DM filter design based on extracted DM impedance according to conventional approach [14]. (a) DM impedance magnitude. (b) Required and estimated DM insertion losses.

DM capacitor that could provide the necessary DM filter insertion loss higher than $IL_{DM,req}$, indicated in Fig. 5(e), is about $1.5 \mu\text{F}$.

On the contrary, the conventional design approach (e.g., [9]), not taking into account the SMPS and LISN impedances, leads to a possible overdesign of the DM capacitor. If we apply the conventional design procedure to our example, we need to satisfy the constraint of the $IL_{DM,req} = 86 \text{ dB}$ at 300 kHz ; hence, the cutoff frequency is given by $f_{c,DM} = f_{n,DM}/10^{IL_{DM,req}/\beta} = 2 \text{ kHz}$, where $f_{n,DM} = 300 \text{ kHz}$ and $\beta = 40 \text{ dB/decade}$ [10], [21]. Accounting for the already-determined choke inductance $L_{DM} = 17.6 \mu\text{H}$, the cutoff frequency formula $f_{c,DM} = 1/2\pi\sqrt{L_{DM}C_X}$ of the simplistic approach allows to determine the DM capacitor value, resulting in about $319 \mu\text{F}$, which is not only an impractical value, but also significantly larger than the capacitance required by the proposed method. This problem is also discussed in [9], and the advocated solution consists in adding DM chokes, which correspond to overdesigning an EMI filter with more components than necessary.

As a further step, let us discuss the impact of an incomplete determination of the load impedances of the filter on the compliance prediction. For comparison purposes, DM impedance is measured according to the procedure proposed by [14] and is compared with the measured results obtained from Section II [17] [see Fig. 7(a)]. This approach is coherent with what is commonly done in practice, i.e., to measure only the magnitude of the noise source impedance, and then using it in the insertion loss expressions as if the impedances were totally resistive [13]. Although [14] suggests to reconstruct the phase by means of

the classical Hilbert transform approach, in reality, often only magnitude of the noise source impedances is taken into consideration in order to avoid complex mathematical manipulations. The use of such incompletely determined DM impedance of SMPS in (9) indicates that the designed filter is unable to meet the $IL_{DM,req}$ for frequencies below 500 kHz , as illustrated in Fig. 7(b). The required DM capacitor that could provide the necessary DM filter insertion loss larger than $IL_{DM,req}$ amounts to about $4 \mu\text{F}$, which is about three times larger than the capacitance required by the proposed method. Again, the reduction of the capacitance value required by the proposed method corresponds to cost saving.

It is worth noting that because the CM noise source impedance is capacitive in nature and in the range of several kilohm, which is much larger than the CM impedance of the LISN (25Ω) [12], CM impedance determination according to [14] has no significant effect on the CM filter design.

E. Actual Insertion Losses and Validations

The impedance behavior of the filter components, chosen according to the aforementioned considerations, were measured by means of a HP 4396B impedance analyzer (100 kHz – 1.8 GHz), and the results are shown in Fig. 8(a)–(f). The actual insertion losses of the DM and CM filters of Fig. 6(b) and (c) can be worked out as an adaptation of (9) and (10) with the inclusion of the parasitic effects of the filter components [7], [8], and (11) as well as (12) shown at the bottom of the page, where

- $Z_{L_{DM}}$ Effective DM impedance of the CM choke [Ω];
- $Z_{L_{CM}}$ CM impedance of the CM choke [Ω];

$$IL_{DM,actual} = 20 \log \left| \frac{Z_{C_{XT}}(Z_{L_{DM}} + Z_{LISN,DM}) + Z_{SMPS,DM}(Z_{C_{XT}} + Z_{L_{DM}} + Z_{LISN,DM})}{Z_{C_{XT}}(Z_{LISN,DM} + Z_{SMPS,DM})} \right| \quad (11)$$

$$IL_{CM,actual} = 20 \log \left| \frac{Z_{C_{YT}}(Z_{L_{CM}} + Z_{LISN,CM}) + Z_{SMPS,CM}(Z_{C_{YT}} + Z_{L_{CM}} + Z_{LISN,CM})}{Z_{C_{YT}}(Z_{LISN,CM} + Z_{SMPS,CM})} \right| \quad (12)$$

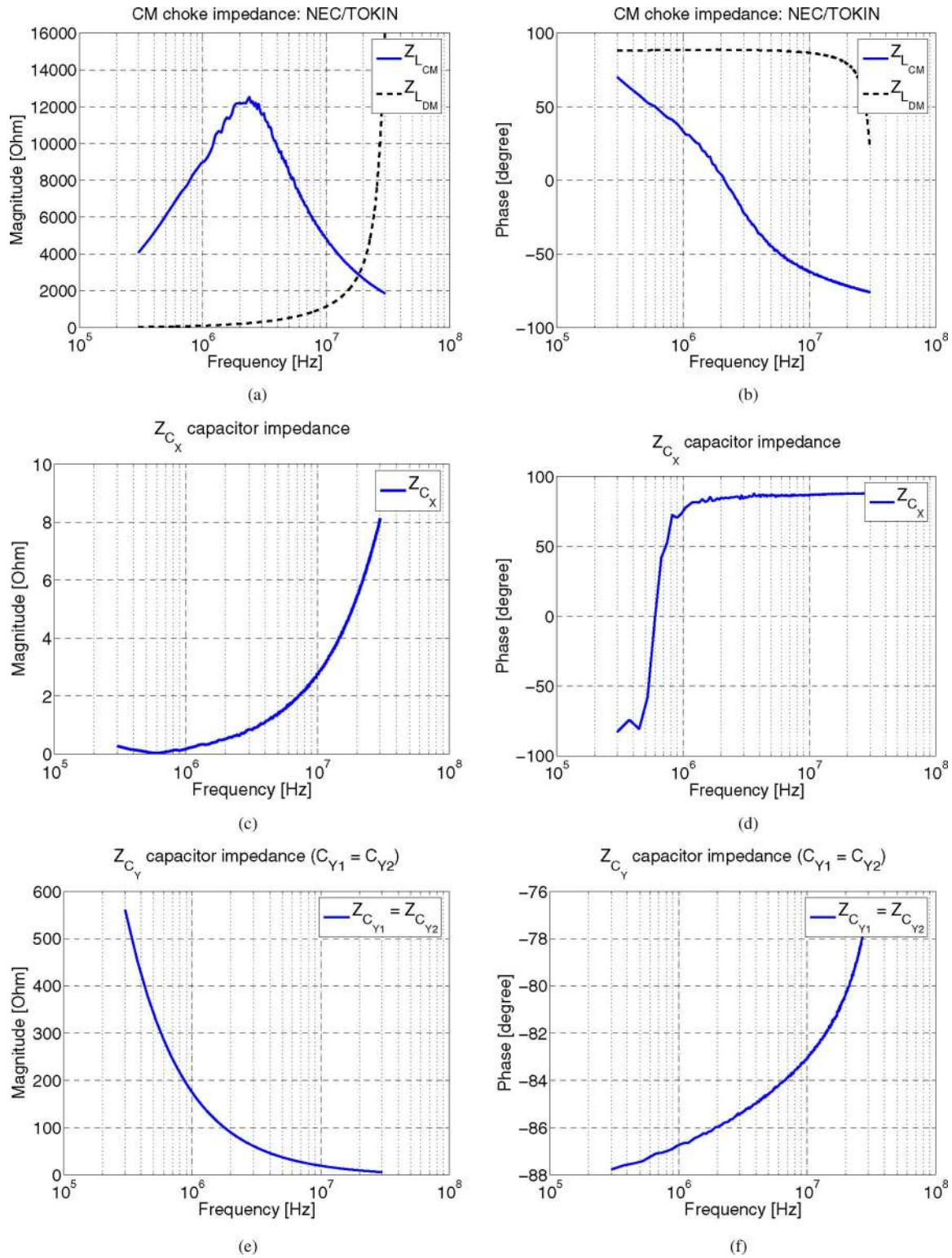


Fig. 8. Measured impedance of the chosen filter components. (a) and (b) CM choke (NEC/TOKIN). (c) and (d) $C_X = 1.5\text{-}\mu\text{F}$ capacitance. (e) and (f) $C_{Y1} = C_{Y2} = 1000\text{-pF}$ capacitances.

$Z_{C_{YT}}$ Effective CM impedance of $C_{Y1} // C_{Y2} [\Omega]$;

$Z_{C_{XT}}$ Effective DM impedance of $C_X // (C_{Y1} + C_{Y2}) [\Omega]$.

Using the measured impedances of all the chosen filter components [see Fig. 8(a)–(f)], as well as the LISN and SMPS impedance behavior [see Fig. 3(a)–(d)], the actual insertion

losses of the DM and the CM filters [computed by means of (11) and (12)] are plotted in Fig. 9(a) and (b), respectively. For comparison, the required DM and CM filter insertion losses are also shown in the same figures. Both the actual DM and CM filter insertion losses are higher than the required ones, which

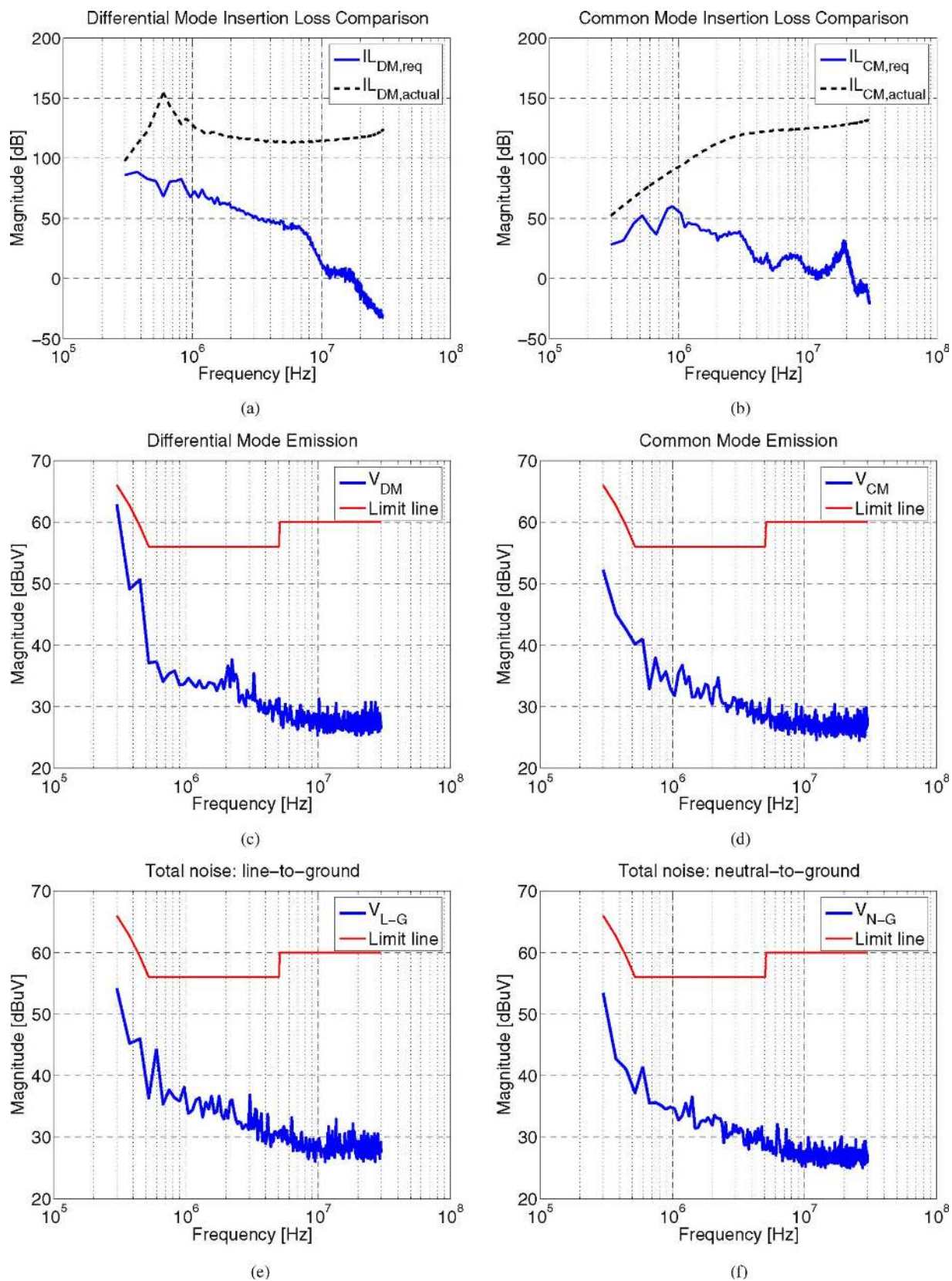


Fig. 9. Effect of the insertion of the EMI filter. (a) Required and designed DM insertion losses; (b) required and designed CM insertion losses; (c) measured DM conducted emissions with filter; (d) measured CM conducted emissions with filter; (e) measured total conducted emissions for line-to-ground; (f) measured total conducted emissions for neutral-to-ground.

indicate that the designed EMI filter is able to suppress the DM and CM conducted emissions below the CISPR 22 Class B limit. Fig. 9(c) and (d) shows the measured DM and CM conducted emissions after the designed EMI filter is inserted. Both the DM and CM conducted emissions are below the limit, confirming that the designed EMI filter fulfills the requirement. As a final compliance check, Fig. 9(e) and (f) shows the line-to-ground and the neutral-to-ground conducted emissions, respectively, and their results indicate that the filtered SMPS complies with the regulations limits.

IV. CONCLUSION

Information on the noise source and termination impedances of an SMPS connected to mains has been proven to be a useful input for designing an optimal EMI filter to meet a specific EMI limit in a systematic manner. The noise source (SMPS) and noise termination (LISN) impedances are measured by means of a two-probe measurement approach under in-circuit operating conditions. Both the DM and CM filter insertion losses for any EMI filter can be determined accurately so that the designer has a very clear picture of the EMI filter insertion loss characteristics. Undoubtedly, designing EMI filters without taking into account the termination impedances or with adopting incomplete measurement of them allow filtered SMPS to pass the regulation limits. However, they are overdesigned, which leads to bulky and costly final products. On the contrary, with the proposed EMI filter design methodology, the appropriate filter configurations and the optimal filter component values can be systematically chosen. Hence, optimal results can be achieved without incurring excessive design costs for EMI compliance. However, the proposed EMI filter design methodology does not take into account mode conversion (CM to DM or DM to CM) that can arise due to asymmetric design and the parasitic coupling of the filter components. A careful layout design is also needed in order to minimize the mode conversion so as to assure EMI compliance of the final product.

REFERENCES

- [1] R. Redl, "Electromagnetic environmental impact of power electronics equipment," *Proc. IEEE*, vol. 89, no. 6, pp. 926–938, Jun. 2001.
- [2] *Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment*, CISPR 22, 2004.
- [3] *Specification for Radio Disturbance and Immunity Measuring Apparatus and Methods Part 1: Radio Disturbance and Immunity Measuring Apparatus*, CISPR 16-1, 1999.
- [4] L. Tihanyi, *Electromagnetic Compatibility in Power Electronics*. Piscataway, NJ: IEEE Press, 1997.
- [5] J. A. Ferreira, P. R. Willcock, and S. R. Holm, "Sources, paths and traps of conducted EMI in switch mode circuits," in *Proc. 1997 IEEE Ind. Appl. Conf.*, pp. 1584–1591.
- [6] B. Garry and R. Nelson, "Effect of impedance and frequency variation on insertion loss for a typical power line filter," in *Proc. 1998 IEEE EMC Symp.*, pp. 691–695.
- [7] B. Audone and L. Bolla, "Insertion loss of mismatched EMI suppressors," *IEEE Trans. Electromagn. Compat.*, vol. EMC-20, no. 3, pp. 384–389, Sep. 1978.
- [8] S. M. Vakil, "A technique for determination of filter insertion loss as a function of arbitrary generator and load impedances," *IEEE Trans. Electromagn. Compat.*, vol. EMC-20, no. 2, pp. 273–278, Sep. 1978.
- [9] F.-Y. Shih *et al.*, "A procedure for designing EMI filters for AC line applications," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 170–181, Jan. 1996.

- [10] M. Kumar and V. Agarwal, "Power line filter design for conducted electromagnetic interference using time-domain measurements," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 1, pp. 178–186, Feb. 2006.
- [11] T. Nussbaumer, M. L. Heldwein, and J. W. Kolar, "Differential mode input filter design for a three-phase buck-type PWM rectifier based on modeling of the EMC test receiver," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1649–1661, Oct. 2006.
- [12] M. J. Nave, *Power Line Filter Design for Switched Mode Power Supplies*. New York: Van Nostrand Reinhold, 1991.
- [13] S. Ye, W. Eberle, and Y. F. Liu, "A novel EMI filter design method for switching power supplies," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1668–1678, Nov. 2004.
- [14] D. Zhang, D. Y. Chen, M. J. Nave, and D. Sable, "Measurement of noise source impedance of off-line converters," *IEEE Trans. Power Electron.*, vol. 15, no. 5, pp. 820–824, Sep. 2000.
- [15] D. M. Mitchell, *DC-DC Switching Regulator Analysis*. New York: McGraw-Hill, 1988, ch. 4.
- [16] K. Y. See and J. Deng, "Measurement of noise source impedance of SMPS using a two probes approach," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 862–868, May 2004.
- [17] V. Tarateeraseth, H. Bo, K. Y. See, and F. Canavero, "Accurate extraction of noise source impedance of SMPS under operating condition," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 111–117, Jan. 2010.
- [18] K. Y. See, "Network for conducted EMI diagnosis," *IEE Electron. Lett.*, vol. 35, no. 17, pp. 1446–1447, Aug. 1999.
- [19] J. J. Goedbloed, *Electromagnetic Compatibility*. Englewood Cliffs, NJ: Prentice-Hall, 1990.
- [20] T. Williams, *EMC for Product Designers*, 4th ed. London, U.K.: Newnes, 2007.
- [21] R. L. Ozenbaugh, *EMI Filter Design*, 2nd ed. New York: Marcel Dekker, 2001.
- [22] S. Wang, F. C. Lee, and J. D. Van Wyk, "A study of integration of parasitic cancellation techniques for EMI filter design with discrete components," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 3094–3102, Nov. 2008.



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