

$t|ket\rangle$: A Retargetable Compiler for NISQ Devices

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Abstract. We present $t|ket\rangle$, a quantum software development platform produced by Cambridge Quantum Computing Ltd. The heart of $t|ket\rangle$ is a language-agnostic optimising compiler designed to generate code for a variety of NISQ devices, which has several features designed to minimise the influence of device error. The compiler has been extensively benchmarked and outperforms most competitors in terms of circuit optimisation and qubit routing.

1. Introduction

Quantum computing devices promise significant advantages for a wide variety of information processing tasks [1, 2, 3]. For some tasks, notably the simulation of condensed-matter physics, the abstract structure of the problem may be sufficiently similar to the physical structure of the device that translation from one to the other is natural and (relatively) straightforward [4]. However, for most problems, and most quantum computers, this is not the case. Quantum algorithms are often described in terms that facilitate proving correctness or deriving asymptotic complexity estimates, without reference to a specific computing device on which to execute them. The translation from a high-level description of the algorithm to a machine-specific sequence of physical operations is called *compilation*, and is essential to realising the supposed computational advantage of quantum algorithms.

In computer science, the term *compiler* was introduced by Grace Hopper in the early 1950s [5], and originally referred to a routine which “compiled” a desired program from pre-existing pieces. Today the term denotes a program that translates a human-readable programming language into the binary language of the machine that will execute it. Early compilers produced code that was grossly inefficient, compared to what an average human programmer could write; however, today’s sophisticated *optimising* compilers reliably generate code that runs more quickly and uses less memory than even the best human programmer could manage [6]. The steady improvement of compiler technology

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4 has, in turn, enabled programming languages to increase in power and sophistication,
5 increasing the conceptual distance between the programmer and the executable machine
6 language.
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9 By comparison, almost all programming systems available for quantum computing are
10 conceptually primitive, remaining extremely close to the basic quantum circuit model [7].
11 Although higher-level application-oriented toolkits are becoming available [8, 9], the
12 programmer must usually describe the algorithm to be run in terms of basic unitary
13 gates. On the other hand, quantum computing hardware displays great diversity.
14 Superconducting and ion-trap-based quantum processors are now available from multiple
15 commercial companies [10, 11, 12, 13, 14], while other technologies such as photonics are
16 not far behind [15, 16]. Different underlying technologies have very different performance
17 parameters and trade-offs, and even broadly similar devices may differ in what basic
18 operations are available. Even in the context of the simple, circuit-centric, programming
19 model, the requirement to translate an abstract circuit into something suitable for the
20 chosen device creates the need for a compiler. Naive approaches to this translation can
21 significantly increase the size of the circuit; therefore the other major task for a quantum
22 compiler is *circuit optimisation*, to minimise the resources required by the program.
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Circuit optimisation is especially pertinent on so-called *noisy intermediate-scale quantum* (NISQ) devices. Preskill [17] defines a NISQ device as having a memory size of 50–100 qubits, and sufficient gate fidelity to carry out around 1000 two-qubit operations with tolerable error rates. We will adopt a wider definition: a NISQ device is any quantum computer for which general-purpose quantum error correction [18] is not feasible and hardware errors are expected. Because of these ineradicable errors, mere qubit count is poor measure of the capability of NISQ devices. The longer the computation runs, the more noise builds up.

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NISQ devices therefore impose strict limitations both on the number of qubits available to algorithms and on the maximum circuit depth that can be achieved. Aside from the obvious requirement to use this limited hardware budget in the most efficient manner possible, the noisiness of NISQ machines introduces further complications. Since many common textbook algorithms such as quantum phase estimation ‡ are not feasible in the available circuit depth, hybrid algorithms such as the Variational Quantum Eigensolver (VQE) [20] and the Quantum Approximate Optimisation Algorithm (QAOA) [21] have been proposed instead. While the circuit depths required by these algorithms are more favourable to NISQ devices, they are based on repeatedly executing circuits inside a classical optimisation loop, where both the rate of convergence and the accuracy of the final result can be adversely affected by device noise. In consequence, any compiler for NISQ devices should aim to maximise the overall fidelity of the computation. Minimising the number of operations helps, but other techniques may be employed [22, 23, 24, 25].

This paper describes $t|ket\rangle$, a compiler system for NISQ devices that aims to achieve

‡ But see O’Brien *et al* [19].

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```

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4   C(·) ← GenerateParameterisedCircuit()
5   M ← GenerateListOfPauliMeasurements()
6    $\bar{\theta} \leftarrow \bar{\theta}_0$ 
7   E ← 0
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9   while E has not converged do
10      for i from 1 to N_ITERS do
11         for m ∈ M do
12             $r_{m,i} \leftarrow \text{Execute}(C(\bar{\theta}); m)$ 
13         end for
14      end for
15      E' ← EstimatorFunction( $\bar{r}$ )
16       $\bar{\theta} \leftarrow \text{ClassicalOptimiser}(\bar{\theta}, E, E')$ 
17      E ← E'
18   end while
19   return E
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Figure 1: The typical structure of a variational quantum algorithm

these objectives. The core of *t|ket>* is a flexible optimising compiler which supports multiple programming frameworks, and multiple quantum devices. It is specifically designed for NISQ devices, and includes features that minimise the influence of device errors on computation. As we demonstrate in Section 9, *t|ket>*'s optimisation and qubit mapping routines reliably outperform other compilers. The system also includes runtime management features to facilitate the variational algorithms typical of NISQ devices.

1.1. NISQ devices and their software

Before addressing the *t|ket>* system, we consider a schematic variational algorithm in the context of the system architecture of an idealised NISQ device. For purposes of illustration, a toy VQE algorithm is shown in Figure 1.

The first point to note in this example is that the central “Execute($C(\bar{\theta}); m$)” subroutine is the only part that runs on the quantum device: the other subroutines and the main loop are classical. The subroutines “EstimatorFunction” and “ClassicalOptimiser” are used repeatedly inside the main loop – the characteristic of a hybrid algorithm – and their outputs are used in the next quantum execution. The first two subroutines, “GenerateParameterisedCircuit” and “GenerateListOfPauliMeasurements”, are tasks that are usually considered part of the compiler, but observe that inside the main loop a fresh quantum circuit must be built using the parameterised circuit $C(\cdot)$, the measurement m , and the new parameters $\bar{\theta}$. How does an algorithm like this map onto a realistic quantum computer system?

While it is common to talk about a “quantum computer” as a unified device, in practice it consists of multiple subsystems, each of which is a computer in its own right.

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5 Running a quantum algorithm therefore involves a large number of software components
6 in a mixture of runtime environments, with very different performance demands. Figure 2
7 displays a realistic architecture for a NISQ computer. The lowest level comprises the
8 programmable *devices* which drive the evolution of the qubits and read out their states.
9 An example of this kind of device is an arbitrary waveform generator, as found in many
10 superconducting architectures. The microwave pulse sequences output by these devices
11 are generated by simple low-level programs optimised for speed of execution. These
12 devices, and the *real-time controller* which synchronises them, operate in a hard real-time
13 environment where the computation takes place on the time-scale of the coherence time
14 of the qubits. These components combine to execute a single instance of a quantum
15 circuit, possibly with some classical control. By analogy with GPU computing, we refer
16 to this layer as a *kernel*.
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19 One level higher, the *scheduler* is responsible for dispatching circuits to be run
20 and packaging the results for the higher layers. It is also likely to be heavily involved
21 in the device calibration process. (Calibration data are an important input to the
22 compiler.) This layer and those below may be thought of as the low-level system software
23 of the quantum computer, and must normally be physically close to the device. In the
24 layer above we find service-oriented middleware, principally the *task manager*, which
25 may distribute jobs to different quantum devices or simulators, GPUs, and perhaps
26 conventional HPC resources, to perform the various subroutines of the quantum algorithm.
27 This layer may also allocate access to the quantum system among multiple users. Finally,
28 at the highest level is the *user runtime*, which defines the overall algorithm and integrates
29 the results of the subcomputations to produce the final answer.
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32 With this picture in mind, we see that the path from a high-level program describing
33 a quantum algorithm to its final result involves many stages of decomposition and
34 compilation in order to run in this heterogeneous environment. In practice, some of these
35 stages may be amalgamated or absent. In this paper we will focus on the generation of
36 the kernel, since this is the indispensable part of the process, and can be (to some extent)
37 decoupled both from the high-level architecture and the low-level system-specific parts.
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40 The picture is further complicated when considering quantum computers capable
41 of error correction. The “logical” kernel must be translated to an encoded equivalent;
42 subroutines to perform gate synthesis must be added; and error detection correction
43 stages must be interleaved in the main algorithm. However, every part of the NISQ
44 process is also required in the error-corrected case, so we focus on compilation in the
45 NISQ context.
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47 48 49 50 51 52 53 1.2. *Related work*

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55 The last few years have seen an explosion of interest in quantum programming languages,
56 and the problems of quantum compilation have been explored at various levels of
57 abstraction [26], from high-level algorithm design to pulse control at the machine level.
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59 Several languages have been developed for quantum programming. Quipper [27] is a
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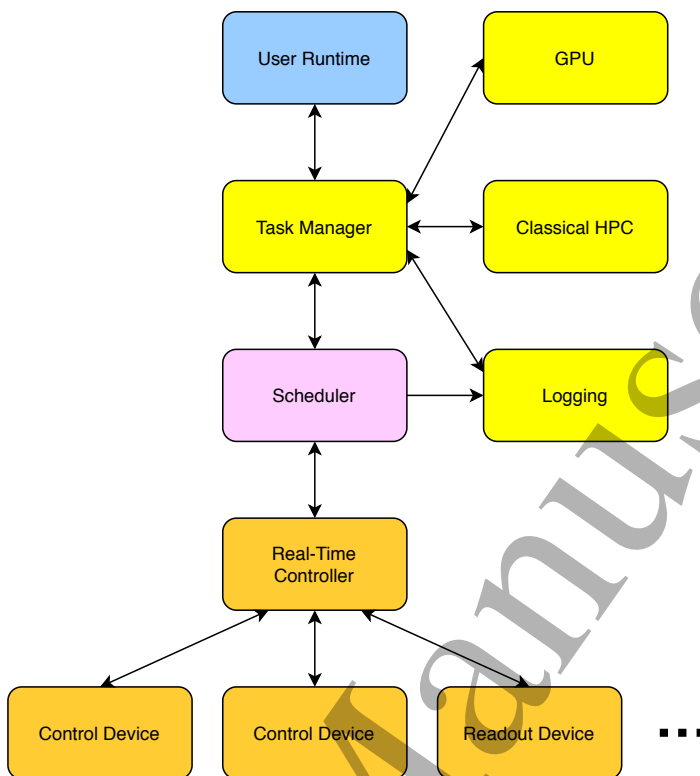


Figure 2: Idealised system architecture for a NISQ Computer

functional language for quantum circuits embedded in Haskell. The ScaffCC compiler [28], based on the LLVM framework, compiles an extension of C, and can be configured for routing to specific architectures. Q# [29] is a hybrid classical–quantum language designed to facilitate the development of programs that can be run on a simulator (and eventually on actual hardware). Strawberry Fields [30] is a Python-based quantum programming framework that is based on the “continuous variable” (CV) model of computation.

Several other compilation systems have been developed as Python modules targeting specific hardware. These include the Forest SDK/pyQuil [31] (for Rigetti backends), Qiskit [32] and ProjectQ [33] (for IBM backends), and Cirq [34] (for Google backends). Other projects have adopted a backend-agnostic approach. XACC [35] is a quantum programming framework that can target several different backends as plug-ins. TriQ [36] uses ScaffCC to compile quantum software for several different architectures in order to study their performance characteristics. Even for the full-stack systems, the compiler element (e.g. Quilc [37] from the Forest SDK or the transpiler passes in Qiskit Terra) can be invoked to compile for arbitrary devices.

A range of gate-level circuit-optimisation techniques have been explored, including the use of phase polynomials [38] and constraint programming [39]. There are also promising results for using information on the noise characteristics and fidelities of the target device to assist compilation [40, 41, 42]. Meanwhile at the level of machine control there have been efforts to optimise the implementation of variational algorithms using

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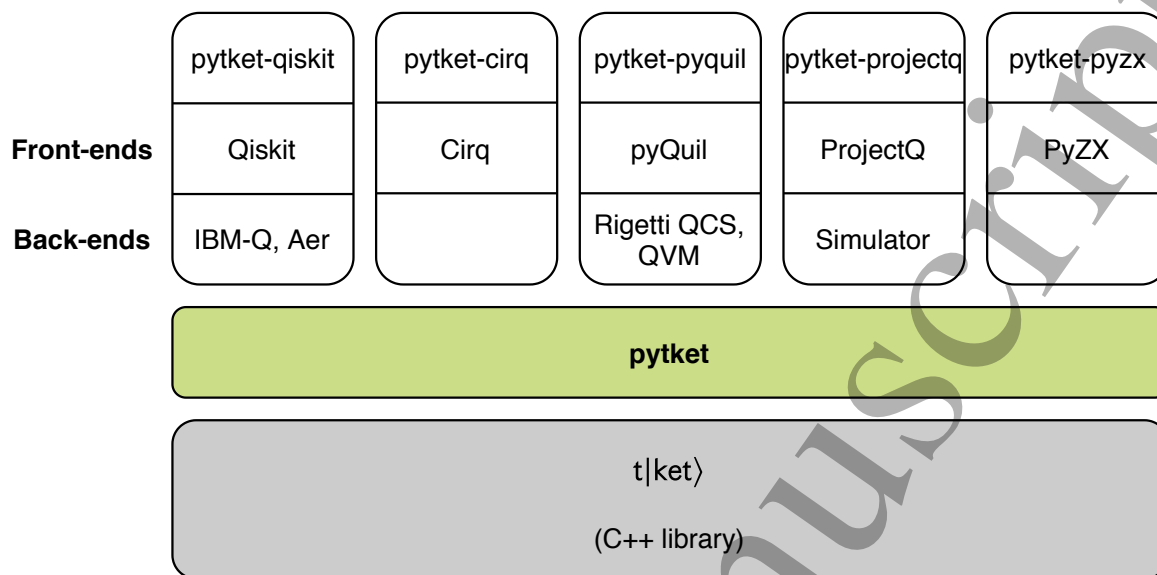


Figure 3: Components of $t|ket\rangle$

automatic differentiation and interleaving compilation with execution [43, 44].

1.3. Synopsis

Here we give an overview of the $t|ket\rangle$ system. Subsequent sections give detailed descriptions of the modular front- and back-ends, the intermediate representation used, the transform system, some of the optimisation methods, and the system of qubit placement and routing. Section 9 provides comparative benchmark results for the performance of the optimiser and qubit allocation engine. The benchmark set of circuits is available for download.

1.4. How to get $t|ket\rangle$

While the core of $t|ket\rangle$ is a highly optimised C++ library, the system is available as the Python module `pytket`, which provides the programming interface and interoperability with other systems. It can be installed on Linux and MacOS using the command:

```
pip install pytket
```

and the documentation is available online at: <https://cqcl.github.io/pytket/>. Figure 3 shows the components that are installed by this command.

To interface with other software packages, and to use back-ends that depend on external software, the user must also install plug-in packages. At the time of writing, the available plug-ins are: `pytket_qiskit`, `pytket_cirq`, `pytket_pyquil`, `pytket_projectq`, and `pytket_pyzx`. All of these can be installed using `pip` in the same manner as the core package. The `pytket` module is free for non-commercial use. We encourage the reader to try it out for themselves!

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2. System Overview

The t|ket> system consists of two main components: a powerful optimising compiler written in C++, and a lightweight user interface and runtime system written in Python. This Python layer allows the user to define circuits and invoke compiler functions, while the runtime environment marshalls and dispatches kernels for execution, and provides convenience methods for defining variational loops, updating parameters, and collating statistics across circuit evaluations. Optional Python extensions provide interfaces to third-party quantum software systems. The overall structure is illustrated in Figure 3.

In the classical setting, a compiler translates a human-readable programming language into machine-executable object code. This process can be divided into three stages: a *front-end*, which handles lexing, parsing, semantic analysis, and other tasks which depend on the source language; a *back-end*, which allocates registers and generates suitable instruction sequences in the target machine language; and an intermediate stage, which performs data and control-flow analysis on an *intermediate representation* (IR) of the program, which is independent of both the source and the target languages. Modern compiler systems, such as LLVM [45], use a standard IR to decouple these three stages, making it relatively simple to add support for a new programming language or machine architecture to an existing compiler framework.

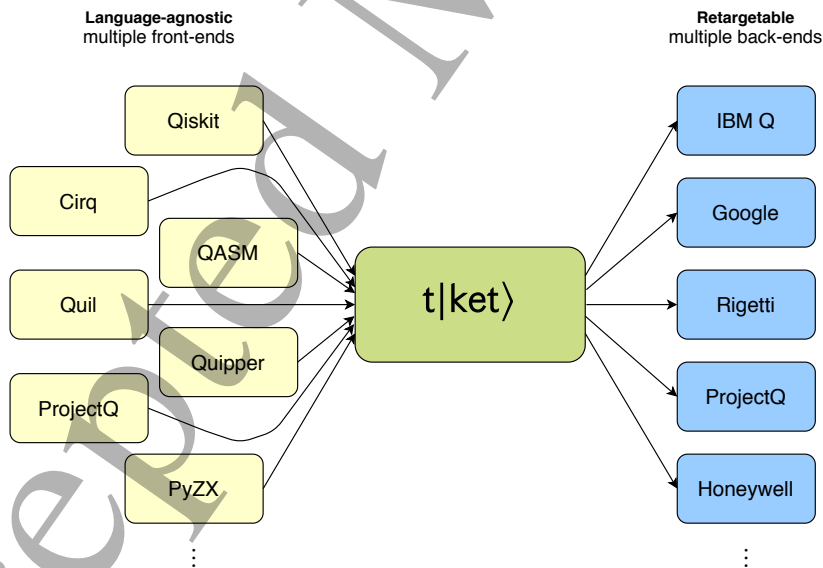


Figure 4: Modular front-ends and back-ends for t|ket>

t|ket> was designed from the ground up to be *retargetable*, meaning that it can generate code for many different quantum devices, and *language agnostic*, meaning that it accepts input from most of the major quantum software platforms. For this reason, its overall structure, shown in Figure 4, follows the same basic pattern as the LLVM. A variety of lightweight front-end units translate the desired input language

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4 into the $t|ket\rangle$ IR. This internal representation is a generalisation of the usual language
5 of quantum circuits based on hierarchical non-planar maps; this is described in more
6 detail in Section 4. Standard quantum circuits are easily embedded into the $t|ket\rangle$ IR –
7 a fact which eases the task of adding new front-ends – but many node types that are not
8 unitary gates are also available.
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11 Once the input has been translated to the IR, the central circuit transformation
12 engine can begin its work. The transformation engine performs a user-configurable
13 sequence of rewrites of the IR; some examples are described in Section 6. Typically this
14 proceeds in two phases: an architecture-independent optimisation phase, which aims to
15 reduce the size and complexity of the circuit; and an architecture-dependent phase, which
16 prepares the circuit for execution on the target machine. This phase itself decomposes
17 into a *rebase*, which maps the gates present in the circuit into those supported by the
18 device, and a *qubit mapping* phase. The mapping phase is necessary to ensure that
19 all qubits that are required to interact during the program are physically able to do
20 so; this typically increases the size of the circuit, since most devices do have restricted
21 interactions between their qubits. This is described in detail in Section 7.
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24 The end product of this process is a *kernel*: a circuit that can be executed on the
25 chosen target device. The kernel may then be scheduled for execution by the runtime
26 environment, or simply saved for later.
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29 In keeping with its focus on NISQ devices, the design of $t|ket\rangle$ is minimalistic
30 compared to the schema proposed by Häner *et al* [26]. There is no error correction, and
31 $t|ket\rangle$ does not include a linker, preferring to rely on application programming frameworks
32 such as CQC’s Eumen or IBM’s Qiskit Aqua to provide libraries of common routines.
33 The lowest layer of compilation – translation of kernels to control signals for the lasers,
34 microwave generators, and so on – is left to the hardware implementor. However, since
35 $t|ket\rangle$ takes into account the device’s architectural constraints during the compilation
36 phase, this last stage of translation can be minimal.
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39 Thanks to its retargetability, $t|ket\rangle$ can be used as a cross-compiler: source programs
40 produced from any supported front-end can be compiled to run on hardware produced
41 by any vendor.
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46 3. Front-ends and Back-ends

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48 The `pytket` interface can be used directly to build quantum circuits from individual
49 gates in the standard way. While this may be acceptable for small experiments, more
50 powerful high-level tools are preferable for larger or more complex tasks. For this
51 reason $t|ket\rangle$ sports a range of lightweight front-end modules for different quantum
52 programming systems. The industry-standard OpenQASM [46] and the functional
53 language Quipper [27] are supported via direct source-file input. Python converters
54 provide support for IBM’s Qiskit [32], Google’s Cirq [34] and Rigetti’s pyQuil [31],
55 as well as the independent open-source projects ProjectQ [33] and PyZX [47]. These
56 Python libraries in turn support higher-level application programming frameworks such
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```
1 circuit = circuit_from_qasm('input.qasm')
2 q0, q1 = circuit.qubits[:2]
3 circuit = circuit.H(q0).CX(q0, q1).measure_all()
4
5 backend = IBMQBackend('ibmq_ourense')
6 if not backend.valid_circuit(circuit):
7     circuit = backend.compile_circuit(circuit)
8     assert backend.valid_circuit(circuit)
9
10 backend.process_circuits([circuit], n_shots=100)
11 results = backend.get_shots(circuit)
```

Figure 5: Code example showing front-end and back-end use. A circuit is read in from a QASM file; operations are appended to it using the `pytket` interface; the circuit is compiled to satisfy the constraints of a back-end, and then executed. The `IBMQBackend` class is included in the `pytket_qiskit` extension package.

as OpenFermion [48] or Rigetti Grove. Support for Q# [29] is planned for the next release.

Similarly, t|ket) offers multiple back-ends, each supporting a different quantum hardware platform or classical simulator. Supporting a given platform implies, firstly, generating a circuit that respects the constraints of the hardware or simulator (generally, connectivity and primitive gate limitations); secondly, the back-end must dispatch the kernel for execution and collate results. The first of these tasks is handled by the system described in Section 5. Each back-end class provides a default compiler pass, which guarantees that a compiled circuit will respect the relevant constraints.

t|ket) attempts to provide a uniform interface across the various back-end platforms, so that a user can easily change back-ends for an experiment without changing anything else in their code. At the time of writing, t|ket) supports all IBM Q and Rigetti devices via their online access services, and experimental devices produced by Honeywell Quantum Systems, Oxford Quantum Circuits and the University of Maryland. In addition, t|ket) can use the ProjectQ, IBM Aer and Rigetti QVM simulators. Various other machines are supported indirectly using either QASM output or t|ket)'s integration with Qiskit and Cirq. Figure 5 shows an example of front-end input followed by circuit compilation, execution and result retrieval via a back-end. For back-ends that support it, circuit submission and job retrieval can be performed separately, allowing asynchronous execution of the quantum circuit.

Utility functions are also provided for postprocessing of results, such as calculation of expectation values. Generic mitigation of classical state-preparation-and-measurement (SPAM) [49] errors across back-ends is scheduled for release in 2020.

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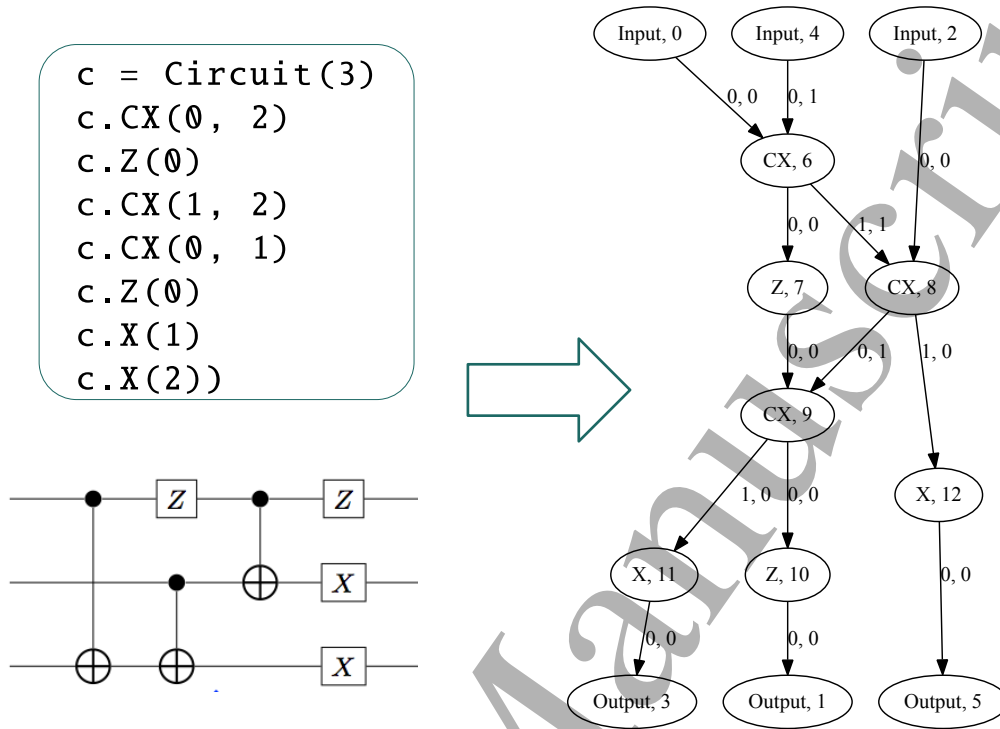


Figure 6: $t|ket\rangle$ circuit internal representation. Pairs of values labeling edges correspond to port numbers at the source and target vertices. Note that the Input and Output label numbers are even and odd respectively, so that qubit 0 corresponds to the path from “Input, 0” to “Output, 1”, qubit 1 is the path from “Input, 2” to “Output, 3”, and so on.

4. Representing Circuits

The standard intermediate representation (IR) in $t|ket\rangle$ is the *circuit*. A circuit is a labelled directed acyclic graph (DAG) with some additional structure. Vertices in the DAG correspond to operations, usually quantum or classical logic gates, but also *boxes*, a kind of opaque container which we will define later, and certain compiler-internal meta-operations. Edges in the DAG track the flow of computational resources from operation to operation. Typically, these resources are qubits, and the operations are unitary gates. Since many operations do not act symmetrically on their inputs, we add port labels for the incoming and outgoing edges at each vertex to distinguish between, for example, the control and target qubits of a CX gate. Each input port of a quantum operation is paired with an output port, allowing the path of a particular resource unit to be traced through the circuit, as shown in Figure 6.

For qubits, this linear resource management is justified by the no-cloning [50] and no-deleting [51] theorems. However, for classical operations, this effectively means that output values must overwrite their previous value. This treatment of classical bits is an

```

cbox = CircBox(c)
c2 = Circuit(4)
c2.add_circbox(cbox, [0, 1, 2], [])
c2.CRz(2, 3, Symbol('alpha'))

```

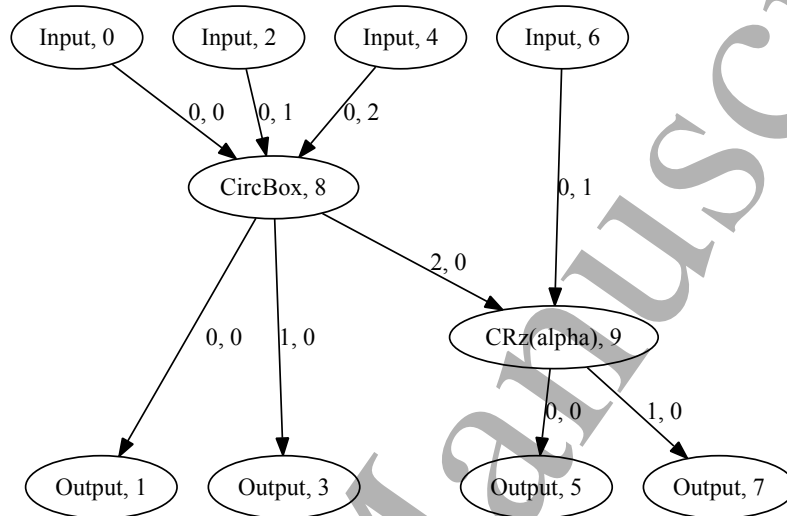


Figure 7: t|ket> circuit with a box containing the circuit from Figure 6. A parameterised controlled-Rz gate is also shown, with a symbolic parameter.

artefact of the simplified classical computational model of QASM [46] and devices that have adopted it, requiring explicit allocation of classical registers (both for classical input to execution and for result retrieval) and forbidding dynamic allocation of scratch space.

At the input and output boundaries of a circuit, the resource units – which we may identify with storage locations – are partitioned into *registers*. A circuit can contain arbitrarily many registers, and resource units are represented within a register by identifiers that are unique within the circuit. The registers specify an ordering of the resource units §. This ordering allows circuits to be composed sequentially and in parallel, and act as “port labels” for entire circuits, just as individual operations have ports within a circuit. This means that the process of composing circuits is identical to the composition of individual operations.

4.1. Gate Types

There are a wide array of allowed logic gates in t|ket>, covering the native gates of the platforms that t|ket> can interface with. An overview of the kinds of supported gates is given in Table 1. The most common quantum gates are one- and two-qubit gates,

§ In category-theoretic terms, the triple (I,O,G) of an input ordering, output ordering and graph corresponds to a structured cospan [52], where G is the apex.

Class of operation	Example
Basic single-qubit gate	Hadamard
Parameterized single-qubit gate	$Rz(\alpha)$
Basic two-qubit gate	CX
Parameterized two-qubit gate	$CRz(\alpha)$
Basic multi-qubit gate	C_nX
Parameterized multi-qubit gate	$C_nRy(\alpha)$
Classical output gate	Measure
Meta-operation	Barrier
Hierarchical vertex	CircBox

Table 1: Classes of operations available for circuits in t|ket)

reflecting the native gates on physical superconducting and ion-trap hardware, but some gates with arbitrary quantum controls are allowed; these must eventually be decomposed to hardware-native gates by the transform engine. All quantum gates in t|ket) can have arbitrary classical control, and primitive classical logic gates are supported. However, adding classical control to gates can limit the ability of the rewrite engine to optimise the circuit. An enumeration of all the allowed operation types in t|ket) can be found in the documentation at <https://cqcl.github.io/pytket/build/html/optype.html>.

Boxes are a special class of operations in t|ket). A box vertex is a container which encapsulates a whole circuit. In Figure 7, the circuit from Figure 6 is put into a box within another circuit. Boxes allow for front-ends to take in high-level descriptions with subroutines. As this subcircuit can also contain box vertices, a single circuit can contain a hierarchy of arbitrary rank. The hierarchy must be decomposed at the kernel generation stage, but this decomposition is trivial because of the compositional structure whereby circuits are equivalent to individual operations. As well as explicit circuits, box vertices can also contain other representations, which can be useful for optimising certain classes of quantum circuits. Because boxes are opaque, the parent circuit is undisturbed by the optimisation procedure acting on the subroutine. The next release of t|ket) will include such optimisations acting directly on boxes.

4.2. Gate Parameters

Unlike large-scale, fault-tolerant quantum computers, NISQ devices generally allow arbitrary angles on parameterised gates. Accordingly, t|ket) allows arbitrary angles on all parameterised gates, up to IEEE 754 double-precision [53].

In Section 1 we briefly described the variational hybrid quantum–classical algorithms proposed for NISQ devices. To enable the efficient compilation of this class of algorithms, t|ket) supports *symbolic* parameters. This allows the compilation of a parameterised circuit corresponding to an entire variational algorithm without requiring repeated compilation from scratch at each iteration of the classical optimiser. The circuit in

Figure 7 contains a parameterised controlled-Rz gate with a symbolic parameter. This class of circuits is handled using *partial compilation*: the circuit is precompiled with unknown, symbolic parameters using an expressive symbolic manipulation library. The result can be used as a template circuit and, after parameter values at a given iteration have been substituted, further simple circuit rewriting can be performed before the resulting kernel is sent to a backend to be run. This minimises the computation required between iterations of the classical optimiser, reducing the overall runtime of a variational algorithm while still using the rewrite engine of t|ket> to minimise the resource costs of the circuits. The implementation of the circuit class uses local adjacency lists at each vertex to allow near constant-time edge and vertex insertion and removal.

5. The t|ket> Transform System

In general, a quantum algorithm can be expressed in multiple ways using a given gate set; the goal is to express it in a way that minimises the gate count and circuit depth. The field of circuit optimisation is well developed, with a variety of optimisation strategies employed for different algorithms and target hardware devices [38, 54, 55]. Most commonly, a circuit can be rewritten using unitary equality between circuits, where a resource-inefficient subcircuit can be found and replaced using a closer-to-optimal one ||. The core of t|ket> is a high-performance circuit rewriting engine, referred to as the *transform system*. A function that performs rewrites using this system is called a *transform pass*. Circuit optimisation in t|ket> is described in more detail in Section 6. Aside from optimisation, the transform system has an essential role in generating circuits that are executable on the target hardware.

Each backend that t|ket> can target has associated with it a series of properties that any valid circuit must satisfy. This will include, as a minimum, the set of supported gates; for many architectures it will also include a graph representing the connectivity between the qubits. Mapping logical qubits to physical qubits also requires rewriting the circuit so that the interactions between qubits correspond only to edges in the associated connectivity graph. The transform pass that performs this rewriting is described in Section 7. Other properties may also be required, depending on the platform, and these also require transform passes.

Transform passes are composed sequentially; the resulting function is also a transform pass. For instance, a typical compiler flow will consist first of some optimisation on the circuit that has no regard for connectivity graph or gate set, followed by passes that bring the circuit closer to satisfying all of the constraints. Only if a circuit satisfies all these properties can it be executed on the target hardware.

To document and constrain the composition of transforms, the t|ket> transform engine implements a simple expression language, which follows the same principles as “contracts” in object-oriented programming [57].

|| The process of finding and replacing subgraphs in this manner is called *double pushout rewriting*. See Ehrig *et al* [56].

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5 The functions that verify that properties are satisfied are called *predicates*. Each
6 predicate is a function from a circuit to a boolean value: *true* if the circuit satisfies
7 the corresponding property and *false* otherwise. These functions can incorporate
8 some external information about the target hardware, such as connectivity graph and
9 desired gate set; when external information is required the predicates are generated by
10 higher-order functions. For example, to verify that the connectivity graph of a specific
11 architecture is satisfied, a higher-order function will take in a connectivity graph and
12 return the corresponding predicate. The full list of allowed predicates is documented at
13 <https://cqcl.github.io/pytket/build/html/predicates.html>.
14
15

16 Each transform pass has a *precondition* and a *postcondition*, so that the resulting
17 compiler pass is a Hoare triple. This is illustrated in Figure 8a. The compiler pass may
18 be used on a circuit that satisfies the precondition, and will guarantee that afterwards
19 the circuit satisfies the postcondition. Both the precondition and the postcondition are
20 sets of predicates. For example, a peephole optimisation may require that the circuit
21 be presented in a certain gate set before it can be applied. This gate-set predicate
22 forms the precondition of the pass. The optimisation can then guarantee to the user
23 that the rewrite rule will return the circuit in a different gate set; this guarantee is the
24 postcondition.
25
26

27 These Hoare triples may then be composed, so that a custom rewriting sequence
28 can be generated, as shown in Figure 8b. If the triples are correctly matched, so that no
29 intermediate conditions are conflicting, the custom sequence is valid.
30
31

32 More sophisticated combinators, such as loops, can be useful for optimisation passes.
33 For example, a user may wish to continue applying a sequence of rewrite rules until no
34 further rewrites are possible. These combinators may be composed in the same way as
35 sequences. When looping combinators are used, termination of the resulting pass is not
36 guaranteed.
37
38

39 The full list of compiler passes and combinators can be found at <https://cqcl.github.io/pytket/build/html/passes.html>.
40
41

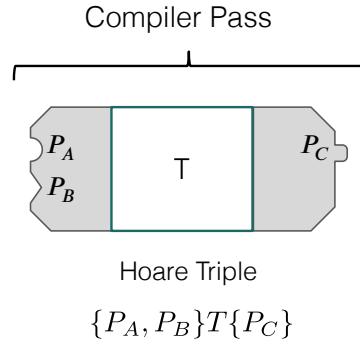
42 43 6. Circuit Optimisation Methods

44
45 With the limited fidelity available on NISQ devices, effective circuit optimisation is
46 essential in order to extract all available performance out of the machines. The goal is
47 to identify equivalent circuits that will accumulate less noise when run on a real device.
48
49

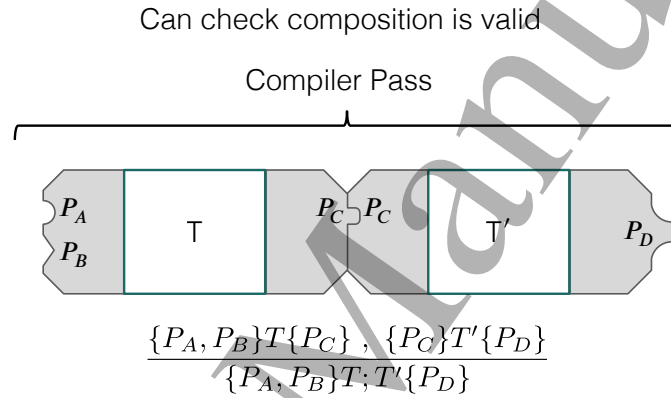
50 Circuit optimisations in $t|ket\rangle$ are provided as compiler passes, which can be
51 composed into larger routines. High performance is obtained by optimising at each
52 stage in the compilation pipeline, so it is beneficial to have both powerful optimisations
53 that can yield better results when not constrained by qubit connectivity or gate set
54 and procedures targeted at specific architectures. $t|ket\rangle$ contains some methods that
55 are architecture-agnostic and others that are architecture-aware (parametrised over the
56 properties of the device). Many of the architecture-agnostic passes will additionally
57 preserve any connectivity already satisfied by the inputs, allowing them to be applied
58
59
60

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(a) A compiler pass is a transform pass with associated pre- and post-conditions.



(b) Composition of compiler passes. The resulting Hoare triple is the standard sequential execution schema for two programs.

after routing. Designing optimisations in this way provides retargetability without sacrificing performance.

6.1. Circuit metrics

Attempting to use the actual fidelity as a cost function would require accurate simulation of the quantum circuit with realistic noise models, which is both computationally expensive and highly dependent on a specific target architecture. Further, because real devices have noise sources that are complex and hard to characterise, simple extrapolation from single-gate performance can significantly overestimate the actual performance of the device, necessitating more sophisticated, holistic measures [58, 59, 60]. However, simpler metrics can give good, device-independent approximations to noise.

Naively optimising for gate count acknowledges the key fact that all gates will introduce some degree of noise. However, NISQ devices tend to provide fast, high-fidelity single-qubit rotations, with the error rates of multi-qubit operations being an order of magnitude worse [61]. The primary focus for most optimisations in $t|ket\rangle$ is to minimise the *two-qubit gate count*, which penalises the use of these slower and less accurate

operations.

Definition 6.1. The *two-qubit gate count* of a circuit is the number of maximally-entangling two-qubit gates used in the circuit.

This is often referred to as CX-count, since any other maximally-entangling two-qubit operation (such as CZ or $e^{iXX\pi/4}$) is equivalent to a single CX up to local unitaries. This is analogous to the *T-count metric* used at the error-correcting level.

Omitting single-qubit gates entirely from consideration improves device-independence, since the number of gates required varies significantly with the gate set (for example, a single U3 gate from the IBM specification can capture any rotation, while up to three are needed if decomposed into the underlying Rz and Ry gates).

The short coherence times of qubits strongly correlates the fidelity of the circuit with the time taken to execute. An ideal device will be able to parallelise gates acting on disjoint qubits to mitigate this. We can obtain a good approximation to the time taken on such a device by considering the *depth* of the circuit.

Definition 6.2. For a gate g with predecessors $P(g)$, we define $\text{depth}(g)$ by:

$$\text{depth}(g) \triangleq \begin{cases} 0 & P(g) = \emptyset \\ 1 + \max_{p \in P(g)} \text{depth}(p) & P(g) \neq \emptyset \end{cases}$$

The *depth* of a circuit is the maximum value of $\text{depth}(g)$ over all gates g . For any gate type G , the *G-depth* of the circuit is obtained by considering only the contribution from G gates.

Again, given the characteristics of multi-qubit operations on current hardware, CX-depth (or depth with respect to any other maximal two-qubit gate) gives a device-agnostic estimate of the time cost of a circuit.

6.2. Peephole optimisations

Circuit optimisations in t|ket) can broadly be categorised into *peephole optimisations* and *macroscopic analysis*. Peephole optimisations are analogous to their namesake in classical compilers, where a sliding window traverses the instruction graph, looking for specific small patterns or classes of subcircuits and substituting equivalent subcircuits (with lower gate counts or depth) in place. Basic examples include the elimination of redundant gates such as identities, gate-inverse pairs, and diagonal gates before measurements. Local gate commutation rules can be considered at the point of pattern identification, or as standalone passes to enable further optimisations.

These techniques are generic, in the sense that they are not tuned for particular applications. The majority are written for best performance in the intermediate gate set of CX, Rz, and Rx, though when they can be expressed more naturally in a different gate set (such as a set of Clifford gates), rebase passes can be applied to convert between them.

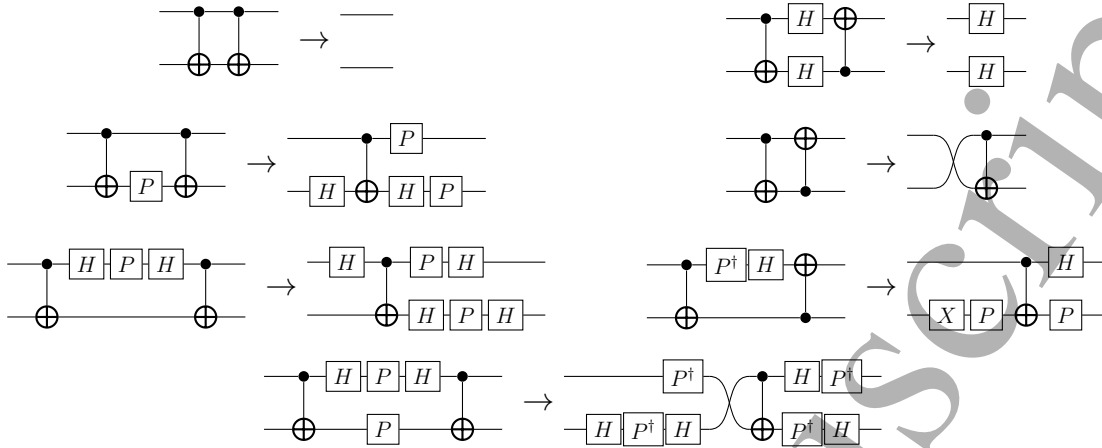


Figure 9: Clifford identities that can be recognised and applied in t|ket) to reduce the CX count. $Rz(\frac{\pi}{2})$ (phase) gates are represented by P in the diagrams. The two identities that would introduce SWAPs can optionally be disabled.

Clifford circuits are defined as the class generated by CX, Hadamard, and $Rz(\frac{\pi}{2})$ gates. These are known to be efficiently simulable [62, 63], and there is a wide literature on simplification techniques [64, 65, 66]. In particular, there are several useful small identities for reducing the CX-count of a circuit, which t|ket) can recognise and apply: these are summarised in Figure 9.

The Cartan decomposition [67] specifies a way to synthesise arbitrary n -qubit unitaries into sequences of local unitaries on fewer qubits and a small number of entangling operations between them. This decomposition gives the following upper bounds for small instances:

Theorem 6.3. *Any single-qubit unitary can be decomposed into a sequence of at most three rotations using any choice of R_x , R_y , and R_z gates. The angles of rotation are given by the Euler-angle decomposition of the combined rotation on the Bloch sphere.*

Theorem 6.4. *Any two-qubit unitary can be synthesised using at most three CX gates and 15 parametrised single-qubit gates (from any choice of R_x , R_y , and R_z), given by the KAK decomposition [68, 69].*

t|ket) implements the Euler and KAK decompositions by scanning the circuit graph for long sequences of gates over one or two qubits and replacing them whenever this helps to reduce CX count or overall gate count. Known closed-form expressions for manipulating Euler angles allow the single-qubit reduction to be performed on symbolic circuits. t|ket) does not currently support performing the KAK decomposition with symbolic gate parameters, or a generic Cartan decomposition for more than two qubits.

6.3. Macroscopic optimisations

Other optimisation procedures aim to identify high-level macroscopic structures in the circuit or alternative mathematical representations of different classes of circuits that are

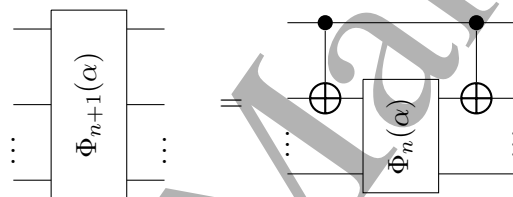
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easier to manipulate than individual gates. The general procedure here is to recognise these structures or subcircuits of the appropriate class and treat them as first-class gates. The algebra of the structure or representation can identify non-local optimisations on the original circuit. Efficient synthesis methods can then be applied to reduce these back down to primitive gates in a way that uses fewer CX gates, parallelises them better, or restructures the circuit to enable more peephole optimisations.

As simulation of molecular systems is a leading candidate application for NISQ devices, $\mathfrak{t}|\text{ket}\rangle$ implements a novel technique for optimising a new class of multi-qubit subcircuits, called *Pauli gadgets*, which occur frequently in chemistry circuits designed for this purpose.

Definition 6.5. The *phase gadget* $\Phi_n(\alpha)$ is a canonical representation of a multi-qubit operator of the form $e^{\frac{1}{2}i\alpha Z^{\otimes n}}$.

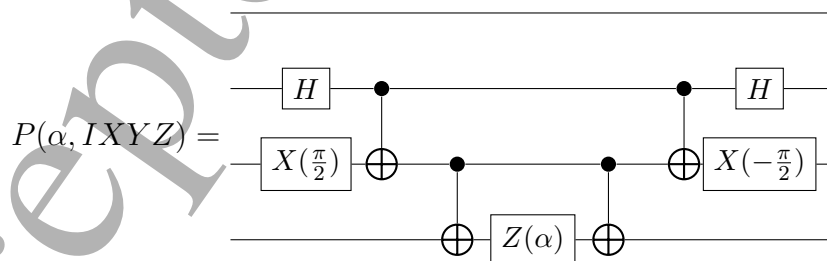
$$\Phi_1(\alpha) := Z(\alpha) \quad \Phi_{n+1}(\alpha) := (CX \otimes 1_{n-1}); (1_1 \otimes \Phi_n(\alpha)); (CX \otimes 1_{n-1})$$



Definition 6.6. The *Pauli gadget* $P(\alpha, s) := U(s); \Phi_{|s|}(\alpha); U(s)^\dagger$ is a canonical representation of a multi-qubit operator of the form $e^{\frac{1}{2}i\alpha s}$, where s is a string (tensor product) of Pauli operators and the unitary $U(s)$ is defined recursively:

$$U(Zs') := I \otimes U(s') \quad U(Ys') := X\left(\frac{\pi}{2}\right) \otimes U(s') \quad U(Xs') := H \otimes U(s')$$

Example 6.7. The simplest construction of a Pauli gadget is a single parameterised rotation gate conjugated by a cascade of CX gates and some single-qubit Clifford gates.



The authors have previously written a comprehensive account of Pauli gadgets and their use in $\mathfrak{t}|\text{ket}\rangle$ [70]. Such gadgets enjoy a powerful equational theory, giving rules for commutation, merging, and interaction with Clifford gates, which are easily proven using the ZX-calculus [71]. By recognising these structures in the input circuit, optimising the sequences of gadgets, and efficiently transforming them back to a standard gate set, we can achieve depth reductions greater than 50%. See Figure 20 for a summary of results comparing this technique in $\mathfrak{t}|\text{ket}\rangle$ to other compiler stacks for optimising circuits relating to electronic structure problems.

The first step when optimising with macroscopic structures is to identify good candidates in the circuit. It is obviously preferable to work with circuits that are already built from the structures to simplify this step. The integration of t|ket) with application software can make this possible by, for instance, allowing users to directly insert Pauli gadgets into the circuit using the corresponding box type.

Future versions of t|ket) will expand on this area of optimisations to cover other useful intermediate representations, including phase polynomials [38, 72], ZX-diagrams [73, 65, 74], Clifford tableaux [63, 75], and linear-reversible functions [76].

6.4. Example procedure

Each of these methods gives rise to a compiler pass that can either be invoked on its own or composed (as described in Section 5) into more effective routines. t|ket) comes with some predefined passes combining several of these optimisations. Each backend has a default compilation pass, which guarantees (as far as possible) that the output will be compatible with the backend’s hardware or simulator requirements; these passes include a small selection of the peephole optimisations for fast, basic gate reduction.

Figure 10 demonstrates how to compose the basic passes in `pytket`, recreating the effect of the pre-built `SynthesiseIBM` pass. Starting with `RebaseIBM` will decompose multi-qubit gates into a consistent gate set that is easier to manipulate. The `RemoveRedundancies` pass covers a handful of optimisations based on removing different types of redundant gates. Applying commutation rules can potentially uncover more candidates for removal, so the `simplify` routine is repeated until the gate count stops decreasing.

7. Mapping to Physical Qubits

Quantum computing devices have different constraints on possible operations between their physical qubits. Some hardware allow two-qubit (or higher order) operations between any set of physical qubits, while others do not. We define some physical qubits as being connected if the hardware’s primitive multi-qubit operations can be executed between them. The connectivity constraints of a hardware can be specified by an undirected graph $G_D = (V_D, E_D)$, where the vertices V_D are the physical qubits and edges E_D connect physical qubits which can interact. Figure 12 shows an example connectivity graph. As logical quantum circuits are usually written without considering these connectivity constraints, they typically must be modified before execution on a hardware to ensure that every logical multi-qubit operation is mapped to connected physical qubits. We define logical qubits and operations as those present in the logical quantum circuit and state the routing problem as finding a mapping of logical operations to allowed physical operations.

The routing problem is solved by permuting the mapping of logical qubits to physical qubits throughout a circuit’s execution, which is achieved by adding SWAP operations.

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```

1  from pytket.passes import (
2      CommuteThroughMultis, RebaseIBM,
3      RemoveRedundancies, USquashIBM, SequencePass,
4      RepeatWithMetricPass)
5
6  simplify = SequencePass([
7      RemoveRedundancies(),
8      CommuteThroughMultis(),
9      USquashIBM()
10 ])
11
12 mypass = SequencePass([
13     RebaseIBM(),
14     simplify,
15     RepeatWithMetricPass(simplify, lambda circ : circ.n_gates)
16 ])

```

Figure 10: Code example showing how individual optimisation passes can be composed into a more complex routine

Sometimes gate decompositions can be used to convert non-adjacent multi-qubit gates to distance 1 implementations. An example of this for the CX gate is shown in Figure 13. Finding an optimal solution to the routing problem in this manner is NP-complete in general [77]. Note that SWAP operations have different implementations on different hardware; ion trap devices have physical SWAPs while superconducting devices require the logical states to be transferred between two physical qubits through three CX gates, shown in Figure 14. A solution is reached when the logical circuit is modified such that there is an injective map of logical qubits to physical qubits, or *placement*, p where for every two-qubit gate acting on logical qubits (q, q') , the mapped physical qubits are connected on the connectivity graph G_D , or that $(p(q), p(q')) \in E_D$.

In some cases a placement p can be found that solves the routing problem without adding SWAP operations. Treating logical qubits as vertices and two-qubit interactions between them in the circuit as edges, we can form an interaction graph for a logical circuit $G_I = (V_I, E_I)$. If there is a subgraph monomorphism $p : V_I \rightarrow V_D$ which respects $(q, q') \in E_I \Rightarrow (p(q), p(q')) \in E_D$, then only a relabelling of logical qubits to physical qubits is required.

In Figure 15, a short example CX circuit is shown. This circuit can be mapped to the connectivity graph from Figure 12 without the addition of additional gates, as shown in Figure 16.

t|ket> solves the problem in two steps: finding an initial placement of logical qubits to physical qubits and subsequent addition of SWAP operations to the circuit. We consider this to be a *dynamic* approach, in contrast to *static* approaches [78, 79, 80], that

CliffordSimp Recognises patterns from Figure 9 to reduce CX count.

CommuteThroughMultis Commutes single-qubit gates through multi-qubit gates towards the front of the circuit.

KAKDecomposition Reduces two-qubit subcircuits to at most three CX gates using the *KAK* decomposition [68, 69].

OptimiseCliffordsZX Represents a Clifford circuit as a ZX-diagram, reduces it to a canonical form, and resynthesises it as a circuit.

OptimisePhaseGadgets Identifies phase gadgets [70] in the circuit and resynthesises them in a shallow manner, attempting to align CX gates between adjacent gadgets for further simplification.

PauliSimp Represents a circuit as a sequence of Pauli gadgets and a Clifford circuit, then resynthesises them pairwise [70].

RemoveRedundancies Removes redundant gates, including gate-inverse pairs, identity rotations, diagonal gates before measurements, and adjacent rotations that can be merged.

USquashIBM Merges adjacent U1, U2, and U3 gates into a single U1 or U3 gate by Euler-angle decomposition.

Figure 11: Some of the elementary optimisation passes available in t|ket)

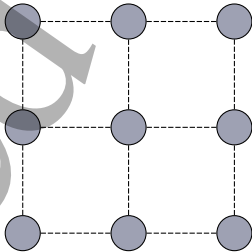


Figure 12: An undirected graph showing connectivity constraints for a hypothetical 9 qubit device.

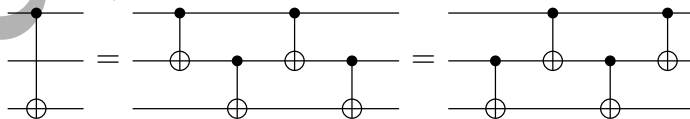


Figure 13: Distance 2 distributed CX gate and decompositions to distance 1 CX gates

partition circuits into parallelised slices of two-qubit interactions, and then use SWAP networks to permute logical qubits between placements that satisfy these slices.

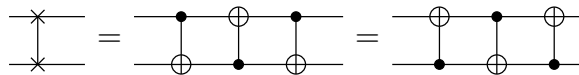


Figure 14: SWAP gate and decompositions to CX gates

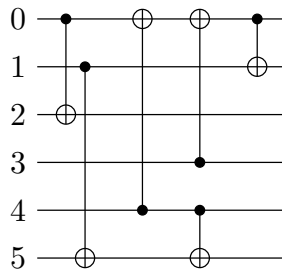


Figure 15: An example 6 qubit circuit with only CX gates.

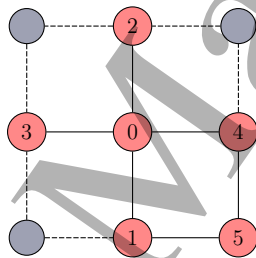


Figure 16: An example mapping of logical qubits in Figure 15 to physical qubits in Figure 12. This example satisfies the routing problem without logical circuit modification. The solid lines between red nodes represent physical interactions performed by the circuit; grey nodes and dashed lines are unused by the circuit.

7.1. Noise aware graph placement

The initial placement p is chosen to maximise the fidelity of the circuit implementation on the device, using both a proxy heuristic which tries to minimise additional gate overhead from routing, and an error heuristic which uses device error characteristics.

Indirectly, knowing only the connectivity graph G_D , candidate placements are chosen to minimise the number of gates the subsequent routing procedure will need to add, as these additional operations are most likely error prone two qubit gates. Routing will add gates dynamically as it proceeds through a circuit, and so it is in general not possible to predict which placements will correspond to the fewest gates added. As a heuristic, placements are found such that a maximum number of two-qubit operations at the beginning of the circuit can be completed with no SWAP gates added.

First this problem is cast as finding a subgraph monomorphism $p : V_I \rightarrow V_D$ which respects $(q, q') \in E_I \Rightarrow (p(q), p(q')) \in E_D$, for the interaction graph $G_I = (V_I, E_I)$ and device graph $G_D = (V_D, E_D)$. If a monomorphism cannot be found, the routine removes an edge from G_I belonging to the latest circuit slice and attempts the graph matching again. This iterates until a monomorphism is found.

Logical qubits $q \in V_I$ which no longer have any edges are removed from G_I , thus the subgraph monomorphism routine in practice produces a set of candidate *partial* placements: maps which only act on a subset of the logical qubits in the circuit. The subsequent routing procedure can accept this as input, and will naively place unmapped qubits near those they next interact with as it proceeds. As device architecture graphs G_D currently have, and will likely continue to have, large regular subgraphs, the set of matches can be large, especially when V_I is small compared to V_D .

If gate fidelity information for individual qubits is available for the target hardware, these candidate placements are scored for maximum expected overall fidelity and the highest scoring is chosen. In NISQ devices qubits and primitive gates often have highly heterogeneous error characteristics, using this to choose from the possible equivalent graph matches can result in a higher fidelity implementation of a given circuit on a given device. Section 9.2 compares the performance of different placement methods available in t|ket>.

7.2. Routing

Given an initial partial placement p , the routing algorithm adds SWAP operations until all logical operations satisfy connectivity constraints. As SWAP operations are added, p is permuted, and so we define a temporary placement p' which is the permutation of p from added SWAP operations up to some slice of circuit gates S .

Two-qubit gates in the circuit are iterated through in time order (via a topological sort of the DAG), finding the first set of two-qubit interactions (q, q') such that $(p(q), p(q'))$ does not respect G_D and no q is in multiple interactions. We call this set the first slice S_0 and log the permutation of p, p' , up to S_0 . The routing algorithm then aims to pick the optimal edge $e \in E_D$ of the connectivity graph to implement a SWAP operation on, given interacting logical qubits in S_0 and p' .

A set of candidate placements $\{p''_0, \dots, p''_n\}$ is constructed by permuting instances of p' with SWAP operations on edges in E_D . If an edge has no qubits in S_0 it is ignored. Each candidate placement is scored and the winning placement is chosen, with the scoring function based on the distance between interactions in S_0 given p'' . If there is no winning placement for S_0 then tied placements are scored for a new slice S_1 , where S_1 is the next set of set of two-qubit interactions (q, q') in the circuit such that $(p(q), p(q'))$ does not respect G_D and no q is in multiple interactions. If there is no winning placement for S_1 then tied placements are scored for a new slice S_2 . This is repeated until there is a winning placement p'' for some S_n .

The winning placement p'' is produced from p' via a permutation along its associated

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4 winning edge e . In most cases a SWAP operation is inserted along e directly before S_0
5 and a new first slice S_0 is found.

6
7 In some cases a distributed CX is considered instead: at least one of the logical
8 qubits associated with e is in an interaction (a two-qubit gate g) in S_0 . If g is a CX gate
9 and its logical qubits are at distance two on the device graph G_D (for the temporary
10 placement p') then a distributed CX may be added instead. A new two element set of
11 candidate placements is constructed comprised of p' and p'' and a similar scoring process
12 is implemented, comparing p' and p'' over multiple slices (S_0, S_1, S_2 and so on). If p'
13 wins g is replaced with a distributed CX and no SWAP operation is added. Else, if p''
14 wins the SWAP operation is added and p' replaced with p'' .

15
16 This whole process is then repeated, finding new first slices S_0 and new winning
17 placements p'' . The algorithm terminates when S_0 is returned empty.

18
19 The algorithm employs a high performance heuristic, which when coupled with an
20 efficient C++ implementation results in fast runtime. $t|\text{ket}\rangle$ routing typically performs at
21 least as well as other software solutions when comparing circuit size and depth [77].

22
23 Heterogeneity in NISQ device noise means a routed circuit with minimal SWAP
24 overhead may not always prove best though. Some solutions consider device noise [36, 81]
25 when routing, using gate fidelity information to produce a routed circuit with best execu-
26 tion fidelity. This motivated a routing solution we implemented that used a fidelity-based
27 heuristic approach to score and pick SWAP operations, for which the scoring method
28 used an estimation of the noise accumulated in realising all interactions in a slice S_0 .
29 The estimate was produced by finding SWAP paths required to permit interactions in
30 S_0 , and then calculating potential error accrued by each logical qubit in realising these
31 paths. In practice we found that the fidelity heuristic could not accurately determine
32 when diverging from adding the minimal number of SWAP gates would improve circuit
33 fidelity, and so in general aiming to minimise SWAP operation overhead provided better
34 results.

35 36 37 38 39 40 41 42 43 44 45 **8. Applications**

46
47 Quantum chemistry simulations are performed using a supplementary software package
48 called Eumen. This provides an interface between traditional quantum chemistry
49 problems and various hybrid classical-quantum algorithms, enabling effective chemistry
50 simulations on NISQ hardware using $t|\text{ket}\rangle$. For such simulations, Eumen accepts a
51 range of input parameters, such as the molecular or lattice geometry, system charge,
52 multiplicity restrictions, type of simulation, ansatz, optimisations, hardware backend,
53 and qubit mapping. $t|\text{ket}\rangle$ mediates between Eumen and the hardware on which the
54 quantum-algorithmic part of the chemistry simulation runs.

55
56 Eumen can compute optimal geometries and properties of the ground state or
57 excited states. For example, ground-state energies may be calculated using VQE or
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3

4 imaginary-time evolution methods. For excited-state calculations, one can use methods
5 such as quantum subspace expansion, reduced density matrix approximation, penalty
6 functions, and symmetry constraints [82]. These methods require the measurement of
7 either the expectation value of many-body operators or the overlap of two different states;
8 these measurements are performed by *t|ket⟩* using results from the quantum hardware.
9 The states may be prepared with hardware-efficient ansätze or the approximated circuit
10 representation of various physically motivated ansätze, such as UCCSD, k-UpCCGSD,
11 or the time evolution operator.
12

13 The depth of the state preparation circuit is significantly reduced by *t|ket⟩*'s ansatz-
14 specific optimisation methods, which can identify specific structures in circuits and
15 reduce the gate count required for their execution, as described in Section 6. Future
16 optimisation methods specific to QAOA instances are also planned. Construction of
17 such structures and subsequent optimisation is aided by boxes: for example, a Pauli
18 gadget can be added to a circuit in abstract form via a `PauliExpBox` operation. These
19 operations, and variational circuits in general, can make use of symbolic parameters
20 and compilation to simplify their use and speed up compilation. Finally, variational
21 algorithms, and other applications that use Hamiltonian estimation via calculation of
22 multiple terms of the Hamiltonian, can benefit from *t|ket⟩*'s back-end methods, which
23 allow compilation and submission of multiple circuits. Circuit execution on the back-end
24 can occur asynchronously, with results being retrieved for processing when execution is
25 complete.
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34 9. Benchmarks

35
36 In this section we provide some benchmarks of *t|ket⟩* compiler performance. First we
37 conduct benchmarks of end-to-end compiler performance, including comparisons with
38 other available quantum compilation tools. Secondly, we perform experiments on a
39 publicly available quantum device to determine whether noise-aware placement offers a
40 benefit. The full datasets and scripts used for generating these results can be found at
41 https://github.com/CQCL/tket_benchmarking.
42
43
44

45 9.1. End-to-end compilation

46 We present a series of benchmarks of end-to-end compiler performance on a set of circuits,
47 and compare the performance of *t|ket⟩* with that of two widely-used alternatives, Qiskit
48 and the Quilc compiler, which are able to do both general circuit optimisation and
49 routing.
50
51

52 We define end-to-end compilation as the process of translating a circuit, presented
53 in OpenQASM, and outputting an equivalent circuit that has been optimised and has
54 the relevant device constraints satisfied, i.e. has been routed and converted to the correct
55 gate set. We do not include high-level algorithm design or low-level pulse optimisation
56 which are respectively beyond the scope of a compiler and only in its infancy as a research
57
58
59
60

topic.

9.1.1. Benchmark circuits The benchmark set is made up of three test sets, with circuits of at most 10^4 initial gates. (This threshold was chosen as circuits larger than this are several orders of magnitude too large for near-term devices. In addition, the runtimes of Qiskit and Quilc already reach several minutes per circuit at this range, making it impractical to benchmark against the larger circuits.)

- (i) The IBM test set is a series of circuits published as part of the Qiskit Developer Challenge, a public competition to design a better routing algorithm. These circuits are not amenable to significant peephole optimisation to restrict the impact this can have and focus on the efficiency of the routing algorithm. However, they were designed to be easily verified for correctness by mapping the $|0\rangle^{\otimes n}$ state into some other computational basis state; as such, these tests could be circumvented by applying state preparation optimisations. The IBM circuit set in OpenQASM can be found at https://github.com/iic-jku/ibm_qx_mapping.
- (ii) The UCCSD test set is a series of circuits for electronic-structure calculations. They correspond to VQE circuits for estimating the ground state energy of small molecules by the Unitary Coupled Cluster approach [83], using some choice of qubit encoding (Jordan–Wigner, parity mapping, or Bravyi–Kitaev [84]). These circuits are very amenable to optimisation, as well as requiring routing. They are representative of algorithms that have been proposed as suitable for application on NISQ devices [83], and were generated using Qiskit Aqua. The set used here updates and extends that used by Cowtan *et al* [70], whose OpenQASM files can be found at <https://github.com/CQCL/pytket>.
- (iii) The Product Formula test set is a series of circuits for Hamiltonian simulation. These circuits are thought to be candidates for quantum advantage [85], and were used as a test case for the circuit optimizer by Nam *et al* [38]. They are given in the ASCII format of the Quipper language, and each is formed of a repeated subroutine. We convert this subroutine to a quantum circuit in OpenQASM. We included circuits both before and after optimisation by Nam *et al* [38], since they still require mapping to the architecture and have potential for further optimisation. We had to further edit the circuits to ensure the rotation angles of gates exceeded Qiskit’s very high cutoff (10^{-5}), below which the rotations would be treated as identities, making these circuits almost trivial. These circuits contain some Pauli gadgets, but also have large regions which are not amenable to this kind of optimisation. These circuits can be found at <https://github.com/njross/optimizer>.

The full collated benchmark set can be found at https://github.com/CQCL/tket_benchmarking.

9.1.2. Experiments We compare compilation for four different architectures:

- 1) The fully-connected graph, for which no routing is required.

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- 2) The connectivity graph of IBM Rochester, a 53-qubit device.
- 3) The connectivity graph of Google’s 53-qubit Sycamore device.
- 4) The Rigetti Aspen 16-qubit architecture. For this case, all circuits with more than 16 qubits were discarded.

These connectivity graphs are shown in Figure 17. Two end-to-end comparisons were made:

- (i) To compare *t|ket* to other available compilation software, the default compiler passes of Qiskit (optimisation level 3) and Quilc, and the recommended generic pass for *t|ket* (`FullPeepholeOptimise`, followed by the default qubit mapping pass, `SynthesiseIBM`, and the rebase pass into the desired gateset, henceforth referred to as ‘FullPass’) were applied to all available circuits.
- (ii) To demonstrate the necessity of appropriate usage of situational compiler optimisations, we compare *t|ket*’s UCCSD-specific pass (the `PauliSimp` pass followed by the ‘FullPass’ routine, henceforth dubbed ‘ChemPass’) against the default Qiskit and Quilc passes, on the UCCSD circuits (test set (ii) above). These circuits contain adjacent Pauli gadgets, and we demonstrate that the reduction in two-qubit gate count and depth can be substantial compared to optimising naively.

The benchmarks were performed using *t|ket* v0.4.1, Quilc v1.16.3 and Qiskit Terra v0.12.0. All results were obtained using a machine with a 2.3 GHz Intel Core i5 processor and 8 GB of 2133 MHz LPDDR3 memory, running MacOS Mojave v10.14.

9.1.3. Metric The figures of merit for these benchmarks are two-qubit gate count and depth. As described in Section 6, two-qubit gates have error rates an order of magnitude higher than single-qubit gates for existing architectures [61], and so the counts and depths are reasonable proxies for the overall expected error rates of a circuit run on a NISQ device.

We defined end-to-end compilation earlier, including the conversion to the device’s native gate set. Google’s Sycamore device can accept CZ gates natively as a two-qubit operation, whereas IBM Rochester only supports CX gates. As only single-qubit Hadamard gates are required for conversion between CX and CZ gates, we discount the gate-conversion step, and accept either gate set for the two-qubit gate-count and depth metrics. Thus, unlike total gate count, for these backends the two-qubit gate count should be independent of final basis set chosen, meaning the comparison between architectures is purely based on connectivity. The exception here is the Rigetti Aspen device which can use both CZ gates and the XY family (including the iSWAP gate) natively. Since these can be obtained with similar fidelities, the simple two-qubit gate count is justified in weighting their costs equally.

9.1.4. Results Two-qubit gate count and depth benchmark results for default compilation are shown in Figures 18 and 19. The corresponding results for chemistry-specific

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3 $t|ket\rangle$: A Retargetable Compiler for NISQ Devices 28

4 compilation are shown in Figures 20 and 21 respectively. Each figure includes results
5 for all three compilers and all four target backends. The figure of merit in each is
6 multiplicative overhead of two-qubit gate count or depth, i.e. the ratio of the values
7 before and after compilation.
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10 The *FullConnectivity* case shows the results without the effects of routing. For
11 default compilation passes the majority of benchmark circuits show little to no change in
12 the number of two-qubit gates, demonstrating the difficulty of entangling-gate reduction
13 with generic optimisation passes. In cases where gains can be made, the optimisations in
14 $t|ket\rangle$ are able to make larger reductions than the other compilers, and are able to make
15 reductions in more instances.
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18 In contrast, as shown in Figures 20 and 21, adding the *PauliSimp* pass leads to
19 more significant reductions on the UCCSD circuits, even after mapping onto a device
20 with restricted connectivity. However, on other classes of circuits that don't resemble
21 the UCCSD set, adding this optimisation can cause a drastic drop in performance, by
22 trying to fit them to this model, and potentially making them less amenable to routing.
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25 Across the end-to-end compilation results targeting restricted-connectivity
26 architectures, the general ranking of performance is: $t|ket\rangle$, followed by Quilc (with special
27 note of their performance for the Aspen device), with Qiskit consistently introducing
28 a very high gate overhead. The results are sufficiently spread that for circuits viable
29 for execution on near-term devices, the choice of compiler and pass sequence makes a
30 significant difference to the size of the final circuit. By comparing to the *FullConnectivity*
31 case, we can see that these differences are dominated by differences in routing performance.
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35 9.2. Noise-aware placement

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37 In Section 7.1 we outlined *graph placement* (GP), a subgraph-monomorphism-based
38 method for finding initial qubit mappings, and *noise-aware graph placement* (NAGP),
39 a fidelity-aware heuristic for scoring those placements. As the effectiveness of these
40 methods depends strongly on the error characteristics of physical devices and the fidelity
41 with which they execute the circuit, we assess and compare their performance by running
42 benchmark circuits on a device with and without the mapping methods applied.
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47 *9.2.1. Benchmark circuits* At the time of writing, it is difficult to implement many
48 common algorithms on publicly-available quantum devices and extract a signal from
49 the noise; this is why implemented algorithms are usually variational. In order to test a
50 large enough data set to have confidence in measured differences, we instead choose to
51 implement random circuits of constrained sizes.
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53 Sets of random circuits are parameterised by number of qubits and total number of
54 gates. Each circuit is generated by uniformly sampling gates from $\{X, Y, Z, H, T, S, CX\}$,
55 and uniformly sampling from all qubits for single-qubit gates and from the set of pairs of
56 all qubits in the case of a CX. As the two-qubit operations are the most error-prone [61],
57 samples that included no CX gates were excluded. Circuit sets of qubit numbers of 4
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and 8, and gate counts of 20, 40, 60 and 80, were generated. Circuits over 4 qubits with 80 gates were too deep and therefore noisy for effective comparison of methods, so were omitted, leaving a total of 7 sets each with 90 samples.

9.2.2. Experiments As described in Section 7, *placement* is the task of finding initial maps from logical qubits of the circuit to physical qubits of the device, and *routing* is the addition of two-qubit gates to satisfy the connectivity constraints of the device. For these experiments, each benchmark circuit was compiled in three different ways, corresponding to three methods of calculating an initial partial placement: “None” (corresponding to no qubits placed, therefore relying on default on-the-fly placement performed by routing), “Graph Placement”, and “Noise-Aware Graph Placement”. Each placed circuit was then compiled with identical routing and post-routing optimisation passes from t|ket).

All circuits were run on the publicly-available `ibmq_16_melbourne` device via the IBM Q Experience [88]. Correspondingly, compilation also included translating the circuits to the IBM Q gate set of $\{U_1, U_2, U_3, CX\}$. Programs for execution on an IBM Q device are sent via the API as “jobs”, with a maximum of 75 circuits in each job. All compiled circuits that corresponded to the same initial circuit were evaluated consecutively and within the same job, to mitigate the effects of device-characteristic deviations between jobs on the method comparisons. Each compiled circuit was evaluated with the maximum 8192 shots.

9.2.3. Metric The ideal metric for comparing the placement methods is overall fidelity of the implemented circuits. However, measurement of this involves a number of circuit measurements that scales exponentially with qubit number and is infeasible for large experiment sets [89]. Instead, we choose a metric that can quantify the distance between the distribution of measurements in the computational basis and the same distribution generated from an ideal simulation. This methodology requires classical resources that scale exponentially with qubit number, as it involves simulation of all circuits. However, as the techniques proposed are only relevant for NISQ-era error rates and device heterogeneity, we expect the number of qubits to remain low enough for applicability of the proposed methods while the same levels of heterogeneity also hold.

The Kullback–Leibler (KL) divergence has been used for comparing measured and simulated distributions [90]. However, it has some shortcomings. The KL divergence between two distributions P, Q over values x_i is defined as:

$$D_{\text{KL}}(P, Q) = \sum_i P(x_i) \log \frac{P(x_i)}{Q(x_i)}$$

This is asymmetric between P and Q . More importantly, it is defined to be infinite if $\text{support}(P) \not\subseteq \text{support}(Q)$. A standard technique to account for this is padding zeroes in the distribution with small values and renormalising. Although this would still show qualitative difference, the absolute value would depend on the free parameter of tuning, so would not be a useful quantitative measure.

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We instead use the Jenses–Shannon divergence D_{JS} [91], which is closely related to D_{KL} . For distributions P, Q and $M = \frac{1}{2}(P + Q)$ it is defined by:

$$D_{\text{JS}}(P, Q) = \frac{1}{2}D_{\text{KL}}(P, M) + \frac{1}{2}D_{\text{KL}}(Q, M)$$

This is a symmetric, finite function with bounds $0 \leq D_{\text{JS}}(P, Q) \leq 1$ when the base-2 logarithm is used.

9.2.4. Results Figure 22 plots the mean value of D_{JS} over each benchmark circuit set for the three placement methods, each benchmark set parameterised by qubit number and gate count. In general, GP is seen to reduce the mean D_{JS} when compared to no initial placement; this can be explained by GP reducing the number of error-prone two-qubit gates that need to be added to map the circuit. We also see that scoring of these placements using device-reported error information by NAGP is able to make further significant reductions to D_{JS} , suggesting that such exploitation of device heterogeneity is a worthwhile avenue of exploration for maximising near-term device use.

Comparing 4-qubit and 8-qubit results, D_{JS} means are higher in the 8-qubit case, as expected, as more qubits are entangled together in general and so the system is more prone to error. In the 8-qubit case, D_{JS} is also seen to monotonically increase with gate count, also matching expectations. The peak for D_{JS} mean at 40 gates for 4 qubits, for all placement methods, is unexpected and warrants further investigation.

10. Conclusions and Future Work

In this paper we have described CQC’s compiler system `t|ket>`, with particular emphasis on its transformation engine and qubit mapping routine. We showed that `t|ket>` offers significant improvement in terms of gate count and gate depth over other comparable compiler systems when evaluated on realistic quantum circuits and real quantum architectures. Further, for devices with heterogeneous gate and qubit error rates `t|ket>` can use the component-level fidelity information to appreciably improve overall device performance. For NISQ-era quantum computing such performance differences may be the margin between success and failure.

The flexible design of `t|ket>` presents many possibilities for future improvements. Here we sketch three promising directions.

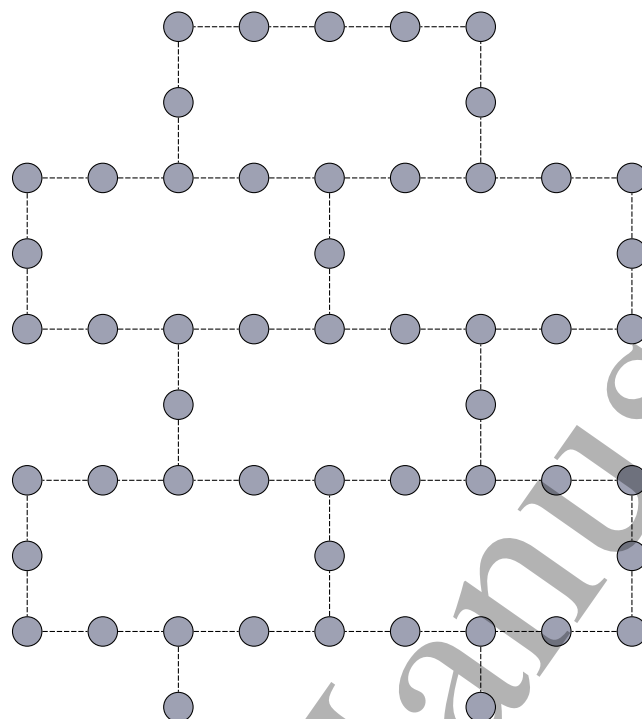
For all-to-all connectivity, the `PauliSimp` pass achieved staggering depth reductions on the chemistry benchmark set, which is not totally surprising because it was designed to exploit the recurring structures found in UCCSD ansätze. However there is a lot of scope to improve this method, particularly if the Pauli Gadgets are treated as multi-qubit gates and synthesised by the architecture-aware phase of the compilation process, solving the problem mentioned in Section 9.1.4. More generally we expect the use of higher level “big gates”, equipped with their own equational theory, and tuned to particular algorithms or ansätze (for example QAOA instances) to yield similar improvements.

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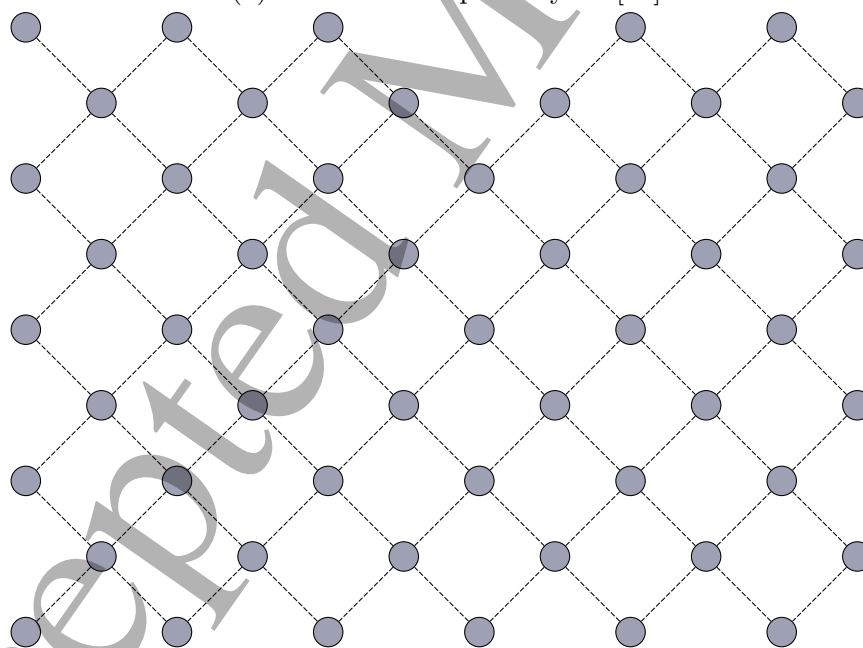
4 This kind of application-specific optimisations cannot be discovered by working with
5 random circuits and require real use cases.
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7 Recent results on quantum volume [58] suggest that available qubit numbers already
8 surpass the gate fidelity by such a margin that a large fraction of the qubits cannot
9 effectively be exploited. This suggests that, in the near term at least, extremely shallow
10 circuits will be required. One possible route to such depth reduction is to exploit large
11 numbers of ancillary qubits, combined with techniques from measurement-based quantum
12 computation [92] to effectively trade time for space. The ZX-calculus [71] is already
13 incorporated into *t|ket*) and has proven an effective tool for MBQC calculations in the
14 past [73, 93, 94].
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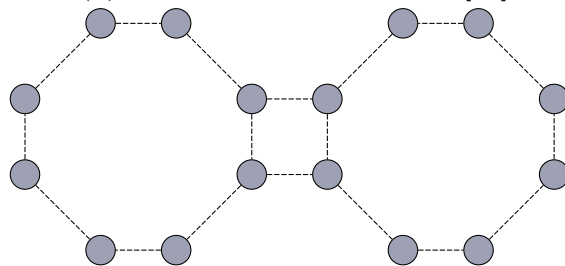
18 Finally, we will look at techniques to attack the noisiness of NISQ devices head
19 on. Incorporating a very naive noise model into *t|ket*)’s qubit placement algorithm
20 (Section 9.2) made a noticeable difference our results. However it is well known that the
21 noise channels in real devices are much more complex and more difficult to characterise
22 [95, 60, 96]. Incorporating better analysis of the device errors into the compilation
23 process, and techniques to suppress and mitigate errors [25, 23, 22] surely have a role to
24 play in the compilation process for NISQ devices for the foreseeable future.
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(a) Rochester 53-qubit layout [86].

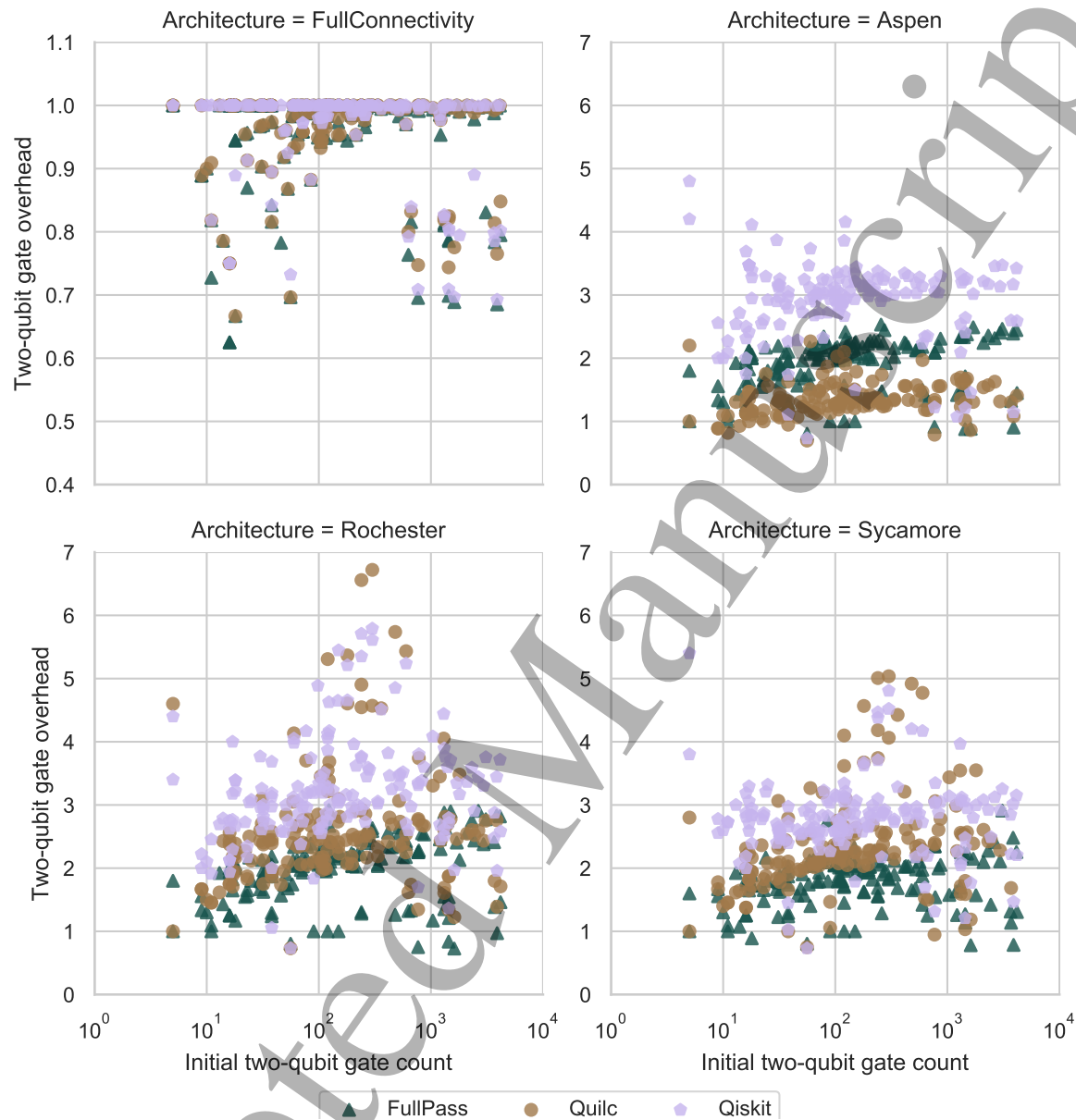


(b) Sycamore 53-qubit layout [61].



(c) Rigetti Aspen 16-qubit layout [87].

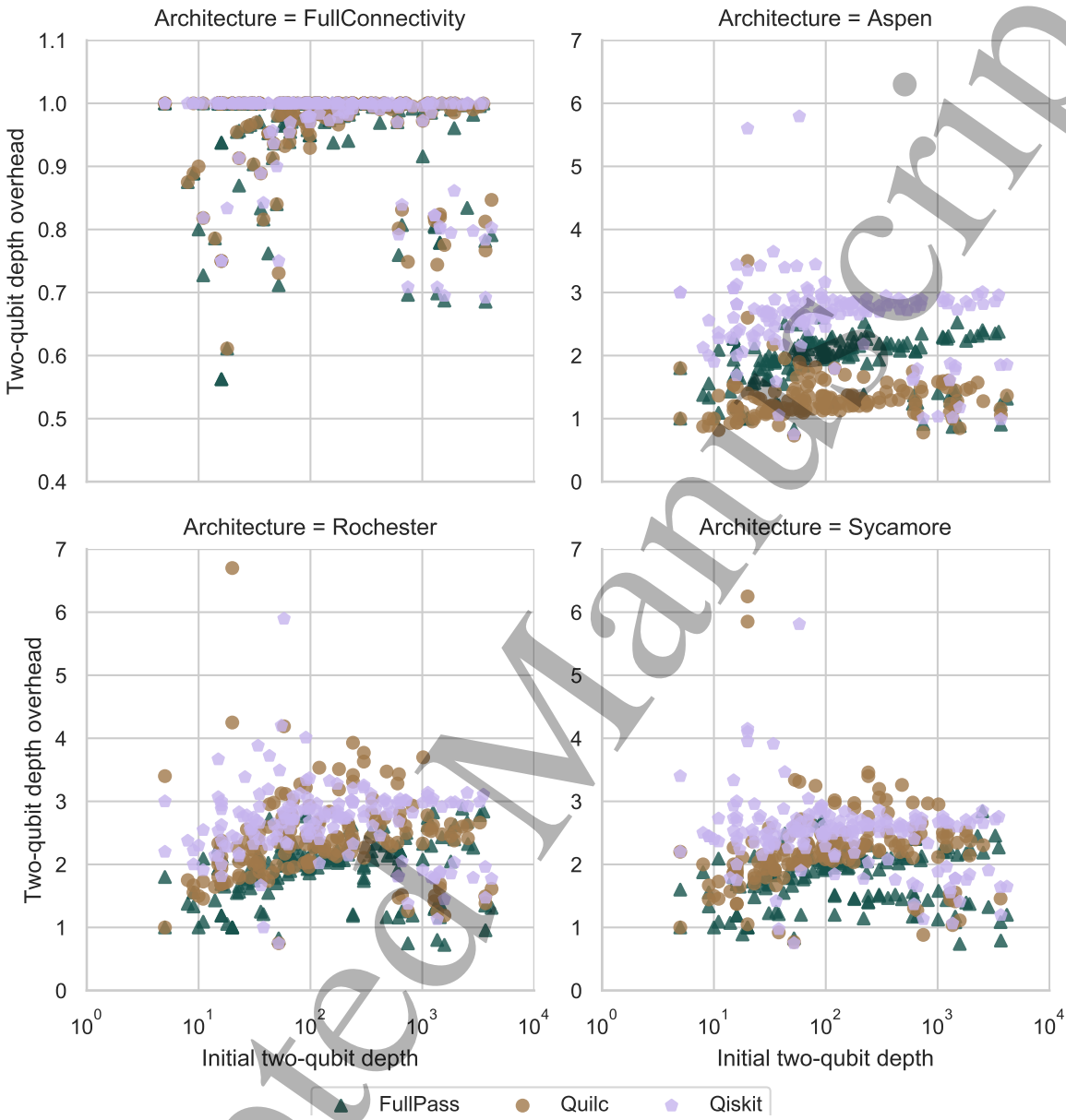
Figure 17: Device connectivity layouts used in end-to-end compilation benchmarks.



	FullConnectivity	Aspen	Rochester	Sycamore
FullPass	0.939 ± 0.011	1.864 ± 0.039	1.975 ± 0.042	1.773 ± 0.034
Quilc	0.949 ± 0.010	1.362 ± 0.022	2.595 ± 0.074	2.343 ± 0.061
Qiskit	0.958 ± 0.010	2.896 ± 0.052	3.201 ± 0.065	2.789 ± 0.047

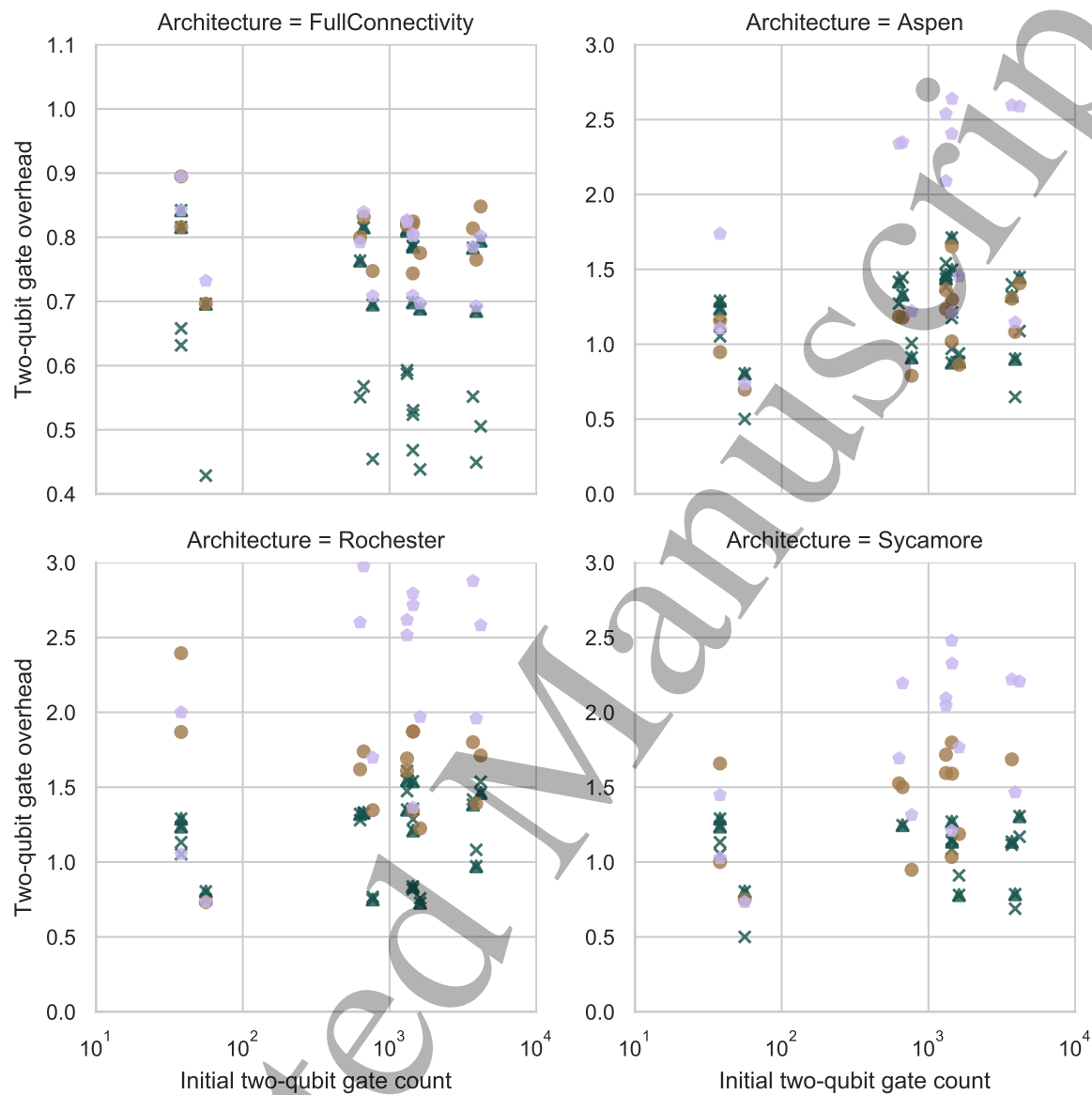
Figure 18: Default compilation benchmarks over all benchmark circuits. The multiplicative overhead in two-qubit gate count from input circuit to output circuit is plotted against input two-qubit gate count. The table shows means across the circuit sets and associated standard error. In general, routing induces a larger-than-1 overhead, but for *FullConnectivity* when no routing is required it is 1 or below. ‘FullPass’ refers to the recommended t|ket) routine, consisting of the `FullPeepholeOptimise` pass, followed by the corresponding qubit mapping pass, `SynthesiseIBM` and rebasing to the final gate set.

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	FullConnectivity	Aspen	Rochester	Sycamore
FullPass	0.937 ± 0.011	1.844 ± 0.040	1.924 ± 0.041	1.780 ± 0.038
Quilc	0.950 ± 0.010	1.312 ± 0.027	2.418 ± 0.063	2.223 ± 0.053
Qiskit	0.955 ± 0.010	2.631 ± 0.065	2.748 ± 0.081	2.473 ± 0.045

Figure 19: Default compilation benchmarks over all benchmark circuits. The multiplicative overhead in two-qubit gate depth from input circuit to output circuit is plotted against input two-qubit depth. The table shows means across the circuit sets and associated standard error. In general, routing induces a larger-than-1 overhead, but for *FullConnectivity* when no routing is required it is 1 or below. ‘FullPass’ refers to the recommended t|ket) routine, consisting of the `FullPeepholeOptimise` pass, followed by the corresponding qubit mapping pass, `SynthesiseIBM` and rebasing to the final gate set.

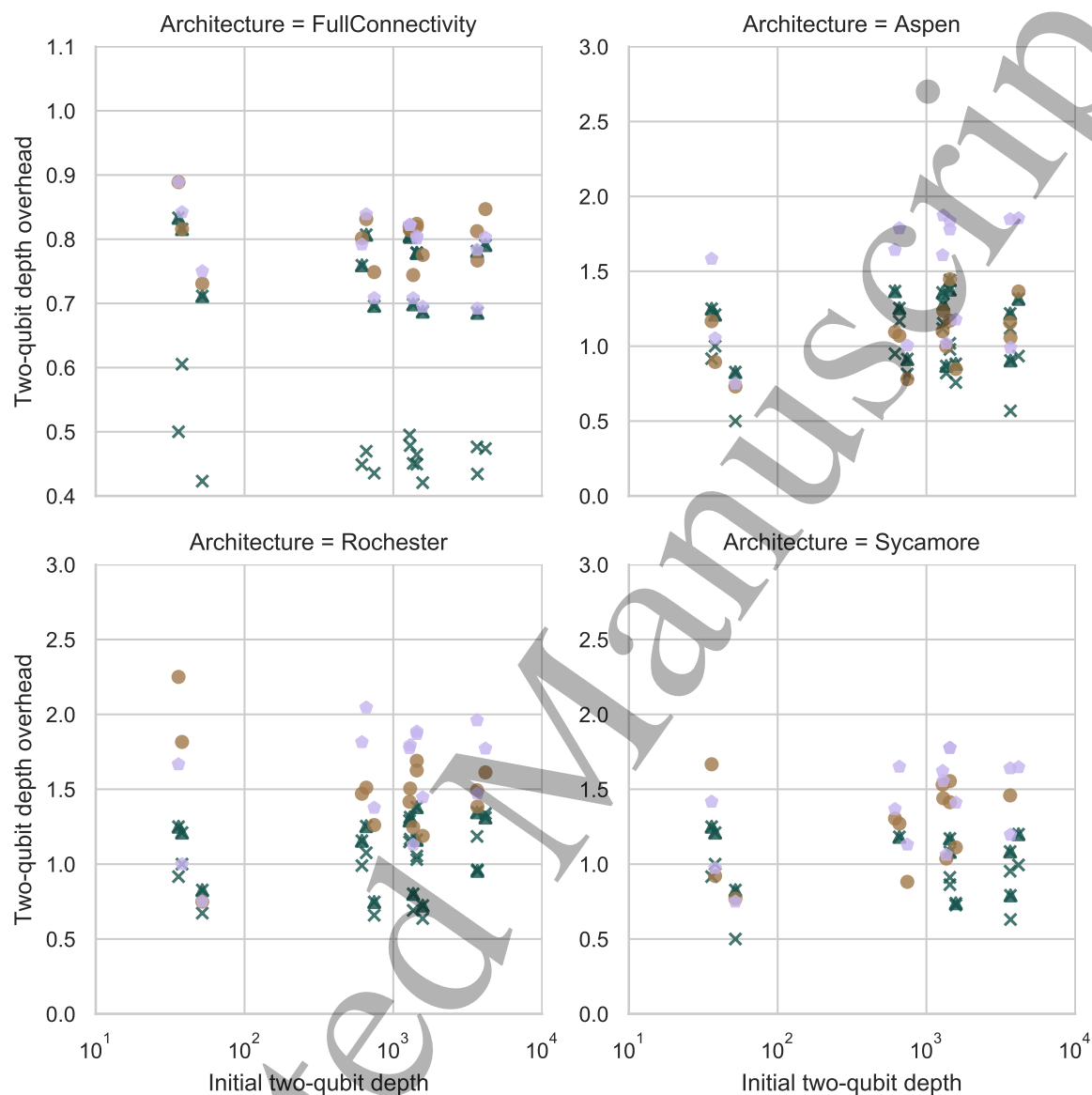


	FullConnectivity	Aspen	Rochester	Sycamore
FullPass	0.765 ± 0.014	1.236 ± 0.074	1.184 ± 0.074	1.099 ± 0.070
ChemPass	0.647 ± 0.025	1.176 ± 0.052	1.180 ± 0.052	1.042 ± 0.053
Quilc	0.801 ± 0.013	1.145 ± 0.065	1.614 ± 0.098	1.384 ± 0.097
Qiskit	0.783 ± 0.016	1.877 ± 0.173	2.163 ± 0.180	1.747 ± 0.136

Figure 20: Chemistry-specific compilation benchmarks over the UCCSD test set. The multiplicative overhead in two-qubit gate count from input circuit to output circuit is plotted against input two-qubit gate count. The table shows means across the circuit sets and associated standard error. ‘ChemPass’ refers to application of the t|ket) PauliSimp pass, followed by the ‘FullPass’ routine.

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	FullConnectivity	Aspen	Rochester	Sycamore
FullPass	0.762 ± 0.013	1.165 ± 0.056	1.115 ± 0.061	1.054 ± 0.061
ChemPass	0.615 ± 0.029	1.043 ± 0.044	1.042 ± 0.043	0.949 ± 0.049
Quilc	0.803 ± 0.011	1.074 ± 0.052	1.481 ± 0.085	1.258 ± 0.080
Qiskit	0.783 ± 0.016	1.454 ± 0.104	1.584 ± 0.098	1.398 ± 0.081

Figure 21: Chemistry-specific compilation benchmarks over the UCCSD test set. The multiplicative overhead in two-qubit depth from input circuit to output circuit is plotted against input two-qubit depth. The table shows means across the circuit sets and associated standard error. ‘ChemPass’ refers to application of the $t|ket\rangle$ PauliSimp pass, followed by the ‘FullPass’ routine.

$t|ket\rangle$: A Retargetable Compiler for NISQ Devices

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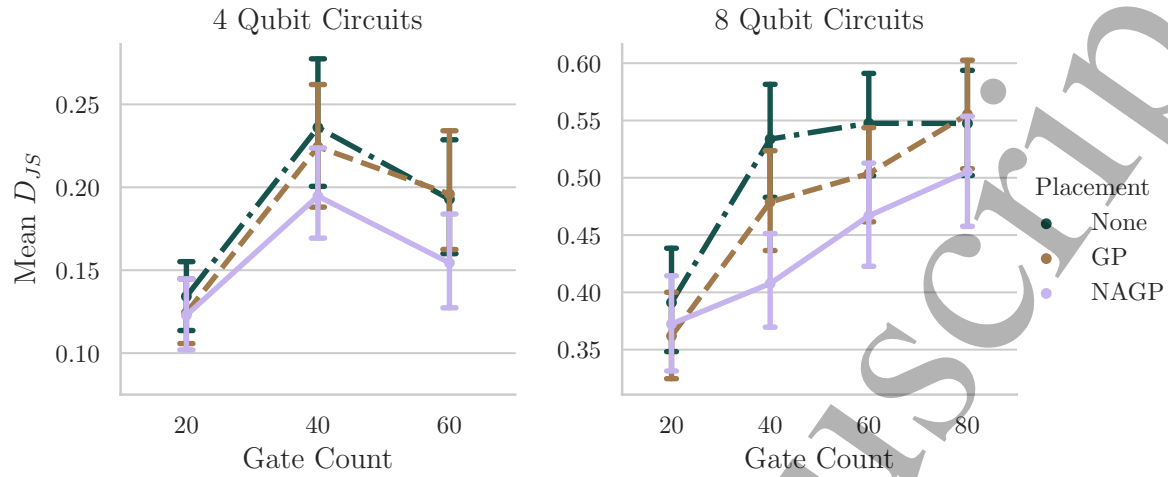


Figure 22: Experimental comparison of placement methods. “None” refers to the case of no initial placement of qubits, “GP” to partial placement via graph placement, and “NAGP” to noise-aware graph placement. Each data point corresponds to a mean Jensen–Shannon divergence D_{JS} of measured distribution from ideal distribution, over the 90 random input circuit samples of the given size, compiled and executed on the device with the three different placement methods.

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