# TCAD simulation vs. experimental results in FDSOI technology: From advanced mobility modeling to 6T-SRAM cell characteristics prediction

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***Abstract*—We present TCAD simulations based on advanced mobility modeling including Surface Roughness (SR) and Remote Coulomb Scattering (RCS) effects, quantum correction and short channel effects. From these calibrated models, FDSOI 6T-SRAM cells are simulated and compared to experimental data. The very good agreement achieved between simulations and electrical data on both mobility and electrical figures of merit (device and SRAM) offers major opportunities for predictive design based on TCAD simulations.**

## I. INTRODUCTION

Giving the various MOSFET architectures under development (FDSOI, Ultra Thin BOx-FDSOI, nanowire, ...), it becomes necessary to have a predictive TCAD tool to assess and quantify the relevance of these different options for advanced nodes (22nm, 16nm, 13nm …) and for small circuit applications [1-3]. Indeed, provided advanced physical models and experimental data validation, TCAD simulation tool is of great interest for i) technological support for advanced nodes development (static and dynamic performances evaluation through single device and ring oscillator, respectively) ii) design and validation of innovative small circuit architectures (typically SRAM cell) iii) providing the input necessary for the establishment of predictive modelcard for advanced nodes. In this work, FDSOI technology is studied and TCAD simulations are systematically compared to recent 300mm wafer FDSOI technology experimental data [4-5] from mobility measurements to 6T-SRAM cell static noise margins. In section II, we present the quantum correction and the improved electron and hole low field mobility introduced in TCAD simulations. Then, after calibrating short channel effects, nFDSOI and pFDSOI electrical characteristics are compared to experimental data in section III. Finally, section IV presents a comparison between TCAD and experimental results obtained on a 6T-SRAM cell, while in section V the conclusions and perspectives of this work are drawn.

## II. QUANTUM CORRECTION & MOBILITY

### A. Quantum correction

The Bohm Quantum Potential (BQP) [6-7] calibrated on self-consistent Schrödinger-Poisson simulations is used as quantum corrected potential. Inversion charge as a function of gate voltage resulting from experiments [4-5] and TCAD without and with quantum correction is plotted in Figure 1. The excellent agreement between experiments and TCAD with quantum correction shows that the inversion thickness is properly taken into account thanks to this correction.

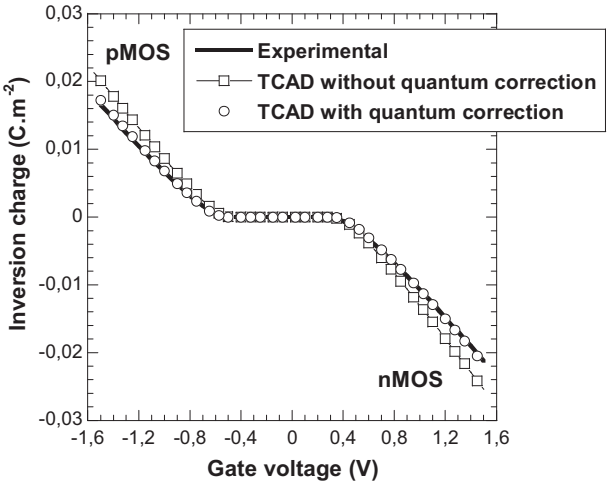


Figure 1. Inversion charge as a function of gate volatge resulting from (line) experiments, TCAD simulations (square) without and (circle) with quantum correction.

### B. Mobility

At low electric field, the usual Lombardi mobility model [8] has been improved through Mathiessen's rule (1) by including i) usual silicon doping-dependent mobility expression and parameters (2), ii) phonon limited mobility using Takagi's expression and parameters (3) [9] that are in accordance with experimental measurements [10], iii) surface roughness limited mobility according to experimental data [10] (4), iv) Remote Coulomb Scattering (RCS) effect due to high-$k$/$SiO_2$ dielectric gate stack (1.2nm equivalent oxide thickness) in accordance with Kubo-Greenwood approach [11-12] (5).

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$$\mu_{eff}^{-1} = \mu_{dop}^{-1} + \mu_{ph}^{-1} + \mu_{sr}^{-1} + \mu_{rcs}^{-1} \quad (1)$$

where $\mu_{dop}$, $\mu_{ph}$, $\mu_{sr}$ and $\mu_{rcs}$ are the doping-dependent mobility, the phonon scattering-dependent mobility, the surface roughness scattering-dependent mobility and the RCS mobility, respectively.

$$\mu_{dop}^{-1} = \left( \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N/N_{ref})^{\theta_{imp}}} \right)^{-1} \quad (2)$$

$$\mu_{ph}^{-1} = \left( \frac{\mu_{0ph}}{E_{eff}^{\theta_{ph}}} \right)^{-1} \quad (3)$$

$$\mu_{sr}^{-1} = \left( \frac{\mu_{0sr}}{E_{eff}^{\theta_{sr}}} \right)^{-1} \quad (4)$$

$$\mu_{rcs}^{-1} = \left( \frac{\mu_{0rcs}}{\left( \frac{E_{eff}}{\gamma_1 (q.N_{fix})^{\gamma_2}} \right)^{\theta_{rcs}}} \right)^{-1} \quad (5)$$

where $\mu_{min}$, $N_{ref}$ and $\theta_{imp}$ are the usual silicon parameters [7], $\mu_{0ph}$ and $\theta_{ph}$ are in accordance with [9] and experimental measurements [10], $\mu_{0sr}$ and $\theta_{sr}$ are in good agreement with experimental data [10], $\mu_{0rcs}$, $\theta_{rcs}$, $\gamma_1$, $\gamma_2$ have been calibrated to reproduce Kubo-Greenwood results [11-12], $\mu_{max}$ and $N_{fix}$ are fitting parameters and $E_{eff}$ is the effective field.

In Figure 2, low field electron and hole mobility as a function of inversion charge obtained by TCAD simulations are compared to experimental data on long and wide FDSOI devices [4-5]. The excellent agreement shows that the mobility is well described by our improved mobility model on a large range of inversion charge.

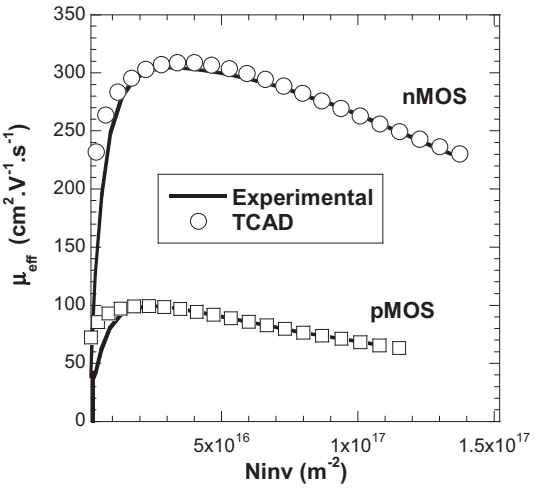


Figure 2. Low field electron and hole mobility as a function of the inversion charge resulting from (line) experiments and (symbol) TCAD simulations on long and wide device.

## III. FDSOI DEVICES

The simulated device is an undoped FDSOI MOSFET with a 6nm silicon film thickness, a 1.2nm $SiO_2$ equivalent oxide thickness and a 145nm BOx thickness as represented in Figure 3. Electrical characteristics for FDSOI nMOSFETs and pMOSFETs devices ranging from 1μm gate length down to 30nm have been simulated at Vds=50mV and Vds=1.0V.

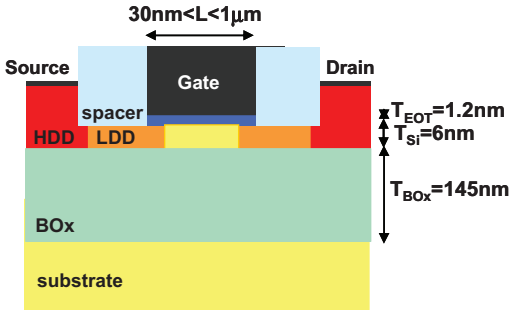


Figure 3. Schematic of the simulated undoped FDSOI devices.

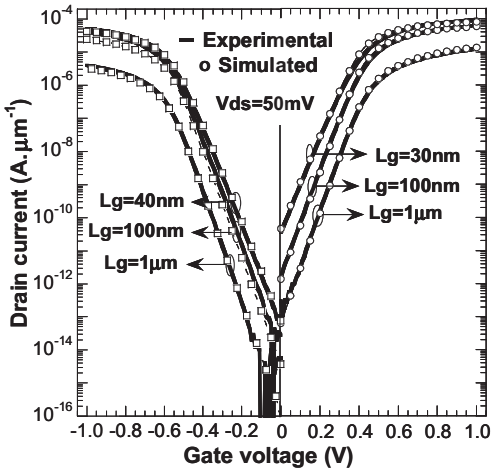


Figure 4. nMOS and pMOS $I_{DS}$-$V_{GS}$ characteristics at $V_{DS}$=50mV, resulting from (line) experiments and (symbol) TCAD simulations.

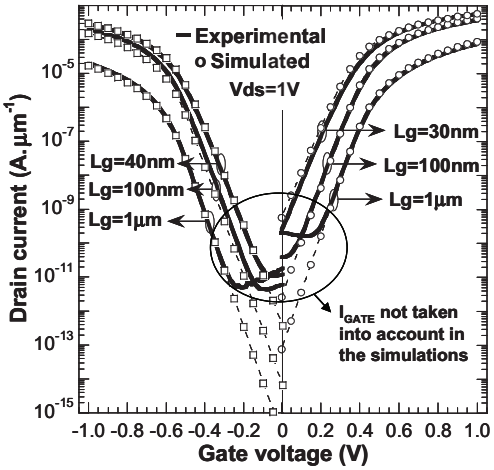


Figure 5. nMOS and pMOS $I_{DS}$-$V_{GS}$ characteristics at $V_{DS}$=1.0V, resulting from (line) experiments and (symbol) TCAD simulations.

Drift-diffusion with BQP correction, usual Shockley-Read-Hall generation-recombination rate and the improved low field mobility model have been used in TCAD simulations. Short channel effects (SS, DIBL) have been calibrated on experimental data by adjusting access doping levels and profiles. The simulated and experimental [4] electrical characteristics for nFDSOI and pFDSOI are plotted in Figures 4 and 5. Considering that the gate tunneling leakage current is not modeled, a very good agreement is obtained between simulations and experiments even for aggressive gate lengths (down to 30nm).

## IV. FDSOI 6T-SRAM

The above ingredients are used in TCAD MixedMode [7] for simulating the 6T-SRAM bit-cell represented in Figure 6.

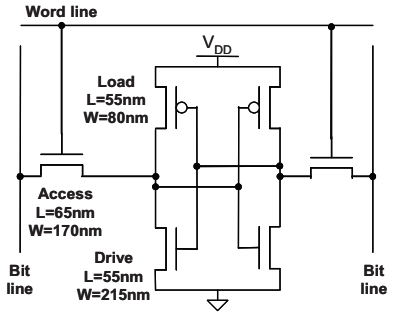


Figure 6. 6T-SRAM cell sizing.

Figure 7 compares experimental and simulated Static Noise Margin (SNM) and Retention Noise Margin (RNM) butterfly obtained at Vdd=1.1V. On this same bit-cell, Figure 8 shows the extracted SNM and RNM at different supply voltage Vdd.

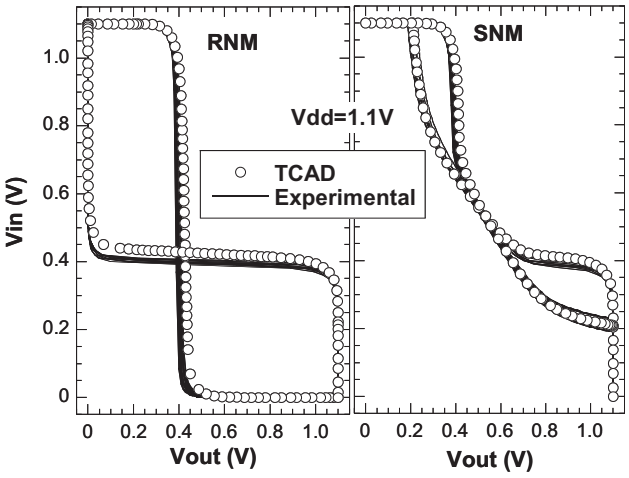


Figure 7. Retention Noise Magin (RNM) and Static Noise Margin (SNM) butterfly at Vdd=1.1V resulting from (line) experiments and (symbol) TCAD simulations.

We observe that simulation results present magnitude and trends consistent with experimental results especially at high Vdd. At low Vdd, discrepancy is mainly explained by a less accurate description of the moderate inversion regime for transistors with short gate length because the reduction of mobility experimentally observed for short dimensions [13] is currently not considered in simulations. Moreover, the gate tunneling current through the oxide is not taking into account in the simulation whereas it is known that this current degrades SRAM cell performances. Therefore, we have checked that on this technology (EOT=1.2nm with high-*k*) the gate tunneling current participates only for few per cents to the SRAM cell noise margins.

Finally, TCAD provides guidelines for the FDSOI technology to improve SRAMs characteristics trade-offs. It is found in Figure 9 that we can achieve better static noise margins by adjusting metal gate workfunctions $\phi_m$ toward midgap.

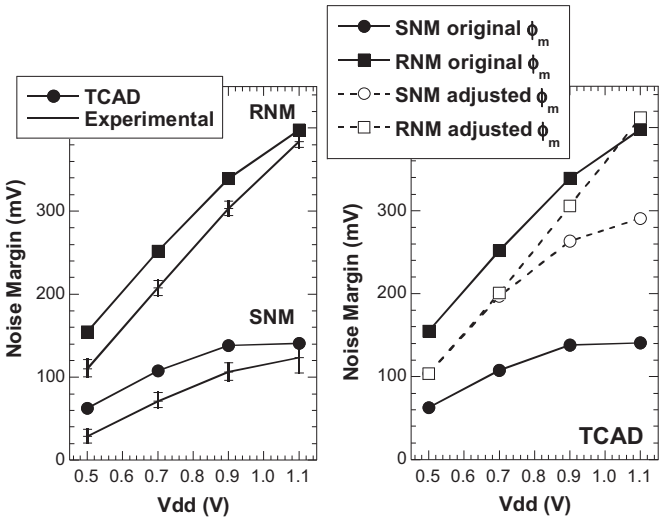


Figure 8. RNM and SNM as a function of Vdd resulting from (line) experiments and (symbol) TCAD simulations

Figure 9. RNM and SNM as a function of Vdd resulting from (filled symbols) TCAD with same $\phi_m$ as experiments and (open symbol) TCAD with adjusted $\phi_m$.

## V. CONCLUSION

A TCAD approach mainly based on improved physical mobility models including Remote Coulomb Scattering and calibrated on recent experimental data is presented. It is used to simulate FDSOI electrical characteristics and 6T-SRAM cells' noise margins. The very good agreement achieved between simulations and experimental data allows us to propose optimized SRAM cells characteristics. Moreover, this "FDSOI TCAD library" can be used to realistically extrapolate this technology to support near future node development (20nm, 16nm). Introduction of experimentally observed mobility degradation with decreasing gate length [13] and gate tunneling current in the "FDSOI TCAD library" are currently underway.

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