Techniques for In-Band Phase Noise Reduction in $\Delta\Sigma$ Synthesizers

Thomas A. D. Riley, *Member, IEEE,* Norman M. Filiol, *Member, IEEE,* Qinghong Du, and Juha Kostamovaara, *Member, IEEE*

***Abstract*—This paper reviews several techniques used to reduce the in-band phase noise contribution of $\Delta\Sigma$ fractional-*N* frequency synthesizers. The paper develops several practical techniques for specifying the noise and linearity of components used in a $\Delta\Sigma$ fractional-*N* synthesizer.**

As an example, it presents a synthesizer with an in-band phase noise floor of −97 dBc/Hz@10 KHz for an RF output frequency of 2.432 GHz and a reference frequency of 16 MHz. The synthesizer has a frequency resolution of 61 Hz and an on-chip crystal oscillator. The synthesizer was implemented in a 0.35-μm SiGe process and consumes 6 mA from a 3 V supply. The in-band phase-noise, spurs, and power consumption of this synthesizer are each low and comparable to the state-of-the-art.

***Index Terms*—Bluetooth, Delta–Sigma, frequency modulation (FM), frequency-shift keying (FSK), Gausian frequency shift keying (GFSK), GMSK minimum shift keying (MSK), general packet radio service (GPRS), global system for mobile communications (GSM), multimode, radio, satellite, Sigma-Delta, wireless.**

I. Introduction

MODERN communication chips are a good example of the level of complexity that system-on-a-chip (SOC) has reached. Both digital control circuits and analog components, such as LNAs, mixers and A/Ds are integrated onto the same substrate. A key mixed signal block in such SOCs is the frequency synthesizer which is used for both up-conversion and down-conversion of signals in the radio.

$\Delta\Sigma$ synthesizers solve several problems faced by radio systems designers. These synthesizers provide opportunities for obtaining small-frequency step sizes, reduced synthesizer phase noise, reduced spurious tones generated by the synthesizer, and flexibility in frequency planning. Although they have been investigated in one form or another since 1978 [1], they have been commonly used commercially only in the last few years [2]–[4]. Although a $\Delta\Sigma$ fractional-*N* frequency synthesizer can have many uses, tuning its performance to any particular application requires many decisions at the component level to obtain acceptable performance of each component and higher level decisions that effect the tolerance of the synthesizer as a whole to component imperfections.

Perhaps the clearest example of this kind of tradeoff involves the three types of noise contribution to a $\Delta\Sigma$ fractional-*N* frequency synthesizer. These are 1) voltage-controlled oscillator (VCO) noise, which can be suppressed inside the loop bandwidth by increasing the loop bandwidth; 2) quantization noise, which can be reduced by decreasing the loop bandwidth; and 3) in-band phase noise, which can also be reduced by decreasing the loop bandwidth. Clearly, in any given case, there is an optimal bandwidth which provides the lowest noise by trading off in-band phase noise and quantization noise against VCO noise.

We have lumped several similarly behaving noise sources into VCO phase noise; it can also include contributions from power amplifiers (PA noise) or circuit noise added in the loop filter. In any case, it is suppressed by the open loop gain of the PLL. Similarly, the in-band phase noise contains contributions from the reference signal path, divider, phase frequency detector (PFD), and charge-pump.

The design presented here was tuned for a cable modem application requiring a quadrature amplitude modulation (QAM) signal constellation with up to 1024 points and which in turn required very low in-band phase noise. Low in-band phase noise is also important in many satellite applications. The phase noise, beyond 2 MHz, for the synthesizer presented here is −123 dB/Hz. The kinds of applications where this would be unacceptable are those that require low out of band noise to prevent interference from strong interfering signals or to meet demanding spectral mask requirements, such as GSM.

This application, with its demanding in-band phase noise requirements, provides an excellent opportunity to review techniques to address the problem. Future work based on [5] will address improvements in quantization noise. There is a wide body of literature on improving VCOs. Several techniques are presented as a case study and tutorial review for improving one metric of synthesizer performance, in-band phase noise.

To put this collection of techniques into the context of a complete synthesizer, the paper walks through the entire synthesizer and describes each relevant component, how it contributes to in-band phase noise and how we selected our approach to addressing the issue. This is done in two passes; first, in terms of architecture and second, discussing some circuit level details.

For experts, the value of this paper is in its description of how to balance the costs and benefits of the various techniques discussed. For the uninitiated, it provides a checklist of issues that need to be addressed and some understanding of how to address them. Several new twists on old themes are also identified throughout the paper and it recommends an overall approach to designing synthesizers with low in-band noise. Another important aspect of the techniques presented in detail here is that they are all, to the best of the authors knowledge, public domain and thus readily available for commercial use. This is a step toward a patent free $\Delta\Sigma$ fractional-*N* frequency synthesizer.

Manuscript received May 1, 2003; revised July 2003. This work was supported in part by the Academy of Finland, Project 51493. This paper was recommended by Guest Editor M. Perrott.

T. A. D. Riley, Q. Du, and J. Kostamovaara are with the University of Oulu, FIN-90401 Oulu, Finland.

N. M. Filiol is with Kaben Research, Inc., Osgoode, ON K0A 2W0, Canada.

Digital Object Identifier 10.1109/TCSII.2003.819132

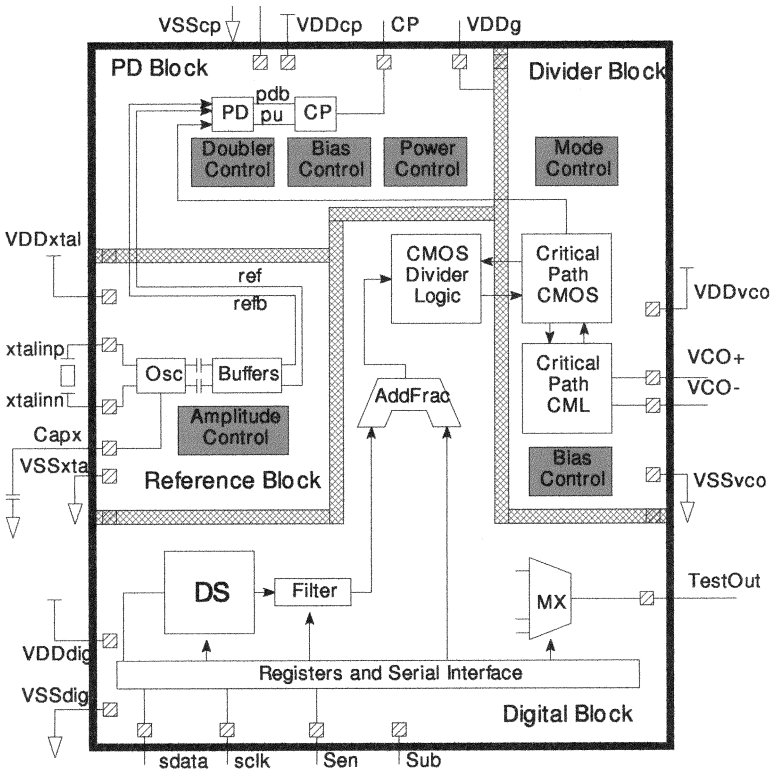


Fig. 1. Synthesizer chip block diagram.

In Section II, we look at high-level issues concerning in-band phase noise and how to set specifications for the components of the design. In Section III, we look at various aspects of the circuit design as they relate to in-band phase noise and the specifications set in Section II. Section IV presents measured results. The conclusions, in Section V, present a summary of our results and recommendations for generalizing our approach to other problems.

II. Sources of In-Band Noise

The top level of a $\Delta\Sigma$ fractional-*N* frequency synthesizer chip consists of six blocks: the digital block containing the $\Delta\Sigma$ modulator (DSM), the divider block, the phase detection (PD) block, reference block, loop filter and VCO. For our case study, the VCO and loop filter were off-chip. The blocks and the overall architecture of the chip are presented in Fig. 1.

The shaded boxes indicate a function controlled by registers in the serial interface. The cross-hatched bars indicate the boundaries between the blocks. The cross-hatched squares indicate pads. The black bars indicate the chip boundary.

This section introduces the major sources of in-band noise describes where they come from and how to set limits on their levels so that an overall in-band noise performance requirement can be met by the following:

- jitter in digital logic,
- noise folding,
- charge-pump current noise,
- offset current noise,
- reference noise.

Synthesizer designs often begin with the designers favorite interactive number crunching software and the models proposed by Crawford [6] and/or Perrott [7]. When it becomes apparent that in-band phase noise could be a limiting factor in a synthesizer design, we recommend replacing all in-band noise sources with an equivalent noise source in the reference

$$\mathrm{L}_{\mathrm{synth}PD}(f) = \mathrm{L}_{\mathrm{synth}PD} = \mathrm{BFM} + 10\log_{10}(f_s) \quad (1)$$

where $\mathrm{L}_{\mathrm{synth}PD}(f)$ is the single-sided in-band phase noise density contribution of the synthesizer at the phase detector and f_s is the sampling frequency of the phase detector. Banerjee figure of merit (BFM) is drawn from work originally published by Banerjee [8]. Its primary benefit is that it can often predict the in-band phase noise performance of given hardware over a wide range of operating conditions. The original form referred the noise to the synthesizer output as

$$\mathrm{L} = \mathrm{BFM} + 10\log_{10}(f_s) + 20\log_{10}(N) \quad (2)$$

which simply acknowledges that the gain from the reference frequency to the synthesizer output is N for offset frequencies well within the loop bandwidth.

With (1) as a starting point, we assume the synthesizer will contribute some constant amount of white noise power that is multiplied by the reference frequency. Then, as usual, the decisions about loop bandwidth, sampling frequency, loop filter design etc. can be made early in the design process. The minor improvement we suggest here is that by starting the design process with BFM included, BFM can serve as an indicator of the difficulty to expect in the circuit design, even for synthesizer designers who are not circuit designers. BFM provides a convenient comparison with other work and, as we will later show, translates easily into component level specifications.

Section II-A–E addresses the major sources of in-band noise and block level decisions made in our case study. We describe

here the allocation of an in-band noise budget to achieve a BFM of -213 dB.

A. Jitter in Digital Logic

One of the major contributors to in-band phase noise is jitter in the digital logic making up the dividers, PFD, and reference path. In this section, we show how to use BFM to set specifications on the tolerable amount of rms jitter in digital logic.

To begin this process, we note that an rms jitter of σ_j will have an equivalent error in radians of $(2\pi\sigma_j)/T_s$ where T_s is the sampling period at the phase detector. As a result, the spectral density of a white, constant rms jitter at the phase detector is

$$S_{\varphi_j} = \left(\frac{2\pi\sigma_j}{T_s}\right)^2 \frac{1}{f_s} = (2\pi\sigma_j)^2 f_s \tag{3}$$

which, when we convert to double sided spectrum and logarithmic notation gives

$$\mathrm{L}_{\varphi_j} = 20\log_{10}\left(\sqrt{2}\pi\sigma_j\right) + 10\log_{10}(f_s). \tag{4}$$

From this form, we can see that a fixed rms jitter directly contributes to the BFM of the overall synthesizer. From this form of the equation we can identify a component of the BFM contributed by component jitter as

$$\mathrm{BFM}_{\sigma_j} = 20\log_{10}\left(\sqrt{2}\pi\sigma_j\right). \tag{5}$$

If we allow one fifth of the BFM to come from jitter and the rest to come from sources yet to be discussed, this will allow a total jitter budget of

$$\sigma_j = \sqrt{\frac{1}{5}}10^{\frac{\mathrm{BFM}}{20}}\frac{1}{\sqrt{2}\pi} = 2.3\ \mathrm{ps}. \tag{6}$$

The next step in allocating the budget is to account for the number of delay stages between the VCO and the phase detector, between the reference and the phase detector, and within the phase detector itself. Using a combination of proprietary techniques and techniques described here, we reduced this to three delays in the divider, three in the reference path and only two within the PFD for a total of eight. This allows an rms jitter per delay stage of

$$\sigma_{j\mathrm{Each}} = \frac{2.3\ \mathrm{ps}}{\sqrt{8}} = 0.8\ \mathrm{ps}. \tag{7}$$

Note that this does not suggest that the delays through the digital logic need to be less than 0.8 ps; it requires that the random changes on these delays be less than 0.8 ps rms.

B. Noise Folding

One of the difficulties that arise in any circuit exploiting $\Delta\Sigma$ techniques is that the high-frequency quantization noise can be brought into the signal bandwidth through intermodulation products caused by nonlinearities in circuit components. In the context of a $\Delta\Sigma$ synthesizer, these nonlinearities occurring anywhere in the phased-locked loop (PLL) cause the quantization noise to fold back into the baseband. This has been reported previously in [2] and [9]. We present here some simple approximations that allow this effect to be quantified so that linearity specifications can be set for the various PLL components. Our presentation is based around nonlinearities in the phase detector such as a dead zone in a phase/frequency detector (PFD) but other nonlinearities have an equally significant impact. This section will provide a method to quantify the amount of error introduced by any nonlinearity, if it were known. This is a preliminary step to setting the limits on how much nonlinearity the synthesizer can tolerate.

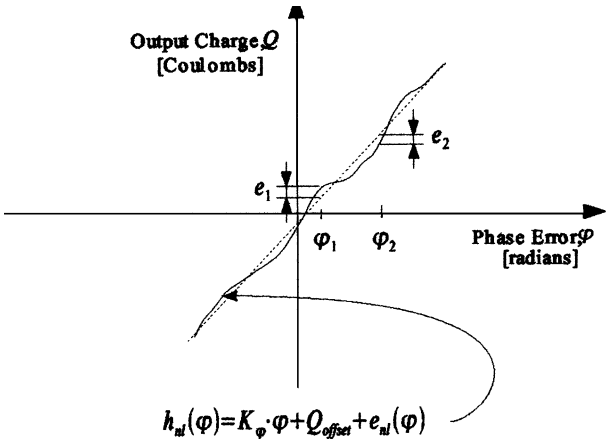


Fig. 2. An arbitrary phase detector nonlinearity.

This section examines the effects of nonlinearities in the PLL components when the sequence length in the bitstream from the DSM is long. By long we mean long enough to produce no visible spurs within the resolution bandwidth of the spectrum analyzer or fast Fourier transform (FFT) evaluating the synthesizer or simulation, respectively. Thus, the meaning of long here is relative to how we are looking at the circuit or simulation. When the bitstream from the DSM is a long sequence, nonlinearities produce the appearance of in-band noise. When the sequence is short, nonlinearities produce in-band spurs.

The initial assumption is that all of the nonlinearity is attributed to the charge-pump; clearly, other nonlinearities occur and can be mapped to equivalent charge-pump nonlinearities. As a result, this section is important to understanding the effects of the other nonlinearities. We will discuss the details that suggest generic ways to reduce the impact of nonlinearities once the impact is understood.

Fig. 2 shows an arbitrary charge-pump/PFD characteristic curve with nonlinearity. The dashed line indicates the best linearized gain which reduces the rms error to a minimum. Gain errors and offset errors being linear are not relevant to this discussion. Whatever error remains represents an additive error in the charge-pump output charge or an equivalent additive error in the reference phase.

Here, we assume the charge-pump output charge is given by a function $h_{nl}(\varphi)$ where h is a nonlinear function and φ is the phase angle of the divider output that is being measured by the phase detector.

We assume that a sequence of phase errors, φ_k, produces a sequence of charge output errors e_k, where e_k is the difference between the actual output charge and the ideal linearized output charge. For example, in Fig. 2, φ_1 causes the error,e_1, φ_2 causes

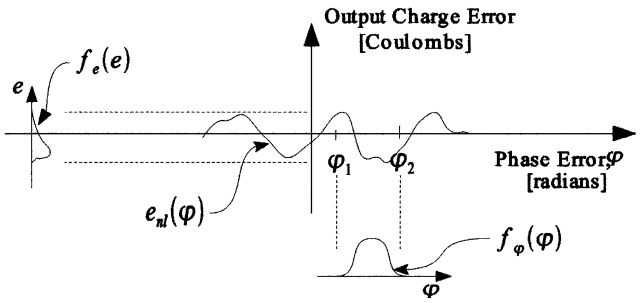


Fig. 3. The distribution of e is determined by a nonlinearity and the distribution of φ.

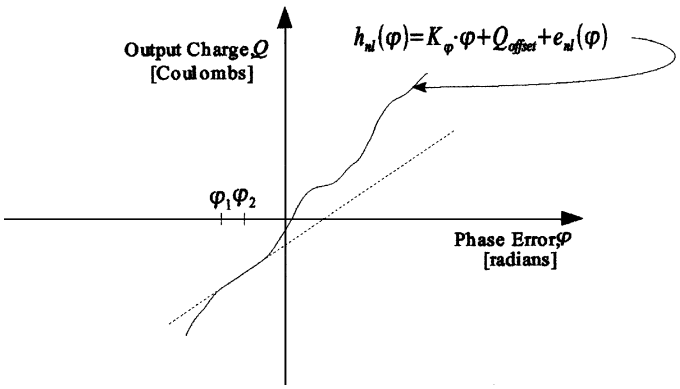


Fig. 4. The same arbitrary nonlinearity with a different linearized gain and a different range of operation.

the error, e_2 and so on. The variance of the sequence e_k will then be as shown in (8)

$$\sigma_e^2 = E\{e^2\} = E\left\{e_{nl}^2(\varphi)\right\} = \int_{-\infty}^{\infty} e_{nl}^2(\varphi) f_\varphi(\varphi) d\varphi \qquad (8)$$

where $E\{\}$ is the expected value operator and $f_\varphi(\varphi)$ is the probability density function of φ. To appreciate the meaning of (8), we should note that the error variance, σ_e^2, is the expected value of all of the individual errors squared, which in this particular case is the expected value of $e_{nl}^2(\varphi)$. As always, the expected value can be evaluated using the integral on the right-hand side of (8).

From (8), we can see that the rms error introduced by nonlinearity could be evaluated numerically if the distribution $f_\varphi(\varphi)$ were known and limited to a finite range and also if the nonlinearity were known.

Fig. 3 illustrates an example, for the same nonlinearity as Fig. 2, where the distribution of φ is now constrained to lie between φ_1 and φ_2. The probability density function, $f_\varphi(\varphi)$, indicates the likelihood that φ will take on some value between φ_1 and φ_2, and hence, the probability that *e* will take on the value set by the nonlinearity. This process can be summarized by pointing out that the rms charge error is the rms nonlinearity of the charge-pump weighted by the probability density function of the φ_k distribution.

An important issue is that the phase detector appears to be more linear when the distribution of φ_k is tightly clustered near a single operating point. This is the familiar "small signal" approximation where a small signal can be analyzed as if it were present in a linear system (provided the signal is sufficiently small). In a $\Delta\Sigma$ system, the quantization noise is often too large to allow this nonlinearity to be ignored as if it were a small signal.

To be more complete about some of the details that were skipped in the example of Figs. 2 and 3, and to emphasize the benefit of reduced quantization noise distribution, we can look at another example in Fig. 4. In this example, the entire range of operation has been set to occur on only one side of the phase error characteristic curve. Details of how this is done are discussed in Section II-D. Here the linearized gain and offset is fitted to the region where the probability density function, $f_\varphi(\varphi)$, is bounded. This example uses the same nonlinearity but a different range of operation. As in the previous example, φ_1 and φ_2 mark the bounds of the range of operation. Clearly, both the range of the error and the rms value of the error will be smaller for this region of operation and this smaller distribution of phase error than in the examples of Figs. 2 or 3. This brings up two practical points for the design and operation of $\Delta\Sigma$ synthesizers: first, it is important to control the distribution of the quantization noise and second, it is important to control the region of operation where the phase detector operates and/or to make sure that it is linear in the region where it operates.

Given that lower quantization noise is preferable, lower-order modulators are also better because they introduce a smaller $\Delta\Sigma$ jitter distribution. Thus, with lower-order modulators, the charge-pump/PFD needs to operate in a linear fashion over a smaller range.

The range and probability density function of φ_k can be accurately estimated from discrete time simulations of the DSM. Thus, the integral in (8) can be approximated numerically because DSMs must produce a bounded phase error at the phase detector to operate properly in $\Delta\Sigma$ PLL synthesizer.

For the sake of developing a better understanding and a simple analytical formula, we will consider the case where the phase error is uniformly distributed. This is only true for first-order DSMs; higher order DSMs have distributions that become increasingly closer to Gaussian in shape. Higher order DSMs tend to clump the probability density function closer to the mean value. This suggests that most of the time the signal is smaller, which slightly offsets the effect of the tails of the distribution where the signal on occasion can be larger. For "gentle" nonlinearities without sharp discontinuities or spikes, the use of a uniform probability density function (i.e. $f_\varphi(\varphi) = 1/(\varphi_{\max} - \varphi_{\min})$) is slightly pessimistic but has the advantage that it simplifies (8) to

$$\sigma_e^2 = \frac{1}{\Delta\varphi} \int_{-\varphi_{\min}}^{\varphi_{\max}} e_{nl}^2(\varphi) d\varphi \qquad (9)$$

where $\Delta\varphi = \varphi_{\max} - \varphi_{\min}$ is the range of the $\Delta\Sigma$ jitter present at the PFD input. In (9), σ_e is the rms error of the nonlinearity averaged over the range of the $\Delta\Sigma$ jitter. From this rms charge error, we can see that the rms output current error is

$$i_{e_{nl}} = \frac{\sigma_e}{T_s} \qquad (10)$$

where T_s is the sampling period at the phase detector. This output-referred error can be referred to the input of the phase detector if we divide the error by the phase detector conversion gain. The input-referred rms phase error at the PFD is

$$\varphi_{e_{nl}} = \frac{i_{e_{nl}}}{K_\varphi} \tag{11}$$

where K_φ is the conversion gain of the phase detector and $\varphi_{e_{nl}}$ is the equivalent phase error at the phase detector.

By assuming that this is a sampled-data sequence with a white, continuous spectrum, the spectral density of the nonlinearity error at the phase detector is

$$S_{\varphi_{e_{nl}}} = \frac{i_{e_{nl}}^2}{f_s K_\varphi^2}. \tag{12}$$

Alternatively, since $f_s = 1/T_s$ we have from 10

$$S_{\varphi_{e_{nl}}} = \frac{\sigma_e^2 f_s}{K_\varphi^2}. \tag{13}$$

The two forms of expressing the phase noise resulting from phase detector nonlinearity can each provide some insight but we will stick with the latter form for now. Then the resulting in-band phase noise at the phase detector will be

$$S_{\varphi_{e_{nl}}} = \left(\frac{2\pi\sigma_e}{I_p}\right)^2 f_s \tag{14}$$

where $K_\varphi = (I_p/2\pi)$ is the gain of the phase detector and charge-pump. Since σ_e and I_p remain fixed as f_s changes expressing (14) as the following:

$$\mathrm{L} = 20\log_{10}\frac{\sqrt{2}\pi\sigma_e}{I_p} + 10\log_{10} f_s \tag{15}$$

describes its tendency to behave in the same deleterious fashion as a fixed amount of rms jitter as discussed in Section II-A.

Again with five independent noise sources we require

$$\frac{\sigma_e}{I_p} < \frac{10^{\frac{\mathrm{BFM}}{10}}}{\sqrt{10}\pi} = 2.3\ \mathrm{ps}. \tag{16}$$

To put this into perspective, we could calculate an equivalent linearity in bits. Having an equivalent nonlinear error less than 2.3 ps over a range of operation of $\Delta\varphi = 15$ VCO cycles or 6.2 ns at 2.43 GHz, requires a linearity better than 11 b.

Although the discussion here has been presented in terms of PFD and charge-pump linearity, it should be noted that this requirement applies to the divider as well. If the divider has a 2.00 ns delay when dividing by 149, a 2.001 ns delay when dividing by 150, and a 2.00 ns delay when dividing by 151, this represents another nonlinearity that can be treated in a similar way. In our case study, we used a proprietary form of resynchronization to make sure that the divider did not contribute significantly to the nonlinearities.

The divider block contains only the analog path of the complete divider. This analog path is the portion of the divider logic in which a VCO edge ultimately triggers a divider output edge sent to the phase detector. The current-mode logic (CML) portion of the divider circuit and some CMOS on the analog path of the divider are in the divider block. Most of the basic CMOS logic, which contains no analog information in the timing edges, is in the digital block so that the CMOS switching noise is less likely to couple into the analog path of the divider. Where the divider block receives several signals from the digital block, these signals are retimed with the output of the CML to CMOS converter for generating the divider output which goes to the PFD for phase comparison. This retiming allows the number of delay stages to be reduced to three even in a low-power divider.

TABLE I
EFFECT OF THE POST DSM FILTER ON DS JITTER

	$\Delta\Sigma$ Jitter at Divider Output (VCO cycles)	
	4th Order DSM	5th Order DSM
Without post DSM filter	±3.67	±7.30
With post DSM filter	±3.05	±5.11

C. Digital Block

Within the digital control of the divider there are opportunities to manipulate the effect of the nonlinearities described in Section II-B.

$\Delta\Sigma$ Modulator: As mentioned earlier, higher order modulators have an impact on the amount of quantization noise introduced into the synthesizer. The DSM is programmable to allow either fourth- or fifth-order noise shaping. This is to allow fairly low-reference frequencies when required. When the desired loop bandwidth is large compared to the reference frequency, fifth-order noise shaping is preferred but extra poles in the loop filter are required. The output of the DSM is 5-b wide.

Post-DSM Filter: In order to obtain extra filtering at fs/2, an optional post DSM filter is included in the digital block. This has a transfer function of $1 + z^{-1}$ which has a notch at fs/2 to reduce the power of the quantization noise at fs/2. The drawback of using this feature is that it increases the baseband quantization noise by 6 dB. Generally it is more useful when the ratio of the loop bandwidth to the sampling frequency is low. This extra filter in the digital block reduces the peak out of band quantization phase noise by 4.8 dB for a fourth-order DSM and by 5.7 dB for a fifth-order DSM and, thereby, reduces the amount of filtering required in the loop filter for a given modulator order. More importantly, for reducing in-band phase noise, it reduces the active range of the $\Delta\Sigma$ jitter coming out of the divider. Table I summarizes the active range of the $\Delta\Sigma$ jitter for the two modulator orders with and without the post-DSM filter.

To be able to use the DSM in any of its desired modes without increasing the amount of noise folding, we have to make sure that the linearity specifications are met in the worst-case, which is fifth-order noise shaping without the post-DSM filter. This is another specification that will come back into play when we get to the circuit design of the charge-pump.

D. Charge-Pump Current Source Noise

The purpose of the charge-pump is to linearly translate the width of the pump-up (PU) and pump-down (PD) pulses to a

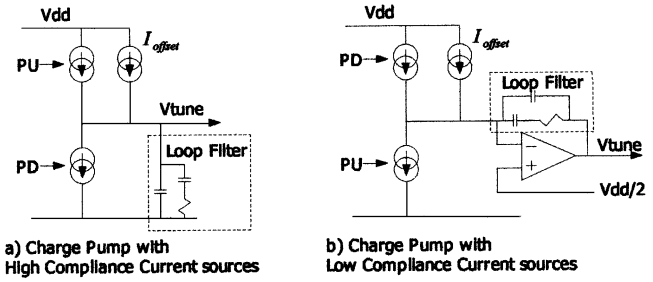


Fig. 5. Two types of loop filters.

charge transferred to the loop filter. For any charge-pump, the charge transferred to the loop filter is $Q = I_p \Delta T$ where I_p is the pump current and ΔT is the width of the PU or PD pulse.

Fig. 5 shows two possible configurations for a loop filter. In the first arrangement, the loop filter is passive and the charge-pump current sources must continue to work over the entire tuning range of the VCO. This requires the current sources to have a high-compliance voltage. Compliance voltage is the voltage range over which a current source is in compliance with its specifications. For a current source in a charge-pump, these specifications are: peak output current, output impedance, noise current etc. In the second configuration, the op-amp 'pins' the voltage to some convenient value and the current sources only need to meet their specifications at that voltage. For this synthesizer, the reference voltage is half the supply rail; ultimately it will be a bias voltage already present on chip.

The loop filter used with this charge-pump is an active loop filter that inverts the current signal from the charge-pump. This is an off-chip loop filter with an op-amp but will be replaced with an on-chip op-amp and loop filter in the next version. Note that the locations of the switches controlled by PU and PD have reversed in order to accommodate the inversion of current polarity caused by the use of an op-amp.

The reason for the use of the active filter is to allow one more degree of freedom in the design of the current sources in the charge-pumps. By relieving the compliance voltage requirement of the current sources it becomes possible to use much more source degeneration. This degeneration makes it easier to reduce the noise of the charge-pump without making the transistors too large. Since phase noise at the synthesizer output is far less sensitive to current noise at the op-amp output than it is to current noise at the charge-pump output, the compliance voltage requirements can met at the op-amp output without a substantial penalty in noise or area.

One simple way to reduce the difficulties of solving the linearity problem outlined in Section II-B is to inject a small offset current I_{offset} in the charge-pump. With this, the lock point of the PLL is no longer at zero degrees of phase offset and, thus, the residual nonlinearity near the center of the PFD is avoided. By injecting a large enough offset current as shown in b), the lock point can be shifted so that only PU is active. This completely avoids nonlinearity introduced by mismatch of the PU or PD currents in the charge-pump.

Under these conditions, the PLL will lock where $I_p(\Delta T/T_s) = I_{\text{offset}}$. By setting I_{offset} such that ΔT is greater than both the $\Delta\Sigma$ jitter on the divider output and the nonlinear region of the PFD, all the $\Delta\Sigma$ jitter can be placed on one side of the phase detector characteristic curve.

We then have two more noise sources to evaluate. The first is the error introduced by the pulsed current I_p. The equivalent noise current density will be $i_n^2(\Delta T/T_s)$ where i_n^2 is the noise current density in the current source I_p. As in the previous cases, dividing by K_φ refers this noise to the phase detector input and simplifies

$$S_{\varphi_{i_n}} = \frac{(2\pi i_n)^2 \Delta T f_s}{I_p^2}. \tag{17}$$

Again, like the other sources of noise, this can be expressed in a form consistent with Banerjee's rule

$$\mathrm{L} = 20\log_{10}\frac{\sqrt{2\Delta T}\pi i_n}{I_p} + 10\log_{10} f_s. \tag{18}$$

Whether or not the noise actually follows the rule clearly depends on whether or not ΔT is kept constant as f_s changes. This is a situation over which the designer has considerable control by adjusting I_{offset}. Clearly as ΔT increases, i_n must decrease to keep the BFM within specification. However, as discussed in Section II-B, we want to keep all of the $\Delta\Sigma$ jitter on one side of the phase detector characteristic curve. The best solution then is to set I_{offset} such that ΔT is just slightly larger that the time corresponding to 15 VCO cycles (the worst-case for our DSM and post-DSM filter) or to have it change adapting to the minimum offset for each case.

As with the other specification requirements, the value inside the $20\log_{10}$ operator must evaluate to something less than 2.3 ps if the BFM specification is going to be met in conjunction with the other sources of noise. For $\Delta T = 16T_{VCO} = 6.5$ ns and $I_p = 500\ \mu$A, we require $i_n < 3.2\ \mathrm{pA}/\sqrt{\mathrm{Hz}}$.

The other source of noise arising from the charge-pump of Fig. 5 is the fixed offset current and its noise. If its current noise density is i_{no}^2, the input referred phase noise contribution from it is

$$S_{\varphi_{i_{\mathrm{no}}}} = \frac{(2\pi i_{\mathrm{no}})^2}{I_p^2} \tag{19}$$

which is constant for any sampling frequency. Since this noise source does not follow the same pattern as the others, we have to set an acceptable noise level for this at the reference frequencies the synthesizer is desired to operate. With a 16-Mhz sampling frequency, a BFM of -213 would require $i_{\mathrm{no}} = 100\,\mathrm{nA}/\sqrt{Hz}$.

E. Limitations of Banerjee Figure of Merit

BFM is, like any benchmark or figure of merit, subject to manipulation and only applies to noise sources that behave in a particular way. We have shown here that in a charge-pump based design the majority of noise sources do behave in a manner predicted by BFM.

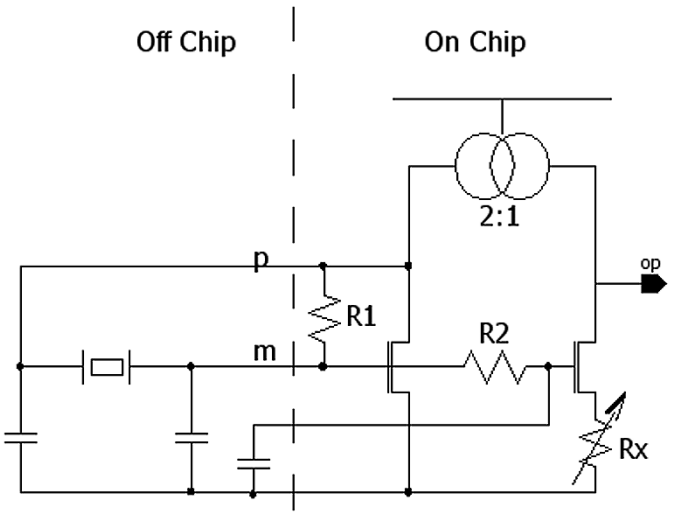


Fig. 6. Crystal oscillator.

III. Circuit Design

A. Reference Block

This section describes the synthesizer reference block. The block consists of the crystal oscillator (XTAL) and level-shifting buffers.

The XTAL has low-power consumption and operates from 4–16 MHz. It uses subthreshold and self-biasing techniques to maintain this low power. It is based on a circuit found in [10]. An external decoupling capacitor is required to achieve low noise.

The level shifters are used to translate the sinusoidal output of the XTAL to CMOS levels in order to make them compatible with the PFD logic while maintaining the phase noise of the XTAL.

Crystal Oscillator: The crystal oscillator is based on low-power subthreshold CMOS oscillator techniques from the 1970s. It is self-biased and has a built in amplitude limiting loop to provide low-phase noise. There is a bank of programmable resistors to control the amplitude of oscillation at various crystal frequencies. The theory of operation is described in the following references [10]–[12].

The oscillator simplified schematic is shown in Fig. 6. The implemented oscillator is also single-ended. However, since the current injected by the oscillator is so small compared to the current through the crystal and the off-chip load capacitors, it produces a reasonably clean differential signal. The mismatch between the voltage amplitudes at the "*p*" and "*m*" nodes is caused primarily by mismatch in the off-chip load capacitors.

Level Shifter: The purpose of the level shifter is to convert the XTAL output to CMOS logic levels. This means that a sinusoid with an amplitude of approximately 800 mVp-p differential must be converted to full-swing logic levels of ~3 V. Doing this while maintaining the low-phase noise of the crystal, is not as simple as it may seem. Through many periodic steady state (PSS) noise simulations, used to evaluate the rms jitter at the level shifter output, it was found that the level shifter had to be done in stages to keep the noise low. Attempts to use a single-stage approach were too noisy or required more power.

The solution used is analogous to a radio receiver. The first stage is like a low-noise amplifier (LNA) in the sense that it must have the lowest-noise contribution. Once the signal has reached larger swing levels the noise of subsequent stages becomes less significant. Once CMOS levels are achieved, the subsequent stages only contribute to the noise while switching as there is no noise gain from input to output once the signal is

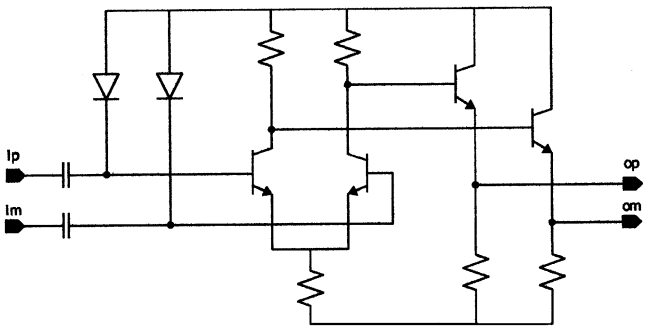


Fig. 7. First-level shifter schematic.

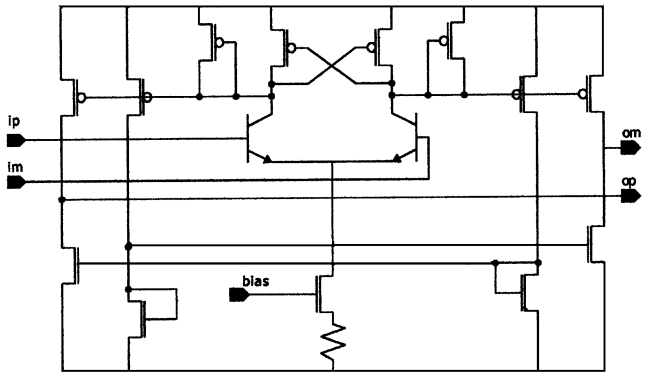


Fig. 8. Second-level shifter schematic.

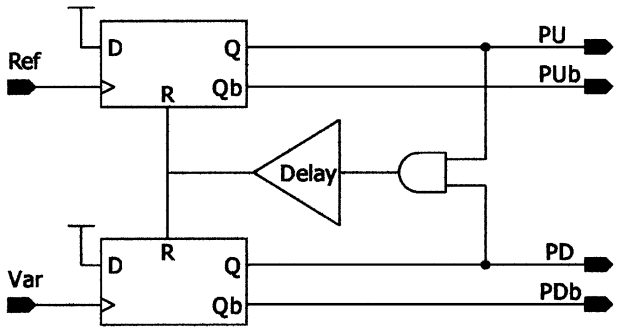


Fig. 9. Phase frequency detector.

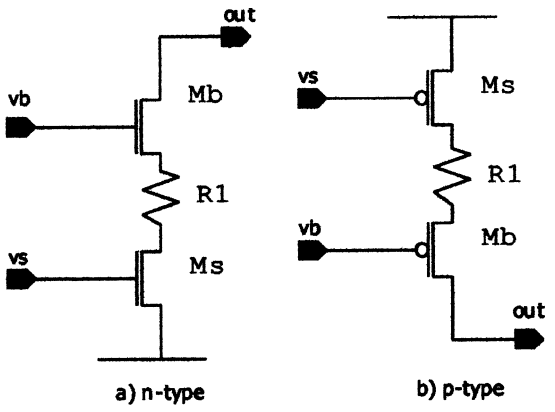


Fig. 10. Switchable current cells.

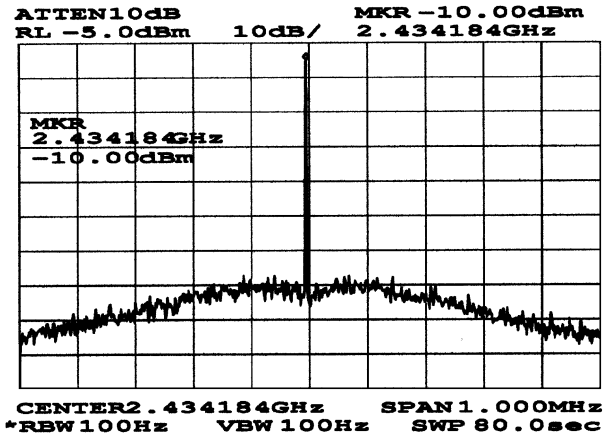


Fig. 11. Synthesizer output spectrum at 2.434 GHz.

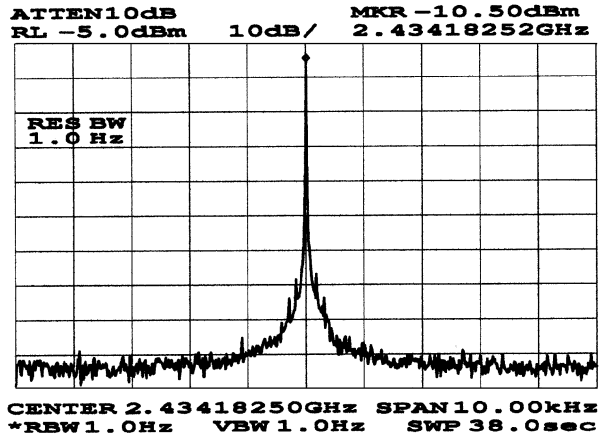


Fig. 12. Synthesizer output spectrum at 2.434 GHz.

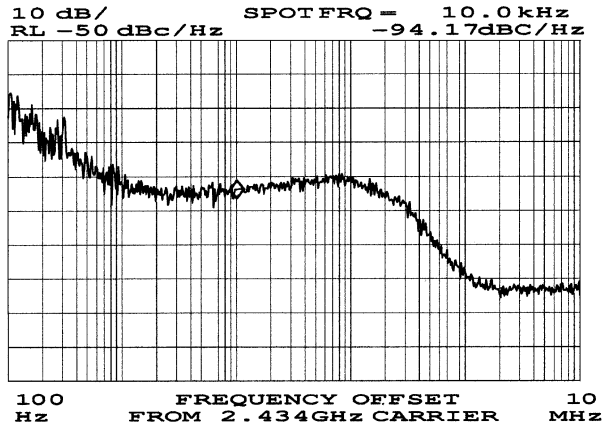


Fig. 13. Phase noise of synthesizer for 50-KHz loop bandwidth.

limited. Our approach of multistage limiting is also similar to the approach used in IF stages of FM receivers.

First Stage of Level Shifting: The first stage of level shifting is shown in Fig. 7. It consists of an ac-coupled bipolar differential pair with resistive loads. There is no current source as a resistive bias is used. The dc bias is provided by two diodes connected between the inputs and vdd.

Second Stage of Level Shifting: The second stage of level shifting is shown in Fig. 8. It consists of a bipolar differential pair with cross coupled CMOS loads. The output currents are mirrored into a push–pull CMOS output stage. The resulting output has CMOS levels.

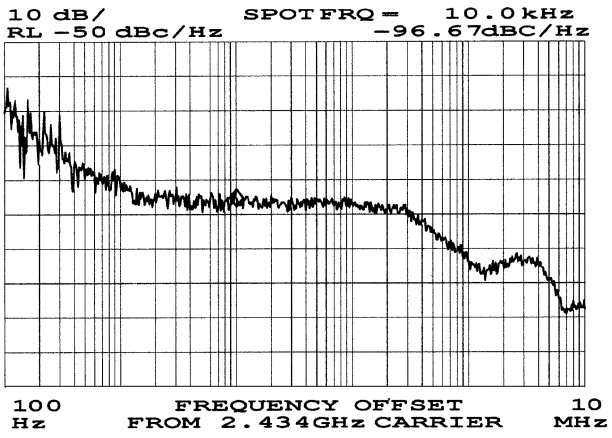


Fig. 14. Synthesizer phase noise for 150-KHz loop bandwidth.

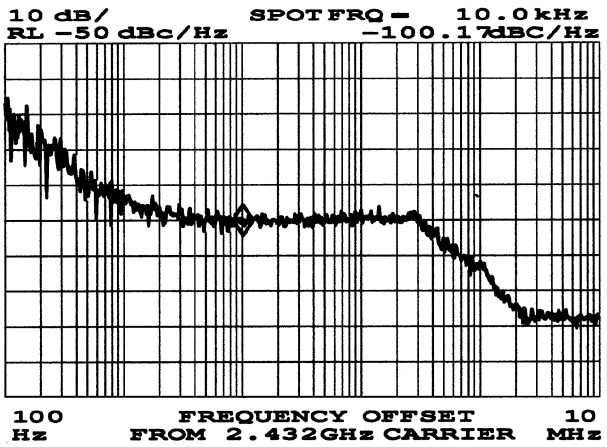


Fig. 15. Synthesizer phase noise for 150-KHz loop bandwidth.

TABLE II
SPECIFICATIONS SUMMARY

Parameter	Value
Supply Voltage	2.7 – 3.6 V
Supply Current	6.3 mA
Maximum Output Frequency	2.485 GHz
Minimum Frequency Resolution	< 100 Hz
Close-in Phase Noise	-97 dBc/Hz*
Close-in Phase Noise	-100 dBc/Hz**
Spurious (Integer boundary)	<-60 dBc***
Spurious Typical	<-80 dBc (noise floor)

* Fractional-N, Fout=2.432 GHz, Fref=16 MHz, Loop Bandwidth 150 KHz.
** Integer-N, Fout=2.432 GHz, Fref=16 MHz, Loop Bandwidth 150 KHz.
**Only when within one loop bandwidth of an integer multiple of Fref.

B. Phase Detection Block

Phase Frequency Detector: The phase frequency detector is a standard resettable *D* flip-flop-based digital phase frequency detector. This is shown in Fig. 9.

C. Charge-Pump

A basic switchable current source cell is shown here in Fig. 10(a). The input,vs, turns on the switching transistor, Ms. The on resistance of Ms is low so that the bias voltage, vb, and resistor R1 set the current through Mb. By using the active loop filter, the current source does not need a high-compliance voltage and R1 can be larger to degenerate the gain on Mb. This makes the output noise current less dependent on noise on the bias voltage, vb,and less dependent on the noise of the

TABLE III
STATE-OF-THE-ART COMPARISON

Reference	Technology	Fout	Fref	Resolution	In-band Noise	BFM	Maximum Power
		(GHz)	(MHz)	(Hz)	(dBc/Hz)	(dB)	(mW)
Rhee et al [2]	0.5 μ m CMOS	900.03	7.99	<1	-92	-202	43
Rhee et al [3]	0.35 μ m BiCMOS	2.47	8	<10	-82	-201	16
De Muer et al [13]	0.25 μ m CMOS	1.8	26	400	-60	-171	70
Perrott et al [7]*	0.6 μ m CMOS	1.84	20		-75	-187	
Ahola et al [14]	0.35 μ m CMOS	1.76	13	<51000	-79	-193	22.6
Heng et al [15]	0.6 μ m CMOS	1.715	20	10	-90	-202	140
Willingham et al [4] *	0.5 μ m CMOS	2.4	48	50	-100	-211	135
This work	0.35 μ m SiGe BiCMOS	2.432	16	< 100	-97	-213	18

transistor Mb. This degeneration also reduces the 1/f noise of the current sources when they are turned on. Even with the use of source degeneration, the transistors have to be fairly large to allow for low noise. The noise contributions of the current sources were evaluated by placing them in a simulation test bench where the currents were turned on continuously. Then a simple ac analysis was used to observe the simulated current noise. From this, their contribution to the BFM was calculated.

The switching transistors can be smaller to present a lighter load to the PU and PD driving signals from the phase detector. The light load is necessary to obtain fast switching which, in turn, prevents the linearity from degrading. Fast switching helps to meet the linearity specification which can be simulated by exercising the charge-pump with pulses of linearly varying width and checking that the output charge also varies linearly.

The p-type current source is shown in Fig. 10(b). It is a p-type version of the n-type current source just described. Both the p-type and n-type current sources are replicated eight times to generate the desired 500 μA.

IV. EXPERIMENTAL RESULTS

The synthesizer chip was designed and fabricated in a 0.35-μ m SiGe process. The parts were packaged in a 24 pin leadless plastic chip carrier (LPCC) package. A test board with a 16-MHz crystal, an op-amp based loop filter and external VCO was built. Two versions of this board were built. One with a 50 KHz loop bandwidth and the other with a 150 KHz loop bandwidth. The output frequency range is 2.4–2.485 GHz. The output spectrum of the synthesizer is shown in Fig. 11 for a 1 MHz frequency span at an output frequency of 2.434 GHz. Fig. 12 shows the output of the synthesizer with a 10 KHz frequency span. These are for the 50 KHz loop bandwidth boards and fractional-*N* operation.

The synthesizer phase noise for a 50 KHz loop bandwidth is shown in Fig. 13 and the phase noise for a 150 KHz loop bandwidth is show in Fig. 14. In both cases, the synthesizer is in fractional-*N* mode. For the 50 KHz case, the phase noise at a 10 KHz offset is -94 dBc/Hz. For the 150 KHz case, the phase noise at a 10 KHz offset is -97 dBc/Hz. This difference is due to the fact that in the 50 KHz case, the in-band VCO contribution to the phase noise is not suppressed enough to show the actual noise floor of the synthesizer. Opening the bandwidth to 150 KHz suppresses the VCO noise enough to view the true noise floor of the synthesizer. Because the loop bandwidth has been increased significantly, the loop is less able to suppress out of band quantization noise. This residual quantization noise is clearly visible in Fig. 14. The -123 dBc/Hz noise floor shown above 2 MHz in Fig. 13 would be inadequate for many applications, but this is entirely contributed by off chip components (VCO, pad, PA, pad) and measurement error.

The rms phase error within a 100 MHz bandwidth of the carrier for this synthesizer in Fractional-*N* mode is about 0.8° or 0.9 ps of rms jitter at 2.43 GHz. For bandwidths less than 100 MHz, the rms phase error is dominated by in-band noise.

It should be noted that no spurs can be observed over the tuning bandwidth (16 MHz) except when the synthesizer is offset from an integer boundary (output frequency which is an integer multiple of the reference frequency) by less than the loop bandwidth of the synthesizer. In this case, a spur appears at an offset from the carrier equal to the offset from the integer boundary. A second spur occurs at one half this offset. Both are less then 60 dB below the carrier peak. It is possible to turn off the $\Delta\Sigma$ modulator and operate the synthesizer in integer-*N* mode. This was done in order to see if the phase noise changed. The resulting phase noise plot is shown in Fig. 15 for the 150 KHz case. It can the seen that the phase noise is -100 dBc/Hz at a 10-KHz offset. The residual quantization noise is no longer present due to integer-*N* operation. The 3-dB increase in phase noise in fractional mode is due to residual nonlinearity in the PFD which folds high-frequency quantization noise into the synthesizer baseband. The rms phase error within a 100-MHz bandwidth of the carrier in integer-*N* mode is about 0.6° or 0.7 ps of rms jitter at 2.43 GHz.

The synthesizer has a control feature which allows the dc phase offset to be disabled. Turning off this offset in integer-*N* mode has no effect on in-band phase noise. However, if the offset is disabled in fractional-*N* mode the in-band phase noise

increases by as much as 20 dB. This illustrates the effect of PFD dead-zone nonlinearity on fractional-*N* operation.

The synthesizer specifications are summarized in Table II.

The BFM for this synthesizer is -216 dB in integer-*N* mode and degraded to -213 dB in fractional-*N* mode. However, this degradation does not arise from a simple linear addition of added quantization noise. Rather, it is due to nonlinearity in the PFD and charge-pump and noise in the offset current. Table III presents a comparison of the synthesizer presented here with other state-of-the-art synthesizers. The table includes the above BFM for in-band phase noise.

V. Conclusion

A 2.4 GHz $\Delta\Sigma$ fractional-*N* frequency synthesizer has been presented which was implemented in a 0.35-μm SiGe process. The synthesizer exhibits a low in-band phase noise of -97 dBc/Hz@10 KHz offset for an output frequency of 2.434 GHz in fractional-N mode. This is a figure of merit (BFM), for in-band phase noise, of -213 dB. In integer-*N* mode the phase noise is -100 dBc/Hz@10 KHz which is a BFM of -216 dB.

The techniques used to design the synthesizer are explained in detail. We have described the use of BFM in a systematic approach to addressing in-band phase noise that gives a very early indication of how difficult the circuit design problems will be. We have shown how the most important sources of noise, including noise folding, all correspond to an equivalent rms jitter and thus contribute to the typical charge-pump behavior described in Banerjee's equation. The techniques presented here appear to be adequate to create a state of the art synthesizer in terms of in-band phase noise.

Acknowledgment

The authors gratefully acknowledge the Academy of Finland for there support.

References

[1] N. J. R. King, "Phase Locked Loop Variable Frequency Generator," U.S. Patent US4 204 174, May 1980.

[2] W. Rhee, B. Sup-Song, and A.Akbar Ali, "A 1.1 GHz CMOS fractional-*N* frequency synthesizer with a 2-b third-order $\Delta\Sigma$ modulator," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1453–1460, Oct. 2000.

[3] W. Rhee, B. Bisanti, and A. Ali, "An 18 mW 2.5 GHz/900-MHz BiCMOS dual frequency synthesizer with <10 Hz carrier resolution," *IEEE J. Solid-State Circuits*, vol. 37, pp. 515–520, Apr. 2002.

[4] S. Willingham *et al.*, "An integrated 2.5 GHz $\Delta\Sigma$ frequency synthesizer with 5 μs settling and 2 Mb/s closed loop modulation," in *Proc. Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2000, pp. 200–201.

[5] T. Riley and J. Kostamovaara, "A hybrid fractional-*N* frequency synthesizer," *IEEE Trans. Circuits Syst. II*, vol. 50, pp. 176–180, Apr. 2003.

[6] J. A. Crawford, *Frequency Synthesizer Design Handbook.* Norwood, MA: Artech House, 1994.

[7] M. Perrott, M. Trott, and C. Sodini, "A modeling approach for $\Delta\Sigma$ fractional-*N* frequency synthesizers allowing straightforward noise analysis," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1028–1038, Aug. 2002.

[8] D. Banerjee. (2001) *PLL Performance, Simulation and Design* [Online] http://www.national.com/appinfo/wireless/files/Deansbook_4_01.pdf

[9] E. Hegazi and A. A. Abidi, "A 17-mW transmitter and frequency synthesizer for 900-MHz GSM fully integrated in 0.35-um CMOS," *IEEE J. Solid-State Circuits*, vol. 38, pp. 782–792, May 2003.

[10] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 224–231, June 1977.

[11] E. Vittoz, M. Degrauwe, and S. Bitz, "High-performance crystal oscillator circuits: theory and application," *IEEE J. Solid-State Circuits*, vol. 23, pp. 774–783, June 1988.

[12] D. Aebischer, H. Oguey, and V. R. von Kaenel, "A 2.1-MHz crystal oscillator time base with a current consumption under 500 nA," *IEEE J. Solid-State Circuits*, vol. 32, pp. 999–1005, July 1997.

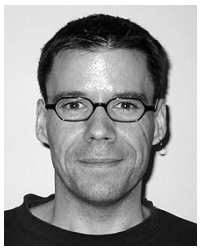
[13] B. De Muer and M. Steyaert, "A CMOS monolithic $\Delta\Sigma$-controlled fractional-*N* frequency synthesizer for DCS-1800," *IEEE J. Solid-State Circuits*, vol. 37, pp. 835–844, July 2002.

[14] R. Ahola and K. Halonen, "A 2 GHz $\Delta\Sigma$ fractional-*N* synthesizer in 0.35 μm CMOS," in *Proc. Eur. Solid-State Circuits Conf.*, Stockholm, Sweden, Sept. 2000, pp. 472–475.

[15] C.-H. Heng and B.-S. Song, "A 1.8 GHz CMOS fractional-*N* frequency synthesizer with randomized multi-phase VCO," in *Proc. Custom Integrated Circuits Conf.*, Orlando, FL, 2002.

Thomas A. D. Riley (M'82) received the B.E.Sc. degree from the The University of Western Ontario, London, ON, Canada, in 1982. He received the M.Eng degree from Carleton University, Ottawa, ON, Canada, through a cooperative research program with Mitel Semiconductor in 1989.

From 1982 to 1986, he was with Phillips Cables, Brockville, ON, a high voltage cable manufacturing company. Since 1995, he has been a Researcher at the University of Oulu, Oulun, Finland. He has also worked with Philsar Semiconductor, where he developed three fractional-*N* synthesizer chips.



Norman M. Filiol (M'97) received the B.Eng., M.Eng., and Ph.D. degrees in electrical engineering, from Carleton University, Ottawa, ON, Canada, in 1992, 1994, and 1999, respectively. His Ph.D. research on highly integrated building blocks for frequency synthesis and frequency discrimination for mobile radio was performed in a cooperative research agreement with Nortel Semiconductor, Ottawa, ON. Canada..

In 1999, he joined Philsar Semiconductor, Ottawa, where he participated in the architecture design of a fully-intgrated, low-power, Bluetooth transceiver. In 2001, he joined Kaben Research, Inc., Ottawa, ON, Canada, a semiconductor intellectual property provider for wireless SoCs. His current research interests include mixed signal IC design and architectures for mobile radio.

Dr. Filiol is currently on the Technical Advisory Board of Intelligent Photonics Control, an Ottawa, Canada based provider of SoC control subsystems for companies building low-cost, high-performance optical networks.

Qinghong Du received the B.Sc. and M.Sc. from Beijing Normal University, Beijing, China, and the Institute of Physics, Chinese Academy of Sciences, Beijing, in 1988 and 1991, respectively. He is currently pursuing the Ph.D. degree at Carleton University, Ottawa, ON, Canada.

His research interests include frequency synthesis and transceiver architectures.

Juha Kostamovaara (M'85) received the Dipl. Eng., Lic. Tech., and Dr. Tech. degrees in electrical engineering, in 1980, 1982, and 1987, respectively.

From 1987 to 1993, he was Acting Associate Professor of electronics, Department of Electrical and Information Engineering, University of Oulu, Oulun, Finland; in 1993, he was nominated for Associate Professor, and invited to become Full Professor of electronics in 1995. He is also currently Head of the electronics laboratory, where his group develops pulsed time-of-flight laser radar techniques especially for industrial applications. In 1994, he was an Alexander von Humboldt Scholar at the Technical University of Darmstadt, Germany. His main research interests include the development of time-to-digital converters, timing pick-off circuits, optical transceivers, and frequency synthesizers for optical measurements and telecommunications.