Techniques Minimize The Phase Noise in Crystal Oscillator Circuits

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***Abstract*—This paper reports a methodology of combining differential-phase-shift-injection-locking (DPSIL) with mode-coupled-delay-feedback (MCDF) techniques to shave the size, cost, and phase noise from Crystal oscillator circuits. An example of 100 MHz, 125 MHz and 155 MHz ovenized crystal oscillator (OCXO) is demonstrated for the validation of the novel approach, which holds good for both fundamental and higher order overtone mode high frequency crystal oscillator circuits.**

I. INTRODUCTION

The novel techniques described in this paper prevents the mode-jumping and minimizes the phase noise of crystal oscillator circuits. The reported technique improves the phase noise performance and stability, even those with relatively low quality-factor (Q) crystal resonators for high frequency low cost low phase noise signal source solutions.

II. DESIGN CONSIDERATION IN CRYSTAL OSCILLATORS

Many research works [1]-[7] have exploited different crystal oscillator circuit architectures, which usually play the important role in improving phase noise and stability performances. Recent publications [8]-[9] describe the design implementation of low phase noise Crystal oscillator circuits but they use high Q-factor expensive crystal resonator, and the topology is not optimized for both fundamental and overtone mode crystal oscillators. In this paper, differential-phase-shift-injection-locking (DPSIL) methods in conjunction with mode-coupled-delay-feedback (MCDF) technique as shown in Fig. 8 enable low phase noise solution for both fundamental and overtone-mode crystal oscillator circuits.

The technique is to dynamically suppress the intrinsic random fluctuation and mode-jumping dynamics of the low Q-factor crystal resonator. The simulated and measured data confirms up to some degree that the phase noise close to the carrier (<10 Hz offset from the carrier) does not primarily depend on the resonator's Q- factor and the 1/f-noise of the active devices but mainly on the fluctuation and intrinsic noise associated with crystal resonator for a given cut (AT/SC- cut). The novel DPSIL-MCDF technique (Fig. 8) minimizes close-in as well as far offset noise for low Q crystal oscillator circuits.

A. Conventional Crystal Resonator Model

Fig. 1 shows the typical representation of crystal resonator, the first *LCR* branch (L_1, C_1, and R_1) represents a fundamental modes (excited by the piezoelectric effect), C_0 is the holder capacitance, and the other branches (L_n, C_n, and R_n) are the odd overtone modes.

The input impedance Z(s) is [3]-[4]:

$$Z(s)=\frac{1}{Y(s)}=\frac{s^2+sR_i/L_i+1/L_iC_i}{sC_0[s^2+sR_i/L_i+(C_0+C_i)/L_iC_iC_0]}=\frac{(s-s_{z1})(s-s_{z2})}{C_0(s-s_{p0})(s-s_{p1})(s-s_{p2})} \quad (1)$$

$$s_{z1,2}=-\frac{\omega_0}{2Q}\pm j\omega_0\sqrt{1-\frac{1}{4Q^2}} \approx -\frac{\omega_0}{2Q}\pm j\omega_0, \quad for \quad Q>>1 \quad (2)$$

$$s_{p1,2}=-\frac{\omega_0}{2Q}\pm j\omega_0\sqrt{1+\frac{C_i}{C_0}-\frac{1}{4Q^2}}\approx -\frac{\omega_0}{2Q}\pm j\omega_0\left(1+\frac{C_i}{2C_0}\right) \quad (3)$$

$$\omega_i=\frac{1}{\sqrt{L_iC_i}}\Rightarrow f_i(series)=\frac{1}{2\pi\sqrt{L_iC_i}}, \quad Q=\frac{L_i\omega_0}{R_i}=\frac{1}{R_iC_i\omega_0} \quad (4)$$

where $s_{z1,2}$ and $s_{p1,2}$ are zero and poles, f_i is the series resonance frequency and Q is the quality factor. One can represent the parallel resonance condition as

$$\omega_p\approx\omega_0\left(1+\frac{C_i}{2C_0}\right)\Big|_{C_0>>C_i}\Rightarrow f_p(parallel)\approx\frac{1}{2\pi\sqrt{L_iC_i}}\left(1+\frac{C_i}{2C_0}\right)\Big|_{C_0>C_i} \quad (5)$$

$$m=\frac{2Q(\omega_p-\omega_0)}{\omega_0}=\frac{2Q(f_p-f_0)}{f_0}, \ m \text{ is mode separation} \quad (6)$$

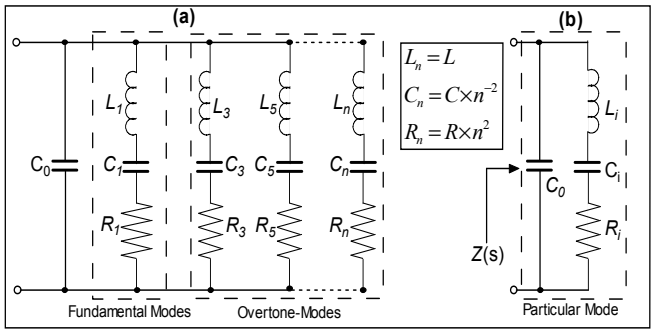

Fig. 1. A typical electrical equivalent circuit of a quartz crystal

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V_{dc}/V	F_{1meas}/MHz	F_{1sim}/MHz	P_{1meas}/dBm	P_{1sim}/dBm
8	155.554	155.551	0.1	0.35
10	155.557	155.551	2.2	2.47
12	155.560	155.551	3.8	4.15

Table 1: Measured Fundamental Frequency and Power vs. Simulated (for different supply voltages)

From (6), the intrinsic fluctuation in crystal influences the mode separation (m), and the degree to which crystal oscillator maintains a stable frequency f_i throughout a specified period of time is defined as the frequency stability of the source.

B. *Inadequacy of Conventional Crystal Resonator Model*

Fig. 2 shows the typical schematic of 155 MHz Colpitts crystal oscillator circuit using active device BFR92A and ideal crystal resonator (noise free) model. The model for the active element BFR92A is based on the EEBJT2 model (courtesy of Agilent ADS 2011) which is extended by a flicker noise source.

The CAD simulation model is expanded by the layout component using S-parameter model for the interconnecting layout, whereas passive components are replaced by accurate substrate scalable models. A DC-bias stabilization circuitry is implemented in order to reduce the noise contribution of the RF Transistor.

The simulated and measured data shown in Table 1 explains the drive-level dependency and nonlinear resonator dynamics. The discrepancies in measured phase noise data close to the carrier is more than 30 dB above the level predicted by utilization of the ideal model for the resonator. This analysis explains the proof of intrinsic fluctuations of the reactance of crystal resonator components.

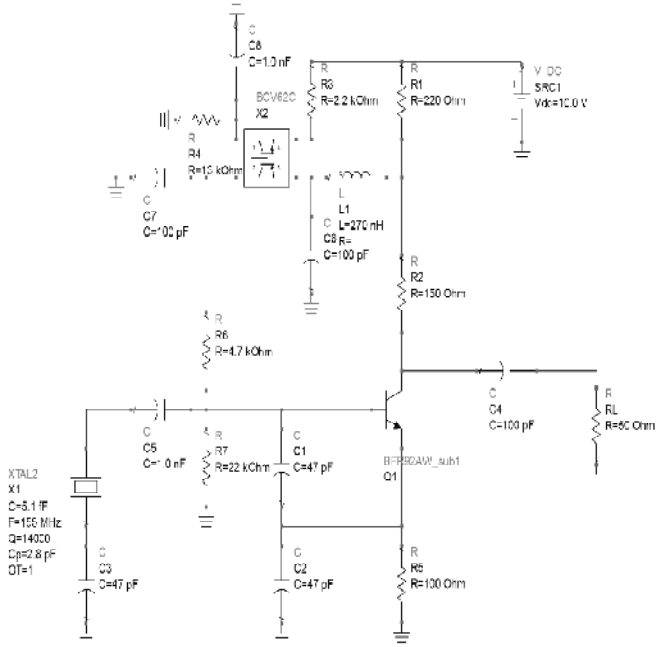

Fig.2. Schematic of 155MHz Crystal oscillator using ideal elements

C. *Real Crsytal Resonator Model (Nonlinear model)*

The conventional linear LCR crystal resonator model as shown in Fig.1 can be extended to nonlinear drive-level dependent $L_{m,k}(t)C_{m,k}(t)R_{m,k}(t)$ model as:

$$L_{m,k}(t) = L_{m0,k}[1 + a_L i_{cr}(t)^2]^{-1} \times [1 + m_{nl}(t)] \quad (7)$$

$$C_{m,k}(t) = C_{m0,k}[1 + a_C i_{cr}(t)^2]^{-1} \times [1 + m_{nc}(t)] \quad (8)$$

The impact of resistive component $R_{m,k}(t)$ on mode-jumping is insignificant as compared to reactive component inductance $L_{m,k}(t)$ and capacitance $C_{m,k}(t)$. The noise-modulation in the frequency domain is given by

$$< M_{nL,C}(f)^2 > = K_{fL,fC} I_{cr}(f_1)^{-n/f} \quad (9)$$

where $< M_n(f)^2 = \int_{-\infty}^{\infty} m(t+\tau)m(t)dt$ (10)

$i_{cr}(t)$: total current thru the crystal in the time-domain

$I_{cr}(f_1)$: spectral component of the current thru the crystal at f_1

From (7)-(10), the instantaneous value of the respective equivalent circuit parameter of the k[th] crystal harmonic is a non-linear function of the total current thru the crystal, modulated by a random time-function formulated as a 1/*f*-noise quantity in the frequency-domain.

Fig.3 shows the implementation of the formulation described in (7)-(10) using SDD (Symbolically-Defined Devices) model in ADS 2011. The formulation of currents thru the dynamic capacitances and conductance of the k^{th} harmonic is done explicitly according to the nodal analysis as

$$i_{kC}(t) = C_{mk0}\frac{d}{dt}\left(\frac{v_k(t)[1+m_n(t)]}{1+ai_{cr}(t)^2}\right) \quad (11)$$

$$i_{kR}(t) = \frac{1}{R_{mk0}}\left(\frac{v_k(t)}{1+bi_{cr}(t)^2}\right) \quad (12)$$

The currents thru the inductance $L_{m,k}(t)$ is formulated implicitly according to the modified nodal analyses as

$$L_{mk0}\frac{d}{dt}\left(\frac{i_{kL}(t)[1+m_n(t)]}{1+ai_{cr}(t)^2}\right) - v_{kL}(t) = 0 \quad (13)$$

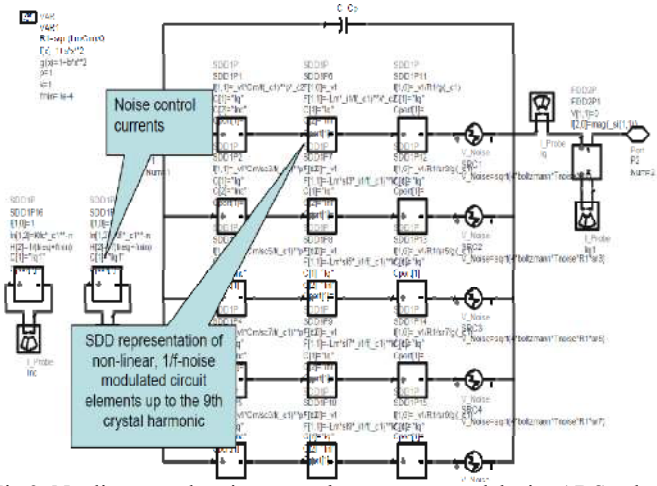

Fig.3 Nonlinear and noisy crystal resonator models in ADS-sub-circuit representation

V_{dc}/V	F_{1meas}/MHz	F_{1sim}/MHz
8	155.554	155.555
10	155.557	155.557
12	155.560	155.560

Table 2 Simulated and measured data: fundamental frequency (varying the DC-bias voltage)

The noise-modulation formulated in (9)-(10) is implemented within the SDDs by use of control-currents as shown in Fig. 3. Table 2 (frequency variation with DC-bias) and Fig. 4 (phase noise variation with DC-bias) show the close agreement between simulated and measured data. Comparison of the phase noise with ideal vs. real resonator explains the inadequacy of the simple LCR-model crystal shown in Fig.1.

D. Verification of Crystal Model with External Resonator

For ideal noiseless crystal resonator, this difference may be less pronounced; the contribution of the crystal's 1/f-noise to the overall phase noise however remains a matter of fact.

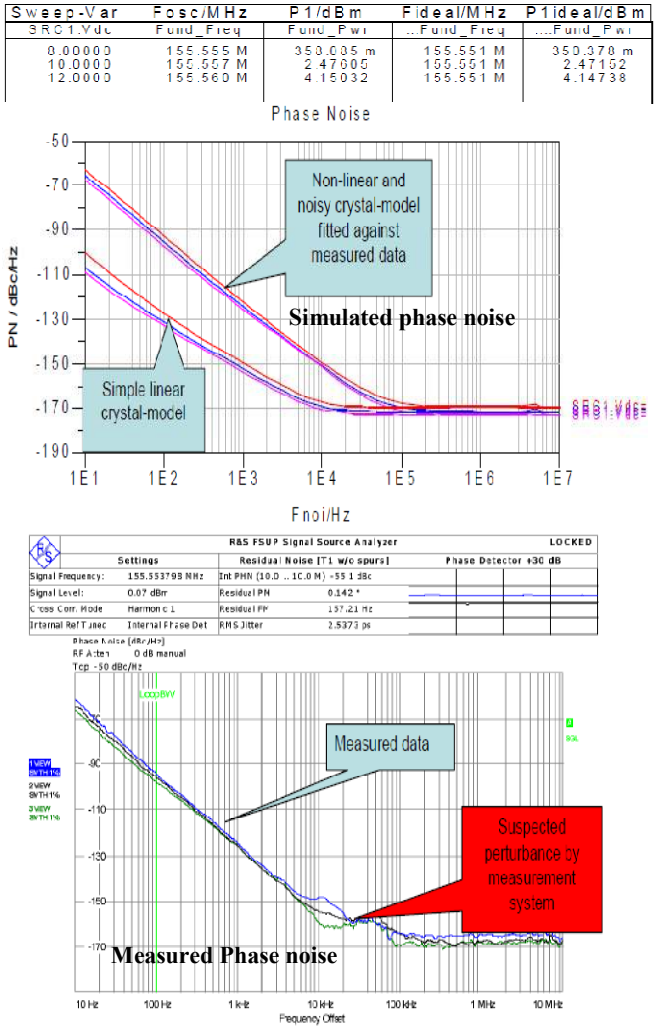

Fig.4 Simulated and measured phase noise plots (nonlinear resonator)

A series resistor is added to the fundamental resonant mode 155 MHz Colpitts oscillator shown in Fig. 5 for the realization of nonlinear noisy resonator (reduced loaded Q-factor).

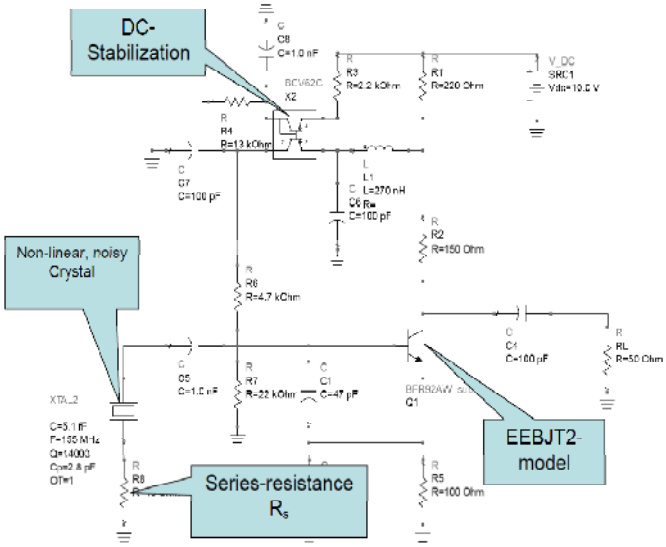

Fig.5. Schematic of 155MHz Crystal oscillator using non ideal resonator (Q-factor degradation due to external resistor)

R_s/Ohm	F1/MHz sim.	F1/MHz meas.	P1/dBm sim.	P1/dBm meas.
0	155.555	155.554	4.19	3.8
10	155.552	155.549	4.03	3.6
20	155.550	155.548	3.85	3.4

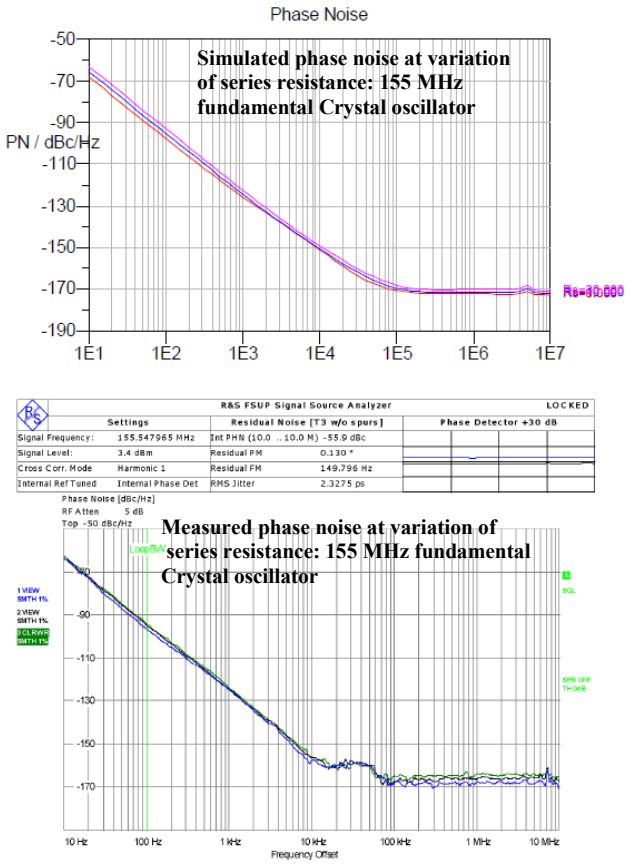

Fig.6 Simulated and measured phase noise (vary resonator resistance)

Fig. 6 shows the good agreement in phase noise with the simulated and measured data, the small differences ~ 0.4 dB in power is due to an uncertainty of the measurement system.

E. Overtone Crystal Oscillator-Verification of Loaded Q

The crystal used in Fig. 5 was replaced by 3rd overtone crystal operating at 100MHz. The static capacitance was neutralized by an appropriate shunt inductance. Fig. 7 shows the good agreement with simulated and measured data, the small discrepancies is the noise increase between 2 kHz and 50 kHz.

The nonlinear crystal resonator model formulated in (7)-(10) using SDD (Symbolically-Defined Devices) model in ADS 2011 (CAD tool from Agilent) is unable to predict mode jumping even in well-planned crystal oscillator circuit design.

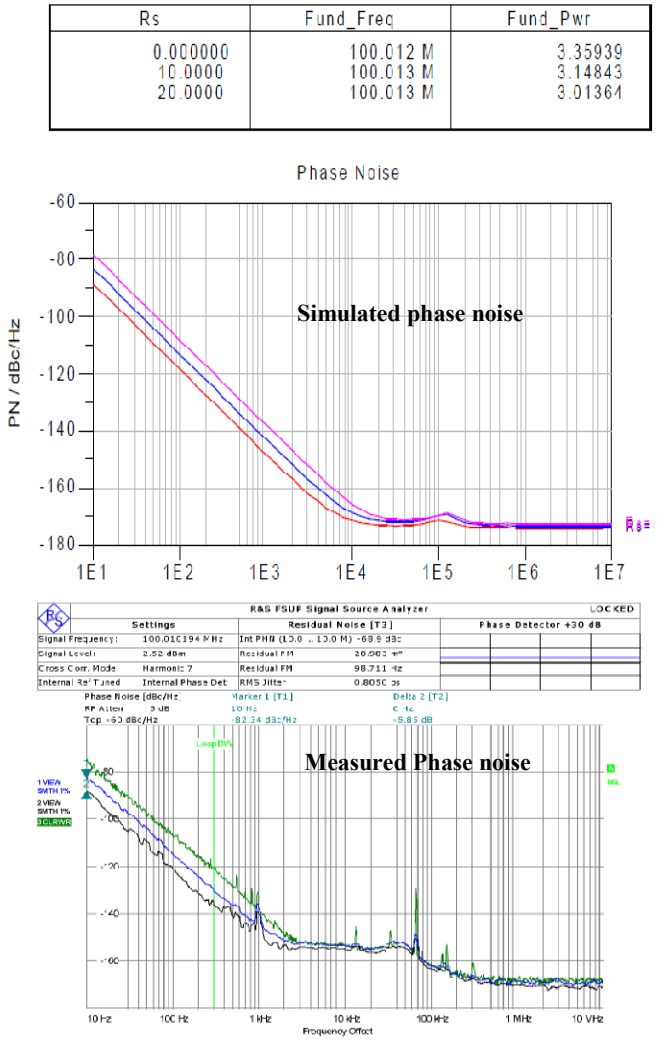

Fig.7 Simulated and measured phase noise plots of crystal oscillator

One simple technique is to minimize the mode separation (m) as described in (6) by incorporating novel mode-locking techniques shown in Fig. 8. The nonlinear drive-level dependent $L_{m,k}(t)C_{m,k}(t)R_{m,k}(t)$ model predicts a reduction of the crystal's noise-modulation contribution formulated in (9) with increasing drive-level but at the cost of uncertainty involved in current-exponents of the 1/f-noise functions (best fit: n=3, leads to a monotonically decreasing noise contribution with increasing drive-level).

III. Low Phase Noise Crystal Oscillator Circuit

The crystal oscillator circuit is, an important and critical module for modern communication system, being traded simultaneously by increase in the stability, improved phase noise performance, low cost, and decrease in physical dimensions. These challenges faced by circuit designers are rapidly increasing in both ovenized controlled crystal oscillators (OCXOs) and voltage controlled crystal oscillators (VCXOs), while the choices for solutions on how these challenges, especially low cost ultra low phase noise solution be best addressed are kept aside.

Unlike other high Q-resonator based oscillator circuits, crystal resonator based oscillators do not behave in totally predictable way, and are sensitive to mode jumping even in well-planned circuit design. Hence "tweaking" has been an accepted mainstay of the OCXOs and VCXOs design towards preventing undesired oscillation modes. One simple technique that can be utilized is to minimize mode separation (m) as described in (6) by using SDDs techniques explained in Fig. 3. This technique improves the stability but does not yield lowest phase noise solution which is critical parameter for frequency reference standards. The reported work describes an example to apply the concept of self-injection for minimization of phase noise and mode-locking for preventing the mode-jumping and improving the stability of OCXOs and VCXOs.

Figs.8 and 9 show the block diagram and prototype of OCXO that offers unified approach for low cost stable signal source solutions. The reported work describes an approach to overcome the uncertainty associated with crystal resonator modeling and suggest the unified topology using differential-phase-shift-injection-locking (DPSIL) methods in conjunction with mode-coupled-delay-feedback (MCDF) technique that enables low cost low phase noise solutions for both fundamental and overtone-modes crystal oscillator circuits. As shown in Fig. 8, DPSIL improves the close-in phase noise performance, whereas, MCDF prevents mode-jumping and improves the stability and far out phase noise performance.

Fig. 10 shows the measured phase noise plots for a 125 MHz OCXO circuits (OCXO#1, Vtune=2V; OCXO# 2, Vtune=5V; OCXO# 3, Vtune=2V; OCXO# 4, Vtune=5V) for giving brief insights about the self-injection mechanism using inexpensive crystal resonator (Q=80,000). By incorporating mode-coupling and phase-injection techniques, phase noise performance can be optimized for a given figure of merit (Fig. 11). As shown in Fig. 11, the measured phase noise for 125 MHz OCXO circuit is -142dBc/Hz at 100Hz offset from the carrier. In addition to this, adaptive filtering in conjunction with DPSIL-MCDF suppresses the intrinsic 1/f noise of crystal resonator, thereby improved close-in phase noise performance of 100 MHz OCXO circuits.

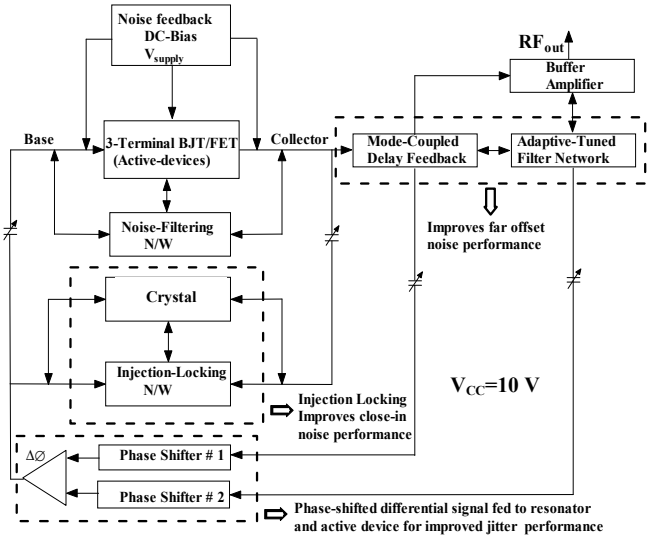

Fig.8. A block diagram of DPSIL-MCDF OCXOs (1x1x0.8 in)

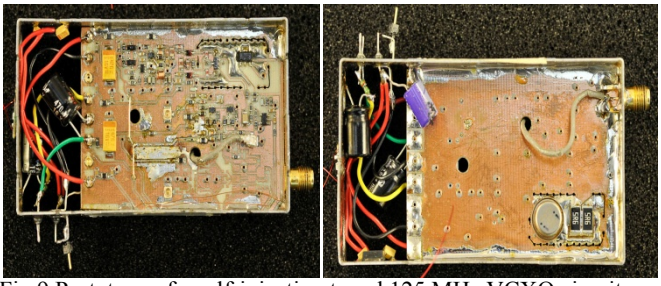

Fig.9 Prototype of a self-injection tuned 125 MHz VCXO circuit

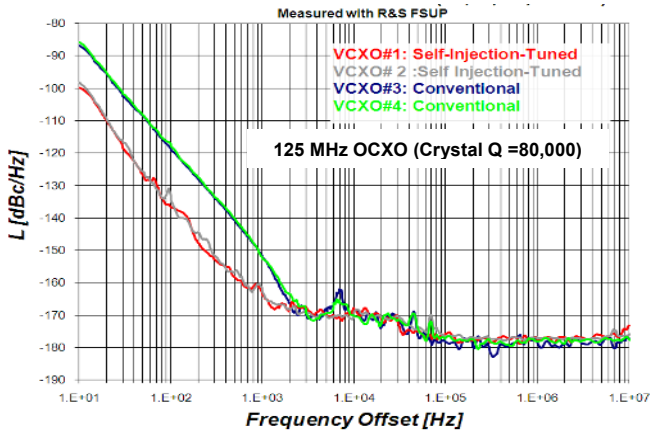

Fig.10. The measured phase noise plots of 125 MHz OCXO circuits

In many applications, OCXO is required to offer very low close-in phase noise. As shown in Fig. 8, differential phase-injection mechanism minimizes the 1/f noise of the crystal, thereby improves the close-in (<100 Hz offset from the carrier) phase noise performance of 100 MHz OCXO (Fig. 11). To author's knowledge, reported phase noise performance of 125 MHz OCXO is best phase noise performance (Fig. 12) to date using low Q quartz resonator (Q=80,000) for a given power consumption, size, stability, and Figure of merit. Figs. 12 and 13 show the phase noise plots of 100 MHz OCXO circuit for the validation of novel approach described in Fig.8. As shown in Fig. 14, minimization of noise performance at far offset (>100 kHz) is achieved by adaptive self-tuning filter network that introduces required delay to generate feedback signal for far out phase noise reduction.

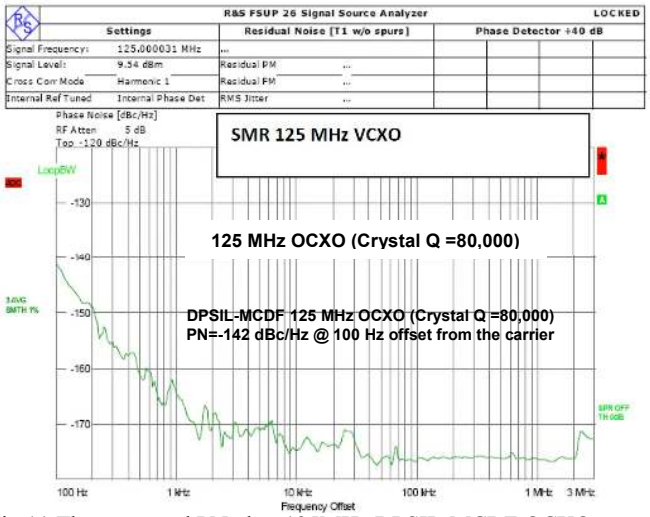

Fig.11 The measured PN plot: 125MHz DPSIL-MCDF OCXO

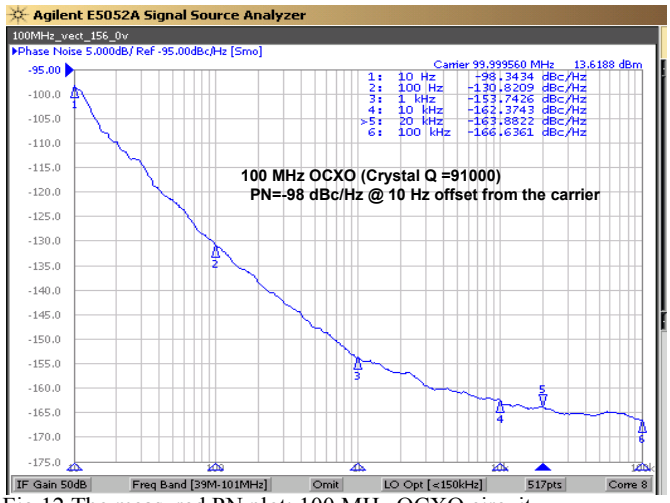

Fig.12 The measured PN plot: 100 MHz OCXO circuit

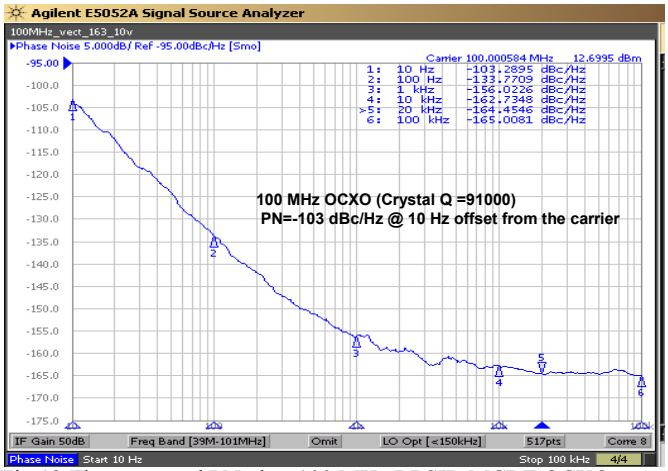

Fig.13 The measured PN plot: 100 MHz DPSIL-MCDF OCXO

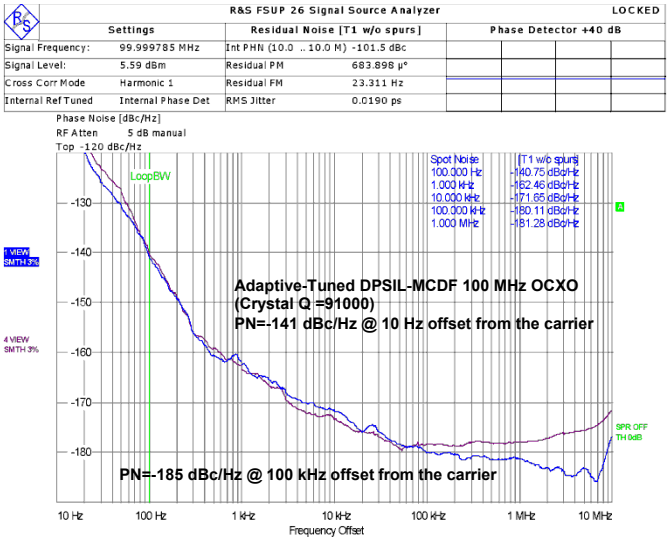

Fig.14 The measured PN plot: adaptive 100MHz DPSIL- OCXO

IV. VALIDATION

For the validation of the novel approach described in Figure 8, commercial OCXO circuit is modifed for enabling low phase noise charetaeristics. Figures 15, 16, 17, 19, and 19 show layout and phase noise plots of OCXO circuts. Fig. 20 shows the plot of Allan Variance of 100 MHz OCXO, and tested for the verification of repeatibility of the performances.

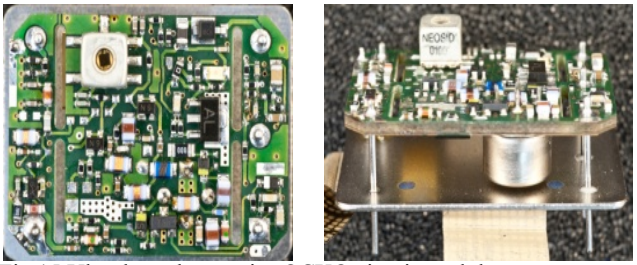

Fig.15 Ultra low phase noise OCXO circuit module

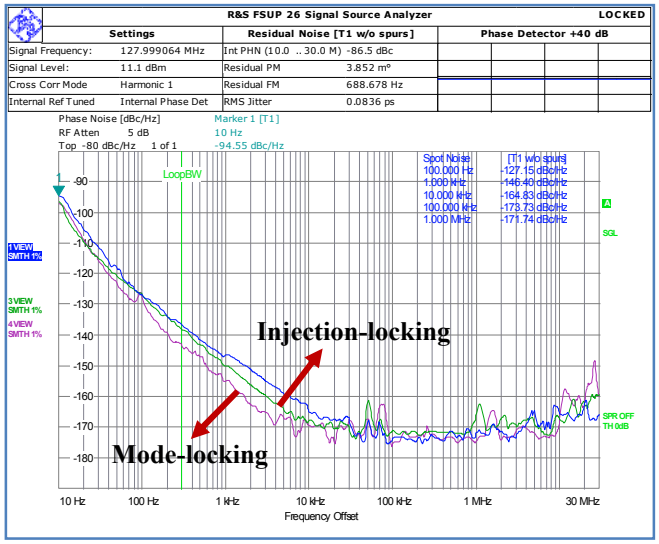

Fig.16 The measured PN plot of 128 MHz OCXO circuit

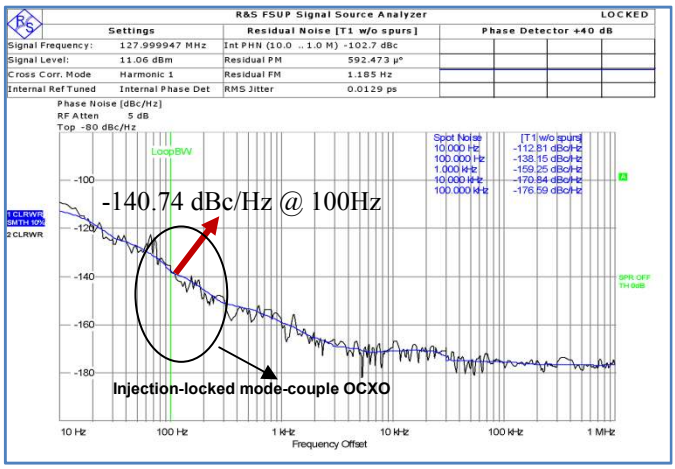

Fig.17. The measured PN plot of injection-locked mode-coupled 128 MHz OCXO

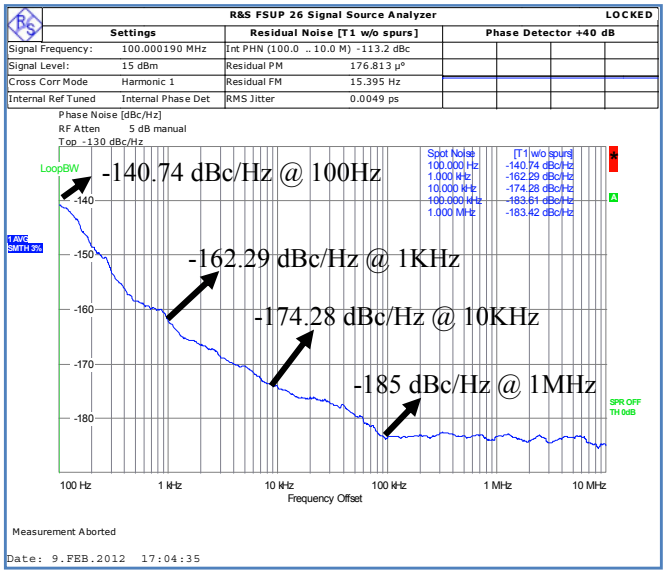

Fig.18 The measured PN plot 100MHz DPSIL-MCDF OCXO

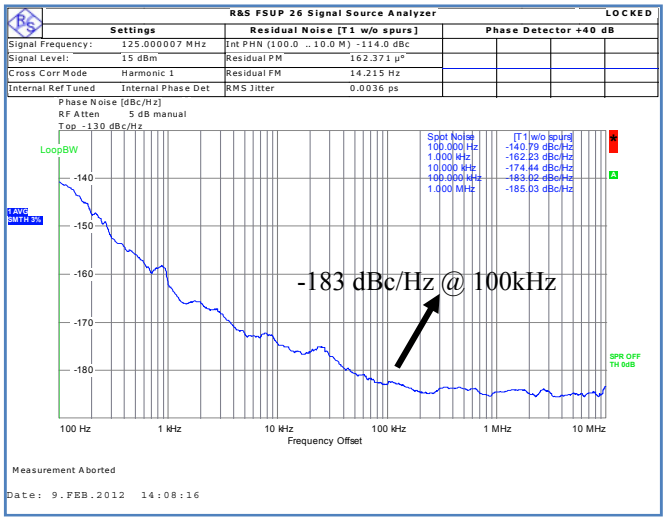

Fig.19 The measured PN plot 125 MHz DPSIL-MCDF OCXO

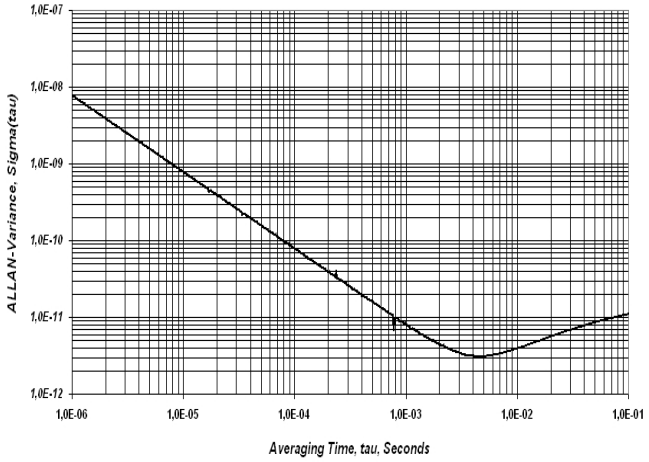

Fig.20 The measured plot of Allan Variance of 125 MHz OCXO

V. CONCLUSION

The reported DPSIL-MCDF topology enables unified approach for designing low cost low phase noise OCXOs.

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