Technology and Reliability Constrained Future Copper Interconnects—Part II: Performance Implications

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***Abstract*—This work extends the realistic resistance modeling of on-chip copper interconnects to assess its impact on key interconnect performance metrics. As quantified in Part I of this work, the effective resistivity of copper is not only significantly larger than its ideal, bulk value but also highly dependent on technology and reliability constraints. Performance is quantified under various technological conditions in the future. In particular, wire delay is extensively addressed. Further, the impact of optimal repeater insertion to improve these parameters is also studied using realistic resistance trends. The impact of technologically constrained resistance on power penalty arising from repeater insertion is briefly addressed. Where relevant, aforementioned results are contrasted with those obtained using ideal copper resistivity.**

***Index Terms*—Cross talk, delay, interconnect performance, repeater power, repeaters, wire inductance.**

I. Introduction

RAPIDLY increasing transistors in the future will lead to an increasing number of wires within a finite chip area. The limited area along with the constraints on the number of metal levels forces an aggressive shrinking of interconnect pitch, even at the global level [1]. The scaling of interconnects coupled with the trend of larger numbers of them having longer lengths in the future will lead them to have a higher resistance and capacitance, and thus, a much larger RC delay. In the future, global wires will not only get slower compared to increasing device speeds but will also get slower in absolute terms. This deterioration in interconnect performance could result in them quickly becoming performance bottleneck. Various solutions, including new materials such as copper (Cu) and low dielectric constant material (low-k) as well as periodically stacked repeaters are employed to alleviate the problem. Repeaters reduce the interconnect delay, increase the wire bandwidth, reduce cross talk, and increase SNR by periodically boosting the signal. However, they have the penalty of increasing chip area and power; and power itself may limit chip performance in the future.

This work attempts to realistically assess the efficacy of the proposed solutions (Cu, low-k and repeaters) for mitigating the interconnect problems. Further, it briefly addresses the penalties of these solutions, in particular, the power penalty arising from repeaters. Most importantly, this work performs the aforementioned analysis accurately using realistic, dimension-dependent, and technology-dictated Cu resistance described in the accompanying paper [2]. It was shown that scaling will dramatically deteriorate the effective Cu resistivity. To our knowledge, it is the first effort to achieve these goals using nonideal resistivity for copper. Significant underestimation of the interconnect problem and overly optimistic assessment of the impact of the deployed solutions can result if ideal copper resistivity is used in analyzing performance. When appropriate, we compare our results with those obtained using ideal copper resistivity to highlight the discrepancy arising from the simplistic assumption.

The interconnect metrics examined in this work fall under the broad categories of 1) delay; 2) data transmission reliability; and 3) power dissipation. Not all metrics are examined in detail and for some of them such as power, the discussion is only limited to penalty arising from repeaters. We have organized the rest of the paper as follows. In Section II, we examine issues related to interconnect latency. This includes characterizing delay with and without repeaters using practical resistance trends to evaluate realistic advantage of repeaters. Using our resistance projections, we further examine the length scales at which it is necessary to incorporate interconnect-inductance in delay calculations. Finally, we explore the possible ways in which the increasing interconnect delay can hinder performance. In Section III, we qualitatively discuss the role of resistance modeling on signal transmission reliability. In Section IV, we briefly discuss the penalties arising from power consumption due to repeaters. Finally, we summarize and conclude in Section V.

II. Delay and Its Impact Using Realistic Resistance Trends

A. Delay of RC Wires

In this section, we develop future global wire delay projections using ITRS'99 data [1]. These interconnects are most critical as they get longer with successive technology node. The delay is critically based on resistance per unit length modeling described in Part I of this work [2], under various technological scenarios. Most subsequent calculations assume reasonable technological conditions. This includes the surface scattering parameter (P) value of 0.5 [3], a chip temperature of 100 °C, a minimum metal barrier thickness of 10 nm and either the best available atomic layer deposition (ALD)-based barrier or the currently prevalent Ionized physical vapor deposition (IPVD)-based barrier.

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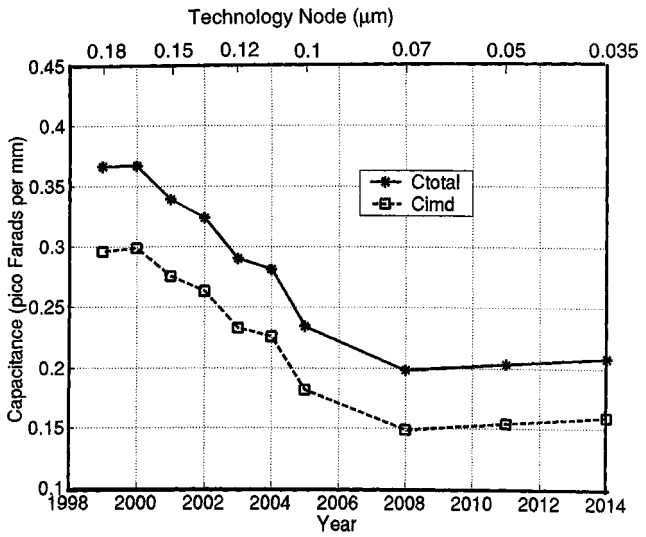

Fig. 1. Worst case capacitance per unit length for global wires in future. Also showing the intermetal capacitance contribution.

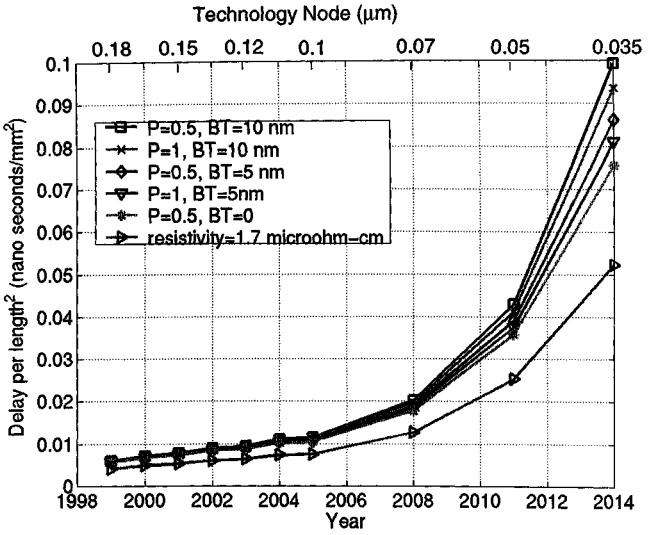

Fig. 2. RC delay per square length for global Cu interconnects under various practical constraints. BT is barrier thickness.

The capacitance per unit length, needed for delay calculations, is obtained using a simplistic parallel plate model consisting of inter and intralevel contributions along with a fringe component. This fringe component is assumed to be approximately constant over future technology nodes and is taken to be the same as its current value of about 0.04 pf/mm [4]. The interlevel dielectric thickness is assumed to be the same as the metal thickness and the intralevel dielectric thickness and wire width is assumed to be half of the pitch. The capacitance trends account for the lowering of dielectric constant with future technology nodes as per ITRS. An average dielectric constant value is used for the case where a range of values is suggested in the roadmap for a given technology node. Further, the capacitance values shown here represent the worst switching scenario when two adjacent wires, on the same level, are simultaneously switching in the apposite direction as the signal line, hence doubling the intralevel capacitance contribution. The worst case capacitance per unit length is thus given by

$$C_w = 2\varepsilon_d\varepsilon_0\left(\frac{1+2AR^2}{AR}\right)+C_{fringe}. \tag{1}$$

Here, C_w is the wire capacitance per unit length, ε_d is the dielectric constant assumed to be homogeneously distributed both between layers and between metal lines within a layer, ε_0 is the permittivity of free space, and AR is the aspect ratio of the wire defined as the thickness to width ratio of the metal. The capacitance per unit length using above formulae is shown for global wires in Fig. 1. The figure also explicitly shows the intralevel (intermetal) capacitance contribution. The gradually decreasing capacitance trend is a result of two competing factors: scaling induced increase and a low-k material induced decrease in capacitance. Using the resistance per unit length [2] R_w and the capacitance C_w per unit length values and the following formula [5], the RC delay per square length τ_l is plotted in Fig. 2

$$\tau_l = 0.4R_wC_w. \tag{2}$$

It is found that delay as high as 99 ps/mm^2 will be obtained at 35 nm technology node (year 2014) using aforementioned realistic technology parameters and the best ALD barrier. This delay is severely underestimated to be 52 ps/mm^2, if the ideal copper resistivity of 1.7 $\mu\Omega$-cm is assumed.

Next, interconnect line delays with and without repeaters is calculated. Repeaters help by converting the length dependence of wire delay from quadratic to linear. They also reduce the dependence of delay on resistance and capacitance per unit length of the wire from linear to square root, thus somewhat absorbing the shock of scaling induced increase in resistance per unit length. Finally, they introduce a square-root dependence on the progressively decreasing transistor delay, which helps to counter the increase in wire RC product. The expression for delay of a driver of resistance R_d and diffusion capacitance C_d driving a load C_L through an interconnect with R_w and C_w resistance and capacitance per unit length, respectively, has five components, namely, R_dC_d, R_dC_w, R_dC_l, R_wC_L, and R_wC_w. For long global lines without repeaters, the interconnect delay term (R_wC_w) tends to dominate. Hence, only this term is considered in calculating the delay without repeaters.

On the other hand, the delay of an optimally buffered (with repeaters) link is obtained by first considering the stage delay defined as the switching delay of a repeater (inverter) driving the subsequent inverter and is given by [5], [6].

$$T_{stage} = b(x)R_{tr}(C_L+C_p)+b(x)(R_{tr}C_w+R_wC_L)l_s + a(x)R_wC_wl_s^2. \tag{3}$$

Here, T_{stage} is the delay per stage, R_{tr} is the resistance of the inverter transistors, C_L is the input capacitance of next inverter, C_p is the diffusion capacitance of the driving inverter, and l_s is the length of the wire between two inverters. The voltage at the output of the repeater is assumed to switch instantaneously when the input reaches a certain fraction x of the total swing [6]. $a(x)$ and $b(x)$ are switching model dependent parameters and for $x = 0.5$, $a(x)$ is 0.4 and $b(x)$ is 0.7 [7]. If the total

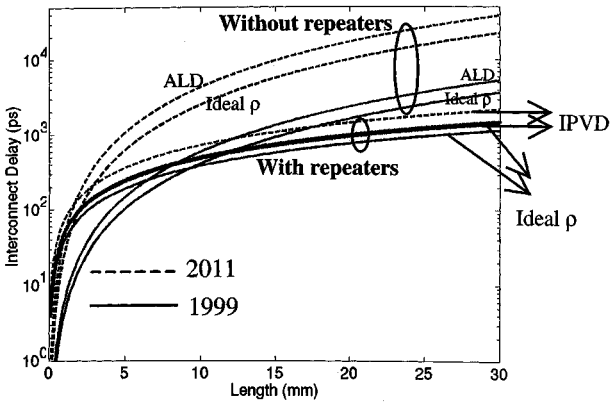

Fig. 3. Global wire delay versus wire length with and without repeaters for various technological constraints.

length of the line is L, then the number of stages equal L/l_s. The total delay from the driver to the load is then

$$T_{total} = \frac{L}{l_s} * T_{stage} = \frac{L}{l_s} \cdot \left(0.7R_{tr}(C_L + C_p + C_w l_s) + 0.7R_w C_L l_s + 0.4R_w C_w l_s^2\right). \quad (4)$$

We assume that the NMOS transistor in the inverter is sized S times the minimum width transistor and that the PMOS FET is twice the size of NMOS FET. We further assume that the diffusion capacitance is approximately the same as the gate capacitance. If C_{nmos} is the capacitance of the minimum width NMOS transistor of a generation and r_o is its resistance then $R_{tr} = r_0/S$, $C_L = C_p = 3SC_{nmos}$. Substituting these values in (4), we get an equation in terms of unknowns, repeater size (S), and spacing (l_s). The equation can be independently optimized with respect to each of these parameters and yields the following results:

$$t_{total} = 5L\sqrt{r_o C_{nmos} R_w C_w} = 2L\sqrt{(0.4R_w C_w)(t_{FO4})} \quad (5)$$

$$l_{opt} = 3.24\sqrt{\frac{r_o C_{nmos}}{R_w C_w}} \quad (6)$$

$$S_{opt} = 0.58\sqrt{\frac{r_o C_w}{R_w C_{nmos}}}. \quad (7)$$

Here, t_{total} is the optimized total delay, l_{opt} is the optimal spacing between repeaters, and S_{opt} is the optimal width-to-length ratio of the NMOS transistor. In (5), t_{Fo4} is the fan-out of four, inverter delay. In units of ps, t_{Fo4} is estimated to scale as $500L_{gate}$, where L_{gate} is in μm and is approximately the same as the technology node [5].

Fig. 3 shows a plot of delay versus the length with and without the repeaters. Delay is plotted for two different years i.e., 1999 and 2011, corresponding to 180 and 50 nm technology node, respectively. Figure contrasts the delay results using ideal resistivity with that obtained using realistic Cu resistivity with reasonable constraints and both ALD and IPVD barrier. It is observed that repeaters substantially mitigate the increase in delay. An interesting observation is that with ideal copper resistivity, the delay per unit length with repeaters remains approximately unchanged in the future. This is because the decreasing transistor gate delay compensates almost exactly for the increase in the interconnect resistance and capacitance. However, if technological constraints are incorporated, the interconnect resistance rises much faster, giving an overall increase in the delay per unit length in the future. This is depicted in Fig. 3 by the, nonoverlapping, year 1999 and 2011 curves with the IPVD barrier technology.

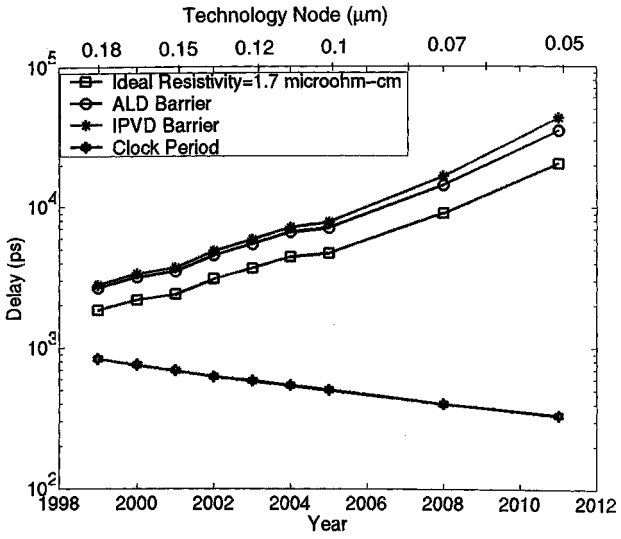

Fig. 4. Global wire delay versus technology node without repeaters under various barrier technologies: $P = 0.5$, temp. = 100 °C, barrier = 10 nm. Clock period is superimposed.

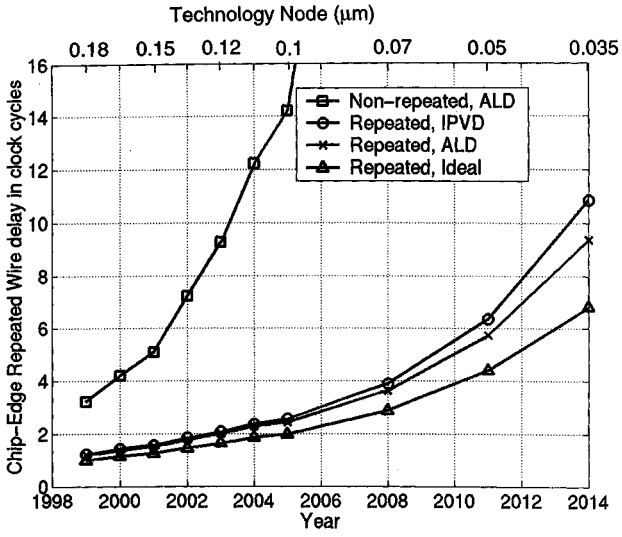

Fig. 5. Chip-edge long repeated global wire latency in terms of clock cycle, using various reasonable technology constraints on resistivity. Nonrepeated wire latency with ALD barrier superimposed partially.

Fig. 4 shows the future chip-edge long delay without repeaters under different technology constraints. The nonrepeated wires with practical constraints result in delays of about 120–130 clock cycles across chip, at 50 nm node. This translates to only about 250 μms of distance in one clock cycle. On the other hand, ideal Cu resistivity yields nonrepeated, across-chip delays of about 60–70 times the clock period. Fig. 5 shows the delay of a chip-edge long wire with repeaters, in terms of clock period for future technology nodes (year). Nonrepeated wire delay with ALD is partially superimposed for comparison.

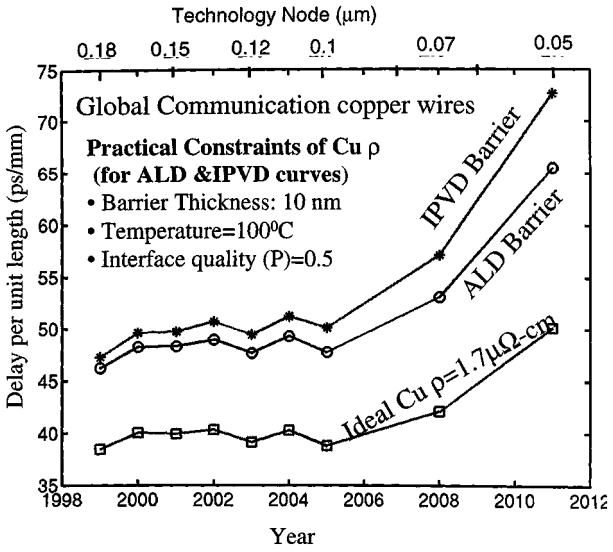

Fig. 6. Effect of practical resistivity modeling on repeated wire latency per unit length. $P = 0.5$, temp. = 100 °C, barrier thick = 10 nm.

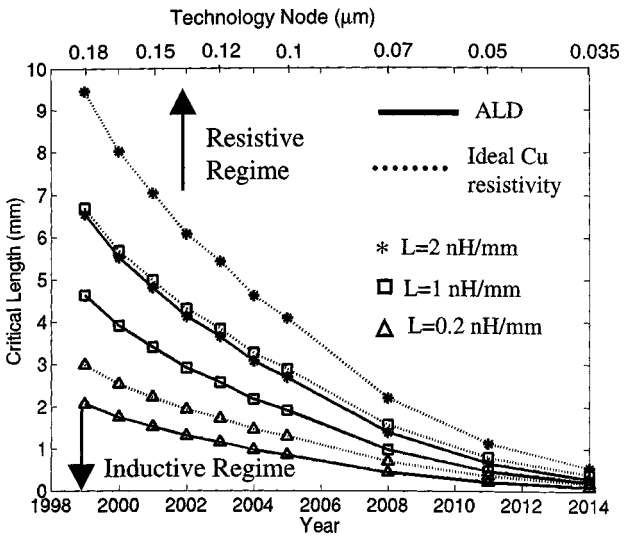

Fig. 7. Critical length below which inductance becomes important for global wires. For ALD, $P = 0.5$, temp. = 100 °C, barrier thick = 10 nm.

Repeated wire delay is plotted for ideal as well as realistic resistivity with ALD and IPVD barriers. It is seen that despite substantial reduction in delay with repeaters, across-chip latency still reaches about 9.4 clock cycles at 35 nm node with realistic resistivity using ALD barrier. With IPVD barrier, this number is about 10.9 clock cycles and is quite underestimated to about 6.8 clock cycles with ideal Cu resistivity. The discrepancy between ideal and practical resistivity calculations, although substantial, is still lesser compared to the case without repeaters because of only a square root dependence of repeated wire delay on resistance per unit length. These delay numbers are for worst case switching scenario. The repeated delay with ALD increases approximately 8 times from about 1.2 times the clock period at 180 nm node to 9.4 times clock period at 35 nm node. This 8× rise in latency occurs due to three independent factors: 1) 3× increase in clock frequency, 2) 1.45× increase in chip edge, and 3) 1.81× increase in delay per unit length of repeated wire. The last component is explicitly plotted in Fig. 6 for three different Cu resistivity scenarios, i.e., ideal, with ALD barrier, and with currently prevalent IPVD barrier. As pointed out earlier, the delay per unit length hardly changes with ideal resistivity, however, it visibly increases with practical resistivity constraints. Even with the best ALD barrier, repeated wires delays of about 66 ps/mm and 85 ps/mm are observed at 50 and 35 nm nodes, respectively. For the sake of comparison with an alternate technology, 85 ps/mm is about 26 times slower than the free space velocity of light.

B. Significance of Inductance Effects in Delay Calculations

So far, our treatment of delay is solely based on a RC behavior of on-chip wires. It is important to evaluate the importance of inductance in these calculations. A significant effort has been invested in this direction [8]–[11]. An accurate assessment of the impact of inductance, critically requires using realistic wire resistance parameters. The use of a smaller wire resistance value can lead to a misleading and exaggerated effect of inductance. The inductance for delay calculations can be ignored and RC delay model becomes more accurate as the length of a wire becomes greater than a critical length [12]. The critical length l_{crit}, below which inductance has to incorporated in delay calculations, depends on relative values of resistance, R_w, capacitance, C_w, and inductance, L_w, per unit length values. It can be evaluated by simply equating the RC and the LC delays of a wire and is given by [13]

$$l_{crit} = \frac{2.77}{R_w}\sqrt{\frac{L_w}{C_w}}. \tag{8}$$

Incidentally, l_{crit} is also approximately the length at which a low loss LC line exhibits attenuation equal to $1/e$ of its original value. There also exist a driver and wire characteristic-impedance dependent second condition, which dictates the importance of inductance [8]. However, in this work, we only discuss the above condition related to l_{crit}, as it has a direct dependence on wire resistance. The critical length l_{crit}, for global wires, as a function of future technology nodes, is shown in Fig. 7. C_w used in (8) is calculated assuming grounded adjacent wires. The l_{crit} may vary slightly depending on the switching conditions of adjacent wires. The figure contrasts l_{crit} obtained using ideal and technology constraint Cu resistivity. A large error in l_{crit} is observed with ideal resistivity, because of a linear dependence of l_{crit} on R_w. Three different inductance values of 0.2, 1, and 2 nH/mm are used for this calculation. Inductance values of 1 nH/mm or less are typical in an on-chip environment [12]. These values are expected to remain in this range and may even decrease in the future at higher frequency [12] as at higher frequency return current path tends to be closer to signal to minimize inductive reactance (ωL)-dominated impedance. Fig. 7 shows that for a typical inductance of 1 nH/mm at 180 nm technology node and for realistic resistance values, minimum pitched global wires greater than about 4.6 mm can be treated as RC lines for delay purposes. This number reduces to about 0.45 mm at the 50 nm technology node showing that wire delay is progressively becoming RC in nature. Inductance effects can

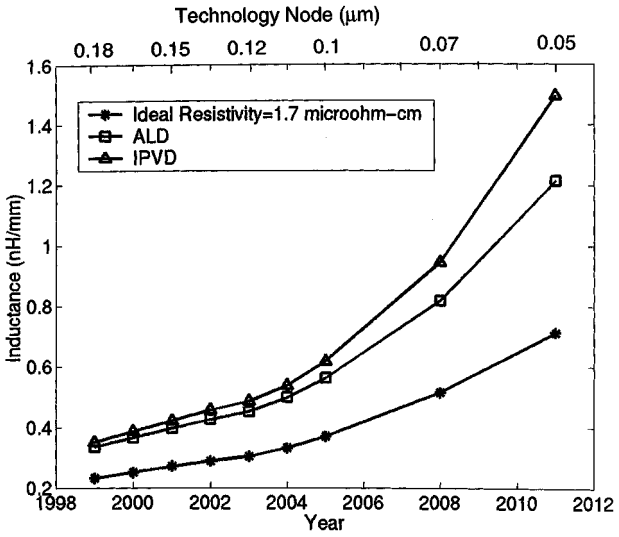

Fig. 8. Critical Inductance above which it becomes important to incorporate it for repeater optimization in global wires. For ALD and IPVD, $P = 0.5$, temp. $= 100\ ^{\circ}$C, barrier thick. $= 10$ nm.

be more pronounced in wider wires, such as those used for clock distribution, because of their lower resistance.

Inductance can also be significant in calculating delay for repeated wire, if the optimal distance between the repeaters is shorter than the critical length given by (8). The critical inductance above which the inductance would impact repeater optimization can be approximately evaluated by equating the l_{opt} from (6) with the l_{crit} for inductance from (8). Thus we have,

$$L_{crit} = 0.09 R_w t_{FO4}. \tag{9}$$

Note, this result is independent of capacitance. L_{crit} is plotted versus technology node in Fig. 8. The figure shows that, in the future, larger inductance value will be required for its impact to become important since the resistance is increasing rapidly with scaling. Fig. 8 also demonstrates the importance of realistic resistance modeling to determine critical inductance parameter. For example at 50 nm technology node with ALD technology, for significant inductance impact on repeater optimization, inductance greater than 1.2 nH/mm will be required. This value is erroneously predicted to be about 0.7 nH/mm with an ideal copper resistivity.

C. Impact of Delay on Performance

A multiclock cycle communication, by itself, allows a very narrow band of clock frequencies, using conventional global synchronous timing [14]. A simple solution to get around this problem is to interpose flip-flops along global wires, thus pipeline the wire. Here, the signal latency in terms of clock cycle would directly dictate the depth of pipelining, hence the power dissipation in the system. Since power is quickly becoming performance bottleneck, this latency can, thus, indirectly also become critical for performance. An accurate realistic resistively modeling helps give a better estimate of this power by characterizing latency more precisely. Fig. 5 depicts that the global wire latency is worse than obtained using ideal resistivity. One of the possible radical alternatives for global synchronous timing with deeper wire pipelining is to revert to different on-chip timing schemes such as source synchronous or pipeline timing which tend to be popular for chip to chip communication. In this timing implementation, the clock period is limited by the uncertainty (skew and jitter) in delay as opposed to the actual delay [14]. Here too, a realistic resistance modeling will play a critical role in evaluating the prowess of this technique. For example, unless the signal lines are very well shielded, a large source of jitter will arise from variability in interconnect delay due to switching state dependent intermetal capacitance. A simultaneous switching transition opposite to the signal line on the adjacent lines can cause the intermetal capacitance to increase, thus maximizing the line delay; whereas, a simultaneous transition in the same direction eliminates the intermetal capacitance completely and decreases the delay. Thus, the worst case difference in delay even on repeated wires will be proportional to product of square root of wire resistance and difference of square root of total wire capacitance in the two extreme switching scenarios. Thus, accurate wire resistance directly effects the clock frequency in this timing scheme.

Another very important factor affecting performance related to interconnects is the within-die variability of interconnect parameters especially that of wire resistance [15]. Among other sources, resistivity itself is becoming a dominant source of delay variability [15]. An effective resistivity dependent on previous technological factors will further contribute to resistivity variation and affect interconnect performance.

III. Signal Transmission Reliability

Reliable data transmission through a medium is a very significant consideration in digital systems. The data reliability constrains the maximum tolerable noise and defines the noise margin for a data link. The noise sources for on-chip lossy RC wires can be broadly categorized into those caused by power supply variation, crosstalk (intralevel, signal return), intersymbol-interference (ISI), and transmitter/receiver offsets [14]. In addition, there are those sources which are statistically modeled such as cross talk between perpendicular wires at adjacent level (interlevel), shot noise, thermal noise, and $1/f$ flicker noise [14]. Among these sources, intralevel interconnect crosstalk and the resistance governed attenuation of the signals are significant. A considerable effort has been invested in modeling the intralevel crosstalk [16], [17]. In the interest of brevity, it suffices to mention here that the on-chip wire crosstalk could be significantly affected by wire resistance, depending on the relationship of the driver rise time and the interconnect step response [13]. In such a case, realistic resistance values, being as large as almost twice that obtained using ideal copper resistivity at the 35 nm technology node [2], would make the cross talk problem much worse than previously assumed, thus making it harder to meet the noise budget.

IV. Power Penalty Due to Repeaters

In this section, we briefly examine the power penalty as a result of repeater insertion as well as the effect of practical Cu

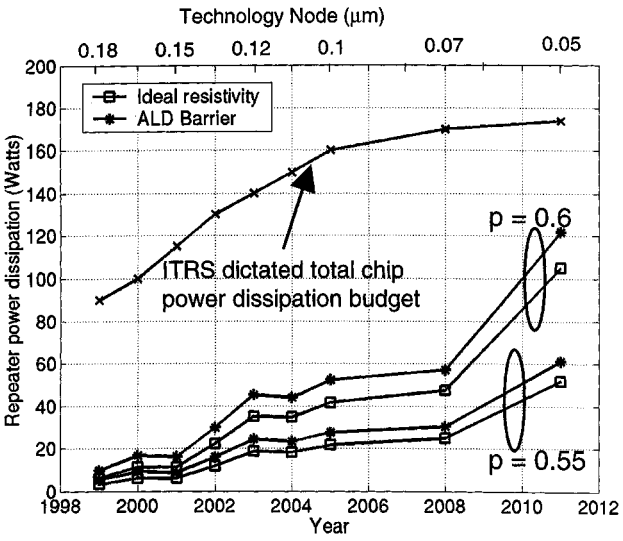

Fig. 9. Power dissipation due to repeaters for different Rent's exponent and using both ideal as well as practical Cu resistivity. For ALD, $P = 0.5$, temperature $= 100\ ^{\circ}$C, barrier thick. $= 10$ nm.

resistivity on it. While it is widely understood that repeaters help alleviate numerous problems in long distance communication on a chip, the penalties due to the repeaters must be examined carefully. A more comprehensive treatment of the penalties due to repeaters has been undertaken in [18]. A new methodology was used for estimating the number of repeaters. In this methodology, the memory and random logic area are considered separately due to a difference in the nature of the wiring in these areas. The number of repeaters in the random logic area is calculated by, first, obtaining the wire length distribution using Rent's rule [19]. Knowing the number of wires at all lengths and assuming that repeaters are stacked on wires if the delay of a repeated wire is less than that of a nonrepeatered wire, we can calculate the total number of repeaters. Only repeaters at global tier are considered in this calculation.

Fig. 9 shows the power dissipation due to repeaters for different technology nodes obtained using the new methodology [18]. The figure shows a nonsmooth variation over future technology nodes. This is because there are competing factors that dictate power consumption, and the trends for some of these factors, as given in ITRS, are not smoothly varying. While the total number of repeaters and clock frequency increase with the technology node, S_{opt}, capacitance and the supply voltage decrease. From the figure, it is evident that the added power dissipation due to repeaters is a serious problem in the future. At 50 nm technology node (year 2011), with a reasonable Rent's exponent of 0.55 [20] and using ideal copper resistivity, the repeater power dissipation is about 50 W, where as with realistic resistivity using ALD barrier this number is about 20% higher (60 W). The repeater power numbers are much worse with a Rent's exponent of 0.6. The resistance of wires effects repeater power by dictating the length after which repeaters are inserted; hence, influences the number of repeaters. Thus, the power penalty is nonnegligibly worse when realistic resistance trends are used for these calculations.

V. Summary

This work examines various performance metrics of on-chip copper interconnects using realistic future resistance trends. These resistance trends are especially important in the case of metrics, which depend strongly on the wire resistance such as latency. The modeling of the resistance trends using technological and reliability constraints is described in the first part of this paper. The metrics analyzed in this paper fall under the broad categories of speed, signal transmission reliability, and power consumption. The speed category includes a discussion on interconnect latency with and without repeaters. In this section, the importance of considering inductance as well as the impact of latency on performance is also briefly discussed. The role of accurate interconnect resistance model for these calculations is also depicted by comparing the results with those obtained using an erroneous ideal, bulk resistivity of copper. Signal transmission reliability is considered by qualitatively discussing the impact of realistic resistance on it. Finally, power issues are addressed only in the context of penalty arising from repeaters. It is found that there is about a 20% underestimation of repeater power dissipation if an ideal bulk copper resistivity is used.

Acknowledgment

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