Technology of GaN-Based Large Area CAVETs With Co-Integrated HEMTs

Philipp Döring, Rachid Driad, Richard Reiner, Patrick Waltereit, Stefano Leone, Michael Mikulla, and Oliver Ambacher

***Abstract*— In this work, multi-finger current aperture vertical electron transistors (CAVETs) are fabricated with co-integrated high electron mobility transistors (HEMTs). The devices are realized by Mg-ion implantation and metalorganic chemical vapor deposition (MOCVD) regrowth. The intrinsic CAVET design is optimized for robust device performance and applied on multi-finger devices having a total gate periphery of $W_G = 13.5$ mm and $W_G = 77$ mm. Mappings of the transfer characteristics revealed reliable turn-off behavior demonstrating the suitability of the intrinsic device layout. The largest CAVETs revealed a total ON-state resistance of $R_{ON} = 1.67\ \Omega$ and a maximum drain current of $I_{D,MAX} = 20.3$ A at $V_{GS} = 3$ V. A pulse robustness of $P_{PULS} = 976$ W at $V_{DS} = 50$ V and a pulsewidth of 500 μs is shown without thermal destruction. Additionally, HEMTs are co-integrated on-chip. This combination of HEMTs and reliable large area CAVETs enables the design of high-performance, monolithically integrated GaN power circuits (GaN power ICs) based on the CAVET technology.**

***Index Terms*— Current aperture vertical electron transistor (CAVET), GaN, power electronics, vertical transistor.**

I. Introduction

GaN-BASED devices offer great potential for high power switching applications due to their superior physical properties, compared to Si and SiC [1], [2]. The most investigated AlGaN/GaN high electron mobility transistor (HEMT) has already entered the high-power and high-frequency electronics market [3], [4]. However, for high power applications, the lateral technology suffers from high gate-to-drain spacing to sustain high voltage operation. In contrast, vertical devices offer better area efficiency in the high voltage region, as the drift region can be scaled independently of the chip area. In contrast to other reported vertical GaN transistor designs [5]–[9], the current aperture vertical electron transistor (CAVET) combines the advantage of the vertical depletion- and drift-region with the proven gate–source module of the lateral HEMT. This combination opens the possibility for monolithic integration of gate drivers as well as protection and sensor systems [10] of the low-voltage HEMT-technology and simultaneously avoids the requirement of an intricate field-plate design since the high electric field is moved into the bulk material. In addition, the current blocking layer (CBL), which serves as a potential barrier between the source and drain in CAVET technology, can be used to shield the low-voltage logic of the HEMT-technology from the high drain/substrate potential of the vertical transistor, when connected to the source contact. Even though CAVETs were demonstrated by various fabrication strategies, the intrinsic device design, the challenges in the fabrication process, and their impact on the performance of the fabricated devices are rarely explored [11]–[20]. The use of Mg-implantation to form the CBL seems to be an advantageous process to allow for the direct implementation of the HEMT surface process technology. In contrast to CAVETs demonstrated by Shibata *et al.* [11] or Nie *et al.* [12], trench etching in the active area can be avoided and a planar regrowth can be used to finalize the CAVET structure, as the Mg-implantation process leaves the surface morphology unaffected. Promising results of CAVETs were presented [17] with Mg-implanted CBL's fabricated by molecular beam epitaxy (MBE) regrowth to prevent Mg-diffusion from the CBL, which compensates the 2-D electron gas (2DEG) at the AlGaN/GaN interface [14]. However, these demonstrated devices were limited to the mA-range and large periphery devices could not be demonstrated. We have recently presented the first results on large area CAVETs completely grown by metalorganic chemical vapor deposition (MOCVD) [21], which circumvents the need for an industrially unsuitable and expensive MBE regrowth step [17]. In this work, recent progress on the technology of large area CAVETs is presented with lateral HEMTs co-integrated on-chip fabricated by Mg-implantation and MOCVD regrowth under standard growth conditions. An analysis of the intrinsic CAVET design and its impact on the ON-state and transfer characteristics of the fabricated devices is given. An optimized

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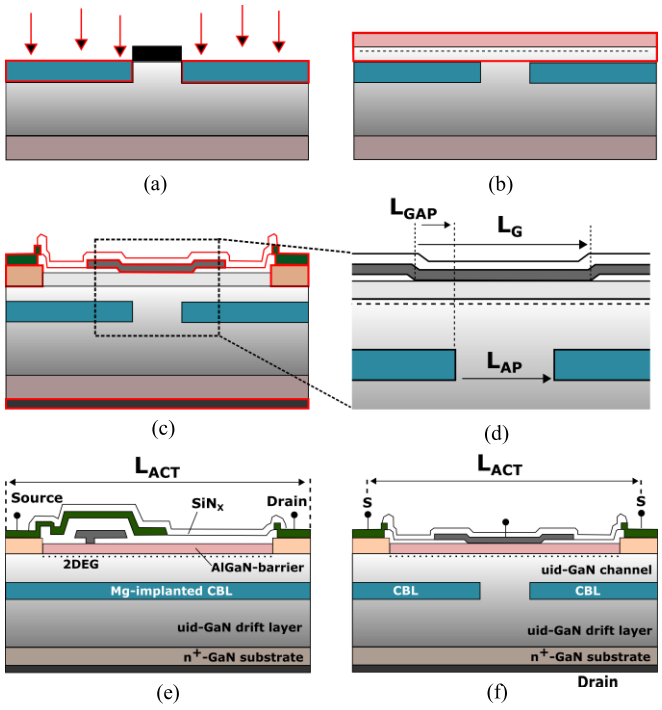

Fig. 1. Schematic overview of the CAVET fabrication process and the final device layout. (a) CBL-formation by Mg-ion implantation. (b) MOCVD AlGaN/GaN regrowth. (c) Metallization and passivation. (d) Definition of intrinsic design parameters. (e) On-chip HEMTs with CBL in vicinity to the AlGaN-barrier. (f) CAVET schematic.

device layout is derived and applied on large area multi-finger CAVETs with a chip size of 1×1 mm^2 and 2×2 mm^2, and their ON-state, transfer, OFF-state characteristics are analyzed as well as their pulse power stability. Vertical and lateral transistors are realized on-chip to compare the vertical device performance directly as a function of the total gate width and to demonstrate the possibility of a direct integration of the AlGaN/GaN-HEMT. The combination of CAVETs and on-chip integrated HEMTs enables the introduction of several new design opportunities in the AlGaN/GaN-technology for high-functional, monolithic integrated GaN power ICs.

II. Experimental Section

The fabrication of the devices started with the growth of a 2 μm n$^-$-GaN layer by MOCVD on 2-in bulk n$^+$-GaN substrates. The HVPE grown substrate has a resistivity of $\rho < 0.5$ Ω·cm and a dislocation density of DD $< 5 \times 10^6$ cm^{-2}. The CBL was formed by Mg-ion implantation [Fig. 1(a)] with an energy of 100 keV and a dose of 2×10^{14} cm^{-2}, which gives a peak Mg-concentration of 1×10^{19} cm^{-3}. This Mg-concentration allows for the regrowth of the following epitaxial layers under standard MOCVD growth conditions [22]. The aperture region was protected by a ~3-μm-thick photoresist during implantation. After the photoresist was removed, the CAVET was finalized by MOCVD regrowth of a 250 nm uid-GaN channel, a 24 nm $Al_{0.24}Ga_{0.76}N$ barrier, and a 4 nm GaN-cap layer [Fig. 1(b)]. The regrowth surface temperature of about 1050 °C also served as *in situ* annealing for the Mg-implanted CBL without the requirement of a capping layer. Atomic force microscopy (AFM) revealed a root mean square of rms = 0.19 nm (10×10 μm^2 scan). The device processing [Fig. 1(c)] is based on standard III–V technology [3]. Alignment markers were etched and protected by SiO_X prior to regrowth to orientate the surface processing with respect to the aperture region. A Ti/Al/Ni/Au metal stack is deposited and alloyed at around 825 °C in N_2 ambient to form the ohmic contacts. Afterward, the devices are passivated with a Si_XN_Y dielectric deposited by plasma-enhanced chemical vapor deposition (PECVD) and then isolated by Ar-implantation. Afterward, the passivation layers are opened by inductively coupled plasma etching (ICP-RIE) and Ni-Au-based Schottky gate contacts are deposited. The surface process is finalized by an additional Si_XN_Y passivation layer and a TiPtAu-based interconnection metallization. The drain contact in the vertical devices is realized on the backside of the GaN substrate by the previously mentioned alloyed ohmic and interconnection metallization.

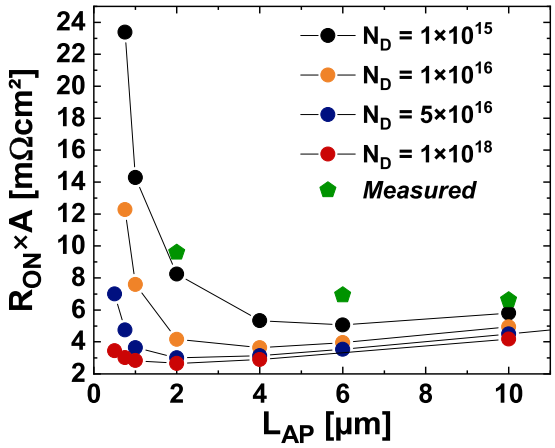

Fig. 2. TCAD simulations of the area-specific ON-state resistance $R_{ON} \times A$ versus the aperture length L_{AP} in dependence of the donor concentration in the aperture region. A free donor concentration of $N_D = 2 \times 10^{16}$ cm^{-3} is assumed in the drift region. Measured data of three single transistors ($W_G = 100$ μm) are given in green.

III. Results and Discussion

The initial testing of the fabricated CAVETs comprises the characterization of standard Hall- and transfer length method (TLM)-structures. Hall measurements on isolated areas reveal sheet carrier density of $n_S = 8.7 \times 10^{12}$ cm^{-2}, electron mobility of $\mu = 1320$ cm^2/V·s, and sheet resistance of $R_S = 538$ Ω/□ . Contact resistance mapping by TLM reveals an $R_C = 0.3 - 0.35$ Ω·mm over the complete wafer, which is slightly above literature values [20]. One of the critical design parameters of the CAVET is the aperture length L_{AP} [Fig. 1(d)] [15], [21], [22]. To avoid current choking, the aperture resistivity should be low, which can be achieved either by intentional n-type doping of the aperture region or by increasing the aperture length. In order to investigate the impact of the aperture resistivity on the total area-specific ON-state resistance $R_{ON} \times A$, TCAD simulations are carried out using a self-consistent Poisson-solver (Silvaco Atlas) (Fig. 2). It is visible, that for small L_{AP}, the $R_{ON} \times A$ is significantly increasing because of the dominating R_{AP}, particularly for low donor concentrations in the aperture. However, the impact

of R_{AP} successively vanishes with increasing L_{AP}, almost independent of the free donor concentration in the aperture. Furthermore, the lowest minimum $R_{ON} \times A$ is shifting to higher L_{AP} with decreasing N_D. Thus, even though low $R_{ON} \times A$ is achievable with small L_{AP}, higher aperture length (>4 μm) still seems beneficial when addressing high voltage stability due to the higher critical fields at low donor concentrations. However, for high aperture length (>10 μm), the lateral spreading of the transistor increases the total $R_{ON} \times A$ which makes very large apertures unsuitable. Small gate width transistors ($W_G = 100$ μm) are fabricated on-chip to measure $R_{ON} \times A$ empirically. The length of the active area L_{ACT} is defined between the centers of the two source contacts of each transistor (gate–source distance of $L_{GS} = 4$ μm and length of the ohmic contacts of $L_{OHM} = 5$ μm).

The measured data reveal higher resistances as expected from the TCAD simulations. It is assumed that the effective donor concentration in the aperture and drift layer is lower due to slight carrier compensation by carbon, which causes a slightly higher resistance. Carbon is a deep acceptor that may be introduced by auto-doping during the epitaxial growth, because of the carbon atoms present in the MOCVD precursors. Another potential contributor could be related to surface contamination during the aperture definition process. Nevertheless, the measured $R_{ON} \times A$ for CAVETs with an aperture length of $L_{AP} = 10$ μm is close to the expected values as the active device area becomes larger and the impact of the low carrier concentration is decreasing. A second critical parameter in the design of the CAVETs is the gate aperture overlap L_{GAP} [13], [17] shown in Fig. 1(d). The gate aperture overlap can be defined as the difference between the length of the gate L_G and the aperture length L_{AP}. L_{GAP} determines the gate control by suppressing source-drain leakage through the GaN-channel below the gate. The required overlap needs to be adjusted with respect to the channel thickness between the CBL and source contact in the fabricated device structure. To determine the required dimension of the gate-aperture overlap, small gate width CAVETs were fabricated with L_{GAP} ranging between 0 and 2 μm and a gate width of $W_G = 100$ μm. The corresponding transfer characteristics at $V_{DS} = 10$ V and varying $V_{GS} = -5$ to 1 V are shown in Fig. 3. The device with an aperture length of $L_{AP} = 10$ μm and $L_{GAP} = 2$ μm presented a threshold voltage of $V_{TH} = -2.82$ V. Similar V_{TH} is obtained for on-chip lateral HEMTs test structures. The device with an aperture length of $L_{AP} = 10$ μm and $L_{GAP} = 2$ μm presented a threshold voltage of $V_{TH} = -2.82$ V. Similar V_{TH} is obtained for on-chip lateral HEMTs test structures. Thus, the turn-off behavior is determined by the depletion of the 2DEG and unmodulated electrons in the GaN-channel seem to play a minor role in the OFF-state at $V_{DS} = 10$ V.

Besides, a sub-threshold slope of $S_{S\text{-}TH} = 87.6$ mV/decade and an I_{ON}/I_{OFF} ratio of 1.18×10^5 are derived from the transfer characteristics. A significant change is not observable for CAVETs with the same gate aperture overlap but different aperture lengths between 2 and 30 μm. Thus, the ratio of the gate aperture overlap and the aperture was found to be not relevant. However, when decreasing the gate-aperture overlap to 1 μm, a significant reduction of the gate control

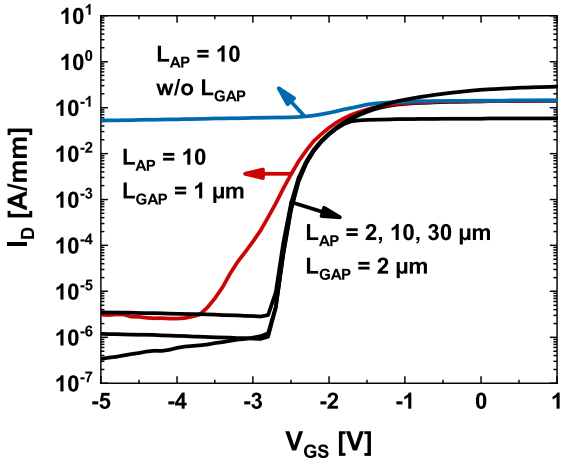

Fig. 3. Transfer characteristics at $V_{DS} = 10$ V of small gate width CAVETs ($W_G = 100$ μm) with a gate aperture overlap of $L_{GAP} = 2$ μm and varying aperture length (black). In addition, the gate aperture overlap of CAVETs with $L_{AP} = 10$ μm is reduced to $L_{GAP} = 1$ μm (red) and $L_{GAP} = 0$ μm (blue), showing increasing loss of the gate control.

is visible, as the sub-threshold swing increases drastically to $S_{S\text{-}TH} = 404.1$ mV/decade and the threshold voltage shifts to $V_{TH} = -3.79$ V.

Devices without any L_{GAP} did not reveal any turn-off behavior and the gate control is completely lost. To investigate the suitability of the intrinsic device layout on the large area cell topology, two different dimensioned comb structures are fabricated with a chip size of 1×1 mm^2 and 2×2 mm^2. The two different multi-finger transistors feature an aperture length of $L_{AP} = 10$ μm, a gate-finger length of $L_G = 14$ μm, and a gate-aperture overlap of $L_{GAP} = 2$ μm. The 1×1 mm^2-chip device has a total gate width of $W_{TOTAL} = 26 \times 0.53$ mm $= 13.78$ mm (number of fingers $\times$ finger width $= N \times W_G$) and an active finger area of $A_{ACT} = 0.53$ mm $\times$ 0.85 mm ($W_G \times L_{ACT}$). The 2×2 mm^2-chip device features a total gate periphery of $W_{TOTAL} = 58 \times 1.32$ mm $= 77$ mm and an active finger area of $A_{ACT} = 1.32$ mm $\times$ 1.85 mm. Both comb structures are realized on the same chip with the previously shown small transistors ($W_G = 100$ μm) to allow a direct comparison. Transfer characteristics of both large-area devices are mapped over the complete wafer (Fig. 4). A threshold voltage shift due to Mg-diffusion, observed for MOCVD-regrown CAVETs [14], is not observable, demonstrating the suitability of our MOCVD-based regrowth process even for much larger devices. In order to analyze the OFF-state behavior of the large area CAVETs, IV-characteristics at $V_{GS} = -5$ V are measured until device breakdown (Fig. 5). The small gate width transistors reveal OFF-state drain currents in the range of $I_{D,OFF} = 8 \times 10^{-6}$ A/cm^2 below $V_{DS} = 200$ V. Breakdown is measured in the range of $V_{BR} = 206 - 222$ V (at room temperature) independent of the aperture length and also for the transistor without an aperture. Thus, it is assumed that breakdown is caused by electrons punch through the CBL.

Further improvement is expected by connecting the CBL with the source contact. In this case, the formation of a body diode improves reverse leakage behavior and self-biasing can be avoided by keeping the CBL at the source potential. The breakdown voltage of the 1×1 mm^2 device is found within

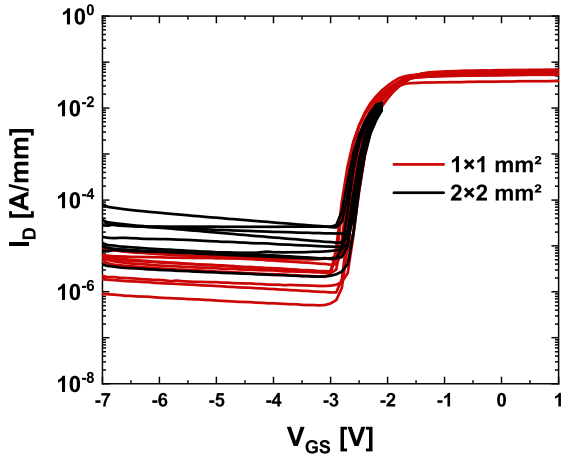

Fig. 4. Mapping of the transfer characteristics at $V_{DS} = 10$ V of large area CAVETs. The devices feature an aperture length of $L_{AP} = 2$ μm, a gate aperture overlap of $L_{GAP} = 2$ μm. Transfer curves are shown for 1×1 mm^2-chip devices (red) and 2×2 mm^2-chip devices (black) having a total gate width of $W_{TOTAL} = 13.5$ mm and $W_{TOTAL} = 77$ mm, respectively. The current compliance was set to 1 A.

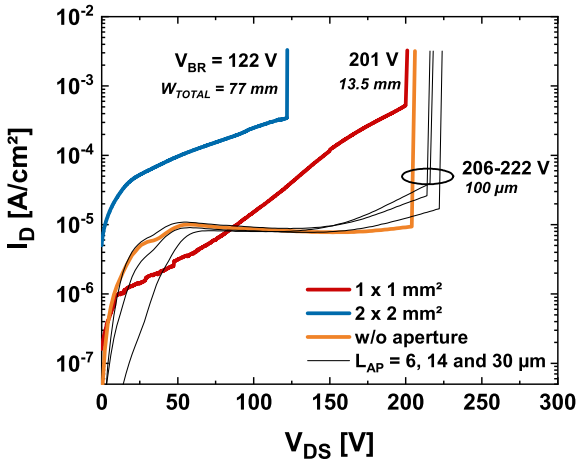

Fig. 5. OFF-state characteristics at $V_{GS} = -5$ V of the large area devices with a chip size of 1×1 mm^2 (red), 2×2 mm^2 (blue). Small gate width CAVETs on the same chip with different aperture lengths are given in black. In addition, a CAVET without an aperture was measured (orange) to force the current through the CBL.

the same range at $V_{BR} = 201$ V. However, the drain leakage current is significantly increased, especially in the range of $V_{DS} > 100$ V. It is assumed that the higher leakage currents are the cause of a lower yield in the upscaled device but further data are needed to verify this assumption. A further increase in the drain leakage current of about two orders of magnitude is observable in the 2×2 mm^2 device, and the breakdown voltage is reduced to $V_{BR} = 122$ V, which is in agreement with the assumption of the loss in yield by further upscaling of the device area. Another reason for the higher leakage and reduced breakdown voltage could also result from dislocations/defects originating from the GaN-substrate.

The measured breakdown voltage of the 2×2 mm^2 device corresponds to a critical field strength of $E_{CRIT} = 1.4$ MV/cm assuming depletion over the complete drift layer distance (according to [2]). It is also worth noting that the calculated field strength is still close to published values

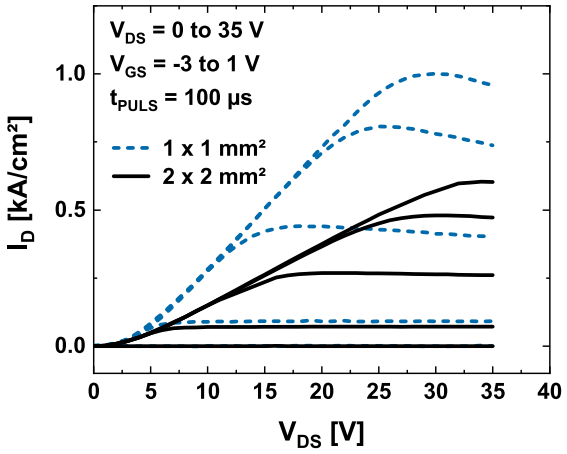

Fig. 6. Pulsed output characteristics of the multi-finger CAVETs with a chip size of 1×1 (blue) and 2×2 mm^2 (black). A pulsewidth of 100 μs and a sample time after 50 μs are used, with a duty cycle below 1%.

of small gate width CAVETs in [17] (1.72 MV/cm, $W_G = 75$ μm). The critical field strength of the 1×1 mm^2 ($E_{CRIT} = 2.3$ MV/cm) is even exceeding these values, which demonstrates the suitability of the present *in situ* annealing/regrowth process for large multi-finger CAVETs as reported in this work. However, a higher breakdown voltage can be expected by increasing the drift layer thickness, as demonstrated in other vertical GaN-designs [5]–[9], [11], [12], in view to increase the area-efficiency with respect to lateral GaN-based power transistors.

To demonstrate the behavior of the devices in terms of current handling capability and pulse power stability, pulsed output characteristics of the fabricated multi-finger CAVETs are measured (Fig. 6). A pulsewidth of 100 μs and a sample time of 50 μs is used with a duty cycle far below 1%. The CAVET with a chip size of 1×1 mm^2 revealed a maximum absolute drain current of $I_{D,MAX} = 4.97$ A (normalized to the active area $I_{D,MAX} = 1.08$ kA/cm^2) and a total differential ON-state resistance of $R_{ON} = 3.56$ Ω ($R_{ON} \times A = 16.2$ mΩ/cm^2) at $V_{GS} = 1$ V. The knee-voltage is found at $V_K = 25$ V, which corresponds with a pulse power of $P_{PULS} = 121$ W or a pulse power density of 26.86 kW/cm^2. The larger multi-finger CAVET with a chip-size of 2×2 mm^2 revealed a maximum absolute drain current of $I_{D,MAX} = 14.76$ A and a total differential ON-state resistance of $R_{ON} = 1.81$ Ω ($R_{ON} \times A = 40.9$ mΩ/cm^2) at $V_{GS} = 1$ V. The maximum drain current normalized to the active device area is reduced to $I_{D,MAX} = 0.61$ kA/cm^2, when compared to the smaller multi-finger CAVET. The knee voltage is found at $V_K = 34$ V, corresponding to a total pulse power of $P_{PULS} = 501.8$ W (20.4 kW/cm^2). As Hall- and TLM-measurements revealed typical values, the high ON-state resistance and the high knee voltage V_K in the fabricated devices are assumed to be the result of reduced effective carrier concentration in the nominally undoped aperture and drift region as mentioned previously. Additional testing of the aperture and drift region further indicated this assumption (not shown here).

To compare the pulse power stability with published data for lateral Schottky-gate HEMTs, a specific destruction energy

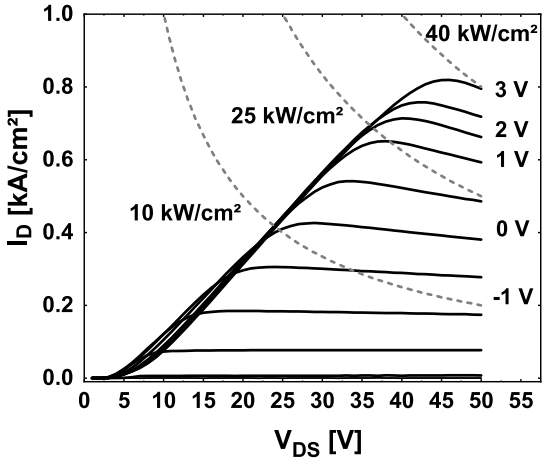

Fig. 7. Pulsed output characteristics of the multi-finger CAVETs with a chip size 2 × 2 mm^2. V_{DS} is measured up to 50 V and V_{GS} is varied from −5 to 3 V. A pulsewidth of 500 μs and a sample time after 50 μs are used. A pulse power of P_{PULS} = 968 W was measured at V_{DS} = 50 V which is close to the predicted device failure of P_{FAIL} = 976 W (using E_{FAIL} = 200 mJ/mm^2).

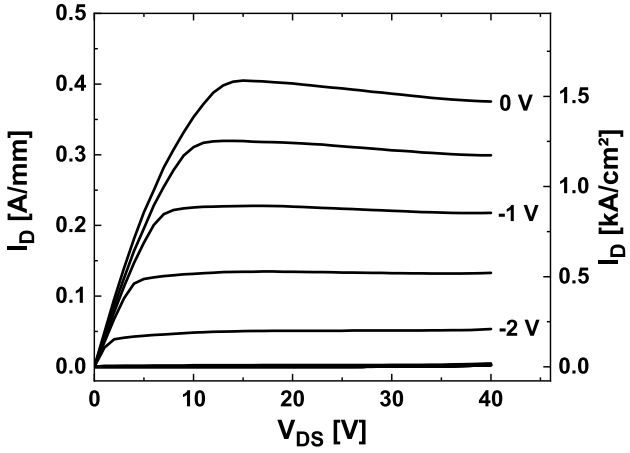

Fig. 8. Output characteristic of the lateral on-chip HEMT with varying gate–source voltage of V_{GS} = −6 to 0 V for V_{DS} = 0 to 40 V. The device features a gate width of W_G = 50 μm, a length of the active area of L_{ACT} = 25.5 μm and a GaN-channel thickness of t_{CHA} = 250 nm between the Mg-implanted CBL and the AlGaN barrier.

of E_{FAIL} = 200 mJ/mm^2 at V_{DS} = 50 V is assumed, which was experimentally derived by Mocanu *et al.* [24]. Using a pulse power P_{PULS} = 500 W and an active area of A_{ACT} = 2.16 mm^2, a destruction power of P_{FAIL} = 976 W is calculated. Pulsed output characteristics of the 2 × 2 mm^2-chip CAVET are measured for V_{DS} = 0 to 50 V and V_{GS} = −5 to 3 V (Fig. 7). The multi-finger CAVET exhibited an absolute drain current of 20.3 A at V_{GS} = 3 V and a total differential ON-state resistance of R_{ON} = 1.67 Ω. A pulse power of P_{PULS} = 968 W was measured at V_{DS} = 50 V, close to the predicted destruction power of a lateral HEMT. Self-heating is visible but device failure in terms of sudden drain current increase or physical breakdown was not observed [24].

Finally, lateral transistors are processed on-chip, without an aperture below the gate. The fabricated HEMTs have a gate width of W_G = 50 μm and an active area length of L_{ACT} = 25.5 μm based on our 600 V HEMT-technology [23] but features the Mg-implanted CBL in the vicinity to the 2DEG [Fig. 1(e)]. Transfer characteristics (not shown here) at V_{DS} = 10 V and V_{GS} = −6 to 0 V revealed a sub-threshold swing of $S_{S\text{-}TH}$ = 93.4 mV/decade and a threshold voltage of V_{TH} = −2.81 V. The measured gate leakage current was lower than 1 × 10^{-4} A/mm^2. Output characteristics are measured for V_{DS} = 0 to 40 V in 0.1 V steps (Fig. 8).

The lateral FET reveals a maximum drain current of $I_{D,MAX}$ = 0.4 A/mm or $I_{D,MAX}$ = 1.59 kA/cm^2 at V_{GS} = 0 V and an area-specific ON-state resistance of $R_{ON} \times A$ = 2.98 mΩ·cm^2. The resulting output characteristics of the lateral FETs demonstrate the suitability of the used fabrication process. However, in comparison to the vertical FETs, a significantly improved current density and ON-state conductivity can be observed. This is an additional indication that the aperture and drift region conductivity is reduced. The measurements of IV-characteristics of the on-chip integrated lateral transistors reveal the potential of future monolithic integration of the conventional HEMT-technology. On one hand, the CBL serves as a potential barrier to suppress source-drain leakage in the vertical transistors. On the other hand, this potential barrier is expected to protect the low-voltage HEMT-logic from the high drain potential. However, connecting the CBL to the source contact of the CAVET will be beneficial to avoid any impact of the drain potential on the static and dynamic behavior of the lateral HEMTs.

IV. Conclusion

In this article, recent progress in the CAVET technology is presented using low-dose Mg-implantation and MOCVD regrowth. The intrinsic CAVET design was optimized with respect to device performance and gate control. Larger aperture lengths were chosen to avoid current choking for low donor concentration. The fabricated multi-finger CAVETs presented in this work exhibit high absolute current capability and high pulse power stability. Lateral HEMTs were co-integrated on-chip, with the 2DEG in the vicinity of the Mg-implanted CBL. This combination of a large area CAVET and an on-chip integrated HEMT demonstrates a pathway to allow monolithically integrated GaN power converters with power switches based on the CAVET technology. Future works will focus on the optimization of the aperture and drift region conductivity, as well as the increase in breakdown voltage to enable higher area efficiency in the vertical design with respect to its lateral counterpart.

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