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Abstract. The semiconductor and hard disk drive industries are investigating nanoimprint for future high volume manufacturing of memory devices and patterned media. Nanoimprint, a form of 1× contact lithography, is one of the few technologies capable of meeting the resolution requirements for next generation electronic and storage devices. Its ability to produce small features with low line width roughness and critical dimension uniformity has been demonstrated by multiple sources. Significant improvements in defectivity have been shown; overlay has improved to within a factor of 2 of that required by the International Technology Roadmap for Semiconductors for 22 nm node flash memory devices; and next generation tools, templates, and processes are being commercialized and tested at end-user sites. Defectivity, throughput, and infrastructure remain as critical challenges, but each has experienced marked improvements in the past year. This technology review and assessment covers critical aspects of nanoimprint for both semiconductor and patterned media manufacturing. It focuses on jet and flash imprint lithography, the type of nanoimprint most often considered for these two applications. The requirements and current status of nanoimprint with respect to high volume manufacturing are presented, and critical aspects are discussed. [DOI: 10.1117/1.3642641]

Subject terms: nanoimprint; jet and flash imprint lithography; step and flash imprint lithography; jet and flash; step and flash; patterned media.

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1 Introduction

Nanoimprint lithography has been advertised as a simple, low cost, high resolution process. It is a type of 1× lithography in which a mold is pressed into a material to form a pattern. Nanoimprint is suitable for university lab research, device prototyping, manufacturing, and many other applications. Of particular interest is its use in semiconductor device and patterned media high volume manufacturing (HVM). The hard disk drive (HDD) industry is considering nanoimprint to reach data densities of one terabit per square inch ($1Tb/in^2$) and above with patterned media. The semiconductor industry is assessing it for device prototyping, unit process development, and device manufacturing at future nodes.

Early demonstrations of nanometer scale patterning, including 10 nm contact hole imprinting in 1997 (Ref. 1) and demonstrations of sub-3 nm resolution in 2004,[2] established nanoimprint as a promising next generation lithography candidate. Current nanoimprint processes are often adaptations of either thermal[3] or ultraviolet nanoimprint (UV-NIL).[4] Jet and flash imprint lithography (J-FIL), a form of UV-NIL, has been demonstrated to be the most suitable type of nanoimprint for semiconductor and patterned media applications. J-FIL uses a room temperature, low pressure, and ultraviolet (UV) resist curing process, which, for semiconductor device and patterned media disk manufacturing, is preferable to the high temperature and high pressure processes typically associated with thermal nanoimprint. In J-FIL, a low viscosity UV-curable liquid resist is dispensed field by field using an ink jet process. A transparent template is then pressed into the resist such that the resist fills the pattern in the template. After filling, a UV light source is used to cure the resist, then the template and imprinted substrate (wafer/disk) are separated. No post-bake or develop is required as would be used in projection lithography. The tools that perform this process operate at atmospheric pressure and room temperature, contain no intricate lens systems, and use low-cost broadband mercury arc lamps for the UV source. J-FIL, also called step and flash imprint lithography (S-FIL), was developed at the University of Texas at Austin and commercialized by Molecular Imprints Inc. Fundamental descriptions of this process and its potential capabilities can be found in many early publications.[4–9] Unless otherwise specified, the data and results included in this paper refer to J-FIL nanoimprint.

To reach high yields, the semiconductor and HDD industries each place stringent requirements on their processes. Both require small, consistently printed features with good imaging control over large areas. Semiconductor devices also must meet tight defectivity, overlay, and other metrics. Patterned media have fewer technical restrictions, but require the finest resolution and face the most extreme cost of ownership (COO) challenge. Patterning capabilities such as resolution, critical dimension uniformity (CDU), and line width roughness (LWR) have been thoroughly documented. Consistent results have been demonstrated by multiple sources, indicating a robust and maturing process. Overlay has improved to

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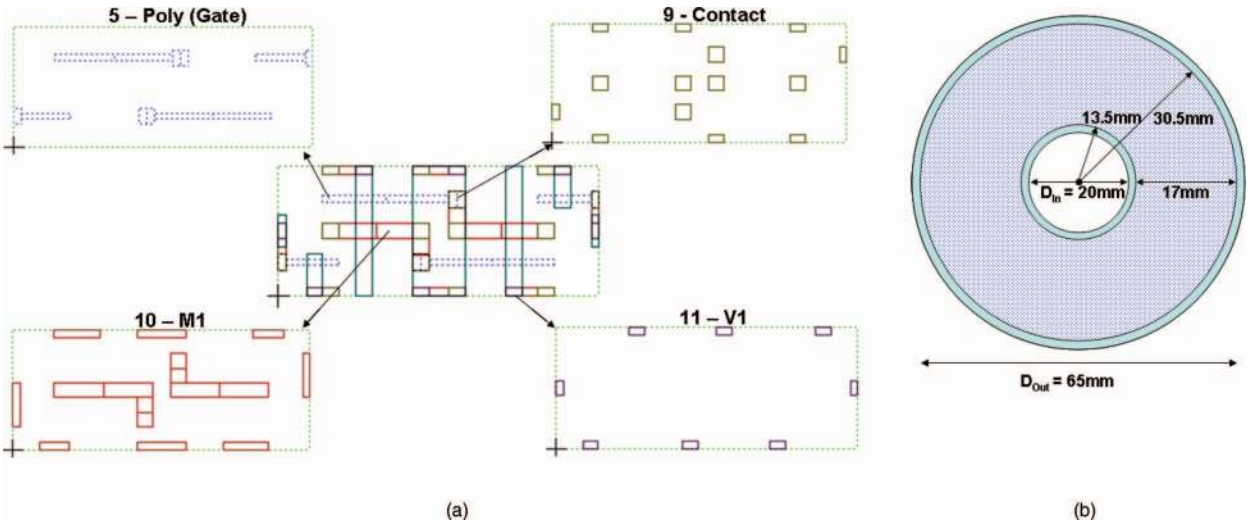

Fig. 1 Example of various semiconductor layers from an SRAM test device courtesy of International SEMATECH Manufacturing Initiative (ISMI) (left) and the single layer that makes up a 65 mm patterned media disk (right). A majority of the disk surface is filled with simple repeating patterns such as dots or lines and spaces.

within a factor of 1.4× for 22 nm flash memory devices.[10] Defectivity and throughput remain the most critical technical issues; however, recent data suggest that low defect nanoimprint processes may be possible,[11] and higher throughputs may be achieved with multiple-module cluster tools and better control of resist spread.[10,12] As with any next generation technology, multiple issues must be resolved before it can be considered for HVM.

In recent years, HDD manufacturers have shown far more interest in nanoimprint than have semiconductor manufacturers; in both industries, interest has been cyclical. Patterned media, for which many tools have been sold and installed,[13] appeared ready to begin production in 2010 to 2011. Hitachi Global Storage Technologies,[14] Seagate,[15] Western Digital,[16] and other leading HDD manufacturers, as well as equipment and template suppliers, demonstrated rapid progress in this area. However, patterned media have now been pushed out by a few years as the HDD industry focuses on an alternative technology called Heat Assisted Magnetic Recording (HAMR).[17,18] Conversely, nanoimprint achieved several significant milestones in the semiconductor industry during this time. For example, the next generation Imprio500 J-FIL tool was commercialized with the first one shipped to a customer in late 2010.[19] It uses an industry standard 6025 (6 in. × 6 in. × 0.25 in.) based form factor template and is specified to operate with a throughput of 20 wafers/hour. Template replication is being commercialized with the first 6025 template replication tool, the MR 5000, installed at Dai Nippon Printing (DNP).[20] Both the Imprio500 and MR 5000 are products of Molecular Imprints Inc. A major lithography tool manufacturer, Canon, has developed a platform for an imprint module.[21] Two memory manufacturers, Toshiba and Samsung, have demonstrated progress toward the use of nanoimprint for semiconductor manufacturing, including Toshiba's publication of preliminary electrical and device test results.[12,22,23] Proof of concept for a low defect J-FIL process has been demonstrated by SEMATECH,[11] and Molecular Imprints is addressing the key issues, such as throughout, defectivity, and infrastructure.[10]

2 Semiconductor and Patterned Media Roadmaps, Requirements, and Status

Semiconductor devices and patterned media disks are vastly different in terms of overall processes and requirements. Semiconductor devices are made up of many layers, each with different geometry and specifications and each requiring precise alignment to the previous layers. Lithography has always been an integral part, if not the primary enabler, behind this industry. Patterned media is a relatively new concept consisting of a single layer of dense, mostly repeating, structures such as dots or lines and spaces. The HDD industry does not use lithography in its traditional disk manufacturing processes as the disks, formally called platters, are made with an unpatterned continuous magnetic media. Figure 1 is a simplified illustration of the two technologies.

Memory products, particularly flash, are the primary target for nanoimprint introduction in the semiconductor industry. Flash memory has aggressive lithography resolution requirements and relaxed overlay requirements,[24] making it an ideal choice for nanoimprint. Memory devices also contain built-in redundancy, making them less sensitive to defects than logic devices such as microprocessors. Patterned media is also defect-sensitive, but less so than semiconductor devices as bad areas of the disk are ignored.

The future of semiconductor device manufacturing is described in the International Technology Roadmap for Semiconductors (ITRS). The industry is targeting 22 nm node flash memory production in 2013. Figure 2 shows the ITRS potential solutions roadmap down to the 11 nm node. The ITRS lists nanoimprint as an option for device manufacturing starting at the 22 nm node, but at this time it is only being investigated by a small number of manufacturers. Instead, 193 nm immersion (193i) double patterning and extreme ultraviolet (EUV) lithography are the most likely candidates for production at future technology nodes. Nanoimprint continues to be investigated as an alternative due to its patterning capability and potentially low cost of ownership. Table 1 shows the status of J-FIL in comparison to the key metrics for 22 nm flash memory. The champion data shown in

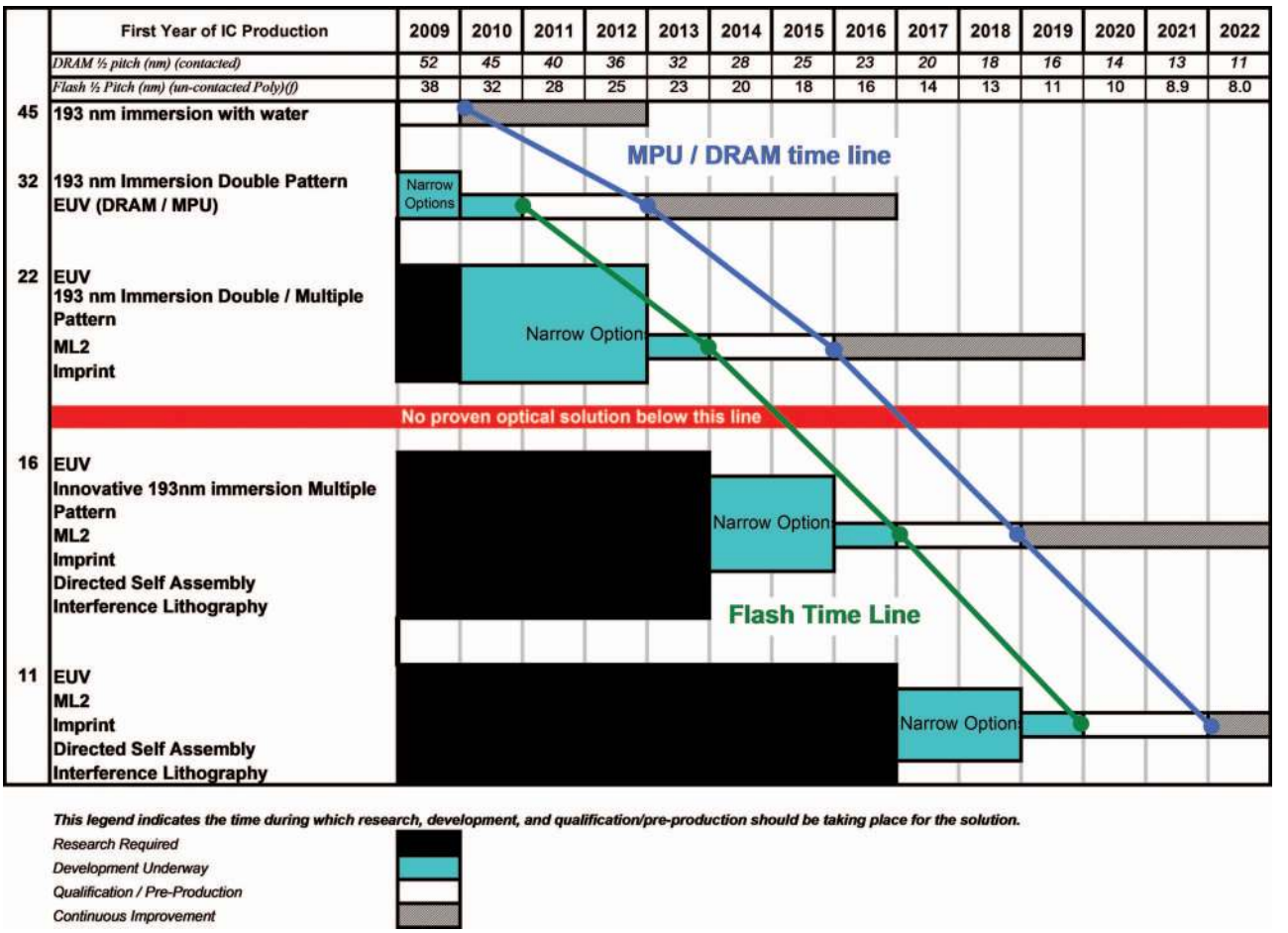

Fig. 2 2009 ITRS potential solutions roadmap. (Reprinted with permission from Ref. 25. Copyright 2009 by the International Technology Roadmap for Semiconductors.)

Table 1 J-FIL status, based on champion results, for 22 nm node flash memory. Requirements from 2010 ITRS (Ref. 24).

	Metric	Requirement	Status	Comments
Process	Resolution	23 nm HP	<22 nm HP (Refs. 26 and 27)	Capability $\ll$ 22 nm
	CDU	2.3 nm 3σ	1.2 nm 3σ (Ref. 26)	At 28 nm HP
	LWR	2.3 nm	2.5 nm (Ref. 27)	At 22 nm HP
	Overlay	7.4 nm	10.3 nm (Ref. 10)	6025 template, full-field
	Defectivity	0.01 def/cm^2	10 def/cm^2 (Refs. 26)	Target spec: 0.1 def/cm^2 (Ref. 26)
Template	Resolution	23 nm HP	22 nm HP (Ref. 28)	<22 nm demonstrated
	CDU	2.3 nm 3σ	<1.2 nm 3σ (Ref. 23)	At 28 nm HP
	LWR	2.3 nm	2.5 nm (Ref. 29)	On 28 nm HP features
	Image Placement	4.3 nm	2.8 nm (Ref. 29)	Residual image placement
	Defectivity	0 def/cm^2 >10% of CD	10 def/cm^2 (Refs. 26)	Without 65 mm post-processing

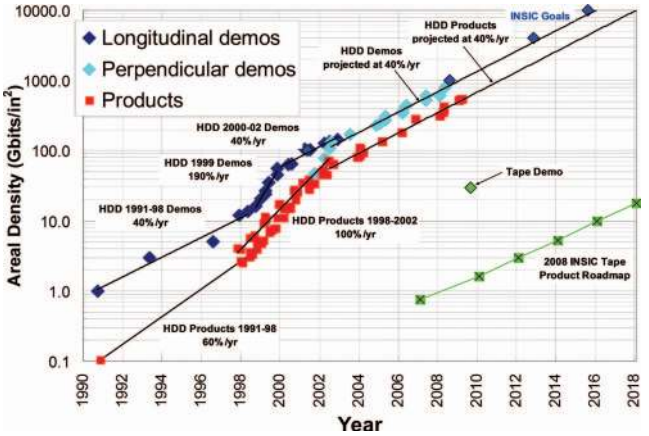

Fig. 3 HDD areal density roadmap. [Courtesy of the Information Storage Industry Consortium (Ref. 30).]

Table 1 was demonstrated by various organizations. Further effort is required to demonstrate that all of the critical requirements (resolution, overlay, defectivity, etc.) can be met simultaneously.

For patterned media, the main goal is to maximize areal density, the number of bits per unit area, and do so with as little cost as possible. It has been estimated that the total added cost for the entire patterned media process must not add more than $1/disk to the existing process. Areal density is a function of bit and track pitch. The smaller the pitch, the more features, or bits, that fit on each square inch of disk surface, therefore increasing data storage capacity. Figure 3 shows the HDD areal density roadmap (including all HDD products, not just patterned media). Table 2 lists the feature dimensions and projected year of insertion for patterned media areal densities of 0.7 to 10.3 Tb/in^2. It was expected that production would have begun in the 2010 to 2011 timeframe, but the industry has delayed the introduction of patterned media in favor of heat-assisted magnetic recording.

Two types of patterned media are being developed: bit-patterned media (BPM) and discrete track media (DTM). Each provides isolated magnetic areas to increase density and reduce noise. For BPM, each bit is completely isolated, while for DTM each bit is isolated in only one direction. In all cases, the disk is patterned on both sides. BPM is the long-term goal, with DTM acting as an interim solution between today's continuous magnetic media and BPM. Figure 4 is an illustration of each of the media types and Fig. 5 shows an example of the dimensional requirements for 1 Tb/in^2 using BPM and DTM.

The requirements and status of patterned media are less clear than those of the semiconductor industry, primarily because there is no industry-wide roadmap similar to the ITRS. Outside of the areal density roadmap, Fig. 3, insight into other requirements is limited. The addition of patterned media requirements to the lithography portion of the ITRS should be considered if nanoimprint is to be used for production.

3 Resolution, Uniformity, and Line Roughness

The ability of nanoimprint processes to resolve small features has been well documented; sub-3 nm imprint capability has been demonstrated;[2] and feature sizes for next generation semiconductor devices and patterned media disks are easily printed. Figure 6 shows examples of the resolution and pattern quality achieved by various nanoimprint processes. Nanoimprint also has the unique capability of printing three-dimensional (3D) structures,[31,32] such as those seen in Fig. 7. Its ultimate resolution limit is not yet known, but for practical purposes, it is limited only by the template. As nanoimprint is a 1× technology, e-beam write tools and processes are required to produce templates with features 4× smaller than conventional photomasks. Gaussian beam (GB) and vector shaped beam (VSB) writers have demonstrated line/space resolution down to 14 nm half-pitch (HP) and 22 nm half-pitch, respectively.[28] VSB tools will be used for semiconductor template fabrication due to the low throughput of GB writers.[33] However, patterned media master templates may be limited to GB tools due to their resolution requirements.

J-FIL consistently produces low CDU and LWR. A CDU of just 1.2 nm 3σ for 28 nm half-pitch features across a 300 mm wafer has been demonstrated (Fig. 8).[26] This result meets the ITRS CDU specification for all 22 nm node devices, surpasses the flash requirement of 2.3 nm by a factor of nearly 2×, and confirms the inherent stability of the imprint process. It also demonstrates that low CDU 1× templates are manufacturable. Additionally, process CDU (i.e., template contribution to CDU removed) for 28 nm half-pitch features has remained at or below 1 nm for 1 month when measuring across 300 mm wafers imprinted with a 26×32 mm field.[29]

Table 2 BPM and DTM approximate dimensions and projected years of insertion. Feature dimensions calculated based on areal density requirements. Years of insertion estimated based on publications and input from various HDD industry manufacturers and suppliers.

	BPM				DTM			
Year	Areal density (Tb/in2)[a]	Track pitch (nm)	Bit pitch (nm)	Bit length[b] (nm)	~ Bar	Track pitch (nm)	Bit pitch (nm)	Bit length[b] (nm)
2015	1.0	25	25	13	4	51	13	13
2016	1.9	18	18	9	2.8	31	11	11
2017	5.3	11	11	6	1.6	14	9	9
2018	10.3	8	8	4	1.3	9	7	7

[a]Assuming 40% increase in density per year.
[b]Bit length may not equal half-pitch as shown here.

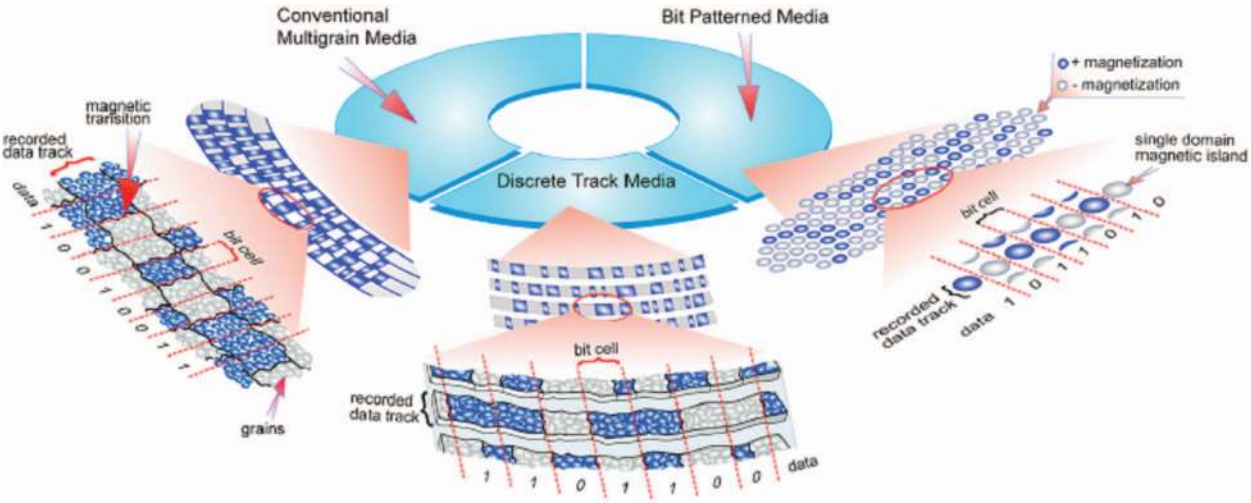

Fig. 4 Comparison of conventional patterned media, DTM, and BMP, courtesy of Hitachi Global Storage Technologies. (Reprinted with permission from Ref. 14).

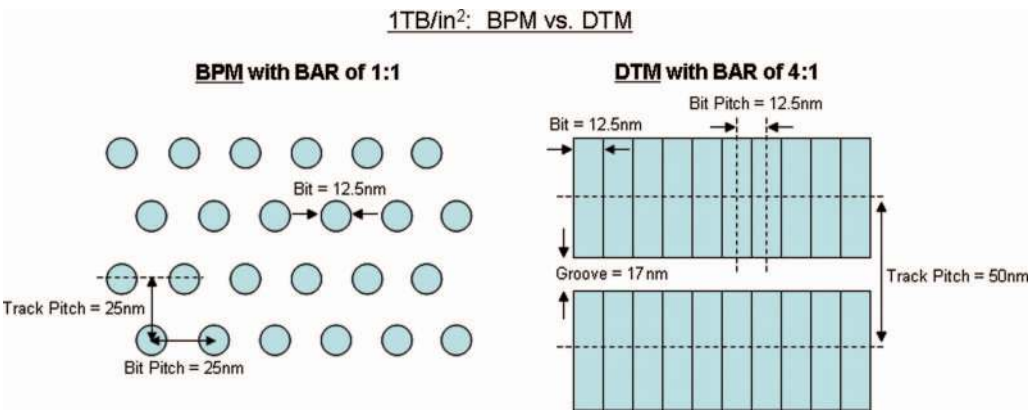

Fig. 5 1 TB/in^2 approximate dimensional requirements for BPM and DTM.

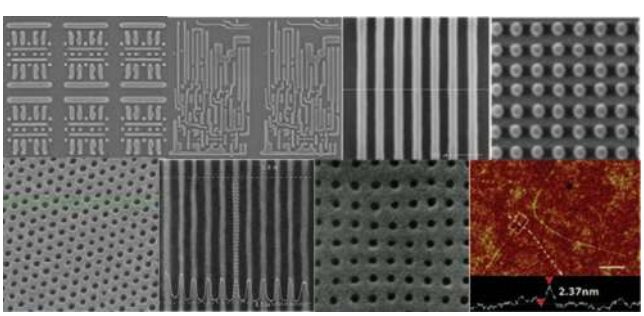

Fig. 6 Imprint resolution examples. First six images are from J-FIL processes. From top left: 32 nm metal 1 (Samsung, Ref. 34), 32 nm logic (Samsung, Ref. 34), 28 nm half-pitch (SEMATECH, Ref. 35), 28 nm posts (SEMATECH, Ref. 29), 25 nm contacts (Samsung, Ref. 34), 11 nm line (Samsung, Ref. 29), 10 nm contacts (Chou, Ref. 1), and 2 nm nanotube imprint (Rogers, Ref. 2).

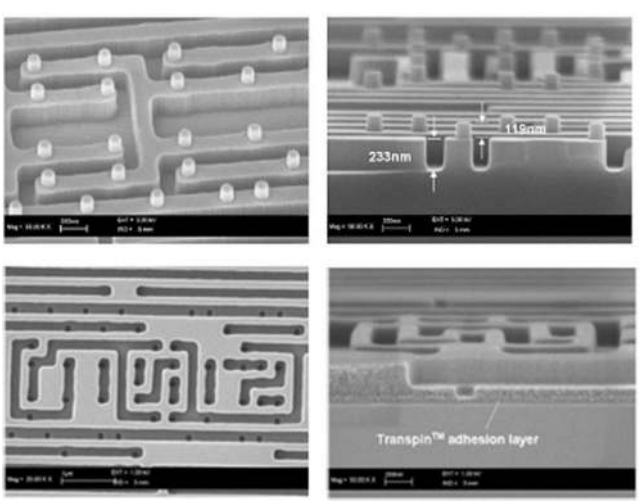

Fig. 7 3D dual damascene template (top) and imprinted (bottom) CMOS structures, courtesy of IMS Chips, ATDF, and University of Texas at Austin. (Reprinted with permission from Ref. 32. Copyright 2008 by SPIE.)

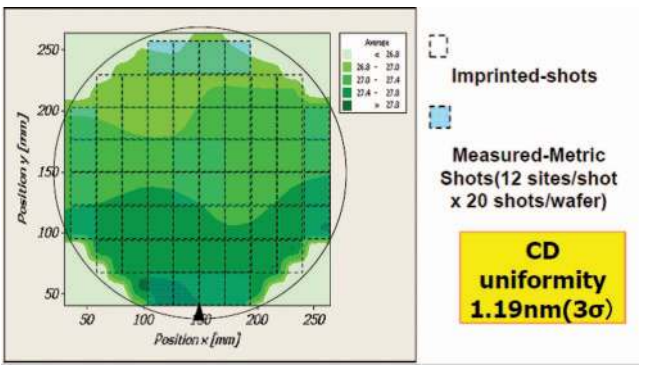

Fig. 8 28 nm half-pitch CDU across 300 mm, courtesy of Toshiba (Ref. 26).

32 nm critical dimension (CD) measurements collected over a set of five consecutive wafers showed an overall CDU of 3.4 nm, with the primary variation due to the template.[35] A breakdown of measurements by location, as listed in Table 3, shows that the CDU at any one location, measured across all five wafers, ranged from 0.9 to 1.6 nm 3σ, again demonstrating the consistency of the J-FIL process.

CDU is also a critical metric for patterned media as small changes in CD size will affect the performance of each bit. The maximum allowable CD variation is approximately 5% of the full pitch[36,37] across a disk. Each side of a 65 mm disk has nearly 3 times more surface area than a full-field semiconductor device, making it more difficult to control CDU across the entire surface. 5.5 nm CDU for 25 nm HP line/space patterns, representative of DTM, have been demonstrated at template level.[36]

Several sources have shown that LWR is consistently in the range of 2 to 3 nm, even on features below 30 nm.[12,35,38] It was also shown that LWR for 28 nm half-pitch features across a 300 mm wafer imprinted with a 26×32 mm field remained at approximately 2.5 nm for 1 month.[29] Another experiment in 2007 demonstrated how line edge roughness (LER) remained at approximately 2 nm for features ranging from 32 to 24 nm,[39] and LER of 2 nm has recently been published.[26]

In summary, J-FIL has demonstrated its ability to meet the resolution requirements of next generation semiconductor devices and patterned media disks (BPM and DTM). Template resolution suitable for 22 nm node devices has been shown. BPM and DTM template resolution capability is improving but requires further development. Both the process and template meet CDU requirements for 22 nm flash and LWR needs to improve only slightly to meet the ITRS specification. Further improvements are required to reduce patterned media CDU.

4 Overlay

Imprinting patterned media needs a basic alignment to ensure the pattern is properly centered on the disk, but it is a single-layer process requiring no layer-to-layer overlay. Conversely, tight overlay between layers is a critical requirement for semiconductor devices. Unlike projection lithography, there are no moveable lenses to correct for distortions between the template and wafer. For nanoimprint, distortions such as magnification are corrected at the template level, primarily by applying physical forces to the edges of the template during each imprint. J-FIL uses a Moiré interference pattern alignment strategy, with X and Y alignment marks located at all four corners of the field.[12] Current generation templates use a moated alignment mark strategy in which the alignment marks are physically separated from the main pattern area by an etched moat.[29] The alignment marks operate with an air gap, and the moat acts as a barrier to prevent the flow of resist from the pattern area into the alignment marks. Alignment is performed field by field.

Next generation J-FIL templates use high contrast moatless alignment marks to prevent alignment mark contamination. Alignment marks are contaminated when imprint resist crosses over the moat and fills the alignment marks, making them nearly invisible to the alignment systems.[29] The high contrast mark strategy uses a thin layer of chrome in the trenches of the alignment marks to provide a signal sufficient for alignment when the marks are filled with resist.[20] Additional benefits of the alignment strategy include reduced scribe area requirements and better process integration as the entire field, including main pattern and alignment marks, is filled with a uniform layer of resist. Table 4 shows how J-FIL mix-and-match overlay has improved in recent years.

Reductions in J-FIL overlay have been primarily driven by improvements in template pattern placement and imprint tool alignment control. Semiconductor template pattern placement residual 3σ improved from 12 nm to just under 3 nm, a $4\times$ improvement, in less than 2 years.[29] Residual pattern placement includes the errors remaining after accounting for distortions that are correctable by the lithography tool (magnification, scaling, ortho, etc.)

While patterned media have no overlay requirements, the pattern placement requirements for both BPM and DTM are

Table 3 Five-wafer run CDU for 32 nm features. Data collected by measuring 15 sites per field, 32 fields measured/wafer, on 5 wafers, for a total of 2400 measurements (160 measurements per individual field location) (Ref. 35).

	Lower Left			Upper Left			Center			Lower Right			Upper Right		
	Line 2	Line 4	Line 6	Line 2	Line 4	Line 6	Line 2	Line 4	Line 6	Line 2	Line 4	Line 6	Line 2	Line 4	Line 6
Average	32.4	33.7	31.9	33.2	34.5	32.5	30.8	33.0	32.3	32.1	33.7	32.0	31.0	30.3	32.8
Min	30.1	30.9	30.2	31.4	32.6	31.0	29.0	31.5	30.9	30.7	32.1	30.4	29.6	29.0	31.5
Max	33.3	34.7	32.8	33.9	35.5	33.4	31.6	33.7	32.8	32.8	34.4	32.6	31.7	31.0	33.6
Range	3.2	3.8	2.6	2.6	2.9	2.5	2.6	2.2	1.9	2.1	2.3	2.2	2.1	2.0	2.1
3 Sigma	1.5	1.6	1.3	1.2	1.2	1.1	1.1	1.0	1.0	1.0	1.1	0.9	0.9	1.0	0.9
% 3σ	4.6	4.9	4.2	3.7	3.4	3.3	3.5	3.2	3.0	3.2	3.1	2.9	3.0	3.2	2.7

Table 4 Progression of J-FIL overlay results.

Date	X mean $+3\sigma$ (nm)	Y mean $+3\sigma$ (nm)	Comments	Source
Early 2008	34	21	18×30 mm field	Samsung (Ref. 34)
Late 2008	10.6	11.3	15×15 mm field	Toshiba (Ref. 38)
Late 2009	13.3	14.6	26×32 mm field	SEMATECH (Ref. 29)
Early 2011	9.5	10.31	26×33 mm field, Imprio500, 6025 template	Molecular Imprints (Ref. 10)
Early 2011	13.3	13.0	Imprio500, high contrast marks	Molecular Imprints (Ref. 20)

as tight as those for semiconductor devices. For BPM, the maximum placement error for 1 Tb/in^2 density must not exceed 3 nm 3σ on any bit,[40,41] including errors from both the template and process. This requirement will become even tighter as feature sizes decrease and densities increase. Full-disk pattern placement data are not readily available at this time.

To summarize, J-FIL overlay has been demonstrated to be within a factor of 1.4× from the ITRS specification for 22 nm flash memory. Similar results have been achieved with a 6025 form factor template fabricated with high contrast alignment marks. Template pattern placement has been shown to meet ITRS requirements. Alignment mark contamination, highlighted as an issue with moated templates, is being addressed with a high contrast alignment mark strategy. While not often discussed, a global alignment strategy may need to be developed for integration into existing manufacturing processes.

5 Defectivity

Defectivity is one of the main technical challenges for nanoimprint.[42] Defects originate from many sources, including templates, processes, materials, and incoming wafers or disks. Examples of commonly observed J-FIL defects are shown in Fig. 9. Line breaks, bridges, mouse bites, and pattern collapse are common to all lithography processes, but other defect types, including nonfill and adhesion failure during separation, are specific to nanoimprint. Particle defects are of particular concern since nanoimprint is a contact process. These defects can affect not only the field in which they occur, but also all subsequent fields if the particle becomes stuck in the template. Hard particles have been shown to cause permanent template glass damage.[42] Ensuring a particle-free process, including particle-free incoming wafers, is a serious challenge for nanoimprint. Nonfill defects are also common. These defects, which occur when template features are not fully filled by the resist, are closely related to throughput. Shorter resist spread times often result in more nonfill defects, but work is being done to improve both throughput and nonfill defectivity with smaller drop sizes and better control over resist spread.[10] Nonfill has also been shown to be proportional to pattern density, in that templates with larger relief structures, such as via layers, exhibit higher levels of nonfill than templates with tightly spaced structures, such as metal layers.[39]

The ITRS specifies that defect density must not exceed 0.01 def/cm^2 at the resist level for all device types.[24] Unlike logic, memory devices have built-in redundancy, making them more tolerant to defects, and therefore the most

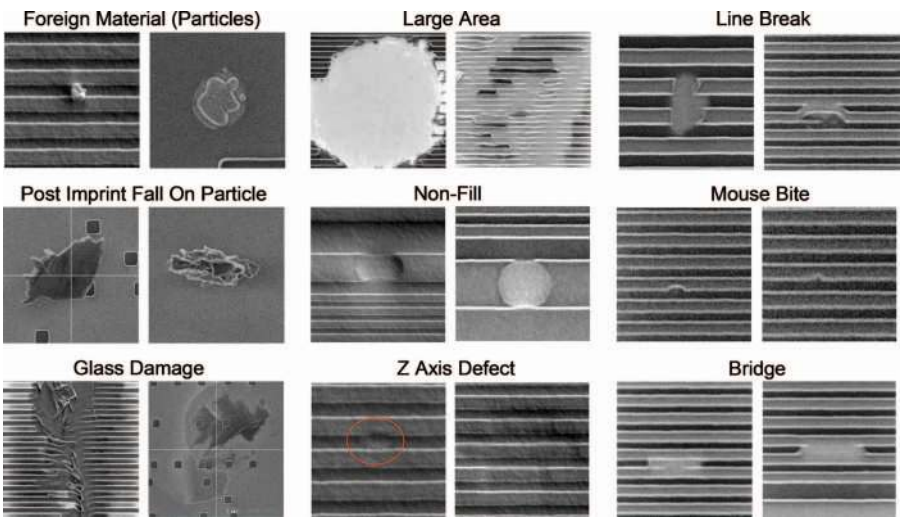

Fig. 9 Examples of commonly observed J-FIL defects (Ref. 11).

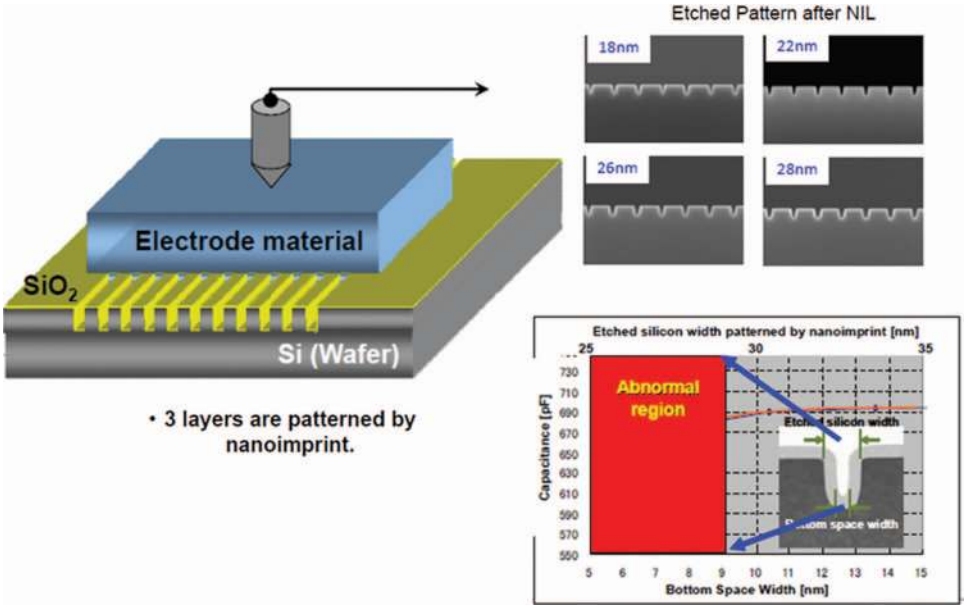

Fig. 10 Gate performance test results, courtesy of Toshiba (Ref. 26).

likely candidate for introducing J-FIL. A major memory manufacturer investigating J-FIL (Toshiba) has stated that a J-FIL defect density <0.1 def/cm^2 is suitable for memory applications.[26]

As in semiconductor devices, the location of a defect in the patterned media area is of utmost importance. Defects in the data area will diminish storage space. However, defects in the servo area, which are less acceptable, may introduce drive performance issues.[36,43] HDD recording heads are within 2 to 3 nm of the disk surface,[16] with disks rotating at 5000 to 15000 rpm,[41] suggesting that large defects in the z-direction may damage the head. Patterned media defect requirements vary by manufacturer and have not been made public.

Until recently, there has been little published evidence of nanoimprint defectivity improvement toward manufacturing requirements. Now, however, multiple sources are showing significant progress in this area. Defect characterization by open circuit electrical testing showed 100% yield on 0.75 mm long test structures for feature widths down to 32 nm, and approximately 70% yield for 24 nm features.[26] Yield decreased as test length increased, but even at 10 m (10,000 mm) the 32 nm features showed yield near 20%. A capacitance evaluation of devices with three J-FIL imprinted layers showed adequate performance for gate lengths down to approximately 30 nm as shown in Fig. 10.[26] This evaluation demonstrates not only device performance but also multilevel integration, including overlay, using J-FIL.

In addition, random process defect density of 0.09 def/cm^2 was demonstrated with a high quality template containing 120 nm half-pitch structures fabricated with a production grade 4× photomask process.[44] While the features were large, the demonstration provided proof of concept for a low defect J-FIL process when using a high quality template. Process defectivity is currently about 10 def/cm^2 for small feature sizes.[19,26]

Template defect densities of 17.3 def/cm^2 (Ref. 44) and 10 def/cm^2 (Ref. 26) have been shown for the latest generation of templates before 65 mm post-processing. The dice, polish, and backside core-out post-processing (see Sec. 6 for details on backside core-out) required for 65 mm form factor templates adds numerous defects, providing motivation to adopt a template form factor using industry standard 6025 (6 in. × 6 in. × 0.25 in.) substrates. Nanoimprint blank defectivity, at 50 nm inspection sensitivity, has been reduced to 0.04 def/cm^2 (Ref. 10).

Inspection capability and throughput for 1× templates are concerns. E-beam reticle/template inspection capability is improving but cannot yet detect defects at 10% of the feature size as specified by the ITRS. Template inspection results on a high end e-beam inspection tool (Hermes Microvision eXplore5200) using a 10 nm pixel size and "leap and scan mode" showed reliable detection of 22 nm clear defects and 30 nm opaque defects on 28 nm half-pitch features.[45] Defects as small as 4 nm were detected in some instances. Full-field (26×33 mm) e-beam inspection of 1× nanoimprint templates has been estimated to take from 1 to 8 days depending on pixel size and type of inspection (die-to-die, die-to-database).[46,47] Frequent full-field inspections will likely be required since nanoimprint is a contact technology and templates can quickly become dirty or damaged. Further development is necessary to reduce inspection time while simultaneously increasing detection capability.

The HDD industry is taking a different approach toward patterned media master, replica, and disk inspection. Full-disk e-beam inspections will be done on every master,[43] and detailed inspections will be done on a certain percentage of replicas. Large area techniques such as scatterometry are being used instead of high resolution inspections. These methods work well for patterned media, which contain simple and consistent patterns across the entire surface. While these techniques are unable to pinpoint individual defects in the pattern, they can detect large particles, defects, and other anomalies at high throughput. For instance, the KLA-Tencor Candela series of tools, used by the HDD industry to inspect conventional magnetic media, has been shown to detect sub-200 nm defects in patterned media.[43]

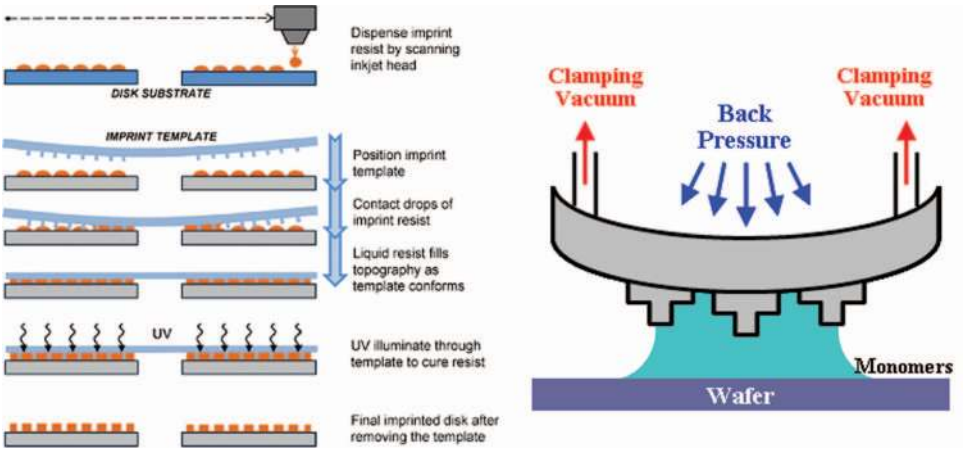

Fig. 11 Patterned media imprint process (left), courtesy of Molecular Imprints. (Reprinted with permission from Ref. 43. Copyright 2009 by SPIE.) Bowing of a template to improve spread time (right), courtesy of Brook Chao at the University of Texas at Austin (Ref. 52).

As defects, particularly due to particles, are a serious concern for nanoimprint, it is important to develop safe and effective cleaning processes for both organic and particle removal. In addition to the commonly used acid-based methods, such as piranha baths (sulfuric acid and hydrogen peroxide), UV/ozone/SP1 acid-free cleaning processes have been shown to be effective for cleaning nanoimprint templates. Early results showed minimal CD changes between cleans of 0.06 nm/clean,[48] and no significant effect on LWR.[35] Further development is required to improve cleaning process throughput and efficiency while eliminating effects on CD size.

Defectivity remains a serious technical challenge for the introduction of nanoimprint into manufacturing, but recent results suggest that low defect processes are possible. Preliminary device testing results, including the integration of multiple J-FIL layers, shows that the technology is maturing to a point at which it may be considered a viable option for memory manufacturing at future nodes. Template defect density has decreased by an order of magnitude in recent years, but it is still a primary driver of overall defectivity. Improvements in 1× inspection capability are required to enable further reductions in template defectivity.

Resist spread time has been identified as the primary throughput-limiting factor for nanoimprint.[50] It is a function of numerous process and template attributes including resist drop size, drop placement, field size, feature size, pattern density, residual layer thickness, imprint material viscosity, and others. The trade-off between resist spread time and defectivity is of particular concern. Spread time is inversely proportional to nonfill defectivity;[29,51] a fundamental challenge for nanoimprint. Reductions in spread time are being addressed through smaller resist drop volume, accurate drop placement, and novel methods of fluid front control. Defectivity has been shown to decrease proportional to drop volume;[10] and as a result, next generation J-FIL tool resist dispensers provide drop volumes as small as 1.5 pL.[19]

In addition, starting the fluid flow at the center of the field or disk, as shown in Fig. 11, increases throughput by accurately controlling the fluid front and preventing nonfill in interior pattern areas by forcing trapped air toward the edges of the template.[43,52] Current generation J-FIL templates for semiconductor applications, such as the one shown in Fig. 12, are fabricated with a backside recess such that the center of the template is thin and can be easily bowed during the imprint process.

6 Throughput

Throughput is another serious concern for nanoimprint. Throughput targets for 300 mm wafer processing are typically on the order of 100 to 200 wafers/h. Each wafer can contain hundreds of imprinted fields. Patterned media throughput is expected to be greater than 1000 double-sided disks/h, with one full disk imprint per side. Current J-FIL development tools for semiconductor applications, such as the Molecular Imprints Imprio300, can print four wafers/h,[35] but throughput must be reduced to minimize defectivity.[29] Throughput for the next generation semiconductor J-FIL tool, the Imprio500, is specified at 20 wafers/h.[19] Multiple module cluster tools, as proven viable for patterned media, will be needed to meet industry throughput demands as a single module will not be able to meet the 100 to 200 wafer/h target. For patterned media, a 300 disk/h tool, the NuTera HD7000, is being used to demonstrate feasibility of a high volume J-FIL process.[49]

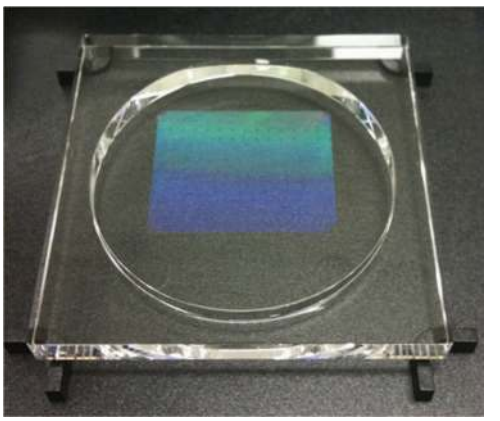

Fig. 12 Current generation 65 mm form factor J-FIL template for semiconductor applications.

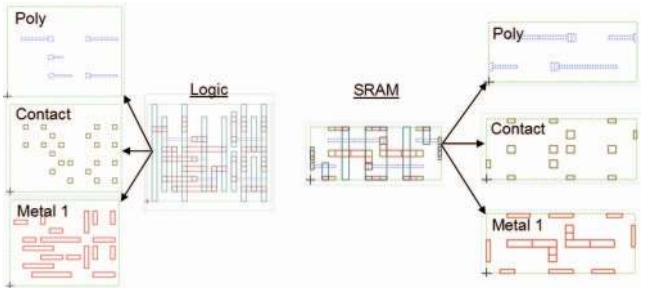

Fig. 13 Sample logic and SRAM layouts for write time estimates. (Layouts courtesy of ISMI.)

While not associated with J-FIL, recent work on gas condensation with pentafluoropropane gas has shown significantly shorter spread times than imprints performed in air.[53] The results demonstrate another potential solution for increased throughput.

Meeting throughput demands will continue to be a challenge for nanoimprint, although excellent progress has been made through several generations of imprint processes and novel approaches to the speed and control of resist spread. The J-FIL cluster tool strategy has proved to be a possible option for both patterned media and semiconductor applications, but further development is required if nanoimprint is to meet high volume manufacturing requirements.

7 Template Infrastructure

Production grade templates are an absolute requirement for introducing nanoimprint into HVM. Template manufacturing capabilities have improved to a preproduction level, as evidenced by recent J-FIL results, but full-field/full-disk templates meeting all of the required specifications may not be available for some time. In addition to challenges such as defectivity and inspection, template write time and cost raise concerns. Recent estimates for semiconductor templates show write times of approximately 2 days for a 22 nm SRAM layer with nondense feature spacing.[29] Table 5 shows write time estimates for various layers of memory and logic devices. The device layers used to create these estimates can be seen in Fig. 13. A previous COO study estimated that the cost of a template with a 25 h write time would be over $600,000.[54]

Table 5 Estimated J-FIL template write times for a 26×33 mm field using a NuFlare EBM-7000 VSB e-beam writer.[a] (Write time estimates courtesy of NuFlare and DNP.)

Device	Layer	32nm (Hours)	22nm (Hours)
Logic	5-Poly	9	17
	9-Contact[b]	18	35
	10-Metal 1[b]	15	29
SRAM	5-Poly	19	37
	9-Contact[b]	26	52
	10-Metal 1[b]	21	42

[a]Number of passes will vary by process and requirements.
[b]Write opposite tone pattern, with positive resist, then flip with replication.

Patterned media master write times are expected to be much longer, with estimates varying from 1 week for a 65 mm DTM master at 90 nm track pitch[16] to 22 days for a 65 mm DTM master at 50 nm track pitch[55] and longer for other disk sizes, feature dimensions, and densities. Figure 14 (left) shows the estimated write time for 65 mm disks, written with a 4 nm spot size, as a function of writer beam current and resist sensitivity.[56] Spot sizes as low as 1 nm and additional write passes may also be required,[57] potentially making write times even longer. According to a patterned media COO study, master costs will range from $1 to $5 million, depending on yield and e-beam writing speed, as shown in Fig. 14 (right).[57] Note that two masters are required, one for each side of the disk.

Multiple development efforts are underway to offset the time and cost associated with master template fabrication. Template replication and directed self-assembly (DSA) have been the primary focus, while additional improvements could be realized through the development and implementation of multiple beam mask writers[58] and faster e-beam resists. The combination of DSA and e-beam writing is likely to be used for the fabrication of patterned media masters. As shown in Fig. 15, block copolymer materials have been used to create densely packed arrays of dots based on a starting sample created with an e-beam writer.[40] DSA is suitable for this

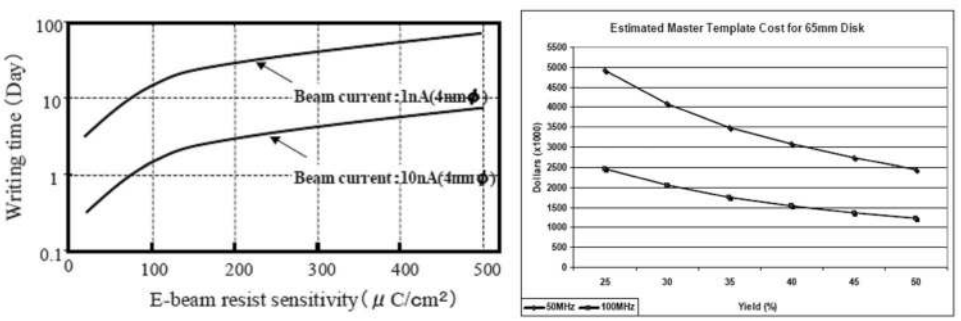

Fig. 14 E-beam write time as a function of beam current and resist sensitivity, based on a 65 mm disk and 4 nm e-beam spot size (left). Courtesy of DNP. (Reprinted with permission from Ref. 56. Copyright 2009 by SPIE.) Patterned media master cost estimates as a function of yield and write speed. Yield based on mask industry history with contact hole masks (right). Courtesy of Grenon Consulting. (Reprinted with permission from Ref. 57. Copyright 2009 by SPIE.)

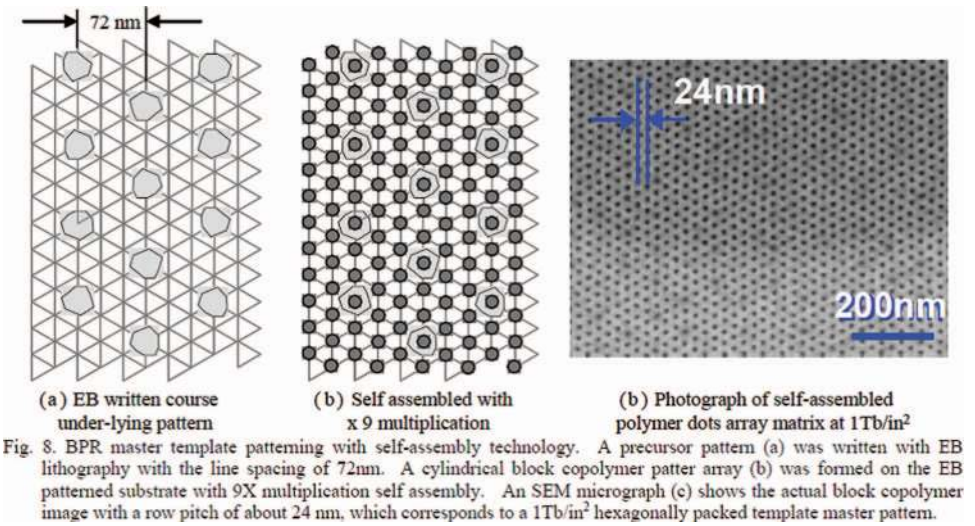

Fig. 15 Combination of DSA and e-beam for patterned media master generation. (Reprinted with permission from Ref. 40. Copyright 2009 by SPIE.)

application due to the simple, constant, and densely packed structures that make up the patterned media surface.

Template replication is a promising solution for meeting COO targets[59] and providing large numbers of high quality templates. Replication for J-FIL templates is similar to the standard imprinting process, except that the substrate is another template rather than a wafer or disk. Recent results have demonstrated that J-FIL replication can produce replicas with image quality and uniformity similar to that of the master.[60]

The benefits of replication are well understood for patterned media for which projections show an estimated 1 billion double-sided disks per year.[14,61] A strategy including masters, sub-masters, and working templates is being developed to meet this goal. If successful, each master would be able to make 10,000 replicas and each replica 10,000 imprints, for a total of 100,000,000 imprints or 50,000,000 double-sided disks.[62]

While replication is also required to introduce nanoimprint into semiconductor manufacturing, the scenario is different. There are many chip manufacturers, each with many products, device layers, and pattern revisions which make cost calculations highly application dependent. From a logistical viewpoint, chip manufacturers are not accustomed to large quantities of replicas in the process line. Yield enhancement and failure analysis would become particularly complicated. One memory manufacturer has stated a template lifetime requirement of 100,000 imprints.[22] Another expects each template to last for 600 wafer lots.[38] Current estimates show that a replicated template will be capable of approximately 50,000 imprints.[60]

Template manufacturing capability continues to improve, and development is underway to enable the production of high quality full-field/full-disk templates. Preproduction grade templates, suitable for demonstrating the capabilities of J-FIL, are now available. Template write time and cost are serious issues for both semiconductor and patterned media applications. Development continues on template replication, DSA, and other techniques designed to provide nanoimprint with a low COO, with template replication tools having been already commercialized.

8 Conclusion

Nanoimprint, specifically J-FIL, continues to be investigated as an HVM solution for next generation semiconductor devices and HDD patterned media. Memory devices, such as 22 nm flash, and HDD products, such as 1 TB/in^2 BPM and DTM, are the primary targets for introducing J-FIL. In addition to its excellent resolution, CDU, and LWR capability, J-FIL overlay, defectivity, and throughput have dramatically improved. Infrastructure too has improved with the commercialization of high volume development tools, 6025 form factor templates, and template replication processes.

Despite the rapid progress, many challenges remain. Defectivity, while having improved significantly in recent years, remains the primary technical challenge as it is orders of magnitude away from industry requirements. Further improvements are also required for other critical aspects such as overlay for semiconductor applications and full-disk CDU for patterned media. Long term testing and comprehensive device/media demonstrations, as opposed to single point champion results, are needed to demonstrate the technology's full potential. However, the most serious issue facing nanoimprint at this time is not technical. It is the declining industrial interest from both the semiconductor and HDD industries. Most semiconductor manufacturers have decided on EUV or 193i double patterning for future nodes. Only a small number are actively investigating nanoimprint. Likewise, the HDD industry has delayed development of patterned media in favor of HAMR. Although nanoimprint has proven itself to be a promising solution for both industries, it is unclear whether or not it will be used for HVM.

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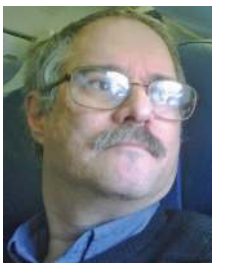

Lloyd C. Litt received his BS and MS degrees in imaging and photographic science from Rochester Institute of Technology. He has worked in semiconductor lithography development since 1985 at companies including IBM, Motorola/Freescale, and AMD/GLOBALFOUNDRIES. He is currently the Alternative Lithography Program Manager at SEMATECH in Albany, NY, and is an assignee from GLOBALFOUNDRIES.