Temperature Compensation in OTA-C Integrators Using a Resistive Bridge

Arash Moradi

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ABSTRACT

Temperature Compensation in OTA-C Integrators

Using a Resistive Bridge

By: Arash Moradi

In this thesis, a new technique for temperature compensation of G_m-C filters is presented. An Operational Transconductance Amplifier (OTA) as well as the output buffers is implemented in STMicroelectronics 90-nm technology with 1.2 V supply voltage. Variation of a gate-capacitance implemented by an NMOS transistor with respect to temperature is investigated. Using negative feedback the G_m-cells' transconductance is locked to the reciprocal of a resistance array. Temperature behaviour of the G_m-C filter is examined by the behaviour of a G_m-C integrator without receiving an external frequency reference. Temperature dependency of the G_m/C ratio, which determines the unity-gain frequency of the integrator, is minimized by arranging the temperature dependency of the resistors. Unique properties of a proposed resistive bridge allow for the synthesis of temperature coefficients beyond the range of coefficients of constituent elements. With a set of practical elements a variation of only 0.66% in G_m/C has been achieved over -40°C to 120°C.

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List of Acronyms

CMC	Canadian Microelectronics Corporation
CMFB	Common-Mode Feedback
DLL	Delay-Locked Loop
FLF	Flipped-Voltage Follower
NMOS	N-type Metal-Oxide-Semiconductor
NRL	Negative Resistive Load
OA	Operational Amplifier
OTA	Operational Transconductance Amplifier
OTA-C	Operational Transconductance Amplifier-Capacitance
PLL	Phase-Locked Loop
TC	Temperature Coefficient
VCO	Voltage-Controlled Oscillator

Chapter 1 Introduction

1.1 Background and Motivation

One of the key building blocks in continuous-time filters is the Operational Transconductance Amplifier (OTA). OTA-Capacitor (OTA-C) filters generally can lead us to a higher operating frequency compared to other continuous-time filters built using, for example, an operational amplifier (OA) [1]. The transconductance (G_m) of the OTA device is an important parameter in the design of an OTA-C filter. The G_m-cells, realize the filter along with capacitances. The G_m of the OTA and the capacitor (C) create a continuous time integrator. Thus, the OTA-C filters are based on G_m-C integrators. Therefore, the OTA-C filters are also referred to as G_m-C filters. Transconductance of these G_m-cells is set by a current or voltage as a control signal.

The frequency characteristics of an OTA-C filter are determined by its parameters G_m and C. Both parameters, G_m and C, vary with process, voltage supply and temperature (PVT) differently and this makes the frequency tuning techniques necessary for OTA-C filters.

Specifically, change of temperature, as a parameter which is considered in this work, results in some changes in characteristics of the transistors of the OTA-C filter. For example, variation in mobility of charges in transistors changes the biasing current and voltage which changes the working point of the circuit. Moreover, frequency response

would also be changed which is not desirable. Therefore, some techniques have to be employed to stabilize the frequency behaviour of the filters against temperature.

In many designs, frequency tuning is done by sensing the frequency using voltage-controlled oscillators (VCO) and employing a voltage-controlled filter or a phase-locked loop (PLL). Employing such technique for frequency tuning has its own challenges and problems [1], such as the need for an external frequency reference or design of the needed circuits [2]. As another example, in [3] a delay-locked loop (DLL) is used for frequency tuning. In Chapter 2, some reported techniques for frequency tuning are discussed in more detail.

Another common technique for filter tuning is to control one OTA such that it satisfies the required G_m characteristics. The tuning signal of this OTA is fed to similar OTAs in the filter, thereby producing the required frequency response [1], [4]. This method is the basic scheme which we have adopted and improved in this thesis. This will be explained in Chapter 4. The unity-gain frequency of the mentioned OTA-C integrator is determined by the ratio G_m/C [5], [6]. Keeping this ratio constant over temperature can lead to a stable frequency response characteristic against temperature variations. In most reported works, the variation of the capacitance with respect to temperature is assumed to be negligible and only G_m is tried to be stabilized over temperature. However, in this thesis, the capacitor's variation with respect to temperature is considered, thereby improving the temperature insensitivity of the OTA-C integrator, and in turn, the frequency response of the realized filter.

1.2 Contribution

After a careful review of several reported OTA circuits in CMOS technology, one structure has been chosen for further improvements. This was necessary to suit the purpose of control of the characteristics over a very wide range of temperature. Design and modification of the chosen OTA is the first contribution in this thesis.

In this thesis, building upon the technique presented in [7], in this thesis the variation in capacitance with temperature, in addition to that of the transconductance of the OTA has been considered. The capacitance is implemented in CMOS technology and simulations are done to observe the behaviour of the capacitance in different conditions such as change of frequency, temperature and biasing voltage. This is the second contribution.

A new way of G_m tuning against temperature in OTA-C filters is presented. In [7], the transconductance is locked to a resistance to be kept constant over temperature. In this work, the temperature dependency of the resistor is chosen such that it cancels the temperature dependency of the capacitor, leading to a nearly temperature independent OTA-C integrator. However, choosing an appropriate resistor is a challenging task. The third contribution lies in the use of a novel bridge structure having unique temperature properties of its trans-resistance. Locking G_m to the proposed resistive bridge facilitates control of the temperature behaviour of the transconductance desirably. The relevant work has been reported and published in *Electronics Letters* (IET, UK) [8].

Finally, by forcing G_m to track the properly chosen resistance structure, G_m changes similar to C with temperature variations, and hence, the ratio of G_m/C is kept constant over temperature. This ratio determines the frequency characteristic of the G_m-C filter.

Positive and negative temperature coefficients of the resistors beyond the range of those of available resistors are achievable by the structure proposed in this thesis.

1.3 Thesis Outline

The rest of the thesis is organized as follows: In Chapter 2, several OTAs reported in the literature are introduced and discussed to choose one specific OTA for implementing our technique. Several frequency tuning techniques reported in the past are discussed. A recently reported technique is considered in detail. In Chapter 3, the chosen OTA is modified for improved performance and simulated successfully. The technique for frequency tuning over wide temperature variation (-40 °C to 120 °C) is then developed in Chapter 4, followed by some suggestions for future work in Chapter 5. Notice that in this thesis, we have focused on the effect of the temperature on frequency behaviour of OTA-C filters by ensuring that the constituent G_m-C integrator has a constant unity-gain frequency across temperature.

Chapter 2 Literature Review

2.1 Introduction

In this chapter, several tuneable OTAs are introduced and studied. One of the OTA circuit is selected for further improvements for application to our case study. Some frequency tuning techniques are also presented in this chapter followed by the introduction of the principles of the chosen technique which is developed in this thesis.

2.2 Tuneable OTAs

Each of the reported OTA is designed for a specific application. In order to choose a good OTA for this project we should find a design with a wide tuning range for the transconductance. In addition, linearity and simplicity of the design are very important issues. Notice that other specifications, such as power consumption and bandwidth are of interest as well.

In Figure 2.1, Figure 2.4 and Figure 2.5 we present the schematics of three notable OTAs reported in [10], [11] and [12], respectively. The OTA of Figure 2.1 is reported to have a linear range for G_m adjustment over the tuning current. It utilizes the Source-Degenerated Current Mirror implemented by transistors $M_{1a,b}$, $M_{2a,b}$, $M_{3a,b}$ and $M_{4a,b}$. Transistors $M_{1a,b}$ and $M_{3a,b}$, working in triode, are the degenerating resistors.

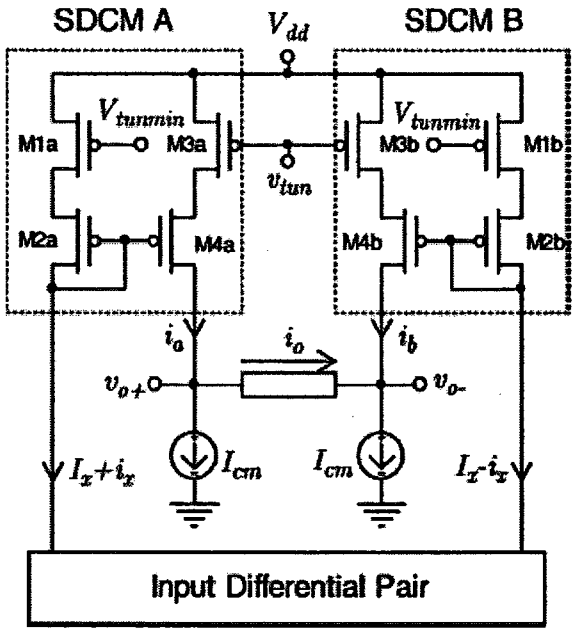

Figure 2.1 Simplified schematic diagram of the OTA in [10]

Assuming all transistors in Figure 2.1 have the same sizing, for $v_{tun}=v_{tunmin}$ the current gains of SDCM A and SDCM B are equal to 1 and controlled by v_{tun}. As v_{tun} increases the conductance of the triode transistors $M_{3a,b}$ decreases. This results in a decrease in the current gains. If we assume that g_{md} is the transconductance of the input differential pair, i_o would be a function of i_x, v_{tun} and v_{in}. Finally, the total OTA transconductance is a function of v_{tun} as well as i_x, g_{md} and etc. [10]. Figure 2.2 shows the complete schematic of this OTA. The circuit for linear adjustment of the transconductance is also shown in Figure 2.3. Although this OTA is reported to have a good linearity, the complexity of the design and number of transistor (55 transistors for the OTA part only) makes the design not appropriate for our project.

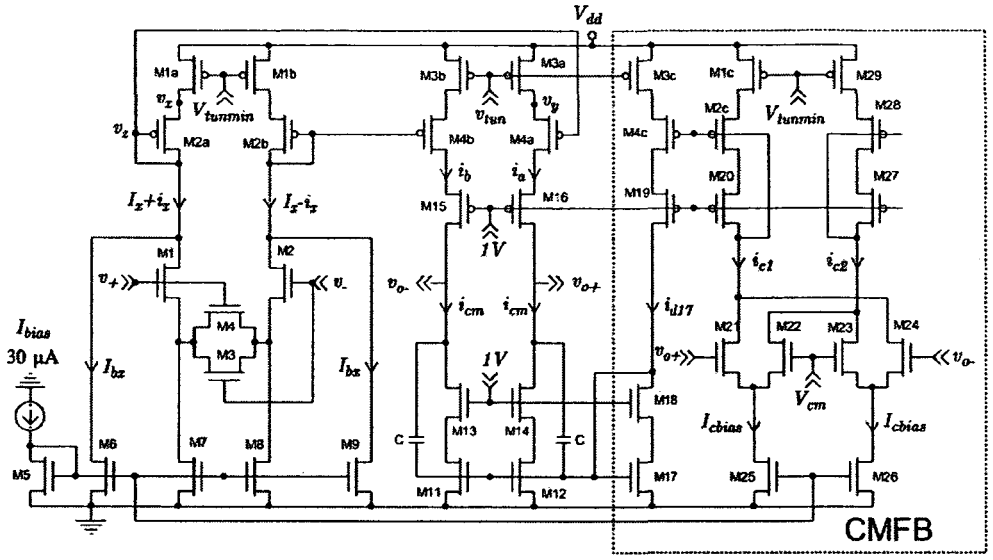

Figure 2.2 Complete schematic of OTA with CMFB reported in [10]

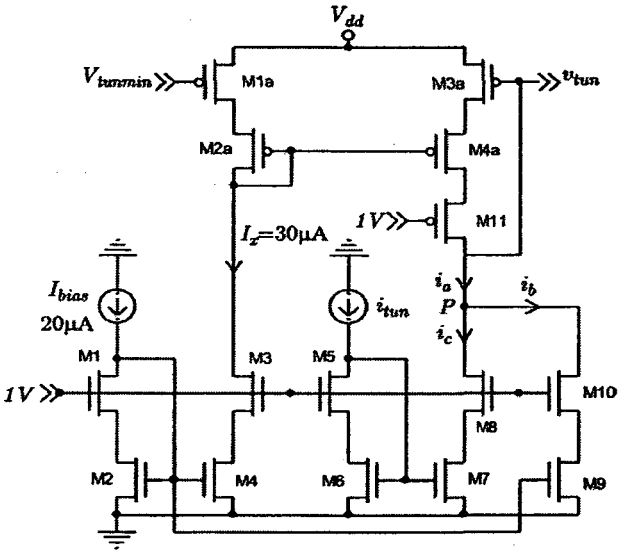

Figure 2.3 Designed circuit for linear adjustment of G_m in [10]

Figure 2.4 shows another OTA reported in [11]. A Negative Resistive Load (NRL) configuration is used in this circuit as well as a floating voltage source. The NRL circuit has a control signal V_A to set the value of the resistance.

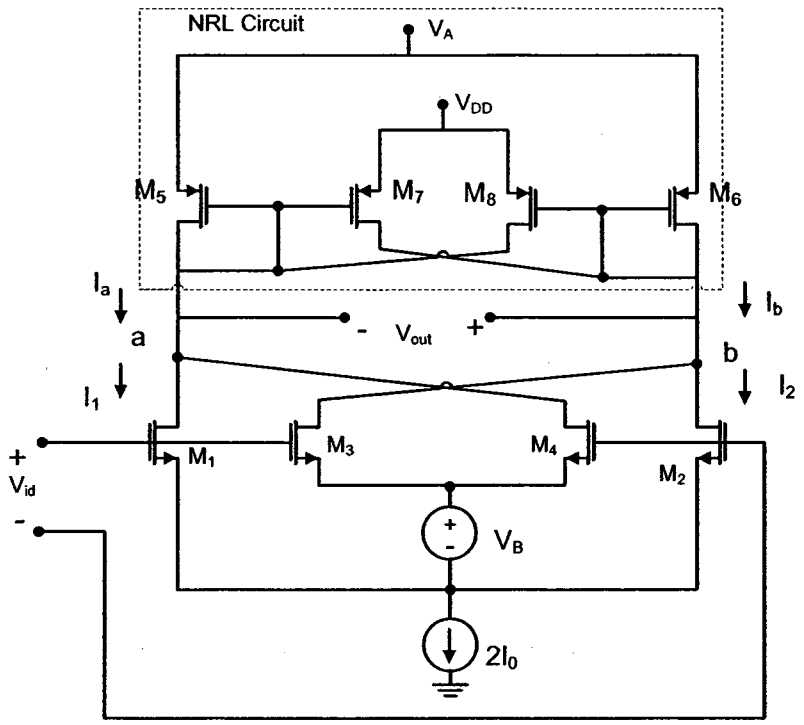

Figure 2.4 OTA schematic with voltage-variable NRL circuit reported in [11]

Some important characteristics of this structure are good linearity and range of tunability. Requirement of a floating voltage source as well as the NRL structure adds complexity to the design. Also, this design creates some extra noise similar to those in [13] and [14].

Figure 2.5 shows the schematic of the OTA proposed in [12]. Transistors P5 and P6 act as negative resistive source degeneration loads. The transistors in bold in Figure 2.5 realize the OTA circuit and transistors Q1–Q5 set up the DC voltage of the inputs such that the differential input impedance is not affected. V_{BP} is the tuning signal for this OTA and is connected to the body terminal of P5 and P6. This tuning signal is claimed to be obtained from a Schmitt-trigger-based feedback loop employing the same OTA of Figure 2.5 based on what has been recommended in [15].

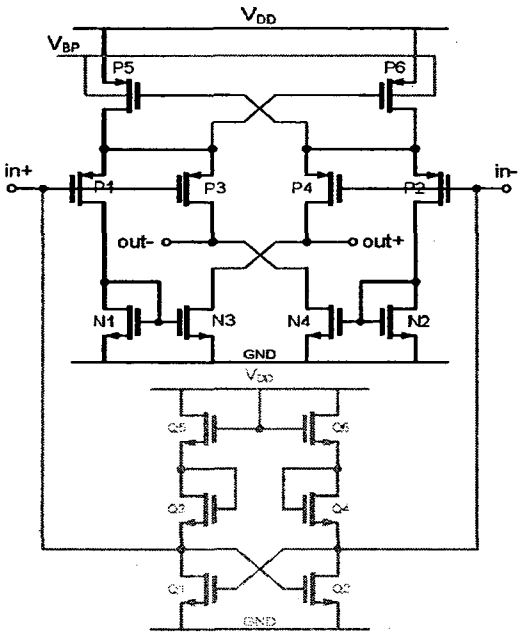

Figure 2.5 OTA schematic reported in [12]

The reported specifications of this OTA as well as the complexity make this OTA inappropriate for the purpose of our work.

In the following, the final chosen OTA, reported in [16], is introduced. Figure 2.6 depicts the schematic of this OTA. This OTA uses NMOS transistors (M_{R1} and M_{R2}) which are working in triode as resistors. I_{B2} is the control signal in Figure 2.6 and is translated to the gate-source voltage of the resistive transistors. Changes in I_{B2} result in changes in the resistance of M_{R1} and M_{R2}. Using the Flipped-Voltage Follower configuration, the differential input voltage is translated to the voltage across the mentioned transistors to produce a current. The produced current flowing into M_{R1} and M_{R2} is then transferred to the output branch to make the output current. Simplicity of the design, small number of transistors and the range of tunability make the OTA of Figure 2.6 suitable to choose for this thesis.

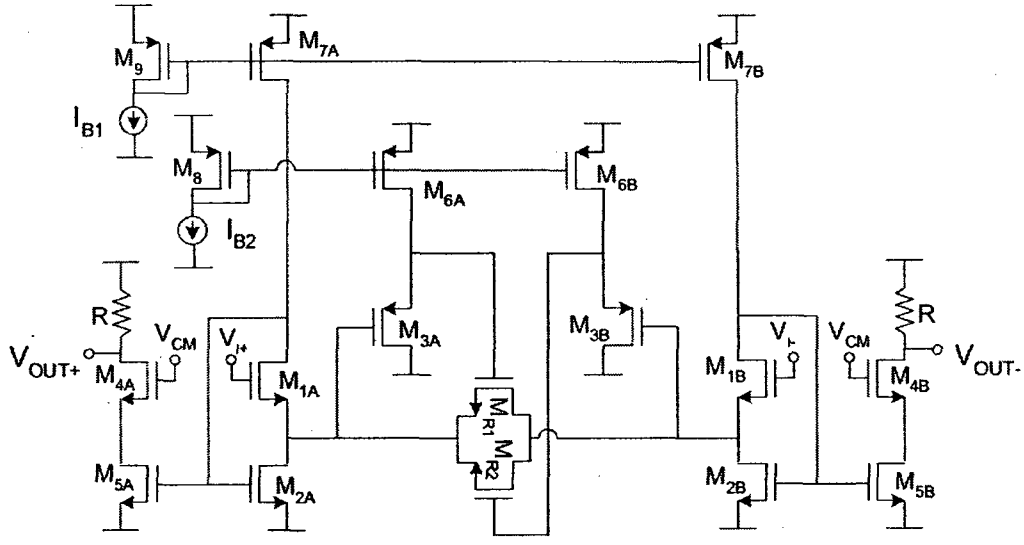

Figure 2.6 Chosen OTA for this thesis reported in [16]

Comparing the characteristics of the above OTAs and our requirements, the system in Fig. 2.6 was chosen to be the starting point of my work. Notice that 35 transistors are finally used to implement this OTA including the common-mode feedback circuit.

2.3 Frequency Tuning and Temperature Compensation

Tuning the frequency response of a filter or filter building block using an external reference frequency is a widely used technique in analog filters. Such a technique is also applicable in mixed signal designs [17]. The tuning is required because the variations in the environmental parameters, such as temperature, causes deviation in the prescribed frequency response. Therefore, different techniques should be employed to temperature compensate the filters.

In [15], in which ultra-low supply voltage designs are investigated, an active-RC filter is made by variable capacitors, resistors and low-voltage OTAs. An MOS transistor

working in weak inversion is used as a three-terminal variable capacitor. The mentioned capacitor is the gate-source capacitance (drain and source are connected) and is controlled by a voltage on the body terminal. For this three-terminal device the inversion level, which defines the capacitance, is changed by the body voltage and, in this way, the capacitance is controlled.

In [15], resistors and variable capacitors are used to make a voltage-controlled oscillator (VCO) which is inside a ring oscillator. A phase-locked loop (PLL), as a phase detector, compares the VCO frequency to an external reference clock and controls the body voltage of the varactor when the PLL is in lock. The VCO varactors and resistors are matched to those in the filter and, as a result, the center frequency of the filter is tuned [15].

In fact, the above mentioned procedure of frequency tuning is the basic idea for frequency stabilization in most filter designs. In particular in OTA-based filter designs, one can control the transconductance of the OTAs so that the overall filter behaves desirably. For instance, in [4] one G_m-cell is placed inside a control loop such that the transconductance is set to a desired G_m and finally the tuning signal of this G_m-cell is provided to the other G_m-cells in the filter. Figure 2.7 shows the control loop circuit. The reference signal, which is shown by *ref* in Figure 2.7, is a sinusoidal voltage with a frequency of f_{ref}. The reference signal is applied to a 1st order low-pass filter. Both the output of the filter and the original reference signal are squared and applied to envelope detectors. The output of the envelope detector with the input of the reference signal is halved. Due to the negative feedback in the loop, the two inputs to the operational amplifier become equal to one another, meaning that gain, $V_{out}/V_{in,}$ is set to $1/\sqrt{2}$.

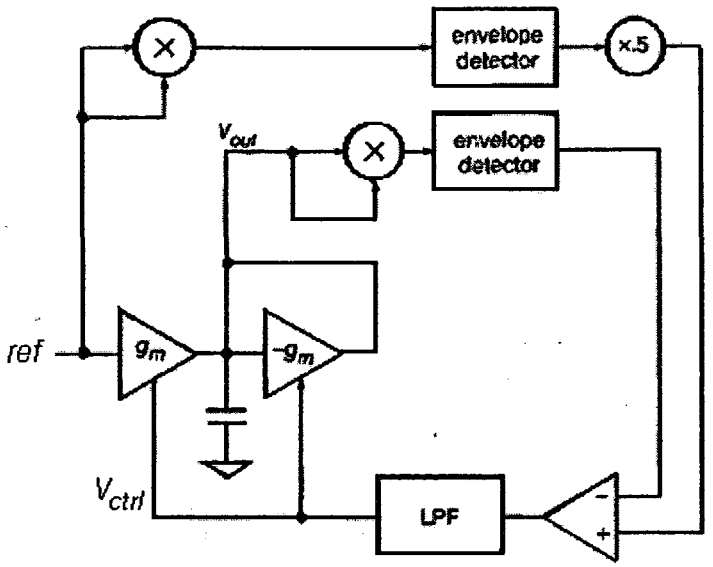

Figure 2.7 Control loop circuit for transconductance reported in [4]

The input and output relationship (gain) is $V_{out}/V_{in}=1/(1+sC/g_m)$ [4]. When g_m/C is smaller than ω_{ref}, therefore, the gain amplitude would be smaller than $1/\sqrt{2}$, and vice versa. In both cases the loop compensates for the transconductance such that g_m/C becomes ω_{ref} (Figure 2.8).

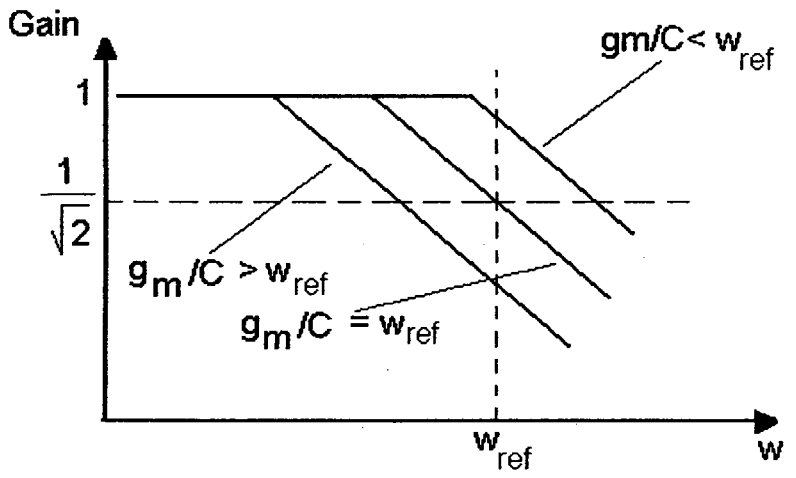

Figure 2.8 Principle of frequency tuning [4]

In the above technique, the basic idea is to tune a filter to have a particular response relative to a reference frequency within a loop including the G_m-cell. As mentioned before, the tuning signal of the transconductance finally goes to the other G_m-cells in the main OTA-C filter. Since this work employs comparison of the envelope detected output voltage levels for frequency tuning, it is required to provide a reference frequency to this loop.

Another case of frequency tuning in G_m-C filters is reported in [18]. In this work, specifically the effect of temperature on the transconductance is reduced. Applying a negative feedback technique, the control loop of Figure 2.9 generates the control voltage for each OTA in the filter. The loop utilizes some building blocks such as amplifiers and sample-and-hold circuits such that the generated control voltage is a function of temperature in the desired way. The range of stability of the tuned filter is between -30 and +85 °C [18].

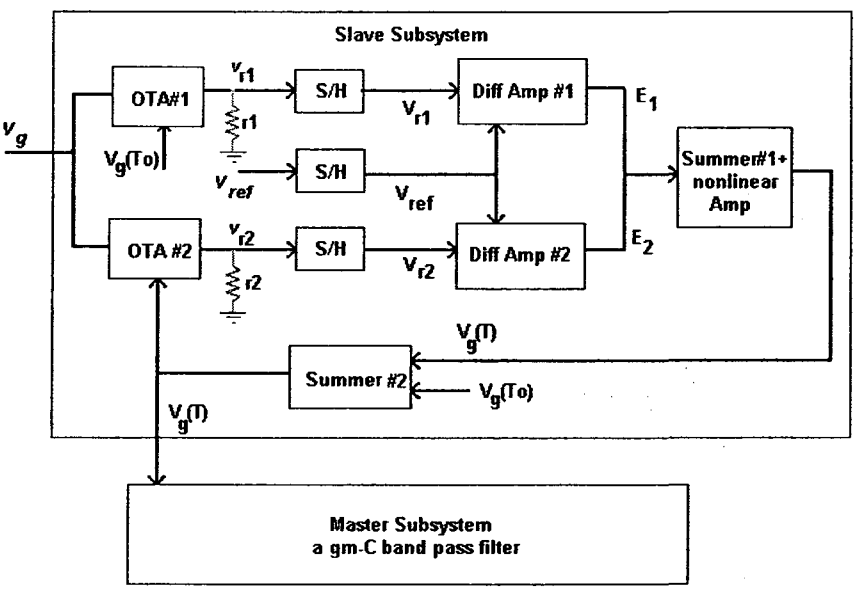

Figure 2.9 Block diagram of control system in [18]

The two techniques introduced in the following are very similar in function. In both cases, a G_m-cell works inside a control loop such that the transconductance varies desirably, for example, it tracks a resistance. Figure 2.10 shows the circuit of the control loop which is reported in [19]. In particular, in this loop, the G_m is:

$$G_m = \frac{1}{R_0}\frac{I_R}{I_0} \tag{2.1}$$

In this technique, as shown in Figure 2.10, the total G_m of a Transconductor is set in a control loop similar to a Master circuit, so that it is kept unchanged as temperature varies. Finally, the tuned G_m from the Master circuit is used in the actual G_m-C filter, the Slave.

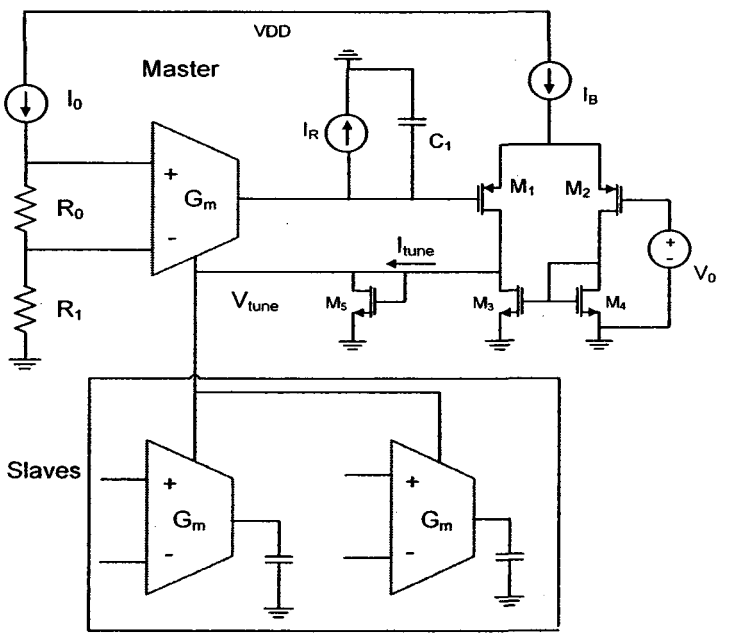

Figure 2.10 Control loop circuit for transconductance reported in [19]

Figure 2.11 shows the control loop for adjustment of the transconductance. This loop has digital inputs (CTRL [N-1:0]) to set the working frequency and a simple digital to analog converter. Once the working frequency is set to the desired value at initial set-up, the

digital input stays unchanged. In this way, the interference noise from the automatic frequency tuning circuit will not affect the operating filter [20]. This loop compensates for both supply voltage and temperature variations. In particular, G_m is locked to the resistance R which is connected across the output of the OTA (Figure 2.11). As R has a very low temperature dependency, G_m stays fairly temperature independent. The input branches in Figure 2.11 which are generating V_{ref} and V_{DAC} are cancelling the unwanted variations of voltage supply, as well.

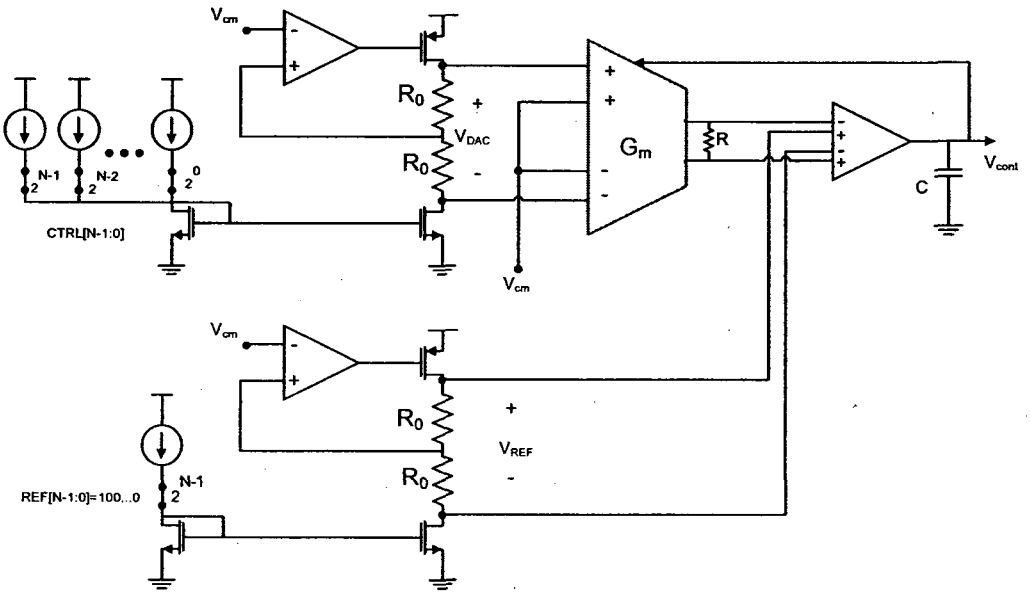

Figure 2.11 Control loop circuit for G_m/VDD compensation [20]

In both the designs of Figure 2.10 and Figure 2.11, the variation of the related resistance as well as the output capacitance over temperature is not taken into account as a controlling parameter. However, the basic idea of locking G_m to a resistance inside a loop similar to that in Figure 2.11 is used to implement our technique in this thesis. In the following, the principles of locking G_m to a resistance are investigated in more detail.

2.4 Locking G_m to a resistor

In this section, the principles of the technique for temperature compensation in a G_m-C filter are explained. The basic idea is to lock the value of the transconductance (G_m) to the value of a resistance so that the G_m tracks the resistance behaviour with respect to temperature. In the next Chapter, it is shown how choosing different resistors affects the temperature behaviour of the transconductance.

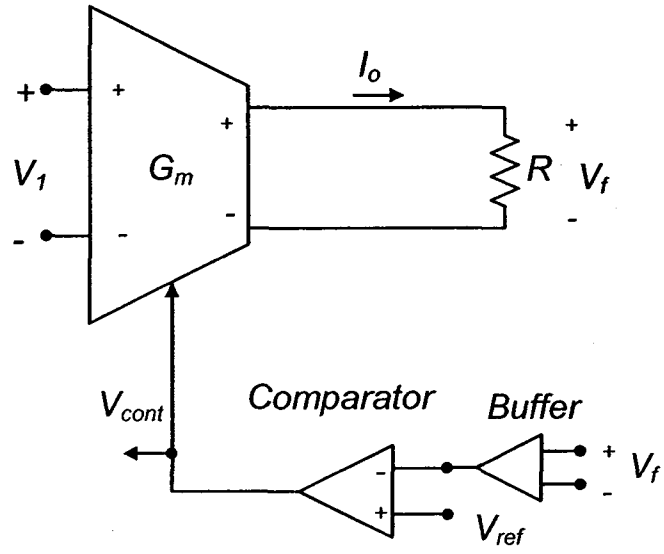

Figure 2.12 Simplified control loop for G_m adjustment, based on [20]

Figure 2.12 shows the simplified control loop for G_m based on [20]. In this circuit, V_1 is the DC input of the OTA to produce the output current of I_o. Flowing I_o to R makes the voltage V_f which is converted to an equal single ended voltage and applied to the comparator amplifier by a buffer. The resistance R is assumed to have practically zero temperature coefficients over temperature variations. The comparator compares V_f with V_{ref}, the reference voltage, to generate V_{cont}. This voltage, V_{cont}, finally goes to the main

OTA-C filter to set the transconductance. According to the configuration shown, one can easily derive G_m as follow:

$$V_f = I_O R = G_m V_1 R \tag{2.2}$$

Referring to Fig. 2.12, $(V_{ref} - V_f)$ A = V_{cont}. As A goes to infinity, V_f would be set to V_{ref} and V_{cont} would be a finite DC value which sets the G_m. Therefore we have:

$$G_m = \frac{1}{R}\left(\frac{V_{ref}}{V_1}\right) \tag{2.3}$$

Thus, the value of G_m is locked to the resistance R, and hence, shows temperature dependence only as much as R allows. As a result, the control voltage, V_{cont} and the transconductance, G_m are set properly to determine the frequency behaviour in the main G_m-C filter (Figure 2.13). Notice that V_{ref} and V_1 are DC voltages and once they are defined for a specific frequency (i.e., the ratio G_m/C) they will not change.

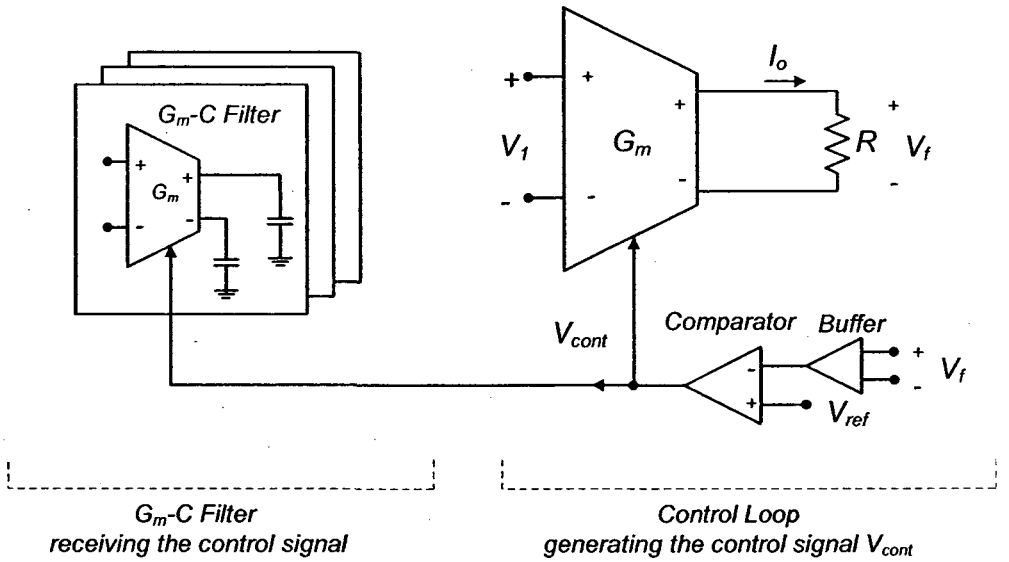

Figure 2.13 Setting the transconductance for a G_m-C filter using the generated control signal, V_{cont}, in the control loop

For the G_m-C Integrator, the temperature effect of the output capacitance is considered in this thesis in addition to that of the transconductance. The behaviour of G_m, which determines the unity-gain frequency ($f_U=1/2\pi\times G_m/C$) of the G_m-C filter, can be controlled in a feedback loop to track the capacitance behaviour. In fact, if G_m and C change similar to each other with respect to temperature, f_U which is determined by their ratio (G_m/C) will stay constant. Therefore, frequency characteristics of the OTA-C filter will stay constant.

2.5 Summary

To conclude this chapter, an overview of some techniques of frequency tuning in OTA-C filters was presented. Several OTA circuits that form the basic amplifier in such systems have been considered. This exercise was undertaken in order to choose one suitable OTA circuit to implement the technique of frequency tuning in this thesis. Finally, the principles by which frequency tuning is achieved were illustrated briefly. In Chapter 3, the analysis and simulation results for the chosen OTA are given. The proposed temperature compensation technique is presented in Chapter 4, followed by suggestions for future works in Chapter 5.

Chapter 3 Analysis, Simulation and Layout of the tuneable OTA

3.1 Introduction

In order to temperature stabilize an OTA-C filter, we first need to design a transconductance amplifier whose transconductance can be adjusted with a control signal (tuning signal). By setting the transconductance with the tuning signal, we are able to control the frequency characteristics of the OTA-C filter. Therefore, the range of tunability is of concern in this design. In this chapter we shall consider the design of a simple OTA from the several OTAs discussed in Chapter 2 and implement it in ST 90-nm CMOS technology. The design is followed up by improvement towards increased linearity. The layout of the final OTA with associated CMFB and output buffer circuits are shown at the end of this chapter. The final designed OTA will be used in the next chapter to illustrate the implementation of the technique for temperature compensation.

3.2 Analysis, Design, and Simulation of the tuneable OTA

In this section, the operation of the OTA chosen for this project is explained and design considerations are discussed. This is followed by improvements in the design and validation using simulation.

3.2.1 The OTA circuit

The simplified schematic of our OTA is shown in the Figure below.

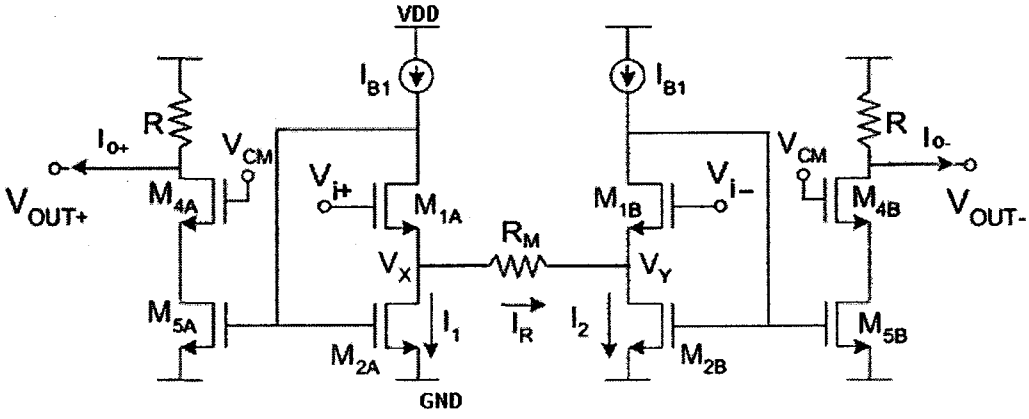

Figure 3.1 Circuit of OTA, based on [16]

M_{1A} (M_{1B}) behaves like a source follower. This configuration is called Flipped-Voltage Follower (FVF) and is common in other designs, such as in [21], [22] and [23]. Ideally, the variation of the input, $V_{id}=V_{i+}-V_{i-}$, will be translated to the variation of V_x-V_y, the voltage across the resistor R_M. This is due to the fact that I_{B1}, the biasing current of M_{1A}, is constant and fairly independent of the input voltage. The other reason would be the existence of the low output impedance buffers [21].

The equivalent resistance at the source of M_{1A} is small such that the pole at this node is large and does not limit the bandwidth adversely. Equation (3.1) shows the equivalent resistance at node V_x in Figure 3.1 (similar to [21]) without considering R_M.

$$Rx_{eq} = \frac{1}{g_{m,1A} \times g_{m,2A} \times r_{O,1A}} \tag{3.1}$$

Also, a low resistance at this node results in lower voltage variation which improves the linearity as well. In other words, if the voltage variation at the source of M_{1A} was large, it could change the biasing point of the circuit very much. Consequently, a modification is applied to this circuit to prevent M_{2A} from going into triode region which is discussed later.

The voltage, V_x-V_y, produces a current, I_R (Figure 3.1) and one can derive the following equation:

$$I_1 - I_2 = (I_{B1} + I_R) - (I_{B1} - I_R) = 2I_R \tag{3.2}$$

Transistors M_{2A} and M_{5A} in Figure 3.1 behave like a current mirror and their currents are proportional to their aspect ratios. For simplicity we can assume that the aspect ratios are equal.

The current, $2I_R$, finally appears in the output branches. The difference in the output branches' currents, I_{o+} - I_{o-}, is proportional to $2I_R$. Assuming equal aspect ratios for M_{2A} and M_{5A} in Figure 3.1 and referring to (3.2) we have:

$$I_{O+} - I_{O-} = I_1 - I_2 = 2I_R \tag{3.3}$$

Finally we can obtain the transconductance (G_m) as a function of R_M.

$$(I_{O+} - I_{O-}) \quad \alpha \quad 2I_R \approx \frac{V_{id}}{R_M} \tag{3.4}$$

$$G_m = \frac{(I_{O+} - I_{O-})}{V_{id}} \quad \alpha \quad \frac{1}{R_M} \tag{3.5}$$

In the circuit of Figure 3.1, the value of G_m is not tuned with any special signal yet. One way of controlling the resistance could be using a transistor operating in triode region while the gate voltage is the tuning voltage. This is shown in Figure 3.2. In [21], another possibility to implement R_M is introduced which is more complicated and consumes more area.

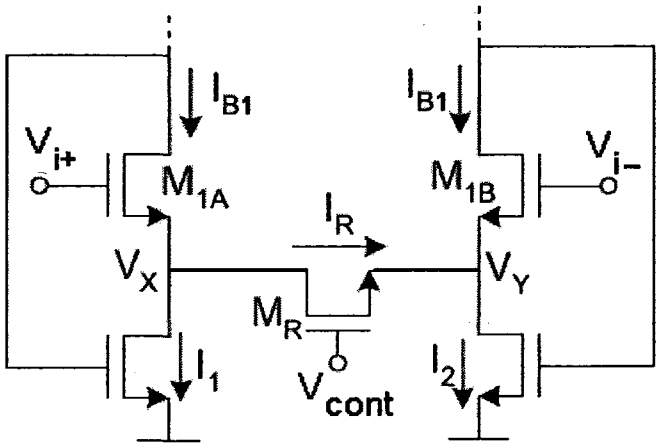

Figure 3.2 Replacing R_M with NMOS transistor, based on [16]

In Figure 3.2 an NMOS transistor operating in triode region is used instead of the resistor R_M. In this configuration, V_{cont} defines the current I_R. Finally, the total G_m becomes a function of V_{cont}, the gate voltage of M_R.

To improve linearity and symmetry [16], the transistor M_R is substituted by two parallel NMOS transistors (i.e., M_{R1} and M_{R2} in Figure 3.3) to replace the resistance R_M of Figure

3.2. Also, the total resistance can get smaller which means a higher pole and higher bandwidth.

Figure 3.3 shows the schematic with the resistor implementation. The constant current flowing into M_{3A} keep $V_{SG,M3A}$ constant. Hence, $V_{GS,MR1}$ remains constant as V_x changes. In this way, the resistance of M_{R1} is kept unchanged and this improves the linearity, as well.

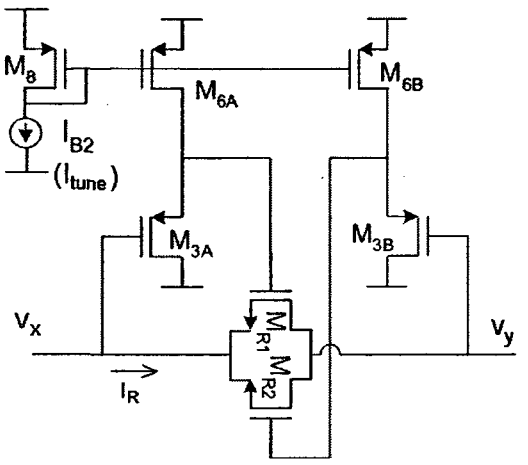

Figure 3.3 Voltage controlled resistor using triode FETs based on [16]

In this Figure, the transistors $M_{3A,B}$, $M_{6A,B}$ and M_8 are used to pass on the control signal (I_{tune}) to the gates of M_{R1} and M_{R2}. I_{B2} (I_{tune}) is the control signal which defines the gate-source voltages of M_{R1} and M_{R2}. Hence, I_R and the output current (referring to (3.3)) are defined. Similar to [16] the following equations show how G_m is derived.

$$V_{id} \approx V_{DS,MR1,2} = Vx - Vy \tag{3.6}$$

$$I_R \approx 2 \times K_n (W/L)_{MR1,2} [(V_{GS,MR1,2} - Vt) V_{id} - .5 V_{id}^{\ 2}] \tag{3.7}$$

Referring to Figure 3.1 and (3.3), we derived the output current equal to $2I_R$. It is worth mentioning again that the assumptions and equations used for the left half of the circuit are true for the right side too.

$M_{6A,B}$ have the same aspect ratios as M_8. This means, I_{tune} gets mirrored and flows through $M_{3A,B}$. In this way, the gate-source voltage of $M_{3A,B}$ is equal to that of $M_{R1,2}$:

$$V_{GS,MR1,2} = V_{SG,M3A,B} \tag{3.8}$$

Therefore, changes in I_{tune} result in changes in V_{GS} of $M_{R1,2}$. (3.9) shows the relation between I_{tune} and V_{GS} of $M_{R1,2}$.

$$I_{tune} \approx 0.5 \times K_p (W/L)_{M3A,B} (V_{GS,MR1,2} - V_t)^2 \tag{3.9}$$

W and L in the above equation are width and length of the transistor, respectively. V_t is the threshold voltage and K_p is the intrinsic transconductance which is equal $\mu_p C_{ox}$. Solving for $V_{GS,MR1,2}$ in (3.7) and putting the result into (3.9), we can derive the output current $I_{O,d}$:

$$I_{O,d} = 4K_n \left(\frac{W}{L}\right)_{MR1,2} \sqrt{\frac{2I_{tune}}{K_p \left(\frac{W}{L}\right)_{M3A,B}}} \times V_{id} \tag{3.10}$$

$$G_m = \frac{I_{O,d}}{V_{id}} = 4K_n \left(\frac{W}{L}\right)_{MR1,2} \sqrt{\frac{2I_{tune}}{K_p \left(\frac{W}{L}\right)_{M3A,B}}} \tag{3.11}$$

Notice that the second order terms are neglected. As shown in (3.11), the total transconductance can be tuned by I_{tune}. The practical ranges for I_{tune} and G_m have to be found out.

However, large changes of the input voltage may slightly change the drain current of the input transistor. This adds some nonlinearity to the circuit as, ideally, variation in V_{i+} is supposed to be equal to that of V_x [16]. Sensitivity to the input common-mode voltage is another drawback of this configuarion [16]. As an example, changes of the input voltage slightly changes the resistance of $M_{R1,2}$ due to the change of their threshold voltage. The gate-source voltages of $M_{R1,2}$ are set by the source-gate voltages of $M_{3A,B}$. Here, $M_{R1,2}$ are NMOS and $M_{3A,B}$ are PMOS transistors. One problem is that the threshold voltages of these transistors do not vary in a similar way over temperature. Figure 3.4 shows the complete OTA schematic which is reported in [16].

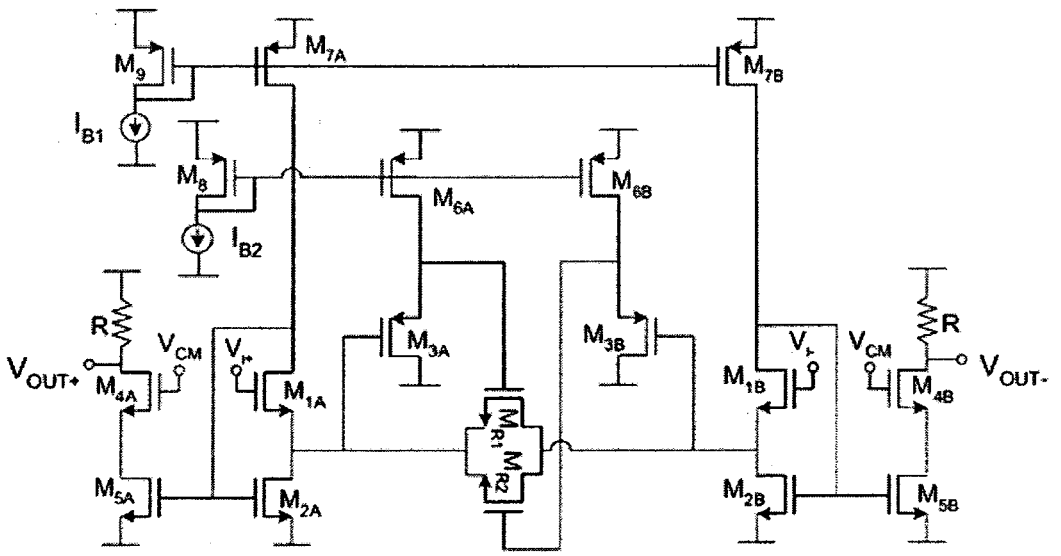

Figure 3.4 Complete schematic of the OTA based on [16]

As another design issue, in order to reduce mismatch, the transistors making current mirrors should be equal in size. It means M_{2A} and M_{2B} should have the same sizing. So do M_{5A} and M_{5B}.

3.2.2 Improvements

In this section, the modifications to the chosen OTA (Figure 3.4) are discussed. Briefly, the output resistors are replaced by active loads. Also, employing NMOS transistors in the OTA circuit the linearity range is increased. In addition, compensation capacitances are employed to guarantee the stability.

As shown in Figure 3.4, on-chip resistors (R) are used at the output nodes. The first change in the circuitry is to replace the resistor loads, R, with PMOS transistors, $M_{RPA,B}$, (Figure 3.5). In this way, the output resistance would be bigger. One can use cascode transistors in the output to achieve a higher output resistance and, hence, a higher gain [21]. Furthermore, this replacement makes the design an only-CMOS one. One advantage could be for those designs in which the output capacitance is important. Thus, for a particular technology if the capacitance of the on-chip resistor is very large, the capacitance of a PMOS transistor in the output, which is an overlap capacitance, is a better choice. Moreover, fabricating a circuit with only CMOS transistors may, in some cases, allow the use of a lower cost fabrication technology.

Further, the signal, V_{bo}, returning from the Common Mode Feedback circuit (CMFB) goes to the gates of these transistors. The circuit of CMFB is explained in the following.

As illustrated in Figure 3.5, the drain of M_{1A} is connected to the gate of M_{2A}. This limits the range of input voltage at the gate of M_{1A}.

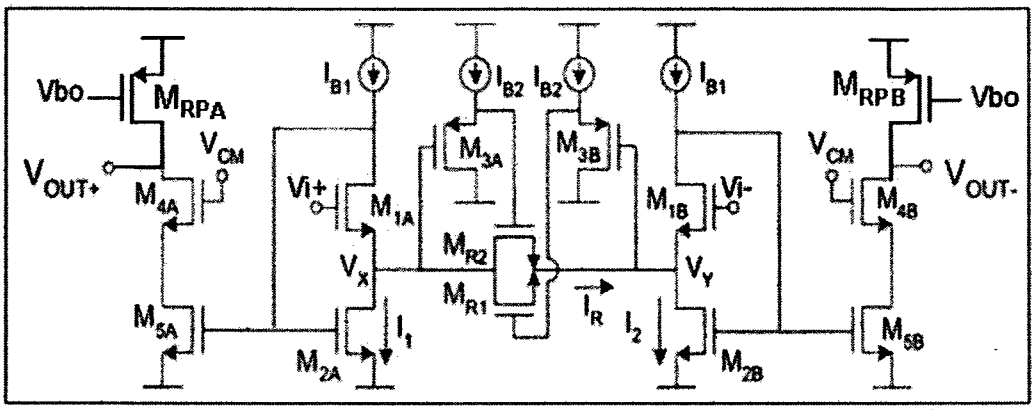

Figure 3.5 Modified OTA by replacing the output resistors with PMOS transistors.

In particular, when V_{i+} significantly goes up, the drain of M_{1A} and, hence, the gate of M_{2A} goes down forcing M_{1A} into triode. On the other hand, when V_{i+} gets very small the gate of M_{2A} goes up which results in M_{2A} working in triode region. Accordingly, the next modification on the chosen OTA is adding the NMOS transistor M_F, as a buffer, similar to what was reported in [24]. The left hand side of the circuit with added M_F is shown in Figure 3.6. The same configuration applies to the right hand side of the OTA. The NMOS transistor M_{Fb} is used to bias M_F.

By adding M_F, there will be a voltage drop between the drain of M_{1A} and the gate of M_{2A}. Notice that these two nodes were connected together before.

Adding M_F rules out the possibility of either transistors, M_{1A} and M_{2A}, becoming off for large inputs. Accordingly, the linearity is improved. Adding M_F introduces one more pole to the circuit. Hence, to diminish this problem, a compensation capacitor, C_C, is added between the gate and the source terminals of M_{FA}, as in [24]. This is shown in Figure 3.7.

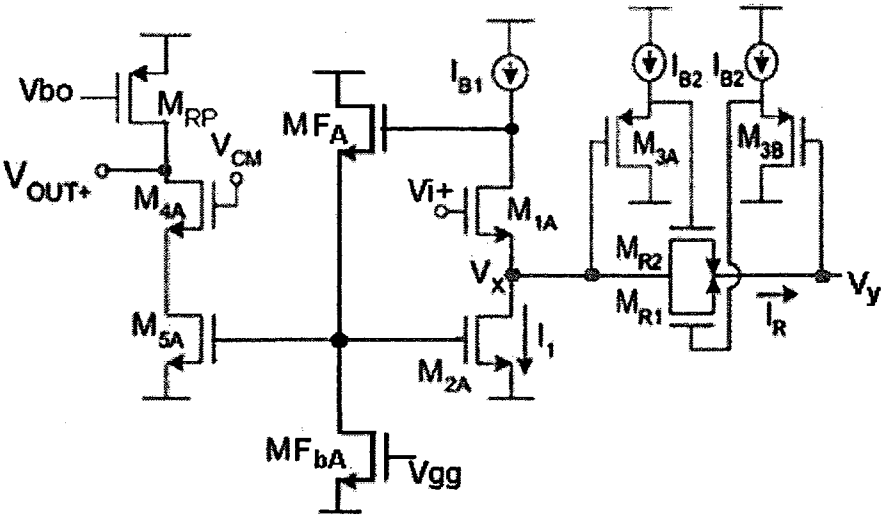

Figure 3.6 Adding MF to the OTA circuit

Consider the created loop by transistors M_{FA}, M_{2A} and M_{1A} in Figure 3.7.

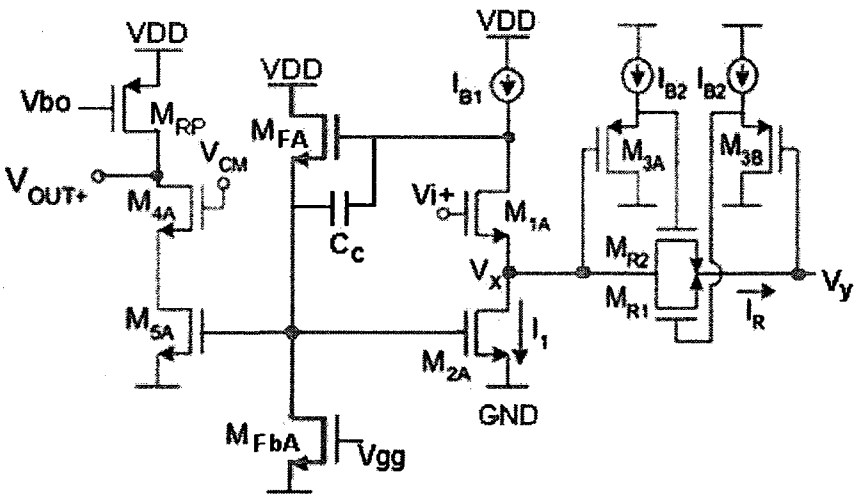

Figure 3.7 Compensation capacitance for the modified OTA

The first dominant pole of this loop is due to the drain of M_{1A} with a total resistance of $r_{O,1A}$. The second pole is due to the gate of M_{2A} with a resistance of about $1/g_{m,MFA}$.

Therefore, the compensation capacitance, C_C, is connected between these two nodes to separate corresponding poles to guarantee the stability.

For the issue of stability for this loop, the non-dominant pole should be larger than the gain bandwidth of the circuit [21]. This condition is satisfied by proper sizing of the transistors and the compensation capacitance. Simulation results also showed the stability.

Implementing the compensation capacitance, C_C in Figure 3.7, is done by using the gate capacitance of an NMOS transistor. Such implementation of the capacitance is common such as in [15]. A complete investigation of such implementation is reported in [25]. In the next chapter, some characteristics of the gate capacitance are investigated.

The gate connection of this NMOS transistor (M_{FA}) is connected to the drain of M_{1A}. The drain and the source connections of this NMOS transistor are also connected to the source connection of M_F. Notice that this new NMOS transistor has enough V_{GS} to form the gate-body capacitance. Lastly, the body of M_{3A} is connected to the source terminal which means wider range for M_{3A} to be in saturation. This resulted in a wider range for I_{tune} while all transistors remain in saturation.

3.2.3 Common-Mode Feedback circuit (CMFB)

The Common-Mode Feedback circuit of Figure 3.8 is used to regulate the OTA's output common-mode voltage.

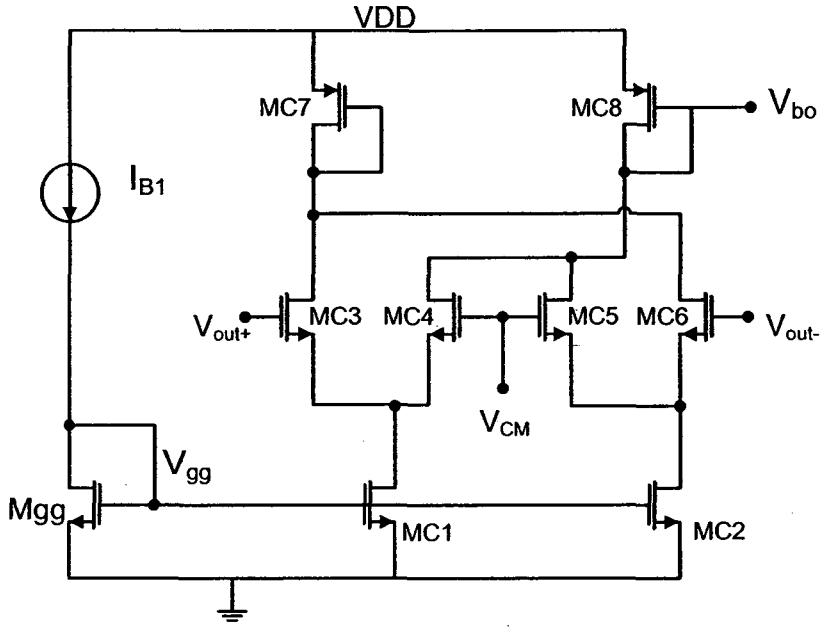

Figure 3.8 Common-Mode Feedback (CMFB) circuit

In the circuit of Figure 3.8, the common mode voltage of the differential input (differential output of the OTA), will be compared with V_{CM}. For instance, if the common mode voltage of V_{out+} and V_{out-} increases, the currents flowing into M_{C3} and M_{C6} get larger. This decreases the currents of M_{C4} and M_{C5} and, hence, M_{C8}. This is due to the fact that M_{C1} and M_{C2} are behaving like constant and equal current sources. Decreasing the current of M_{C8} makes V_{bo} go higher.

Finally, V_{bo} returns to the OTA (to the gate terminal of M_{RP}) to set the DC level of the output voltages, V_{out+} and V_{out-}. In fact, when V_{bo}, the gate voltage of M_{Rp} in Figure 3.5, gets larger in magnitude, the total source-gate voltage of M_{Rp} gets smaller which results in less current flowing to the output nodes. Finally, this will decrease the DC level of the output voltages. The CMFB circuit is also symmetrical. It means M_{C3}, M_{C4}, M_{C5} and M_{C6} have the same sizing. M_{C7} and M_{C8} are also equal. Notice that the CMFB circuit is sensitive to the common mode level of its differential input (V_{out+}-V_{out-}). Differential variation of the OTA's outputs does not significantly change the total current of M_{C6} and M_{C3}. As a result, when there is only differential variation in V_{out+}-V_{out-}, the total current of MC4 and MC5 and, hence, V_{bo} remain constant.

Transistor M_{gg} is put there to make the voltage V_{gg} to feed the biasing transistors such as $M_{C1,2}$ in Figure 3.8 and M_{FbA} in Figure 3.8. Use of such configuration is very common to implement a current source.

Stability of the loop created by the CMFB circuit is considered through the simulations. The pole related to the node V_{bo} sees a resistance as low as 1/gm due to the PMOS transistor, M_{C8}. According to the simulations, this generated high frequency pole does not limit the bandwidth.

In order to reduce mismatch, the transistors making current mirrors should be equal in size. In Figure 3.9 M_{2A} and M_{5A} have the same length as well as M_{7A}. Figure 3.9 shows the circuit of the designed OTA after applying the modifications. It is worth mentioning again that 35 transistors are used to implement the total OTA including the CMFB circuit.

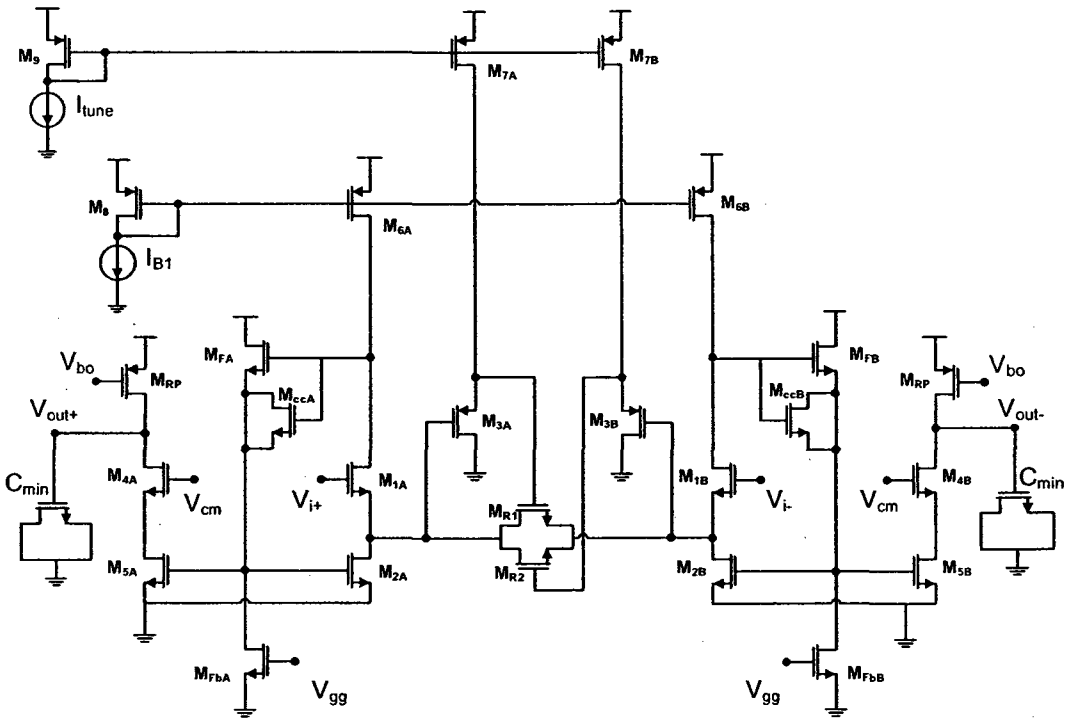

Figure 3.9 Final OTA circuit

3.2.4 Simulations and Comparison

In this section, the widths and lengths of transistors as well as the simulation results of the designed OTA are reported. After that, the results are compared to some other reported works. Notice that, the main objective of our design is to achieve an OTA with large enough transconductance as well as a wide range of controllability. In fact, by wisely controlling the transconductance in an OTA-C filter, the frequency characteristics of the OTA-C filter would be controllable over wider range of temperature variations. The details of such technique for temperature stabilization of OTA-C filters are discussed in the next chapter.

Table 3.1 shows the W/L sizing of the transistors in the OTA circuit of Figure 3.9 and in the associated CMFB circuit (Figure 3.8). The values in this table are reported in micrometers (μm).

Table 3.1 Sizing of transistors making the OTA and its CMFB circuits (μm/μm)

$M_{1A,B}$	5.75/0.8	M_8	0.60/0.1
$M_{2A,B}$	3.12/0.6	M_9	2.20/0.3
$M_{3A,B}$	0.12/0.1	$M_{C1,2}$	1.80/0.2
$M_{4A,B}$	5.32/0.5	$M_{C3,4,5,6}$	0.8/0.25
$M_{5A,B}$	4.90/0.6	$M_{C7,8}$	1.12/0.4
$M_{6A,B}$	0.12/0.1	$M_{FA,B}$	2.5/0.1
$M_{7A,B}$	5.67/0.6	$M_{FbA,B}$	3.0/0.1
$M_{R1,R2}$	0.30/0.1	M_{gg}	1.99/0.41

Employing such transistors for the circuit of our OTA, the following results are obtained. In the following Figures, the tuning current I_t (same as I_{tune}) is swept from 20 μA to 130 μA in five steps (i.e. I_t=20 μA, 40 μA, 70 μA, 100 μA and 130 μA).

In the Figure 3.10 the frequency behaviour of transconductance of the OTA is shown with the I_t (the tuning current) as a parameter. As shown in this Figure, the transconductance does not have a significant change at frequencies lower than 100MHz. This means that the transconductance remains unchanged at frequencies lower than that frequency. In Table 3.2 the total range of G_m as well as other parameters is provided.

To obtain the curves of Figure 3.10, a 1 Ω resistor is connected between the outputs of the OTA. The output current of the OTA is the transconductance due to the fact that the input AC voltage is set to '1'.

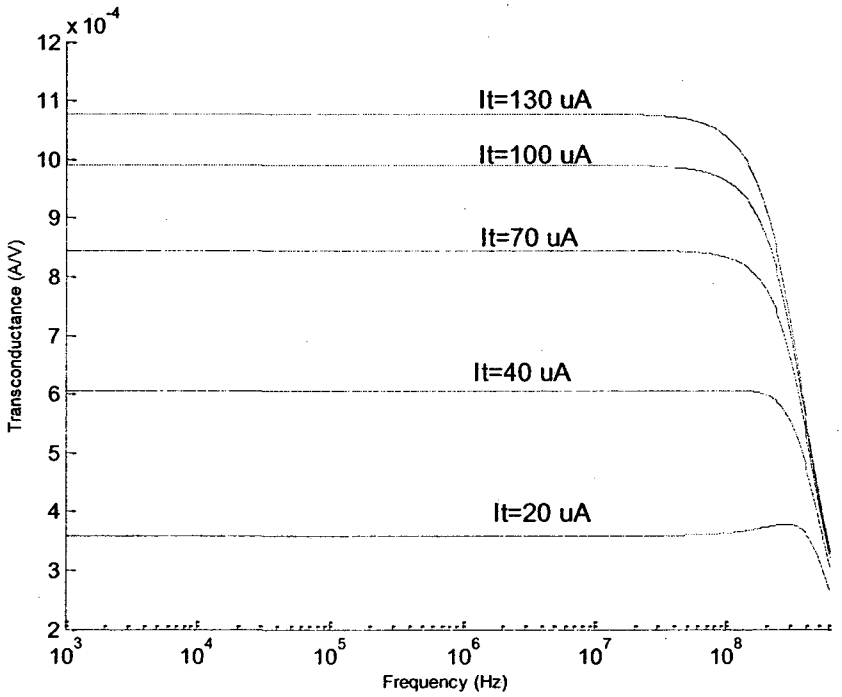

Figure 3.10 Short circuit transconductance vs. frequency with swept tuning current

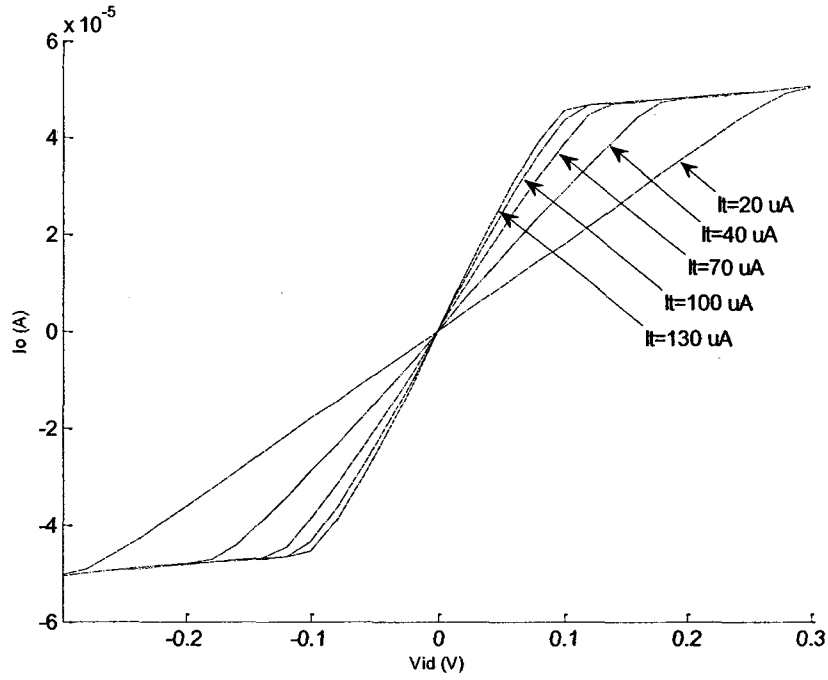

Figure 3.11 I_o vs. V_{id} with swept tuning current

Figure 3.11 represent the large signal characteristics of the designed OTA circuit. The I_{tune} is used as a parameter. As shown in this Figure, the linearity range is dependent upon the It, and the range is wider with smaller value of the I_t. Here, the right-most curve corresponding to I_t=20 μA has the largest linear range.

Figure 3.12 and Figure 3.13 show the Voltage Gain and the Phase response of the OTA in open-loop configuration. As shown, increasing the tuning current increases the transconductance and hence the voltage gain. Although, the unity-gain frequency is increased, the Phase Margin remains above 65 degrees (Table 3.2).

The simulation results are summarized in Table 3.2. Notice that the ranges are obtained as the tuning current varies between 6 μA and 130 μA. In this range, actually, all transistors remain in the saturation region.

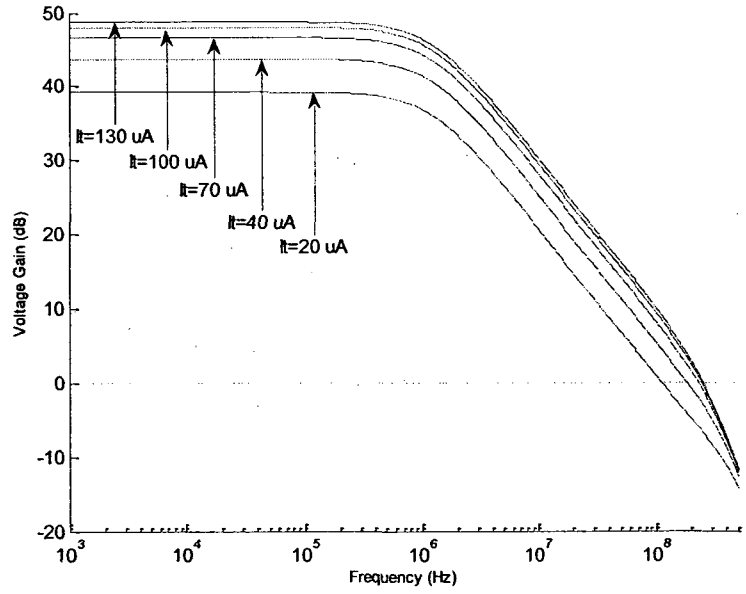

Figure 3.12 Voltage Gain (dB) vs. frequency with swept tuning current

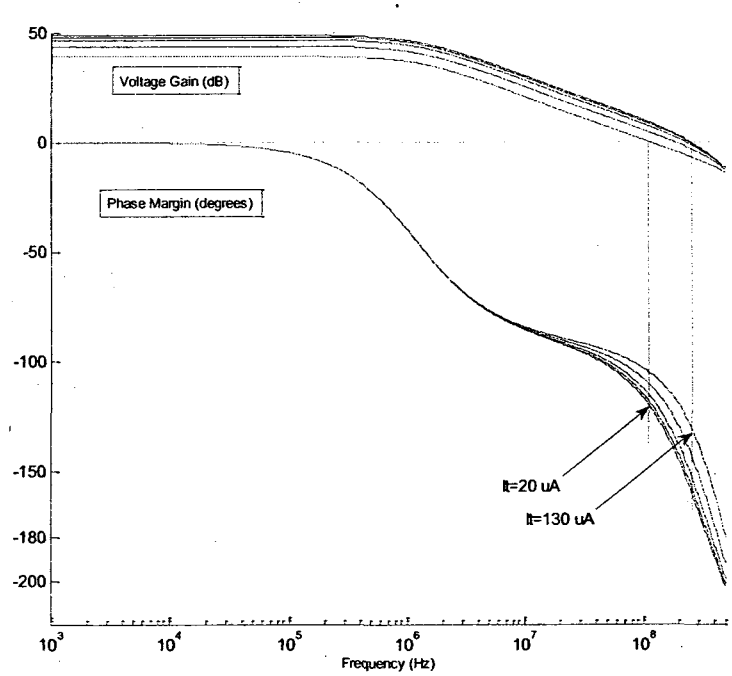

Figure 3.13 Phase Angle vs. frequency with swept tuning current

Table 3.2 Simulation results of the designed OTA

Parameters	Values Range	
Tuning Current (μA)	6	132
Transconductance (μA/V)	131	1078
Voltage Gain (dB)	30.37	48.75
Phase Margin (degrees)	80	65
f_{-3dB} (MHz)	1.21	1.21
f_{Unity} (MHz)	40.14	254.9
Phase Margin (degrees)	80	65
Offset	0.2 mV	
Integrated Input Noise (1-100MHz) @ It=30 μA	113 μV	
Power @ It=30 μA	419 μW	
Technology	STMicroelectronics 90-nm	
Supply Voltage (V)	1.2	

Figure 3.14 depict the noise density of the designed OTA.

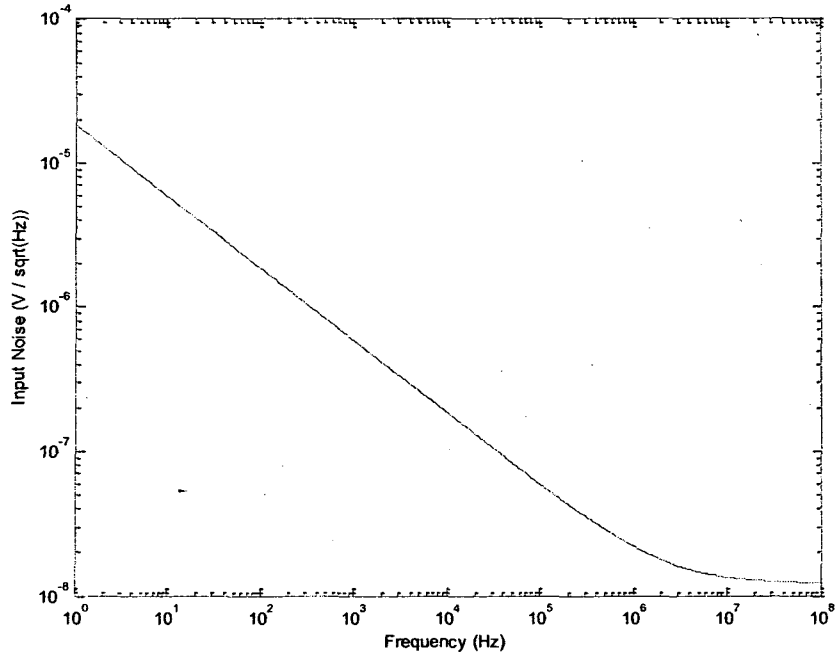

Figure 3.14 Noise density of the designed OTA at It=30 μA

Table 3.3 shows a comparison between this work and some other reported work. It is worth mentioning again that the purpose of designing such OTA was to have a controllable OTA with a wide range of controllability over transconductance.

Table 3.3 Comparison of this work (OTA) with other works

	This work	[26]	[16]	[10]	[11]	[27]	[28]	[29]	[30]
Technology (CMOS)	90 nm	0.18 μm	0.5 μm	0.35 μm	2 μm	0.18 μm	0.18 μm	0.18 μm	1.2 μm
Supply Voltage (V)	1.2	2	2	2.5	5	1.8	2.5	1.5	5
G_m (μA/V)	131 to1078	314-1030	450 to 1000	3 to 30	98 to 396	8 to 131	1161-1423	-	5 to 50
Tuning Current range (μA)	6 to 132	1-150	91 to 350	-	3 to14	-	20 to 300	-	9 to 70
Voltage Gain (dB)	35 to 49	10-23	-	78 to 83	55dB	57	23	15-34	50 to70
Integrated Input Noise (1-50MHz)	90-136 μV	-	-	-	79 to 388 μV	-	-	-	-
Power (mW)	0.38 to 0.56	-	0.92	0.24 to 0.377	2.7	0.581	-	-	7.65
Silicon Area	0.0045 mm^2	-	0.07 mm^2	-	-	-	-	-	-

3.3 Layout and Test Plan

In this section, the test plan as well as the layout of the designed OTA is given. It is worth mentioning that after extracting the layout and repeating all the simulations, the circuit of the OTA is fine tuned to meet the desired specifications, such as right working points.

3.3.1 Test Plan

In Figure 3.15, a block diagram of the fabricated chip including the input and output ports is shown. In the following, the test plan to measure the output voltage is explained. Finally, the layout of the complete designed chip is given.

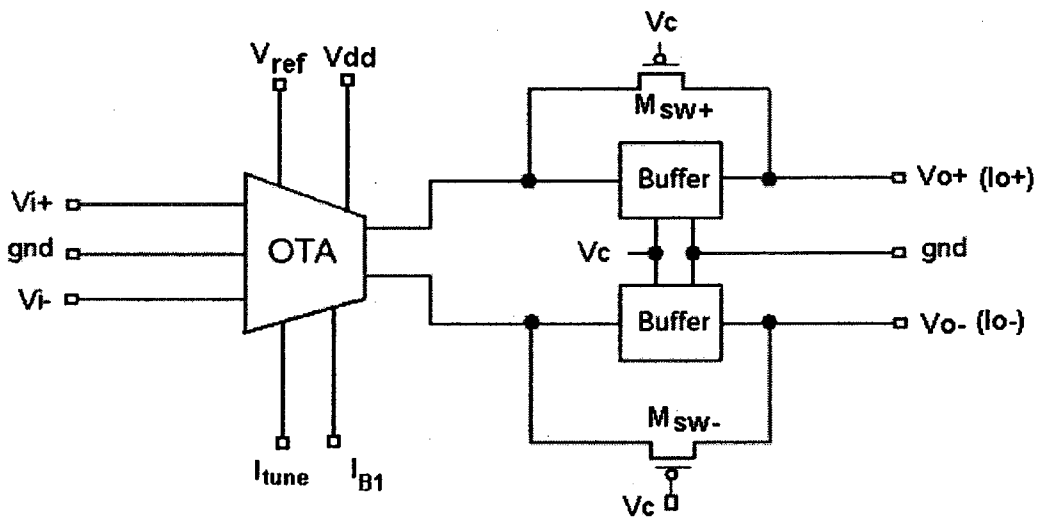

Figure 3.15 Block diagram of the chip

To measure the output voltage, the control voltage, Vc, is set to 1.2 V so that the buffers are in the signal path. The output voltage is measured at Vo+ and Vo-. In the other case, to measure the output current, Vc is set to 0. So, the switch transistors M_{sw+} and M_{sw-} are ON to let the output current of the OTA flow to the output nodes, Io+ and Io- (Figure

3.15). The buffers remain inactive. According to the simulations, the effect of the ON resistances of the switches in the path of output current with Vc=0 V is observed to be negligible. The buffers consist of two-stage voltage amplifiers which are explained in the following.

3.3.2 Output Buffer

The circuit of the output buffer is shown in Figure 3.16. This buffer is a 2-stage voltage amplifier with a compensation capacitance. This amplifier is in a negative feedback configuration. It means, the output is connected to the negative input and the positive input is the actual input of this buffer. In order to have a differential voltage, two of these amplifiers are used.

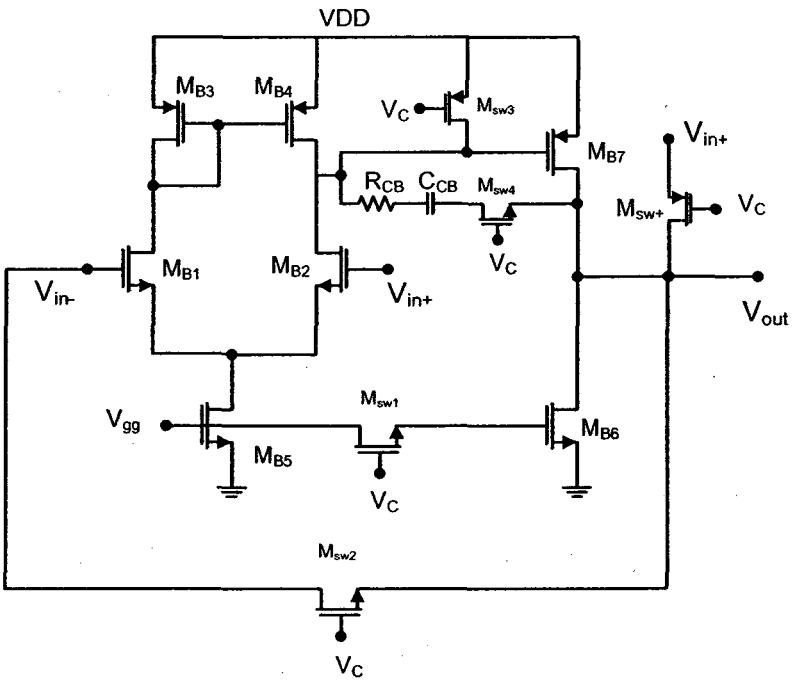

Figure 3.16 Output Buffer

Table 3.4 shows the sizing of the transistors of the output buffer of Figure 3.16. Figure 3.17 shows the voltage gain of the output buffer versus frequency. Bandwidth of this buffer is more than 1.5 GHz. Also, the output resistance of the buffer is shown in Figure 3.18. To have maximum power transfer from OTA to the 50 ohm-probes and also to minimize the reflection from the probe station, the output resistance of the output buffer has to be 50 ohm. Notice that the resistance of the wires in the actual layout will be added to the total output resistance. That is the reason why the output resistance is not exactly 50 ohm. The power consumption of the output buffer is 5.16 mW.

Table 3.4 Sizing of transistors making the OTA and its CMFB circuits (μm/μm)

$M_{1,2}$	12.27/0.3	M_6	80/0.13
$M_{3,4}$	9.47/0.3	M_7	20/0.13
M_5	48.3/0.13	$M_{sw+,-}$ and $M_{sw1,2,3,4}$	5/0.1

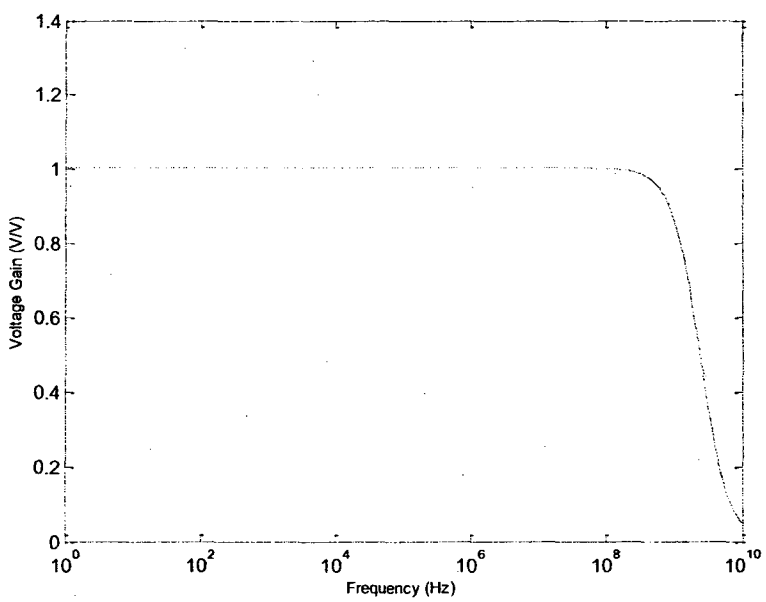

Figure 3.17 Voltage gain of the Output Buffer

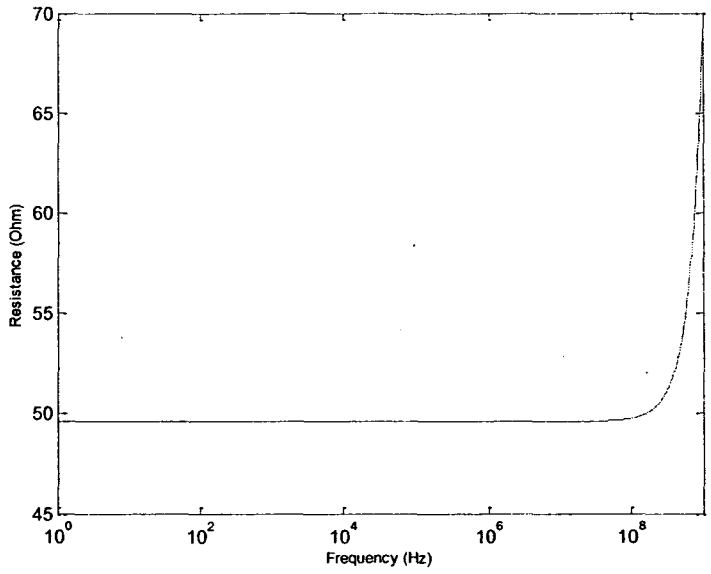

Figure 3.18 Output resistance of the Output Buffer

3.3.3 Layout

Figure 3.19 shows the layout of the designed OTA as well as the output buffers. Notice that the pads are not shown in this layout. The designed layout is successfully extracted and simulated in ST 90nm technology using Spectre-Spice and sent out for fabrication through Canadian Microelectronics Corporation (CMC).

It is worth mentioning that, at the beginning of this project, fabrication was not an objective for the whole project. However, making the layout of the designed circuit and sending it for fabrication granted a beneficial experience.

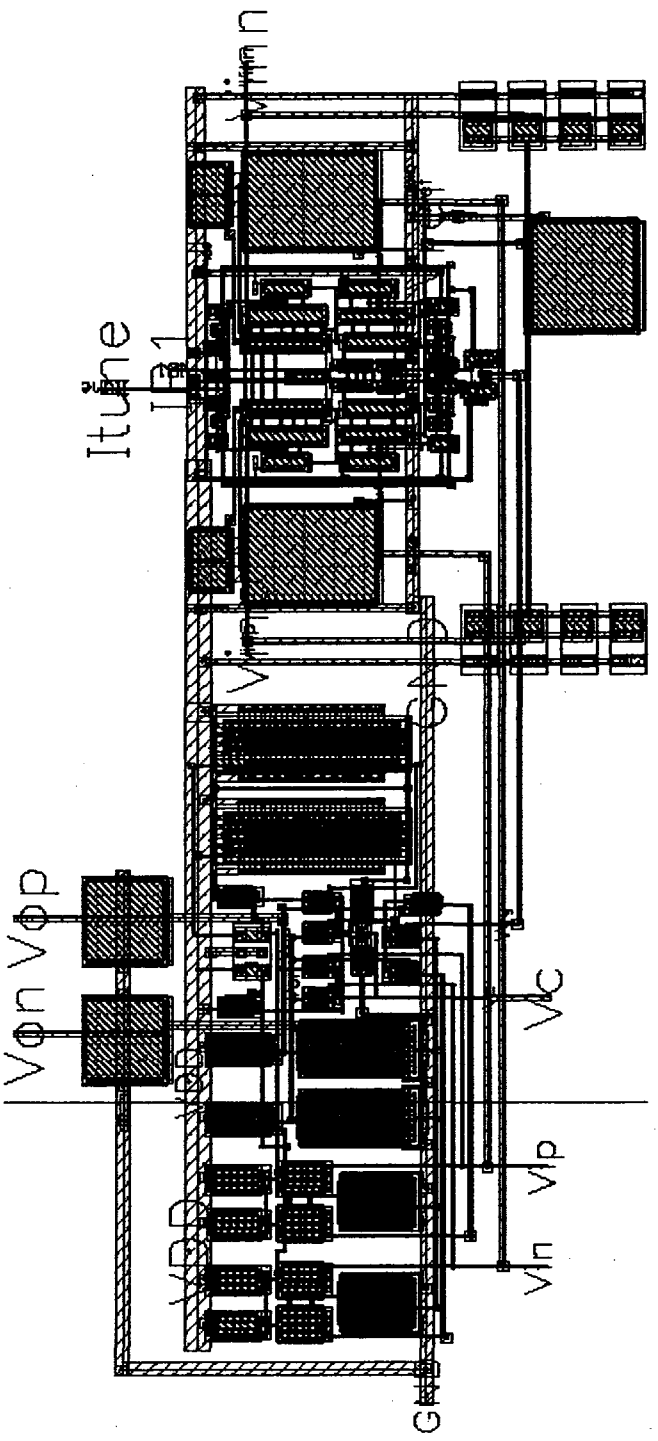

Figure 3.19 Layout of the OTA and Output Buffers (100 × 45 µm)

3.4 Summary

In this chapter steps towards implementation of an OTA from the several OTAs introduced in Chapter 2 have been taken up. The OTA has been implemented in ST 90-nm CMOS technology. The circuit of the CMFB as well as the output buffer has been presented and modifications on the OTA employed to increase the linearity. Finally, the layout of the fabricated chip including OTA and output buffer have been presented. A test plan has also been included. In the following, temperature behaviour of the transconductance and the capacitance is investigated and the proposed temperature compensation technique is presented.

Chapter 4 Temperature Compensation in the OTA-C integrator

4.1 Introduction

As mentioned before in Chapter 2, variation in temperature, process and voltage supply makes the frequency tuning of filters and filter building blocks an important issue for analog designers. In this thesis, frequency characteristics of G_m-C filters with respect to temperature are of interest. Therefore, investigating temperature behaviour of G_m-C filters' components, a technique for temperature compensation for OTA-C filters is proposed and demonstrated by simulation.

The simulation of the corresponding circuits is done in *Cadence* environment. Also, Monte-Carlo simulation is used to show how the design behaves from chip to chip. Monte-Carlo simulation which can be used for physical and mathematical systems is based on random sampling. In other words, values of the corresponding parameters are randomly chosen from their ranges. In [9] a detailed example of how Monte-Carlo simulation works is brought.

In this thesis, Monte-Carlo simulation is used at some points. In each iteration in Monte-Carlo simulation, parameters of transistors such as mobility of charges, gate-oxide

thickness, sheet-resistance, doping levels, transistors dimensions and threshold voltage are randomly varied by the simulator, *Spectre*.

4.2 Temperature dependency of components

The main components of G_m-C filters are G_m, the transconductance, and C, the output capacitance. To control the total temperature behaviour of a G_m-C filter, we need to study the characteristics of each component with respect to temperature. In this Chapter, the temperature behaviour of the G_m-cell and of the output capacitance is investigated. After that, a technique for temperature compensation which is reported in [20] is explained. Finally, the improved and proposed technique is introduced. Simulation results are also given.

4.2.1 Temperature dependence of Transconductance

In this section, the temperature behaviour of the OTA is shown. It should be noted that the designed OTA in previous sections, which was sent for fabrication, has been modified in a way that the departure from linearity is reduced. With an input voltage of 50 mV the departure was 0.021% in previous design which is reduced to 0.011% in the new OTA. In fact, the DC input range of the OTA has to be larger. This issue is explained in the following sections where the new technique for temperature compensation is described. Table 4.1 shows the new sizing for the OTA's transistors.

Based on the new transistors' sizing, the following curves (Figure 4.1) for the total transconductance are obtained.

Table 4.1 New dimensions of OTA's transistors

$M_{1A,B}$	3/0.4	M_8	0.60/0.1
$M_{2A,B}$	2.9/1	M_9	8/1
$M_{3A,B}$	0.12/0.1	$M_{C1,2}$	5/0.3
$M_{4A,B}$	5/0.3	$M_{C3,4,5,6}$	4/1
$M_{5A,B}$	3.4/1	$M_{C7,8}$	1.4/0.1
$M_{6A,B}$	0.12/0.1	$M_{FA,B}$	2.5/0.1
$M_{7A,B}$	7.3/1	$M_{FbA,B}$	3.0/0.1
$M_{R1,R2}$	0.30/0.1	M_{gg}	1.99/0.4

The transconductance changes as a function of the tuning current. Figure 4.2 shows the variation in transconductance at different temperatures.

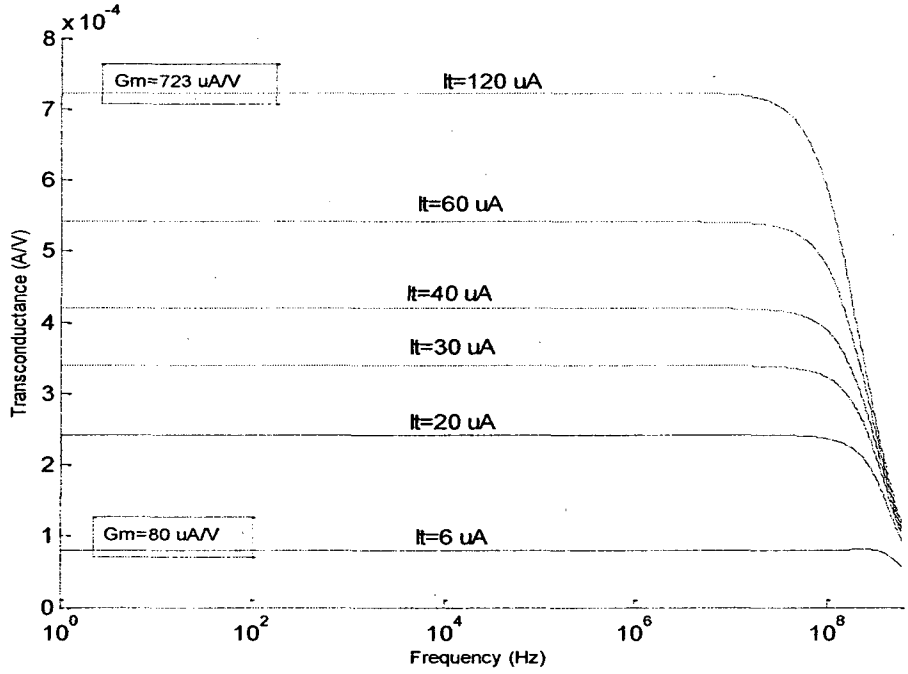

Figure 4.1Transconductance vs. Frequency for different tuning currents at 27 °C

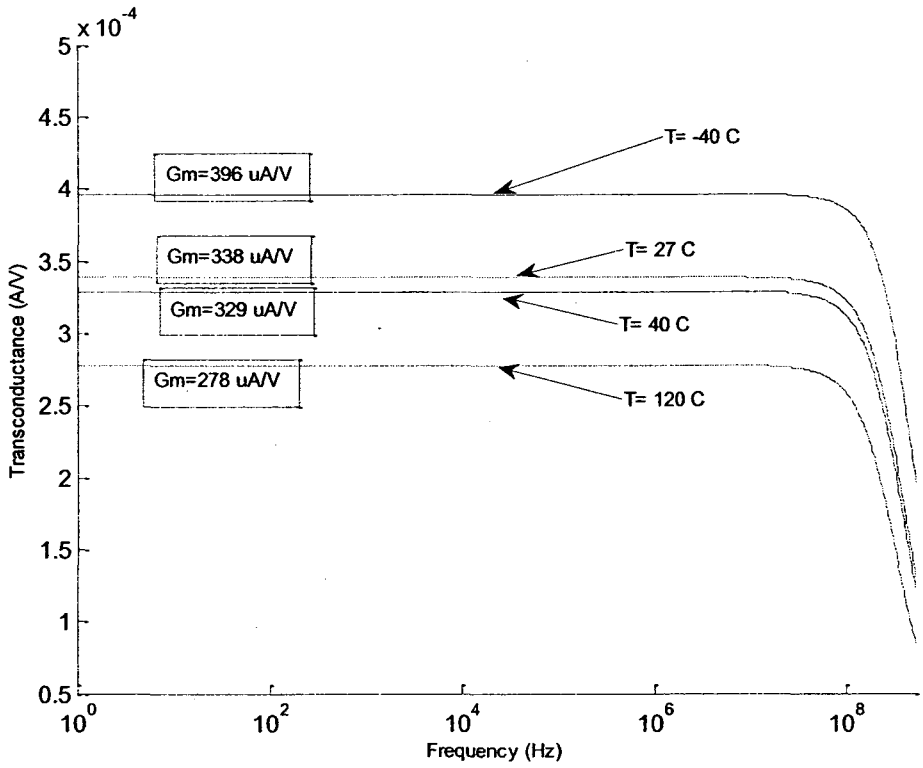

Figure 4.2 Variation in transconductance for three temperatures at I_{tune}=30μA

As shown in Figure 4.2, the variation in transconductance is approximately 35.87% over 160 degrees (0.22 %/°C or 2242 ppm/°C). Notice that a rise in temperature makes G_m get smaller.

Using such a transconductance amplifier results in a huge variation in unity-gain frequency of a simple integrator, for example, as temperature varies. The unity-gain frequency of an OTA-C integrator is determined by the ratio G_m/C, as mentioned before. Therefore, in an ideal case, when the output capacitance has no temperature dependency, variation of the unity-gain frequency follows the variation of the transconductance.

Consequently, we need to control the transconductance such that the unity-gain frequency remains constant. Therefore, the temperature characteristics of both transconductance and

output capacitance have to be investigated. In the following section, temperature behaviour of the output capacitance is investigated.

4.2.2 Temperature dependence of Capacitance

G_m-C filters frequently use MOSFETs as grounded capacitors, such as in [15]. Such implementation of capacitance is used in this thesis, as well. A simple circuit like the one in Figure 4.3 is used to study how the capacitance changes at different temperatures, frequencies and biasing voltages in simulation.

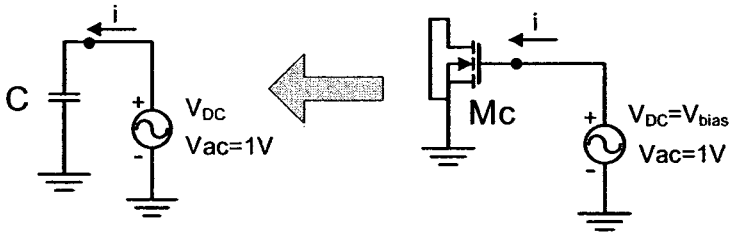

Figure 4.3 Test Circuit to observe the capacitance dependency on temperature

In this circuit, we are looking at the input current of the gate of the transistor while applying an AC input voltage with amplitude of one volt.

Hence, Setting Vac to 1V we have $|i|=|\ Vac\ |\times|j.\omega.C\ |=|2.\pi.f.C|$. Then one can simply solve for C as follows:

$$|C| = \frac{|i|}{2\pi \cdot f} \tag{4.1}$$

Here, the behaviour of this capacitance is investigated over different parameters such as biasing voltage, frequency and, more importantly, temperature.

Figure 4.4 shows the gate capacitance versus the biasing voltage, V_{bias}, at three different temepratures. To implement this circuit, 12 parallel NMOS transistors with W/L=10/7 are used. This configuration is actually used for the output capacitance in the final implementation explained in the following sections.

For a small V_{bias} the depletion region at the gate of transistor is not formed completely and this results in a voltage dependent capacitance. For example, as shown in Figure 4.4, for a small V_{bias}, such as 250 mV, the capacitance is changing significantly with voltage.

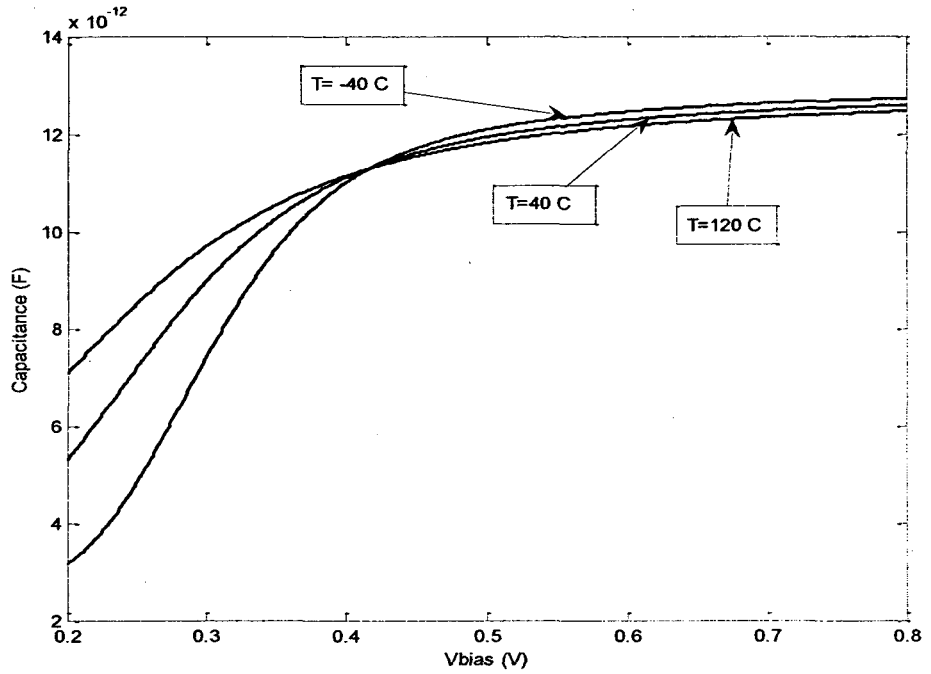

Figure 4.4 Capacitance vs. V_{bias} at T= -40, 40 and 120 °C

However, for a larger V_{bias} the change is not substantial, but a trend of C(-40°C) > C(40°C) > C(120°C) is observed. In other words, as we increase the temperature, C is decreased. At low bias voltage the trend is reversed. In other words, the capacitance looks more stable and less voltage dependent for a large V_{bias} such as 600 mV. Therefore,

biasing the NMOS transistor in the Test Circuit of Figure 4.3 at a voltage around 600 mV (i.e., maintaining V_{GS} around 600 mV) can help us understand the behaviour of the capacitance with temperature changes somewhat independent of the bias voltage.
Notice that the point at which all three curves cross could be a good biasing point in order to have a temperature independent capacitance. However, this issue is not discussed in this project since the capacitance is highly voltage dependent at this point.

Table 4.2 shows the temperature dependency of the MOS capacitance at frequencies below 100MHz. In particular, the transistor has a sizing of W/L=20μ/2μ and the temperature is swept from -40 °C to 120 °C. The technology in which the transistor is simulated is STMicroelectronics 90-nm.

Table 4.2 Dependency of capacitance on frequency

Frequency	Swept Temp. (°C)	V_{GS} (V)	Δ|i| (A)	ΔC (F)
1MHz	-40 to 120	0.8	76.9n	.122f
		0.6	87.5n	.107f
10MHz	-40 to 120	0.8	769n	.122f
		0.6	875n	.107f
100MHz	-40 to 120	0.8	7.69u	.122f
		0.6	8.75u	.107f

Referring to Equation (4.1), the obtained difference in capacitance (ΔC) due to the temperature variation is equal in all cases. This ensures the frequency independence of

the output capacitance when V_{GS}=0.6, for example. Temperature behaviour of the output capacitance is illustrated in Figure 4.5.

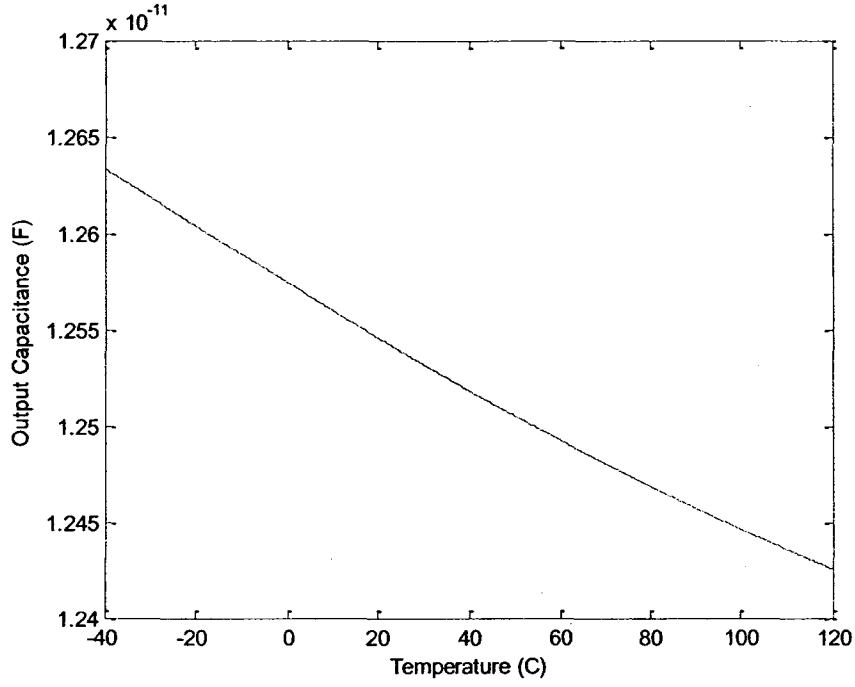

Figure 4.5 Variation in gate capacitance vs. temperature

As shown in Figure 4.5, the variation of the total capacitance is 2.41% over 160 °C. The total capacitance at 27 degrees is 12.5 pF. It is worth reiterating that the total input capacitance of gate connections of 12 parallel NMOS transistors with W/L=10μm/7μm is used for simulation. This sizing is actually the same sizing used for the output capacitance in the final implementation of the integrator for which the new proposed technique in this thesis has been used for temperature compensation.

The total capacitance as a function of temperature can be expressed as [5, page 116] (keeping up to linear term (T-T_0)):

$$C(T) = C_0[1 + \alpha_C(T - T_0) + ...] \tag{4.2}$$

where C_0 is the capacitance at T_0 and the first-order temperature coefficient of the capacitance, α_C, is:

$$\alpha_C(T_0) = \frac{dC/dT}{C(T_0)} \tag{4.3}$$

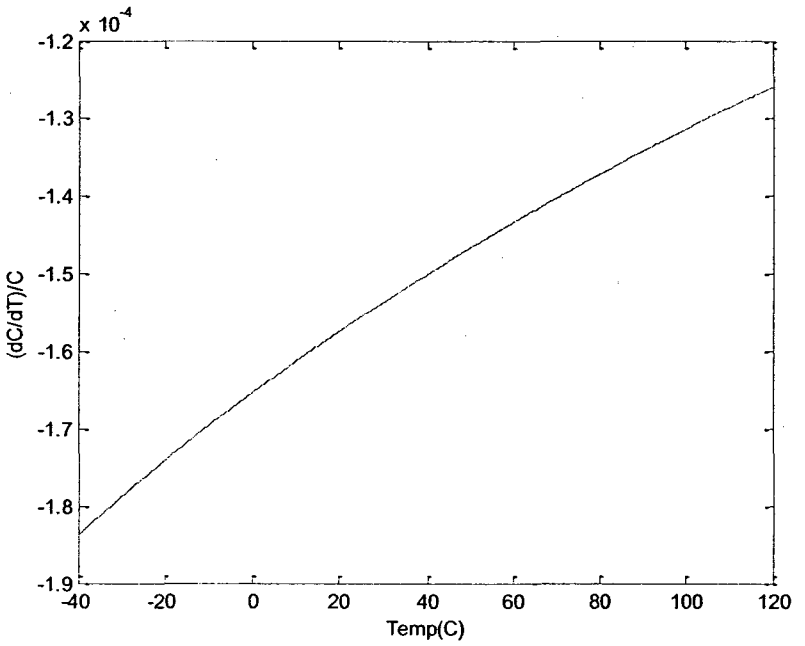

Figure 4.6 Nominalised value of α_C = (dC/dT)/C vs. Temperature (°C)

The temperature coefficient (TC) of our capacitance is -152 μ at 27 °C (Figure 4.6). If the curve of the capacitance (C) versus temperature (T) was a straight line in Figure 4.5 or, equivalently, if the curve in Figure 4.6 was a flat line with value of -152 μ, then we could simply multiply 152 (μ/°C) by 160 (°C) to get the value 2.43 %. According to the simulation results, as shown in Figure 4.5, the variation in the gate capacitance is 2.41 %. Notice that this value can vary depending on the capacitor's biasing voltage.

The Test Circuit is also simulated 100 times using Monte-Carlo simulation to see the difference in the temperature coefficient from chip to chip. Figure 4.7 shows the

magnitude of α_C for 100 iterations for temperatures from -40 to 120 °C. From this Figure, we can see that all curves are crossing near 152 μ/°C at 27 °C. Figure 4.8 illustrates the values of temperature coefficients at room temperature for each iteration.

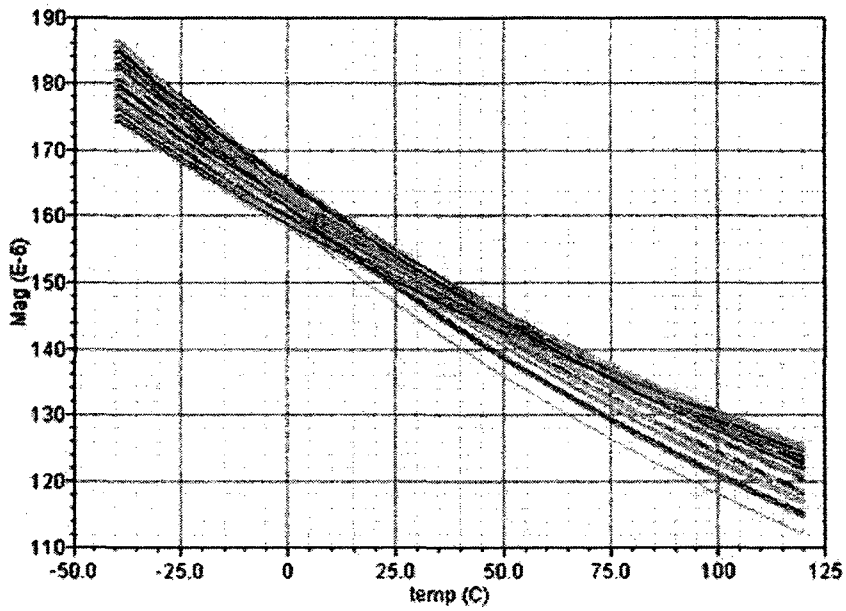

Figure 4.7 Absolute values of α_C vs. temperature for 100 iterations

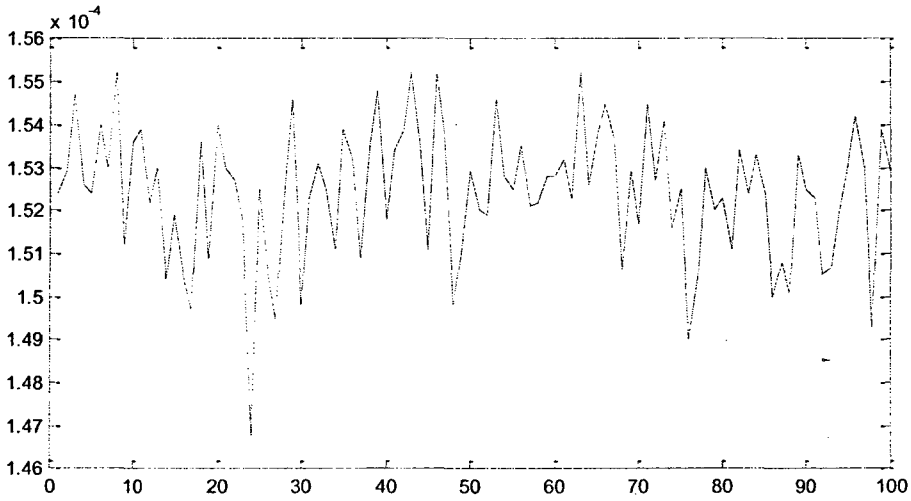

Figure 4.8 Temperature coefficient of the capacitance at 27 °C for 100 iterations.

The distribution of the values of α_C (shown in Figure 4.8) at 27 °C is shown in Figure 4.9. The values are around the average of 152μ with a standard deviation of σ_N =1.5μ.

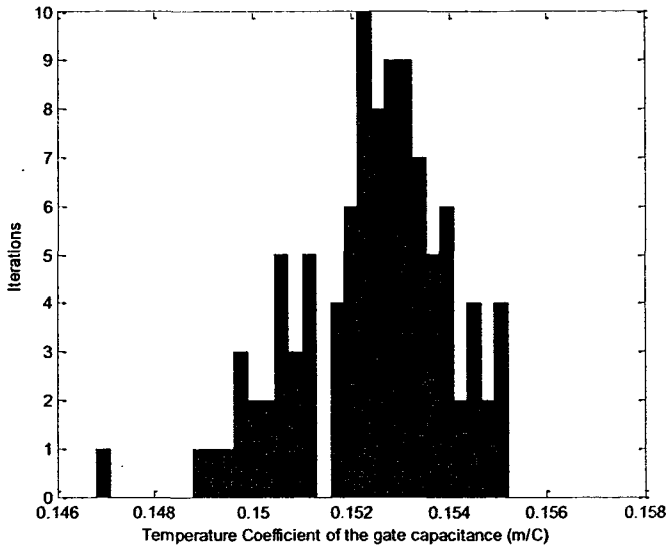

Figure 4.9 Distribution of the magnitude of the TC of the gate capacitance (in m/°C) for 100 iterations of Monte-Carlo Simulation at 27 °C. Actual values are negative.

As a result, we can take the average value of the temperature coefficient, (α_C = -152 μ/°C), for our calculation.

4.3 Temperature Compensation Technique

As mentioned in Chapter 2, in [20] the value of transconductance is locked to a resistance to keep it unchanged with respect to temperature. In this section, after an initial introduction of the technique, different possibilities for available resistors to which we intend to lock the transconductance are studied. After that, the proposed technique is described.

4.3.1 Basic Theory

The unity-gain frequency (f_U) of a G_m-C integrator (an Operational Transconductance Amplifier loaded with a Capacitor) is determined by the ratio of the total Transconductance over the output Capacitance ($f_U = 1/2\pi \times G_m/C$).

These components can be expressed in terms of temperature [5, page 116]:

$$C(T) = C_0[1 + \alpha_C(T - T_0) + ...] \tag{4.4}$$

$$G_m(T) = G_{m0}[1 + \alpha_g(T - T_0) + ...] \tag{4.5}$$

Neglecting second and higher order terms, one can derive the following equation:

$$\frac{df}{dT} = \frac{(\frac{dG_m}{dT} \times C - \frac{dC}{dT} \times G_m)}{C^2} = \frac{dG_m}{dT} \times (\frac{1}{C}) - \frac{dC}{dT} \times (\frac{G_m}{C^2}) \tag{4.6}$$

Dividing both sides of (4.6) by '$f = 1/2\pi \times G_m/C$', the temperature coefficient (TC) of the unity-gain frequency can be derived as:

$$\alpha_f = \frac{1}{f}\frac{df}{dT} = \frac{C}{g_m}\frac{d(G_m/C)}{dT} = \frac{dG_m}{dT}\frac{1}{G_m} - \frac{dC}{dT}\frac{1}{C} = \alpha_g - \alpha_C \tag{4.7}$$

where α_g and α_C are the first order temperature coefficients (TCs) of G_m and C [5, page 116], respectively. Therefore, in order to have a frequency characteristic with zero dependency on temperature ($\alpha_f = 0$), the TCs of the transconductance and the capacitance must be equal, i.e. $\alpha_C = \alpha_g$. Consequently, the ratio of G_m/C will be constant as

temperature varies. Figure 4.10 shows the basic feedback loop for locking G_m to a resistance R as was already introduced in Chapter 2.

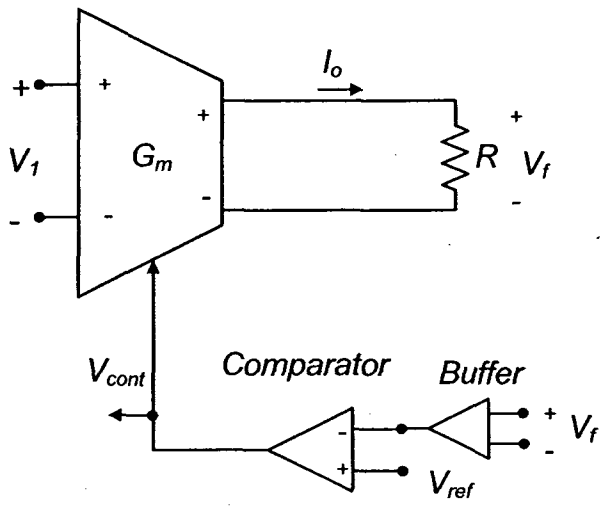

Figure 4.10 Basic control loop for locking G_m to resistance R based on [16]

Similar to (4.2), the resistance R can be expressed as:

$$R(T) = R_0[1 + \alpha_R(T - T_0) + ...] \tag{4.8}$$

where R_0 is the resistance at T_0 (27°C) and α_R is the first-order TC of R. Referring to (2.3), we can derive α_g, the TC for G_m:

$$\alpha_g = \frac{1}{G_m}\frac{dG_m}{dT} = -\frac{1}{R}\frac{dR}{dT} = -\alpha_R \tag{4.9}$$

This equation shows that choosing a resistor with desired temperature behaviour can lead us to the desired α_g. Thus, we need a resistor which has a TC of α_R = -α_C. In this way, α_g and α_C are equal and this results in α_f=0. Therefore, we need to investigate some characteristics of available resistors, which are described in the following sections.

4.3.2 Locking G_m to different resistors

Figure 4.11 (a) shows the more complete circuitry for the control loop of Figure 4.10. For a better understanding, a box called "Resistor Box" is used which is connected to the output of the OTA.

As a first step, an ideal temperature-independent resistor, R, is employed inside the resistor box (Figure 4.11 b). The output of the resistor box, V_f, is compared with the reference voltage, V_{ref}, to generate the control signal, V_{cont}. Finally the control signal goes to the main OTA-C filter.

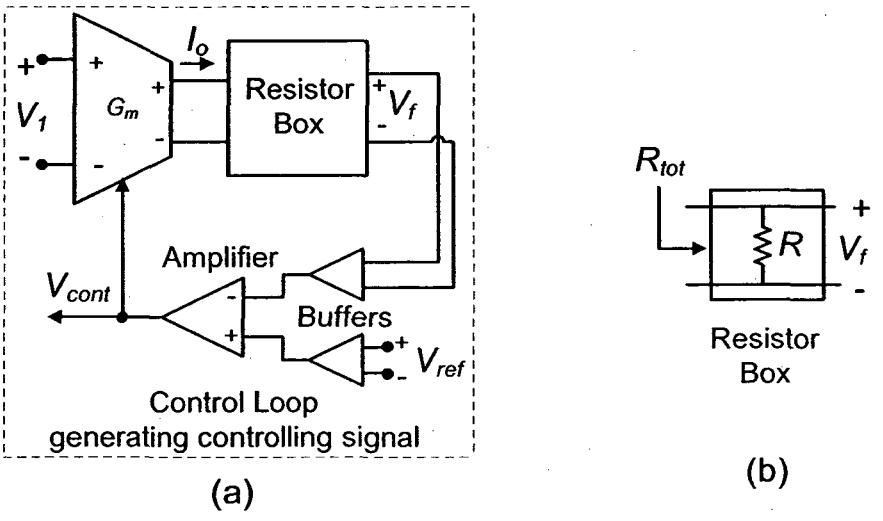

Figure 4.11 a) Control loop for G_m based on [16] b) Resistor Box with ideal resistor

As mentioned before, if the comparator amplifier has an infinite gain, then, V_f would be set to V_{ref} and the value of G_m would be locked to 1/R, referring to (2.3). As the ideal resistor does not change with temperature, the value of G_m is supposed to be constant and, hence, has no temperature dependency. In other words, $\alpha_g = \alpha_R = 0$. Zero TC for G_m

could be a good achievement if the α_C was zero. In that case, the temperature coefficient of the unity-gain frequency of the G_m-C integrator (f_U) will be zero:

$$\alpha_f = \alpha_g - \alpha_C = 0 - 0 = 0 \tag{4.10}$$

It is worth mentioning again that $\alpha_C \neq 0$ (Figure 4.5). According to this change, it is not appropriate to use an ideal resistor with $\alpha_R = 0$ (if such a component existed) for G_m to be locked to. In addition, the temperature coefficient of the capacitor changes with respect to temperature. This variation can cause some error as well. In order to have a more realistic simulation, we used an ideal resistor with nonzero temperature coefficient. As shown before, G_m is proportional to 1/R. Also, G_m and C have to behave similar to each other with respect to temperature. Taking the inverse of the capacitance as Y = 1/C, one can say that the functions Y and R should behave similar to each other w.r.t temperature.

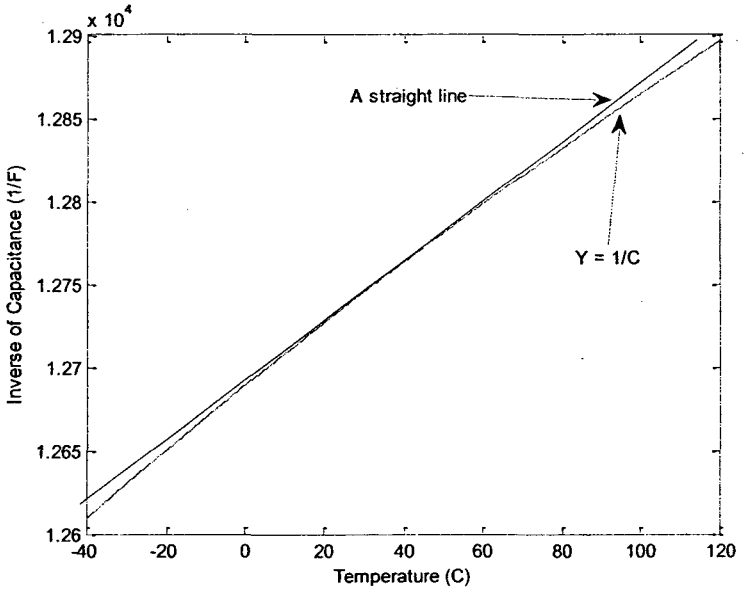

Figure 4.12 Inverse of Capacitance, Y.

As shown before in Figure 4.5, the Capacitance's curve versus temperature is not a straight line. The curve of 1/C is not a straight line either (Figure 4.12). We can detect a

small amount of second order variations with temperature. This means that the resistance to which G_m is to be locked has to have at least a first and a second order TC, say, TC1 and TC2, respectively. According to simulation results, choosing TC1=100 μ/°C and TC2= -10 n/°C2 results in 0.19% change in the unity-gain frequency over 160 °C. Notice that the reason for choosing the above values for TC1 and TC2 is only to show how a resistor with suitable set of TCs could result in small variation in f_U. . Table 4.3 shows the variation in f_U from -40 to 120 °C for the mentioned case.

Table 4.3 Variation in f_U for ideal resistor with TC1 and TC2

T (°C)	-40	0	27	40	80	120
f_U (MHz)	5.213	5.217	5.218	5.218	5.22	5.223

Notice that the variation of 0.19% in f_U is obtained by dividing the difference of the maximum and the minimum frequencies by the average frequency.

The results of employing ideal resistors with zero and non-zero TCs were discussed above. We could get an idea of the temperature characteristic of the resistor to which we intend to lock the transconductance device such that the G_m-C integrator's unity gain frequency remains constant over a wide range of temperature variations. Now, we employ real resistors inside the loop. One kind of available resistor in STMicroelectronics 90-nm technology is a Poly-Silicon resistor called "*rnporpo*" for the N-type as well as "*rpporpo*" for the P-type. Figure 4.13 shows how these resistors with nominal values of 1.5 kΩ change over temperature. Further, Figure 4.14 shows the temperature coefficients of these resistors. In [31], characteristics of integrated resistors in CMOS technologies are investigated in detail.

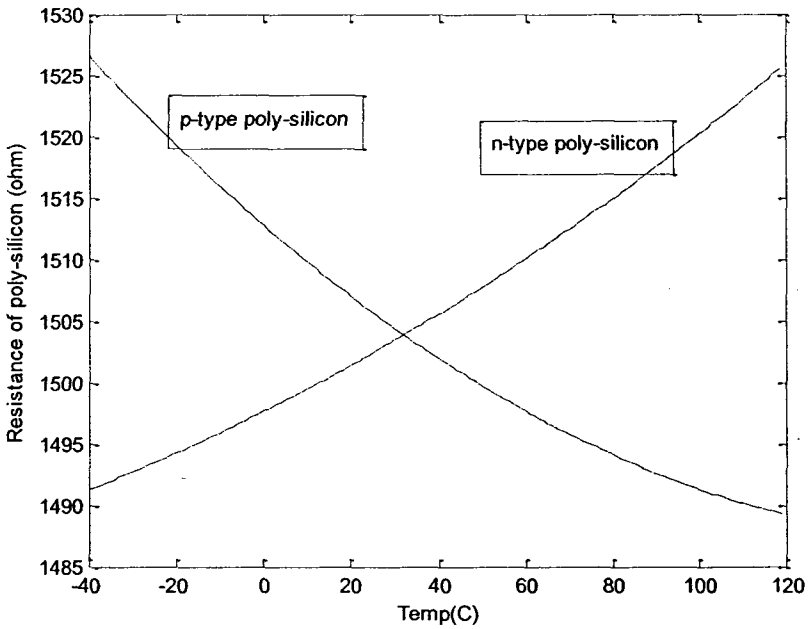

Figure 4.13 Two Poly-silicon resistances vs. temperature

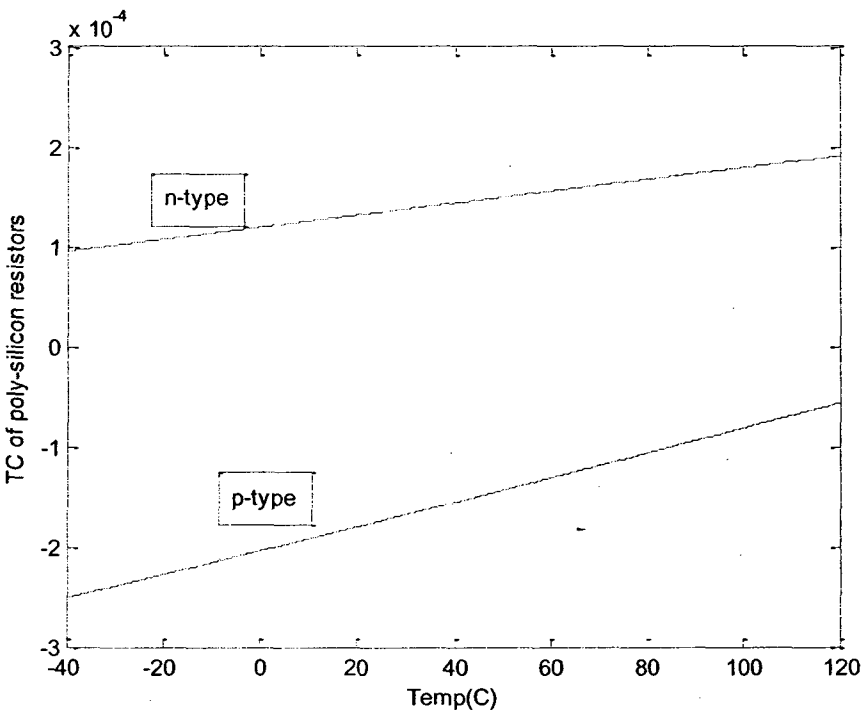

Figure 4.14 Temperature Coefficients of two Poly-Silicon Resistors

As mentioned before, the change in the resistance has to be similar to the change in the inverse of the capacitance. In addition, referring to (4.9), the TC of the chosen resistor has to be positive in order to obtain a negative TC for G_m. In this case, the N-type poly-silicon resistor could be a good choice.

Figure 4.15 shows the normalized variations of the N-type Poly-Silicon resistor and the inverse of our Capacitance, Y. Normalized variations are calculated using the following expressions:

$$Y_{NORM} = \frac{Y(T) - Y(25)}{Y(25)} \tag{4.11}$$

$$R_{NORM} = \frac{R(T) - R(25)}{R(25)} \tag{4.12}$$

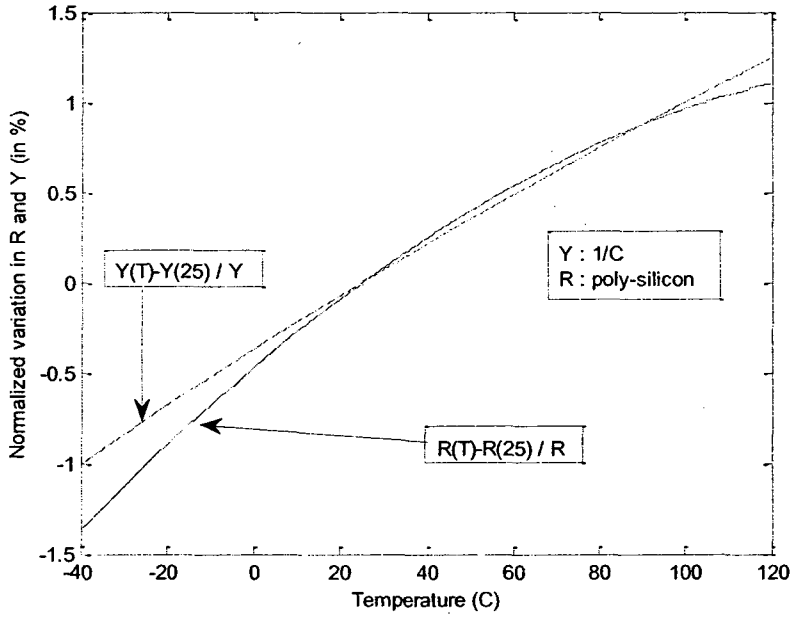

Figure 4.15 Normalized variation of R, the poly-silicon resistance and Y, the inverse of the Capacitance

According to the above simulation results, the best available on-chip resistor is the N-type Poly-Silicon resistor named '*rnporpo*'. In other words, among available resistors in the library of the selected technology, this resistor has the closest temperature behaviour to the inverse of the Capacitance.

Referring to (2.3), with the values of Table 4.4, the resistance should be 10 kΩ.

Table 4.4 Parameters to set the loop circuit with N-type Poly resistor

V_{ref}	V_1	R_{tot} (N-type Poly-R)	G_m
20mV	10mV	10KΩ	200μA/V

Employing the values of Table 4.4 results in 0.54% variation in unity-gain frequency over a span of 160°C for the nominal case. In addition, to show the robustness of the design to process variation, the loop circuit is simulated 100 times using Monte-Carlo simulation (considering process variations). Figure 4.16 shows the distribution of the variations of f_U.

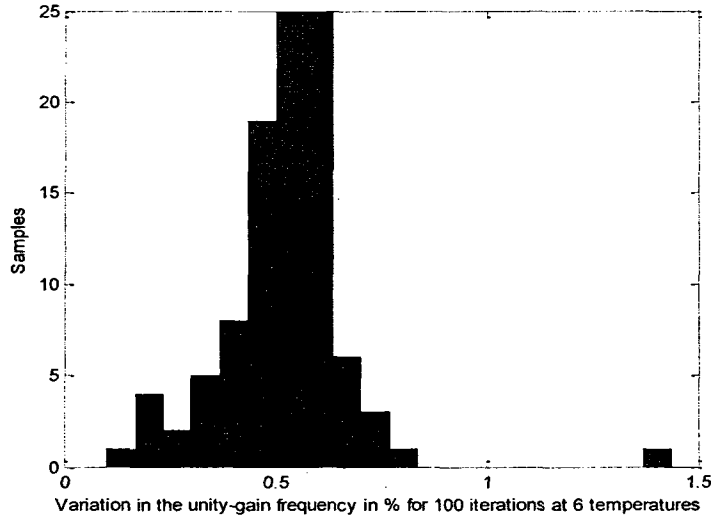

Figure 4.16 Distribution of variations in f_U (in %) for 100 iterations in Monte-Carlo Simulation for 6 temperatures

Notice that for 6 different temperatures (-40, 0, 27, 40, 80 and 120°C) the loop circuit is simulated 100 times. Then, the minimum, maximum and the average value of the unity-gain frequency are obtained and using the following equation, the variation in f_U is calculated for each process variation iteration.

$$\frac{\Delta f_U}{f_U} = \frac{\max(f_U) - \min(f_U)}{avg(f_U)} \tag{4.13}$$

Finally, the distribution of the final values is reported in percentage in Figure 4.16. The average value of variations is 0.54% for 100 iterations which is the same value as the nominal case.

4.3.3 Locking G_m to the Bridge Structure

In the previous section, the transconductance was locked to a single resistor. In that scenario, the TC of G_m followed the TC of the resistor. That approach was successful only because the STMicroelectronics technology happened to have a resistor with the appropriate temperature behaviour. In general, this cannot be assumed to be the case. In this section, an improved technique for achieving other TCs beyond the range of TCs of available resistors is introduced.

First, let us take two resistors with TCs opposite in sign in series inside the resistor box in which we had previously a single resistor. Figure 4.17 (a) shows the control loop circuit with the two mentioned resistors R_p and R_n inside the resistor box of Figure 4.17 (b). R_p and R_n are the P-type and the N-type resistors, respectively.

For this configuration, we can derive G_m as:

$$V_O = I_O R_{tot} = G_m V_1 R_{tot} = V_{ref} \Rightarrow G_m = \frac{1}{R_{tot}}\left(\frac{V_{ref}}{V_1}\right) \tag{4.14}$$

where R_{tot} is the total resistance of the resistor box.

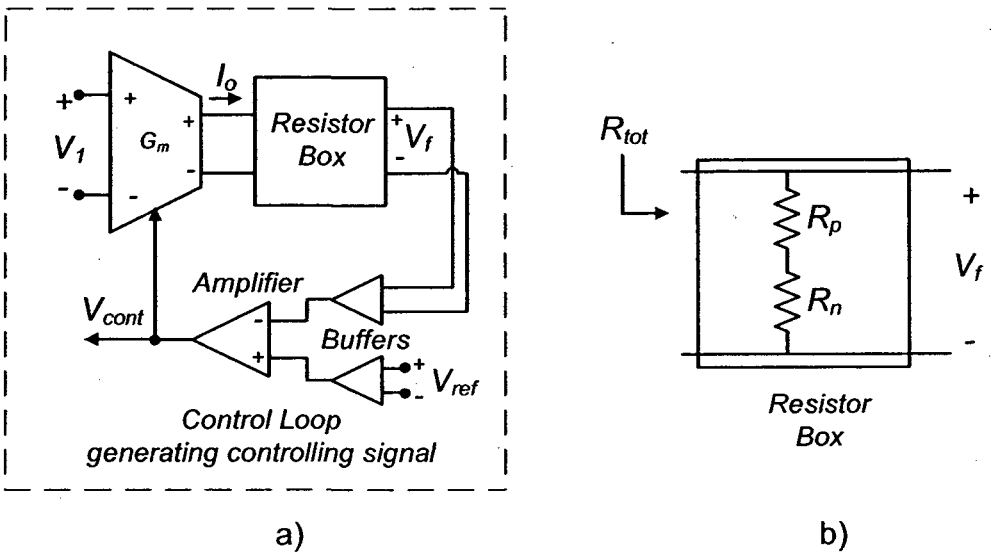

Figure 4.17 a) Control loop circuit for G_m based on [16] b) Resistor box with 2 Poly-Silicon resistors.

Furthermore, one can derive the following equations:

$$\frac{dG_m}{dT} = \frac{-\dfrac{d(R_p + R_n)}{dT}}{(R_p + R_n)^2}\left(\frac{V_{ref}}{V_1}\right) = -\frac{\dfrac{dR_p}{dT} + \dfrac{dR_n}{dT}}{(R_p + R_n)^2}\left(\frac{V_{ref}}{V_1}\right) \tag{4.15}$$

$$\alpha_g G_m = -\frac{R_p \alpha_p + R_n \alpha_n}{(R_p + R_n)^2}\left(\frac{V_{ref}}{V_1}\right) \tag{4.16}$$

where α_n and α_p are temperature coefficients of R_n and R_p, respectively. If we assume V_{ref} = V_1 for simplicity, then we can derive the expression for the TC of G_m as a function of α_p and α_n and resistors' absolute values:

$$\alpha_g = -\frac{R_p\alpha_p + R_n\alpha_n}{R_p + R_n} \tag{4.17}$$

The above equation can be rearranged to:

$$\alpha_g = -\frac{\alpha_n M + \alpha_p}{M + 1} \tag{4.18}$$

where M is the ratio of R_n/R_p. Investigation of (4.18) shows that the value of α_g is between the two temperature coefficients, α_n and α_p. Notice that temperature coefficients of these types of resistors are opposite in sign. As a result, this technique turned out to be convenient only if a TC between the two TCs of Poly-Silicon resistors (Figure 4.14) is required. To achieve to a temperature coefficient beyond the temperature coefficients of the two resistors, the Bridge structure is proposed which is described in the following. Figure 4.18 shows the proposed structure, called Bridge Structure, which is put inside the resistor box.

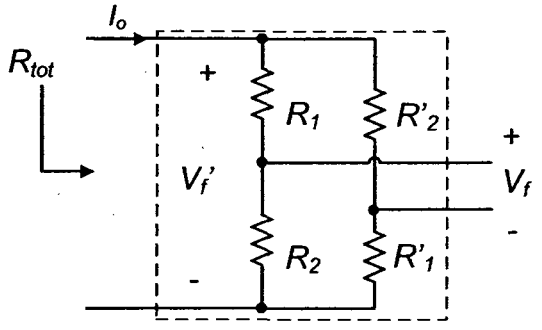

Figure 4.18 Resistor box (the Bridge Structure).

For this configuration, one can derive the following equations.

$$V_f' = I_O R_{tot} = G_m V_1 R_{tot} \tag{4.19}$$

Notice that V_1 (assumed to be temperature independent) is the dc input of the OTA in the control loop circuit (Figure 4.17 a).

$$R_{tot} = (R_1 + R_2) \| (R'_1 + R'_2) \tag{4.20}$$

Referring to the control loop circuit of Figure 4.17 a) we have:

$$V_{ref} = V_f = V_f' \left(\frac{R_2}{R_2 + R_1} - \frac{R'_1}{R'_2 + R'_1} \right) \tag{4.21}$$

Substituting (4.20) and (4.21) into (4.19), and solving for G_m, we derive the following equation:

$$G_m = \frac{R_1 + R'_1 + R_2 + R'_2}{R_2 R'_2 - R_1 R'_1} \left(\frac{V_{ref}}{V_1} \right) \tag{4.22}$$

If $V_{ref} = V_1$, $R_2 / R_1 = M$, $R_1 = R'_1$ and $R_2 = R'_2$, we can derive α_g as:

$$\alpha_g = \frac{(\alpha_1 - M\alpha_2)}{(M - 1)} \tag{4.23}$$

where α_1 and α_2 are temperature coefficients of R_1 and R_2, respectively. An investigation of (4.23) shows several interesting properties. First, consider equal and opposite TCs for R_1 and R_2. That is, $\alpha_1 = -\alpha_2$, which results in:

$$\frac{\alpha_g}{\alpha_2} = -\frac{M+1}{M-1} \tag{4.24}$$

According to (4.24) α_g can be larger than that of the individual resistors. For example, if M=1.5, $\alpha_g = 5\alpha_1$. That is, we get an "amplification" of 5 in the TC of G_m relative to the constituent resistors, as shown in Figure 4.19. The amount of amplification increases as $M \rightarrow 1$. Also, as M goes to infinity, $\alpha_g = -\alpha_2$ which is similar to the case of Figure 4.11(b).

Equation (4.23) can be re-arranged to (4.25) to show how a positive TC for G_m can be synthesized from negative TCs for both R_1 and R_2:

$$\alpha_g = \frac{(\alpha_1 - M\alpha_2)}{(M-1)} = \frac{\alpha_2(\alpha_1/\alpha_2 - M)}{(M-1)} \tag{4.25}$$

In particular if α_1 and α_2 are both negative and α_1/α_2 is smaller than M, α_g would be positive. For example, for α_1/α_2=0.5 and M=2, α_g is $-1.5\alpha_2$ which is positive and larger in magnitude than either α_1 or α_2. This is shown in Figure 4.19.

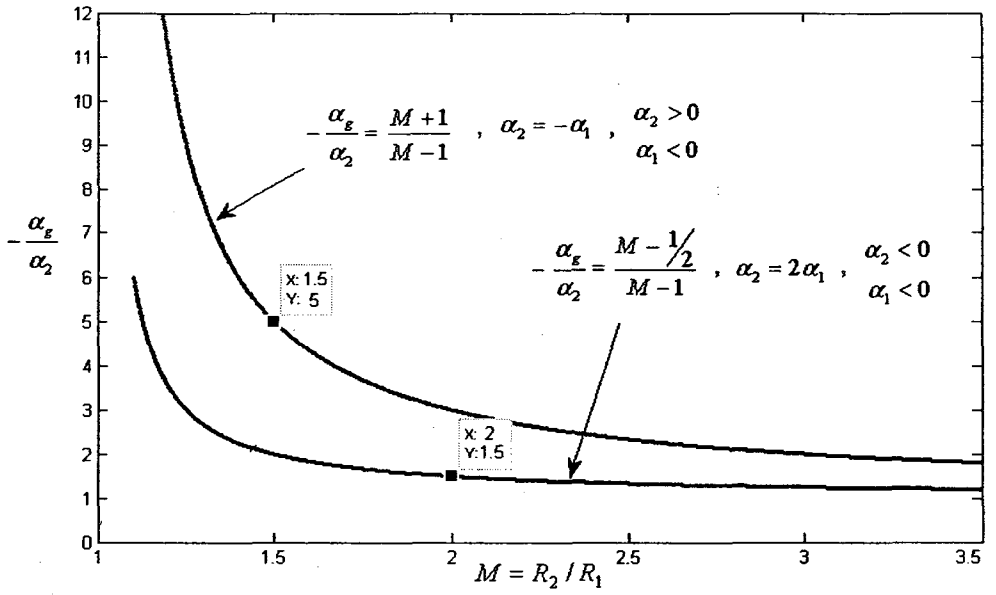

Figure 4.19 Amplification in G_m-cell's TC vs. M, the resistors' ratio

In Figure 4.20, two more characteristics that are obtainable from the bridge structure, (i.e. $\alpha_1 = -M\alpha_2$ and $\alpha_1 = \alpha_2$) are shown.

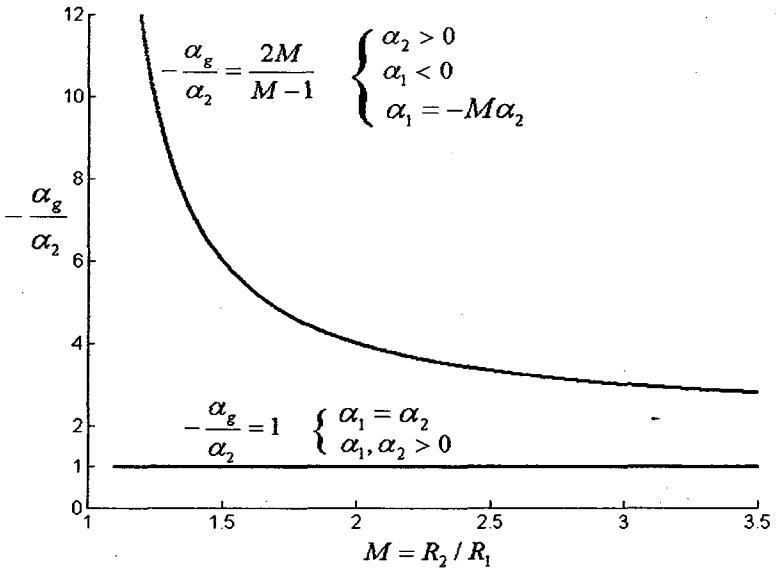

Figure 4.20 Two other possibilities for resistors' TCs in Bridge Structure

Notice that the tuning signal for the OTA is a current. In order to convert the control signal V_{cont} to the tuning current I_{tune}, one NMOS transistor, M_0, is used (Figure 4.21). Obviously, such conversion can be applied for other G_m-cells. Temperature dependency of this transistor is also taken into account while simulating the control loop.

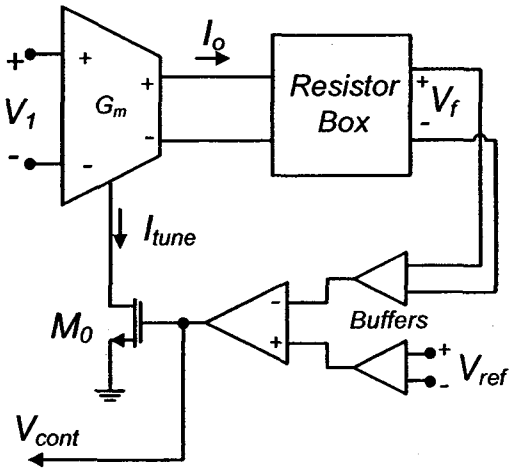

Figure 4.21 Converting the control voltage, V_{cont}, to the control current I_{tune}

Using the two available poly-silicon resistors in STM90nm, *rnporpo* (N-type) and *rpporpo* (P-type) for the resistor bridge resulted in 0.66% change in f_U (Table 4.5). However, the required TC for α_g is -152 μ/°C and this value is between the two TCs of the mentioned resistors. In Figure 4.14 the TCs of the two mentioned resistors were shown. To show the efficacy of our proposed resistor box (Figure 4.18), we considered the case in which the technology's available resistors have a TC that is half of that in STM 90-nm technology. That is, α_{Rp}= -85μ and α_{Rn}=68μ at 27°C. These were simulated by using series combinations of equal-valued poly-silicon resistors and ideal resistors (Figure 4.22). In this case, the desired temperature coefficient to stabilize the unity-gain frequency across temperature is outside of the range for which the configuration in Figure

4.17 (b) can be used. The available resistors necessitate using the proposed Bridge Structure. According to (4.23), taking M=2.83, R_1= R_1'=6 kΩ (P-type) and R_2= R_2' =17 kΩ (N-type) resulted in 0.69 % change in f_U (Table 4.5). Although this result is not as good as that reported for the single resistor case, this example presumed that no such single resistor could be found.

Table 4.5 shows the simulation results for the unity-gain frequency of the OTA-C integrator for different resistor boxes in the control loop circuit. The simulation result for the case of having no control loop is also reported in this Table. The remaining error (Table 4.5) when a control loop is present is primarily due to the finite gain of the comparator in the feedback loop as well as the change in TCs of the resistors and the capacitance over temperature.

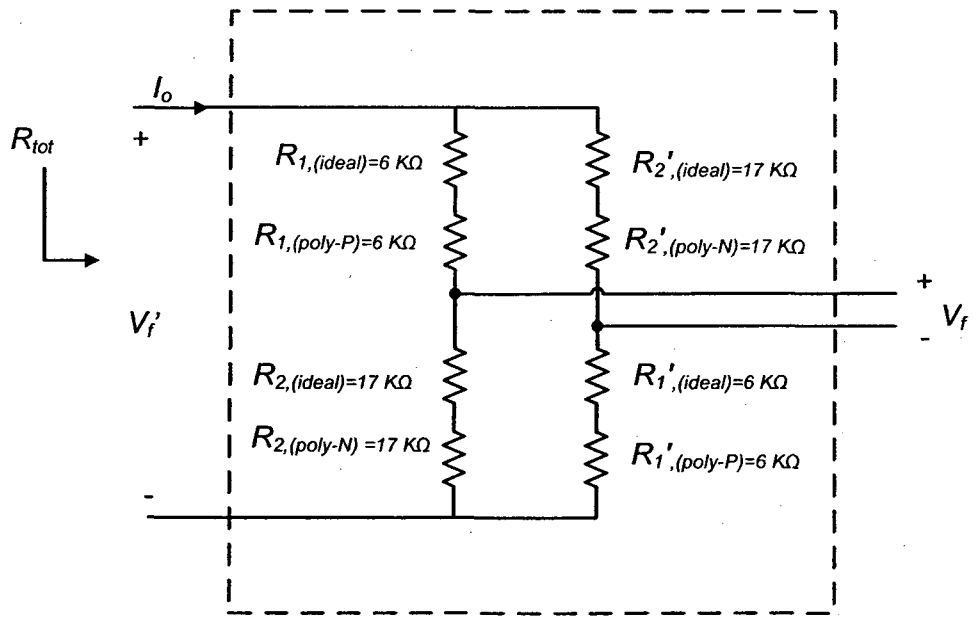

Figure 4.22 Building half-TC resistors in the Resistor box at simulation level

The Monte-Carlo simulation with 100 iterations is also done for the final proposed loop with bridge structure. The result is similar to what was shown in Figure 4.16 with the average value of 0.66 %/°C when real poly-silicon resistors are employed inside the resistor box.

Table 4.5 Variations in f_U for an OTA-C integrator with different cases

	With the loop			Without the loop
T(°C)	Locked to ideal R with TC=0	Locked to the Bridge Structure with available poly-resistors	Locked to the Bridge Structure with half-TC resistors	
-40	5.178 MHz	5.249 MHz	5.181 MHz	5.644 MHz
0	5.203 MHz	5.249 MHz	5.193 MHz	5.337 MHz
40	5.225 MHz	5.242 MHz	5.203 MHz	4.993 MHz
80	5.247 MHz	5.23 MHz	5.212 MHz	4.663 MHz
120	5.27 MHz	5.214 MHz	5.217 MHz	4.369 MHz
Δf/f	1.77%	0.66%	0.69%	24.5%

The proposed bridge structure shows a better performance comparing to the ideal resistor with no temperature dependency. It means, even if one locks G_m to a resistor with TC=0, we would see more variation in f_U rather than using the proposed technique. It is worth mentioning again that in this technique the effect of temperature dependency of the output capacitance is also taken into account.

As shown in Figure 4.22, V_f is a portion of V_f'. If V_f is a small protion of V_f', the total loop gain would decrease. Also, to sense V_f, V_f' has to be so large which means the OTA has left its linear region. As a result, the loop should be set such that V_f / V_f' is not much smaller than 1. Equivalently, $M = R_2/R_1$ should not be much larger than 1.

4.4 Summary

In this chapter, investigations of the temperature dependency of OTA-C filter's components, i.e. G_m and C have been carried out. The principles of a new technique for temperature compensation are explained. Locking G_m to a resistance in a control loop is the basic idea to control the temperature sensitivity of the OTA. Choosing a proper resistor, which changes similar to the output capacitance with respect to temperature, resulted in good stabilization of the unity gain frequency over temperature variations. The Bridge Structure, which is a combination of resistors, is proposed finally and its characteristics as well as the simulation results regarding the insensitivity of the unity-gain frequency of the OTA-C integrator with temperature variations have been reported. In the next chapter, a summary of the work presented so far and the suggestions for future work are discussed.

Chapter 5 Conclusion and Future Work

5.1 Work done and discussions

In this thesis, a novel technique for stabilizing the unity gain frequency of a G_m-C integrator in CMOS technology over a range of temperature variation has been presented. The considered range for temperature is between -40 °C and 120 °C, and STMicroelectronics 90-nm technology with 1.2 V supply voltage has been used for the implementation. An appropriate OTA has been chosen from a list of several OTAs. This has been improved for linearity and common-mode stabilized with CMFB circuit before adaptation for the implementation of a G_m-C integrator. The simulation results and the layout of the OTA are reported, as well.

The proposed technique decreases the variation in the unity-gain frequency in a G_m-C integrator with respect to the temperature variations. By locking the transconductance value to a combination of resistors (called Bridge Structure) with a suitably designed TC the ratio of G_m/C is kept nearly constant in the presence of significant temperature induced variation in transistor parameters such as V_T and μC_{OX}.

In particular, a G_m-cell is put inside a control loop. In this way, the control signal for the G_m-cell and, hence, the total transconductance behaves desirably. The control signal generated in the control loop finally goes to similar G_m cells of the OTA-C filter to set the

transconductances. As a result, the frequency behaviour of the filter remains stable against temperature variations as G_m/C is rendered temperature independent. The relevant work has been reported and published in *Electronics Letters* (IET, UK) [8].

The proposed technique is also robust to the process variation. Additionally, appropriate use of a resistive bridge broadens the range of capacitor's TCs that can be compensated using a technology's available resistors. The resistors used in this scheme may be standard on-chip resistors, or programmable TC components as in [32].

5.2 Suggestions for Future Work

In this work, the G_m of the OTA tracks the temperature behaviour of the integrating capacitance. As shown in Chapter 4, the mentioned capacitance is changing by temperature with a varying slope which means the output capacitance has at least two temperature coefficients. The resistance, to which we locked G_m, has to have exactly the same temperature behaviour as the capacitance for best temperature compensation. Moreover, the capacitance changes by the biasing voltage and this causes some error, too. Therefore, employing controllable capacitors [15] inside the control loop to control the capacitance as well as the transconductance could be a good idea.

In addition to variations due to temperature, considering supply voltage variations could be next step for frequency stabilization. In fact, it makes the design robust to unwanted variations from VDD. As an example, in [20] VDD variation is taken into account in the proposed frequency tuning technique.

As mentioned in Chapter 4, the resistors used in this scheme may be standard on-chip resistors or programmable TC components as in [32]. Newly invented re-adjustable

resistors in [32], called *Rejustors*, have the ability of being programmed to have the desired positive or negative TCs. For instance, when there is a voltage-division structure made by resistors, setting the TCs is easier and the best nonlinearity cancellation is achieved. In addition, post-packaging adjustment will be available for analog circuits. Applying such resistors with the desired programmed TCs for the resistive bridge for the presented technique in this thesis will be an interesting future step for this work.

The loop gives a TC=0, however, it does not set the unity gain frequency. Combining a frequency tuning technique with the proposed transconductance tuning technique in this thesis to get a robust filter would be a next step to this work. This would be done in a way that would only require the periodic use of the frequency reference, perhaps only when the chip is powered on.

In Chapter 4, it is observed that there is a bias voltage at which the capacitor appears to be temperature independent, although quite voltage dependent. One may do more investigations into the behaviour of filters with capacitors biased at this point. A first step would be to see if this phenomenon of temperature independent capacitance is real, or an artefact of modelling.

Finally, measuring results of the fabricated OTA help to better understand the future designs. Also, implementing a filter by employing the presented transconductance tuning technique will further prove the value of the proposed work in this thesis.

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