Progress in PHOTOVOLTAICS

PROGRESS IN PHOTOVOLTAICS: RESEARCH AND APPLICATIONS
Prog. Photovolt: Res. Appl. (2015)
Published online in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/pip.2587

RESEARCH ARTICLE

Temperature-dependency analysis and correction methods of *in situ* power-loss estimation for crystalline silicon modules undergoing potential-induced degradation stress testing

Sergiu Spataru[1]*, Peter Hacke[2], Dezso Sera[1], Corinne Packard[2,3], Tamas Kerekes[1] and Remus Teodorescu[1]

[1] Energy Technology, Aalborg University, Aalborg, Denmark
[2] National Renewable Energy Laboratory, Golden, CO, USA
[3] Metallurgical and Materials Engineering, Colorado School of Mines, Golden, CO, USA

ABSTRACT

We propose a method for *in situ* characterization of the photovoltaic module power at standard test conditions, using superposition of the dark current–voltage (*I–V*) curve measured at the elevated stress temperature, during potential-induced degradation (PID) testing. PID chamber studies were performed on several crystalline silicon module designs to determine the extent to which the temperature dependency of maximum power is affected by the degradation of the modules. The results using the superposition principle show a mismatch between the power degradation measured at stress temperature and the degradation measured at 25 °C, dependent on module design, stress temperature, and level of degradation. We investigate the correction of this mismatch using two maximum-power temperature translation methods found in the literature. For the first method, which is based on the maximum-power temperature coefficient, we find that the temperature coefficient changes as the module degrades by PID, thus limiting its applicability. The second method investigated is founded on the two-diode model, which allows for fundamental analysis of the degradation, but does not lend itself to large-scale data collection and analysis. Last, we propose and validate experimentally a simpler and more accurate maximum-power temperature translation method, by taking advantage of the near-linear relationship between the mismatch and power degradation. This method reduces test duration and cost, avoids stress transients while ramping to and from the stress temperature, eliminates flash testing except at the initial and final data points, and enables significantly faster and more detailed acquisition of statistical data for future application of various statistical reliability models. Copyright © 2015 John Wiley & Sons, Ltd.

KEYWORDS

potential-induced degradation; crystalline silicon; degradation; current-voltage charactersitic; accelerated stress testing; temperature dependency

***Correspondence**

Sergiu Viorel Spataru, Energy Technology, Aalborg University, Aalborg, Denmark.
E-mail: ssp@et.aau.dk

Received 24 March 2014; Revised 28 November 2014; Accepted 1 December 2014

1. INTRODUCTION

Potential-induced degradation (PID) stress testing of photovoltaic (PV) modules is critical for understanding how the modules are affected by system voltage bias, as well as for developing relevant qualification tests and lifetime models. PID studies (through environmental chamber testing or field testing) typically require accurate performance measurements reported at standard testing conditions (STC) of 1000 W/m^2 and 25 °C, during the module degradation process. Collecting sufficient STC maximum power (P_{max}) degradation data from modules undergoing PID stress testing, either from chamber testing or outdoor field testing, has always been a time-consuming and expensive task. Monitoring the performance degradation of PV modules undergoing accelerated PID stress testing generally involves intermittently removing the module from the chamber and measuring power on a flash tester, which can require considerable time and effort when numerous samples are involved [1]. Often, this method yields only

a few intermediate P_{max} degradation measurement points, which can make the data analysis and modeling of the degradation mechanism difficult and insufficiently accurate.

Moreover, outdoor characterization and performance monitoring of PV modules degrading by PID is dependent on the ambient conditions, which are rarely close to STC; thus, P_{max} is most often measured at near 1000 W/m^2 and at a higher temperature under irradiance. Simple temperature translation of module P_{max} data to 25 °C, using datasheet temperature coefficients, would be a trivial task if the PV modules were not affected by PID, and the temperature-dependent properties of the modules remain unchanged. A study [2], concerning accelerated stress testing of crystalline silicon PV modules, has shown that the P_{max} temperature coefficient (γ), determined from light *I–V* measurements, decreases in absolute magnitude as the modules degrade through PID, and reverts back, close to the initial value, as the module recovers from PID [2].

To investigate this behavior for the "dark" temperature-dependent properties of crystalline silicon modules undergoing PID, we perform an initial evaluation of how the P_{max} temperature coefficient (calculated from the dark *I–V* characteristic and denoted γ_{dark} from hereon) changes over the course of the degradation. However, future investigation is still required to evaluate the extent to which the light (γ) and dark (γ_{dark}) *I–V* determined P_{max} temperature coefficients correlate, as well as to confirm this behavior for fielded modules suffering from PID. Nevertheless, understanding the dark *I–V* temperature behavior of modules undergoing PID is necessary for developing *in situ* characterization methods that can estimate the STC power of the module from a dark *I–V* measurement taken directly at the elevated stress temperature during the accelerated lifetime testing for PID.

The current work is based on such an *in situ* module degradation characterization method, first proposed in [3], that can estimate the STC P_{max} degradation of modules, from the 25 °C dark *I–V* characteristic of the PV modules, taken during the PID stress test. The method involves periodic measurement of the 25 °C dark *I–V* characteristic of the PV modules, while in the chamber, followed by the superposition of the dark *I–V* curves to light conditions, using the short-circuit current (I_{sc}) of each module, measured at STC (or other irradiance conditions of interest such as low in light [3]), before and after the PID stress test. Because the photocurrent (at I_{sc}) is only weakly influenced by PID, as previously observed for crystalline modules [3–5], the P_{max} degradation estimated by the superposition of the dark *I–V* curves corresponds very well with the degradation measured using a flash tester, for a wide range of irradiance conditions [3]. This method so far has been limited to dark *I–V* curves captured at 25 °C, requiring interruption of the stress test, ramping down the temperature of the PV module to 25 °C for dark *I–V* characterization, and then ramping back up again to the elevated temperature for resuming the stress test.

The *in situ* module degradation characterization method [3], assumes the superposition principle (or "shifting approximation"), which has been shown to work well for most crystalline *pn* single junctions [6,7]; however, there are some limitations that must be considered when applying this method. One of the most common cases mentioned in the literature, for which the superposition principle breaks down, is for solar cells exhibiting a significant series resistance ($R_s > 10\ \Omega cm^2$) [7–10], for which the I_{sc} does not match the light-generated current anymore. Another case for which the superposition does not hold any more, is for crystalline silicon solar cells in which the recombination via defect levels with unequal electron and hole capture rates, dominates the *I–V* characteristic [9,11], as is the case for recombination in high-efficiency solar cells with oxidized surfaces [12]. Other cases when superposition does not apply are as follows: (i) a higher bulk recombination level at low forward bias under illumination conditions, as compared with the recombination level experienced at the same forward bias but under dark conditions [9,11]; (ii) significant recombination and generation in the depletion region [7,9,13]; and (iii) voltage dependence of the depletion-region width [7,9]. As a best practice, the validity of the superposition principle should be tested when applying the *in situ* degradation characterization method to new module designs. This testing can easily be achieved by performing pre-experiment and post-experiment light *I–V* and dark *I–V* measurements on the modules, and comparing the relative P_{max} degradation in the two cases.

In addition to estimating power loss from dark *I–V* measurements acquired during the PID test, analyzing the characteristic curves through the perspective of a fundamental solar cell model (such as the two-diode model) could lend insight into the degradation mechanisms occurring in the PV device [1]. The two-diode model has been successfully employed over the years to accurately represent and analyze solar cell behavior (especially monocrystalline solar cells) and the underlying physical processes [14]. On the solar cell level, the two-diode model parameters can be a useful tool for monitoring the solar-cell manufacturing processes [15], as well as for solar cell design and optimization. On the module level, the model has been successfully employed in power simulation studies [16], due to its capability to accurately describe *I–V* characteristics of PV generators when the incident light intensity varies [17]. However, there are some limitations to the diode model, such as the case of industrial solar cells with manufacturing defects in which the dark *I–V* characteristic can deviate strongly from the textbook exponential behavior [18] and can be difficult to explain through the prism of the two-diode model. Furthermore, when applying the model to PV modules, it is not clear to what extent the variability in various cell properties across the module will affect the applicability of the two-diode model.

The work presented in the current paper extends the *in situ* power degradation test method previously described [3] to the elevated stress temperature at which the accelerated PID test is being performed, calculating the P_{max} degradation from the dark *I–V* curve measured at the

stress temperature. Although the current work is limited to estimating STC power degradation, it could easily be extended to low light-performance estimation, based on the results in [3].

For this purpose, in the first part of the paper, we analyze experimental data recorded for crystalline PV modules undergoing PID stress testing to determine the extent to which the temperature dependency of P_{max} is affected by PID.

Second, we evaluate the degree to which the P_{max} temperature coefficient can be applied to translate P_{max} measured at a high stress temperature to 25 °C conditions, and we show how the P_{max} temperature coefficient of the PV module changes as the PV module degrades.

In the third part of the paper, we explore the capability of the two-diode model, to translate dark *I–V* characteristic curves measured at the stress temperature down to 25 °C conditions, as the PV module degrades through PID.

In the last part of the paper, we introduce a simple and accurate method for temperature translation of P_{max} during degradation, from any stress temperature down to 25 °C conditions, independent of module parameters, to obtain the STC power of modules undergoing PID. We also validate the method experimentally with monocrystalline and multicrystalline PV modules.

2. EXPERIMENT

The method for accelerated PID stress testing and *in situ* characterization of crystalline PV modules was previously described in [19]. The test method is based on climatic chamber testing at elevated temperature and humidity, where module nameplate system voltage bias of −1000 V was applied continuously to the cells in the module by connecting the shorted leads to a high-voltage power supply and grounding the module frame [19]. The method has been shown to activate PID mechanisms in susceptible modules with temperature, humidity, and voltage factors that modules also experience in the field. During testing, the temperature and leakage currents of the test modules are continuously monitored, and the operator measures the module performance periodically, through characterization such as *in situ* dark *I–V* or external light *I–V* measurements.

For the purpose of *in situ* power-loss determination (at any temperature) of PV modules undergoing PID, a fully automatized test setup (shown in Figure 1) was developed to run the experiment profile, and acquire module-level measurements and dark *I–V* characteristics at preprogrammed temperature levels to develop the sought temperature-dependent relationships. This setup has reduced operator effort in monitoring and characterizing the modules and has allowed a much more granular characterization of the PV modules as they degrade.

For the purpose of understanding the temperature dependency of the P_{max} degradation of modules undergoing PID, we designed and performed an experiment having

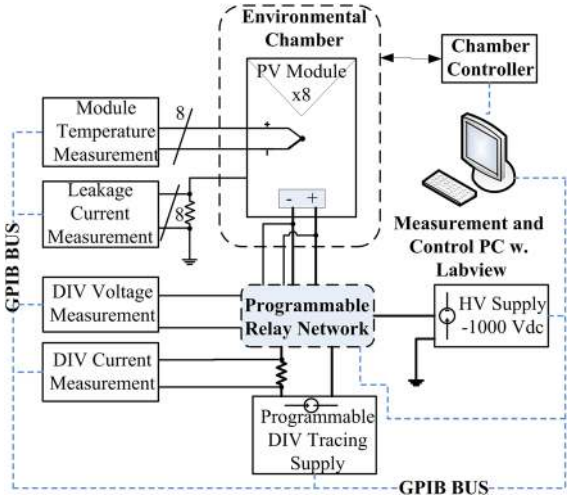

Figure 1. Fully automated experiment setup for performing potential-induced degradation stress testing on photovoltaic modules.

the profile depicted in Figure 2. Five crystalline module designs (denoted from A to E), with two replicates each, underwent system voltage stress testing at elevated heat (60 °C) and relative humidity (85% RH), with negative voltage bias (−1000 V) applied between the active material (shorted leads) and the frame of each module. Every 3 h, the dark *I–V* characteristic of each module was acquired at 60, 50, 40, 30, and 25 °C by automatically

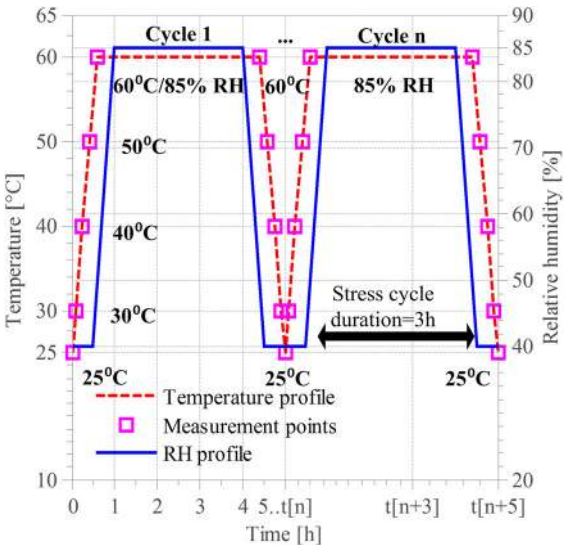

Figure 2. Chamber temperature and relative humidity profiles for performing system voltage stress testing (−1000 V) at elevated heat and humidity (60 °C/85% RH). At the start and end of each cycle, the dark *I–V* characteristic curves of the photovoltaic module samples are measured automatically at (60, 50, 40, 30, and 25 °C) by ramping down the chamber temperature and monitoring each photovoltaic module temperature until it reaches measurement temperature.

ramping down the chamber temperature and RH; however, keeping the high voltage stress until the actual dark *I–V* measurement process. The temperature of each module was monitored by the test system, until it reached the desired set points, and the dark *I–V* characteristics were measured. The dark *I–V* curves acquired on the ramp-down of the module temperature were approximately matched with those acquired on the ramp-up, showing negligible influence of the ramps on the module degradation. Furthermore, the experiment profile and chamber control were significantly optimized to keep the temperature transients short in duration. Once all measurement points at the specified temperature are taken, the stress test is resumed automatically according to the profile in Figure 2.

In addition, STC light *I–V* measurements were acquired for every test module, pre (t_0) and post (t_n) experiment/degradation on a class A + A + A+ flash tester. The resulting STC I_{sc} and $P_{\max}$ values, summarized in Table I, are used check the superposition assumptions and calculate the final STC degradation of the module. From Table I we can observe that the pre-degradation and post-degradation STC I_{sc} does not change more than 1%, indicating that the light-generated current (I_L) of the PV modules does not change significantly due to PID, which is in line with previous observations [3–5].

3. RESULTS AND DISCUSSION

3.1. Validation of the dark *I–V* superposition method

The initial (t_0) and final (t_n) STC I_{sc} measurements from Table I are used to approximate I_L as the average value of the STC I_{sc}, translated to an arbitrary temperature T, as showed in (1), where α is the I_{sc} temperature coefficient specified in the PV module datasheet.

Table I. Standard testing conditions short-circuit current (I_{sc}) and maximum power ($P_{\max}$) of the 10 test modules, measured pre (t_0) and post (t_n) potential-induced degradation stress testing, on a class A + A + A+ flash tester.

	STC I_{sc}		STC $P_{\max}$		
Mod.	t_0 [A]	t_n [A]	t_0 [W]	t_n [W]	t_n [%]
A-1	8.33	8.31	222.1	150.8	67.9
A-2	8.31	8.34	224.5	173.2	77.1
B-1	5.25	5.23	173	138.6	80.1
B-2	5.29	5.24	173.7	128.5	74
C-1	8.65	8.64	236.5	204.6	86.5
C-2	8.63	8.61	237.3	224.7	94.7
D-1	8.86	8.84	249.1	191.2	76.7
D-2	8.77	8.76	247.6	196	79.1
E-1	8.74	8.72	244.7	219.7	89.8
E-2	8.74	8.72	245	223	91

Remaining $P_{\max}(t_n)$ [%] is calculated relative to the initial measured $P_{\max}$ (t_0). Module types are indicated by letters and their replicas by numbers.

Next, the dark *I–V* curves ($I_{\text{dark}}(t,T)$-$V_{\text{dark}}(t, T)$) of each module are shifted with I_L , and the $P_{\max}$ degradation ($P_{\deg}(t, T)$) is calculated as a function of stress time t, and module temperature T, relative to the pre-degradation (t_0) measurements, as in (1). A detailed description of the *in situ* degradation measurement method for a single temperature can be found in [3].

$$
\begin{aligned}
P_{\deg}(t,T) &= \frac{P_{\max}(t,T)}{P_{\max}(t_0,T)} \\
&= \frac{\max\{[I_{\text{dark}}(t,T)+I_L(T)]V_{\text{dark}}(t,T)\}}{\max\{[I_{\text{dark}}(t_0,T)+I_L(T)]V_{\text{dark}}(t_0,T)\}} \\
I_L &= \frac{I_{sc}(t_0,25°C)+I_{sc}(t_n,25°C)}{2} \\
&\quad \text{x}\,[1+\alpha(T-25°C)]
\end{aligned}
\tag{1}
$$

Figure 3 shows the relative $P_{\max}$ degradation curves $P_{\max}(t, T)/P_{\max}(t_0)$ for the 10 modules undergoing PID, both at 25 °C and 60 °C. To validate the *in situ* degradation characterization method and check if the superposition principle holds, the final $P_{\max}$ degradation, calculated from the 25 °C dark *I–V* characteristics and plotted in solid lines in Figure 3, is compared with the flash-tester-measured STC power degradation, calculated from the STC $P_{\max}$ measurements in Table I, and plotted with star markers in Figure 3. From here we can observe that the final values of $P_{\max}$ degradation match very well. These results are in line with previous findings and validate the *in situ* degradation characterization method [1,3] where $P_{\max}$ degradation calculated from the 25 °C dark *I–V* characteristics showed excellent correspondence with the flash-tester-measured $P_{\max}$ degradation, both at STC and lower illumination levels. Considering these findings, we can reasonably approximate the flash-tester-measured STC $P_{\max}$ degradation curve, with the $P_{\max}$ degradation determined from the 25 °C dark *I–V* characteristics, which will be used interchangeably from hereon.

In contrast, the $P_{\max}$ degradation, calculated from the 60 °C dark *I–V* characteristics, displayed with dashed lines in Figure 3, underestimates the 25 °C measured power degradation by several percent, which is consistent for each module we tested.

3.2. Temperature dependency of the power-loss estimation

This difference between the 25 and 60 °C measured $P_{\max}$ degradation is quantified in (2), by calculating the *relative power-loss estimation error* ($\delta P_{\deg}$) as a relative percentage error between the $P_{\max}$ degradation determined at the stress temperature T_{stress}, and the module degradation determined at 25 °C.

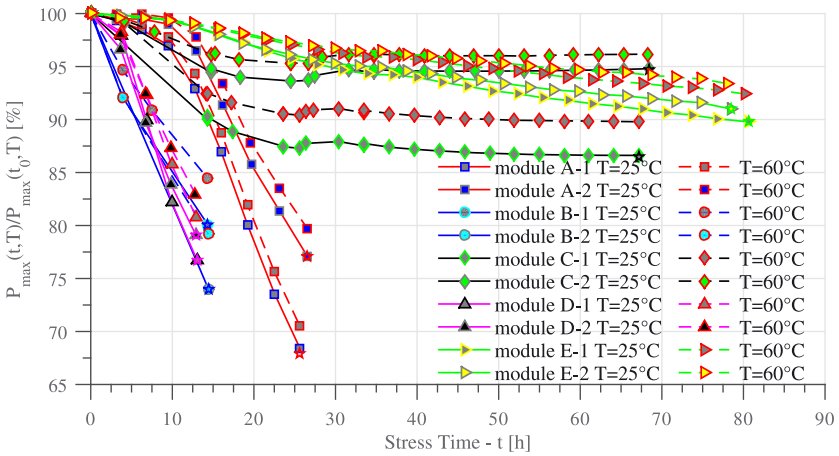

Figure 3. Maximum power (P_{max}) degradation curves calculated from the dark *I–V* measurements at 25 °C, solid lines; and 60 °C, dashed lines, for PV modules undergoing PID stress testing. Each P_{max} on the *y*-axis is normalized to the P_{max} measured before the start of degradation at the same temperature (either 25 or 60 °C). The final degradation levels are validated using light *I–V* measurements at the finish of the experiment, and plotted as star symbols on the graph (matching the degradation levels estimated from the 25 °C dark *I–V* measurements—full lines).

$$\partial P_{\deg}[\%] = \frac{P_{\deg}(t, T_{\text{stress}}) - P_{\deg}(t, 25°C)}{P_{\deg}(t, 25°C)} * 100 \qquad (2)$$

By plotting $\delta P_{\deg}$ for the stress temperature of 60 °C, as shown in Figure 4, it is evident that the estimation error is present for all modules tested, and the error progresses in magnitude as the modules degrade.

Furthermore, by plotting the $\delta P_{\deg}$ curves in Figure 5, calculated from the dark *I–V* curves measured at different temperatures (25, 30, 40, 50, 60, 70, and 85 °C) for module design D, we observe that the estimation error also depends on the module temperature at which the dark *I–V* curve is acquired, as well as the degradation state of the PV module.

If the power loss estimated from dark *I–V* characteristics measured at the stress temperature is to be used for statistical analysis, acceleration-factor determination [20], or lifetime modeling [1] of PID of crystalline PV modules, it is preferable to determine the STC values as accurately as possible. In this regard, we investigated two existing P_{max} temperature-correction methods and propose a new method that is most accurate and easier to apply for the case of PID being evaluated *in situ* at test temperature.

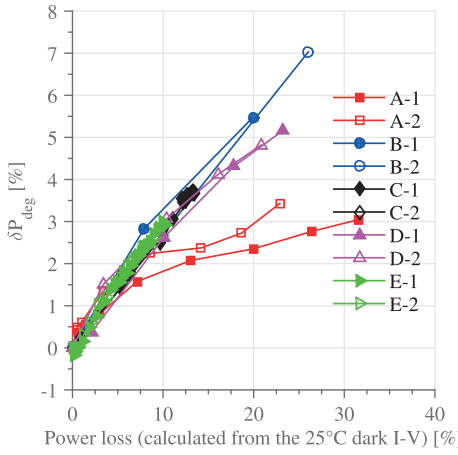

Figure 4. Relative power-loss estimation error $\delta P_{\deg}$, measured at 60 °C, as a function of degradation level (calculated from the dark *I–V* characteristics measured at 25 °C) for all modules considered in the experiment.

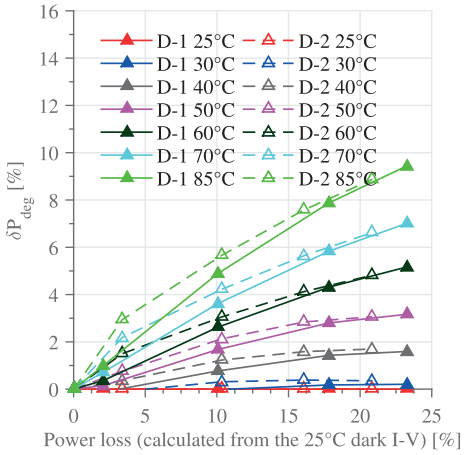

Figure 5. Relative power-loss estimation error $\delta P_{\deg}$ (at temperature levels 25, 30, 40, 50, 60, 70, and 85 °C) as a function of degradation (calculated from the dark *I–V* characteristics measured at 25 °C) for module design D. The error in power-loss estimation increases as a function of module temperature and module degradation.

3.3. Correction of the power-loss estimation using the temperature coefficient of the maximum power

The temperature dependency of the maximum power of PV modules has been extensively investigated in the literature [21–24], and several models have been proposed over the years; an overview of which has been carried out in [25]. A simple but widespread model of P_{max} temperature dependency is based on the P_{max} temperature coefficient γ, calculated as in (3) [21], and assumes a linear relationship (4) between P_{max} and the solar cell temperature (T_c).

$$\gamma = \frac{1}{P_{max}} \frac{\delta P_{max}}{\delta T}\bigg|_{T_{ref}=25°C} \tag{3}$$

$$P_{max}(T_{ref}) = \frac{P_{max}(T_c)}{1+\gamma(T_c - T_{ref})} \tag{4}$$

The model in (4) has been successfully applied to crystalline PV modules under constant (or near-constant) illumination conditions despite certain limitations [21,23,24], making a very simple way of translating P_{max} measurements from one temperature to another. Typical γ values for crystalline silicon solar cells range from -0.3%/°C to −0.6%/°C [21,23,25], depending on cell technology and method of calculation, and most often it is stated in the manufacturer's datasheet. However, applying this model to modules undergoing PID remains in question.

To determine the applicability of this temperature model for the case when P_{max} is estimated from dark *I–V* measurements using the *in situ* method in (1), we calculated a similar "dark" temperature coefficient, denoted as γ_{dark}, by linear fitting the model in (4) to the dark *I–V* P_{max} estimates obtained by superposition and the module temperature. Here, we approximated the solar cell temperature T_c with the temperature measured on the backside of the module using a thermocouple, which is a valid assumption considering that in the case of environmental chamber testing, the PV modules are heated uniformly from all sides. The dark *I–V* estimated P_{max} temperature dependency and the resulting γ_{dark} temperature coefficients are presented in Figure 6a—measured before PID, and in Figure 6b—measured after the PID stress test when the flash tester-determined STC power fraction remaining after the degradation is shown in Table I for each PV module.

The initial γ_{dark} temperature coefficients are presented in Figure 6a and have values between −0.4%/°C and −0.46%/°C, similar to γ values given in the manufacturer's datasheet and the literature. However, the post-PID γ_{dark} measurements in Figure 6b show a significant decrease in absolute magnitude, ranging from −0.22%/°C to −0.39%/°C, comparable with what was reported in [2] for the light *I–V* determined STC P_{max} temperature coefficient γ of crystalline silicon modules undergoing PID. The extent to which γ_{dark} and γ correlate has not been investigated; nevertheless, is it clear in both cases that the temperature dependency of the P_{max} changes as the modules degrade by PID, making the model in (4) unreliable in translating P_{max} degradation from one temperature level to another, for modules undergoing PID.

For the purpose of understanding how the γ_{dark} temperature coefficients degrade in relation to module power loss during PID, we performed temperature ramps and dark *I–V* measurements on the PV modules during the accelerated degradation tests according to the experiment profile in Figure 2. From these intermediate dark *I–V* measurements, we calculated γ_{dark} coefficients as a function of PV module degradation (calculated by referencing the measured 25 °C dark *I–V* characteristics). The relative change of γ_{dark} is calculated from the start of the experiment t_0 to a point at time t of the experiment, as shown in Figure 7.

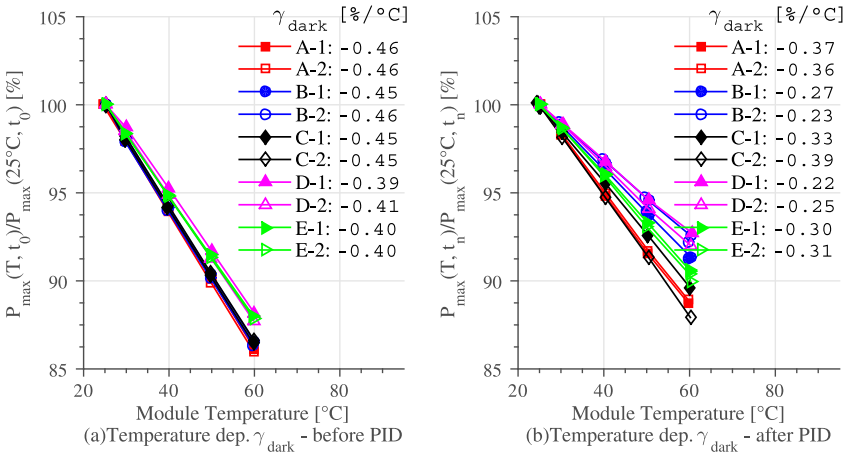

Figure 6. Temperature dependency γ_{dark} of the dark *I–V* estimated maximum power (P_{max}), normalized to the 25 °C P_{max} value. The P_{max} temperature coefficient γ_{dark} is linearly fitted from the P_{max} temperature-dependency curve, measured for each photovoltaic module test sample: (a) before the potential-induced degradation (PID) stress testing (t_0); (b) after the PID stress testing (t_n).

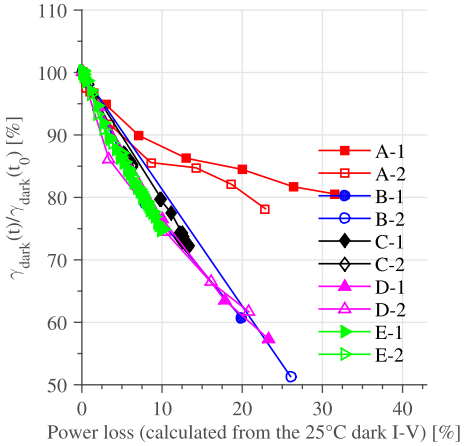

Figure 7. Maximum power-temperature coefficient (γ_{dark}) versus P_{max} degradation (through potential-induced degradation). The temperature coefficient γ_{dark} decreases in absolute magnitude as the photovoltaic module degrades.

The results in Figure 7 show that that temperature coefficient γ_{dark} varies depending on the module type and not necessarily linearly with the module power loss, making estimation difficult and hindering the applicability of this P_{max} temperature dependency model.

3.4. Correction of the power-loss estimation using the diode temperature translation equations

Another possible method for translating P_{max} degradation from elevated stress temperature measurements down to reference conditions (25 °C) would be to determine the parameters of the two-diode model (5) from the dark *I–V* characteristics measured at the stress temperature and translate those parameters to 25 °C conditions using the fundamental temperature-dependency equations of the solar cell model parameters (6):

$$J = J_L - J_{01}\left\{\exp\left[\frac{q(V+JR_s)}{n_1 kT}\right]-1\right\} - J_{02}\left\{\exp\left[\frac{q(V+JR_s)}{n_2 kT}\right]-1\right\}+\frac{V+JR_s}{R_{sh}} \quad (5)$$

where J is the current density; J_L is the light-induced current density; V is the terminal voltage; J_{01} and J_{02} are the diode saturation current densities corresponding to diffusion and recombination processes, respectively, occurring in the solar cell; n_1 and n_2 are the diode ideality factors; R_s and R_{sh} are the area-specific series and shunt resistance parameters, respectively, of the solar cell; T is the cell temperature; k is the Boltzmann constant; and q is the elementary charge.

It has been previously shown that increasing temperature leads to an exponential increase of the saturation currents J_{01} and J_{02}, following the relation in (6) [26,27]; this in turn causes a decrease in open-circuit voltage (V_{oc}), hence reducing the fill factor and efficiency of the solar cell [27,28]:

$$J_{01}(T) = A_1 T^{\gamma 1}\exp\left[-\frac{Eg(T)}{m_1 kT}\right]$$
$$J_{02}(T) = A_2 T^{\gamma 2}\exp\left[-\frac{Eg(T)}{m_2 kT}\right] \quad (6)$$

where A_1 and A_2 are empirical parameters assumed to be independent of temperature [26]; Eg is the bandgap energy; γ_1 and γ_2 are material constants incorporating the possible temperature dependencies of the other material parameters; and m_1 and m_2 are also empirical parameters depending on the quality of the cell material and junction [26].

Considering we have identified $J_{01}(T_{stress})$ and $J_{02}(T_{stress})$ from dark *I–V* measurements at a stress temperature T_{stress}, we can translate their values to a reference temperature T_{ref} = 25 °C by rewriting the equations in (6) into the temperature-translation equations (7–9). Equations (7) and (8) are used to translate the saturation currents to a desired temperature (T_{ref}), whereas (9) is used to calculate the bandgap energy at that temperature [29]. Additionally, the material constants γ_1 and γ_2 have to be determined through curve-fitting or assumed from the literature (γ_1 = 3 and γ_2 = 3/2) [16,26].

$$J_{01}(T_{ref}) = J_{01}(T_{stress})\left(\frac{T_{ref}}{T_{stress}}\right)^{\gamma 1} \exp\left\{\frac{q}{km_1}\left[\frac{Eg(T_{stress})}{T_{stress}}-\frac{Eg(T_{ref})}{T_{ref}}\right]\right\} \quad (7)$$

$$J_{02}(T_{ref}) = J_{02}(T_{stress})\left(\frac{T_{ref}}{T_{stress}}\right)^{\gamma 2} \exp\left\{\frac{q}{km_2}\left[\frac{Eg(T_{stress})}{T_{stress}}-\frac{Eg(T_{ref})}{T_{ref}}\right]\right\} \quad (8)$$

$$Eg(T) = Eg_{ref}[1 - 0.0002677(T - T_{ref})] \quad (9)$$

The series (R_s) and shunt resistance (R_{sh}) parameters, as well as the diode ideality factors (n_1 and n_2), have been shown to vary slightly with temperature [30,31], but their effect on solar cell efficiency is small compared to the exponential changes in saturation currents (J_{01} and J_{02}) with temperature [28].

To validate the temperature-translation equations of the diode saturation currents, we analyzed the dark *I–V* characteristics of one of the test modules (A-2) during its degradation through PID. The module undergoes five stress cycles (3 h of 60 °C/85% with −1000 V bias each cycle); in between cycles, dark *I–V* measurements were performed at 25, 30, 40, 50, and 60 °C, according to the profiles shown in Figure 2. From the 25 °C dark *I–V* curves, plotted in Figure 8, we can observe that the dark *I–V* characteristics of the PV module are mostly affected in the fill factor, due to the increasing diode saturation currents, which indicate increased recombination losses.

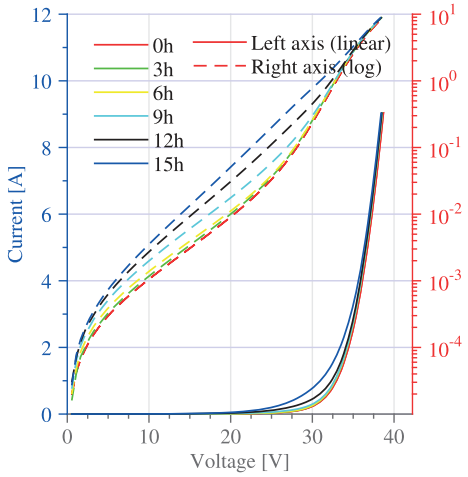

Figure 8. Example of dark *I–V* characteristic curves for module A-2, undergoing 15 h of system voltage stress (−1000 V) at elevated temperature and humidity (60 °C/85% RH), measured *in situ* at 25 °C by ramping down the module temperature every 3 h. The 25 °C P_{max} degraded down to 91.4% of the initial value.

Next, the two-diode model parameters, shown in Figure 9, are curve-fitted from dark *I–V* measurements acquired at reference temperature $T_{ref} = 25\,°C$ and a stress temperature $T_{stress} = 60\,°C$, at the start and end of each 3-h stress cycle. As module A-2 reached the end of the fifth stress cycle, totaling 15 h of PID stress with P_{deg} (*15 h*, 25 °C) = 91.4% remaining power after the degradation (blue dark *I–V* lines and dashes in Figure 8), the two-diode model curve-fitting started to fail. This is to be expected considering that the assumptions for applying the two-diode model to a PV module are that all the cells within the module can be aggregated for modeling purposes. This aggregation cannot be assumed for pronounced PID-type degradation, where the cells near the module frame degrade faster than the ones in the center, due to the increased conductivity paths near the edges of the module.

Up to the model breakdown occurring after 15 h of PID stress, we can observe in Figure 9 the following: increased J_{02} diode saturation current due to additional recombination losses occurring in the module, as well as a near-constant series resistance (up to 12 h of stress when the model starts to break down). Similar findings were reported in [1]; however, to the extent we could apply the two-diode model, an increase in the second diode ideality factor was not found in this module design.

By examining the 25 and 60 °C data obtained from the two-diode model parameters in Figure 9, we can observe that the diode saturation currents increase significantly with temperature, as was expected. Similarly, the ideality factors n_1 and n_2 also show a slight decrease with temperature, as reported in the literature [30–32]. The lumped series resistance R_s calculated from the dark *I–V* characteristic is increasing with temperature, which can be explained by the distributed nature of the solar cell series resistance, and the differences between dark and light operating conditions [33]. In light conditions, the current is generated approximately uniformly across the solar cell; in dark conditions, the current is conducted along the paths

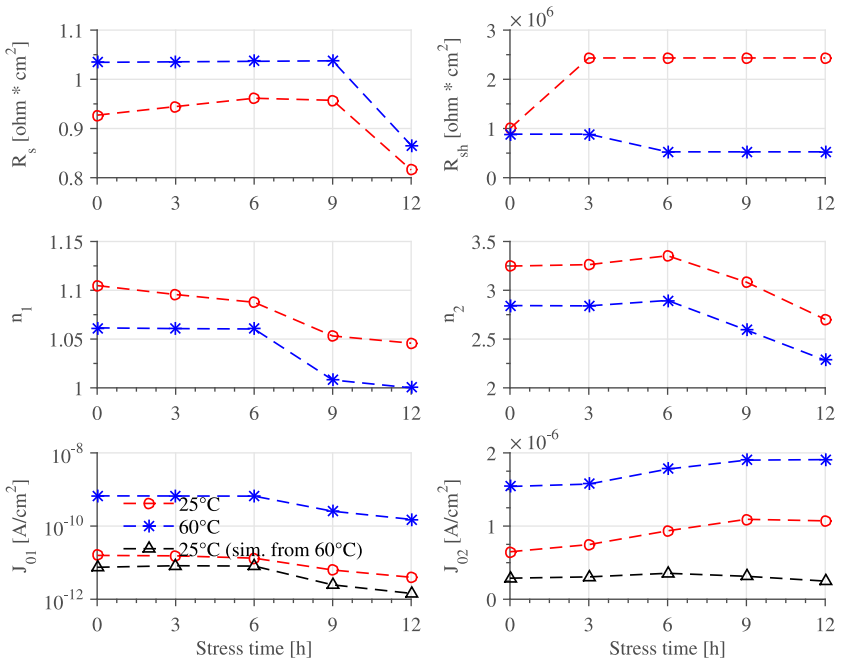

Figure 9. Two-diode model parameters for module A-2 (undergoing PID) as a function of PID stress duration. The model parameters are fitted from the 25 °C dark *I–V* curves, measured *in situ* every 3 h.

DOI: 10.1002/pip

with the lowest resistivity, which is mostly of a metallic nature (busbars, grid fingers); thus, the "dark" lumped series resistance increases with temperature. Similar results have been reported for dark *I–V* measurements in [16,34]. The shunt resistance R_{sh} fitting parameter has been limited to 5×10^5 Ωcm^2, because larger values have no significant effect on the curve-fitting results.

The values of material parameters γ_1, γ_2, m_1, m_2 and the 25 °C energy bandgap Eg_{ref} are assumed from the literature ($\gamma_1 = 3$, $\gamma_2 = 3/2$, $m_1 = n_1/1.07$, $m_2 = n_2/1.07$, and $Eg_{\text{ref}} = 1.14$ eV) [16,26,27,29], and in conjunction with Eq. (7–9), they are used to translate the J_{01}(60 °C) and J_{02}(60 °C) saturation currents, fitted from 60 °C dark *I–V* measurements, to the reference temperature (25 °C). The results of the temperature translation (from 60 to 25 °C) are plotted in Figure 9, with black lines. The temperature-translated saturation currents do not match exactly those obtained from curve-fitting the 25 °C dark *I–V* measurements, and they seem to diverge as the module degrades. This divergence would indicate PV device properties that are not captured by the model, or imply inaccuracies in identifying or choosing some of the model parameters, such as γ_1, γ_2, m_1, or m_2.

Despite these modeling inaccuracies, if we simulate the 25 °C dark *I–V* characteristics using the temperature-translated model parameters (originally curve-fitted from 60 °C) and calculate the P_{max} degradation from these dark *I–V* curves using the superposition method as previously described, we can observe in Figure 10 that the "25 °C-simulated" P_{max} degradation curve (black) lies between the "25 °C-measured" (red) and "60 °C-measured" (blue) P_{max} degradation curves.

Although the "25 °C-simulated" P_{max} degradation curve that was obtained by temperature-translating the 60 °C two-diode model parameters does not perfectly match the "25 °C-measured" degradation curve (which is our best estimation of the real STC P_{max} degradation), it is a closer match than the "60 °C-measured" degradation curve, for low power loss levels (3–5%). This method could be further improved by identifying more accurate values for some of the model parameters.

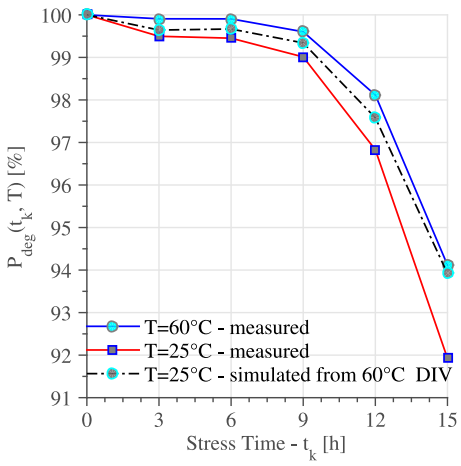

Figure 10. Maximum power (P_{max}) degradation curves for module A-2 calculated from: the dark *I–V* measurements at 25 °C—red; dark *I–V* measurements at 60 °C—blue; and the 25 °C simulated dark *I–V* measurements—black, obtained by the temperature-translating (to 25 °C) of the two-diode model parameters (curve-fitted from the 60 °C dark *I–V*).

When the module power degradation exceeds 5%, the "25 °C-simulated" P_{max} degradation curve starts to deviate from the "25 °C-measured" degradation curve, signifying that the power-loss correction using the diode temperature translation equations starts to deteriorate. This is most probably a limitation of the curve-fitting, the assumptions made, and of the two-diode model applied to PV modules degrading by PID. If we look at the dark *I–V* measurements of the module of the last stress cycle (at 15 h blue) in Figure 8, we can observe that the dark *I–V* characteristic does not exhibit typical two-diode behavior. This is to be expected because the PV module dark *I–V* curve represents an aggregation of the dark *I–V* characteristics of its constituent solar cells, which usually lose their diode-like characteristics unevenly through PID.

Furthermore, we did not investigate the extent to which the temperature dependence of the other model parameters (R_s, R_{sh}, n_1, n_2) affects the power-loss estimation. If this dependence is significant, then it should be modeled as well.

3.5. Correction of the power-loss estimation using the error compensation method

As was shown in the previous two sections, the P_{max} temperature coefficient γ_{dark} changes as the PV module degrades through PID; thus, a constant γ_{dark} coefficient cannot be used to accurately translate P_{max} degradation measured at a stress temperature down to 25 °C, which is the most often-cited benchmark for power performance of PV modules. Furthermore, curve-fitting the two-diode model to the dark *I–V* characteristics measured at the stress temperature, and then translating the model parameters to 25 °C conditions, for estimating the 25 °C dark *I–V* curve from them, has proven unsuccessful. This problem is caused by the failure of the model to account for all changes in material properties, which is a consequence of PID, as well. Still, we need a simple and accurate method for correctly estimating P_{max} degradation at STC when measuring a dark *I–V* curve at the stress temperature *in situ* in the chamber. Next, we will present a simple empirical method that compensates for the power loss measured at the stress temperature to match the power loss measured at STC.

By analyzing Figures 4 and 5, where the relative power-loss estimation error δP_{deg} is plotted versus the P_{max} degradation at 25 °C, we can observe a near-linear relationship between them for a given stress temperature and module design. Thus, if we can approximate what the estimation error would be for a given power-loss level, stress

temperature, and module design, we can compensate it. This can be achieved by modeling the power-loss estimation error as a linear function of the P_{max} degradation measured at the stress temperature. The parameters of the linear function can be easily calculated from P_{max} degradation measurements (at stress and reference temperature, i.e., 25 °C), performed at the end of the experiment, for each module. Once the linear function has been identified, we can approximate what the power-loss estimation error would be for intermediate P_{max} degradation measurements (at the stress temperature) and compensate for the error.

To demonstrate the error compensation method, we denote $d(t_k, T_{stress})$ to be the *absolute power-loss estimation error*, for a measurement point t_k during the PID test at the stress temperature T_{stress}. This error can be calculated as the difference between the dark *I–V*-determined P_{max} degradation, measured at the stress temperature, and the "real" degradation, namely P_{max} degradation measured at 25 °C (either by dark *I–V* or light *I–V* characterization, equivalently) as in (10). The absolute power-loss estimation error curve $d(t_k, T_{stress})$ is depicted in Figure 11 (red curve) for module D-1.

$$d(t_k, T_{stress}) = P_{deg}(t_k, T_{stress}) - P_{deg}(t_k, 25°C) \quad (10)$$

The error curve $d(t_k, T_{stress})$ is specific for each module and stress temperature and depends on the degradation level of the module. Because the real error curve cannot be measured directly during the PID stress test (which would require ramping down the chamber/module temperature to 25 °C), we approximate it with the linear relationship $\hat{d}(t_k, T_{stress})$ as in (11), considering the found near-linear dependence between the error d and the P_{max} degradation measured at the stress temperature. The linear relationship $\hat{d}(t_k, T_{stress})$ consists of a proportion (or slope) m and an intercept b, and it can be easily calculated from two points of the real error curve $d(t_k, T_{stress})$. If we consider t_0 to be the initial measurement point, before the degradation of the module starts, then the absolute power-loss estimation error becomes $d(t_0, T_{stress}) = 0$, and the P_{max} degradation measured at the stress temperature $P_{deg}(t_0, T_{stress}) = 1$. Similarly, t_n will be the final measurement point, at the end of the PID stress test, when the P_{max} degradation is measured at the stress temperature, and then again at 25 °C, from which $d(t_n, T_{stress})$ is calculated as in (10). From these two measurement points (t_0 and t_n) for which we know both $d(t_{0,n}, T_{stress})$ and $P_{deg}(t_{0,n}, T_{stress})$, we can calculate the parameters (slope m and intercept b) of the linear approximation function $\hat{d}(t_k, T_{stress})$, as in (11). An example of this approximation function is depicted in Figure 11 (blue curve) for module D-1.

$$\hat{d}(t_k, T_{stress}) = mP_{deg}(t_k, T_{stress}) + b = \frac{d(t_n, T_{stress})}{P_{deg}(t_n, T_{stress}) - 1}\left[P_{deg}(t_k, T_{stress} - 1)\right] \quad (11)$$

Finally, correcting the P_{max} degradation to 25 °C conditions at any measurement point t_k during the PID test becomes straightforward by replacing $d(t_k, T_{stress})$ in (10) with its linear approximation $\hat{d}(t_k, T_{stress})$, and solving for $P_{deg}(t_k,\ 25°C)$, denoted as $\hat{P}_{deg}(t_k,\ 25°C)$ in (12). Figure 12 shows the corrected P_{max} degradation curve $\hat{P}_{deg}(t_k,\ 25°C)$, compared with the 25 and 60 °C measured degradation curves, for module D-1. The corrected P_{max}

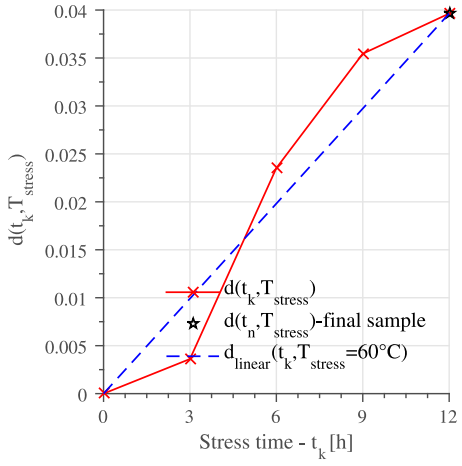

Figure 11. Example of the P_{max} absolute power-loss estimation error d, measured at a stress temperature of 60 °C for module D-1. The red curve represents the measured error (relative to the 25 °C reference measurement); the blue curve represents the linear approximation of the error, resulting from fitting the initial and final values of the measured error.

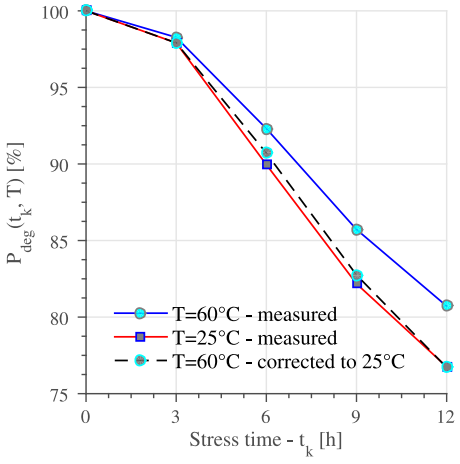

Figure 12. Example of the error compensation method, for translating the maximum power degradation (P_{deg}) for module D-1, measured at a stress temperature of 60 °C, down to 25 °C conditions. The P_{deg} curve, calculated from 25 °C dark *I–V* measurements (red), matches the corrected 25 °C degradation curve (black) very well. This curve (black) was adjusted using the error compensation method from the measured 60 °C degradation curve (blue).

degradation curve matches the measured degradation curve very well.

$$\hat{P}_{\mathrm{deg}}(t_k, 25°\mathrm{C}) = P_{\mathrm{deg}}(t_k, T_{\mathrm{stress}}) - \frac{d(t_n, T_{\mathrm{stress}})\left[P_{\mathrm{deg}}(t_k, T_{\mathrm{stress}}) - 1\right]}{P_{\mathrm{deg}}(t_n, T_{\mathrm{stress}}) - 1} \quad (12)$$

To validate the method and quantify its performance, the 60 °C P_{max} degradation curves for all PV module test samples (Figure 3) are corrected to 25 °C conditions, and the relative estimation error δP_{deg}, calculated as in (2), is plotted in Figure 13a. If we compare the relative error δP_{deg} before correction (Figure 4) with the relative error calculated after correction (Figure 13a), we can observe a significant reduction.

To better quantify the performance of the method, we calculate a normalized residual sum of squares RSS_{NORM} as in (13), which measures how much the estimation error has been reduced after correction, in relative percent values.

$$RSS_{NORM}[\%] = \frac{\sum_{k=0}^{n}\left[\hat{P}_{\mathrm{deg}}(t_k, 25°C) - P_{\mathrm{deg}}(t_k, 25°C)\right]^2}{\sum_{k=0}^{n}\left[P_{\mathrm{deg}}(t_k, T_{\mathrm{stress}}) - P_{\mathrm{deg}}(t_k, 25°C)\right]^2} * 100 \quad (13)$$

From Figure 13b, we can observe, for example, that the total estimation error for module A-1 has been reduced about 5.8 times, close to 17% of the initial estimation error. The reduction in error for the other module samples is even greater. Considering that errors in flash testing also exist, we conclude that our method achieves cost reduction and more rapid and greater accumulation of statistical data for future application of various statistical reliability models because of: the time savings for not ramping sample temperature to and from the stress temperature to 25 °C, the reductions in stress transients while ramping to and from the stress temperature, and elimination of flash testing except at the initial and (optionally) final data points.

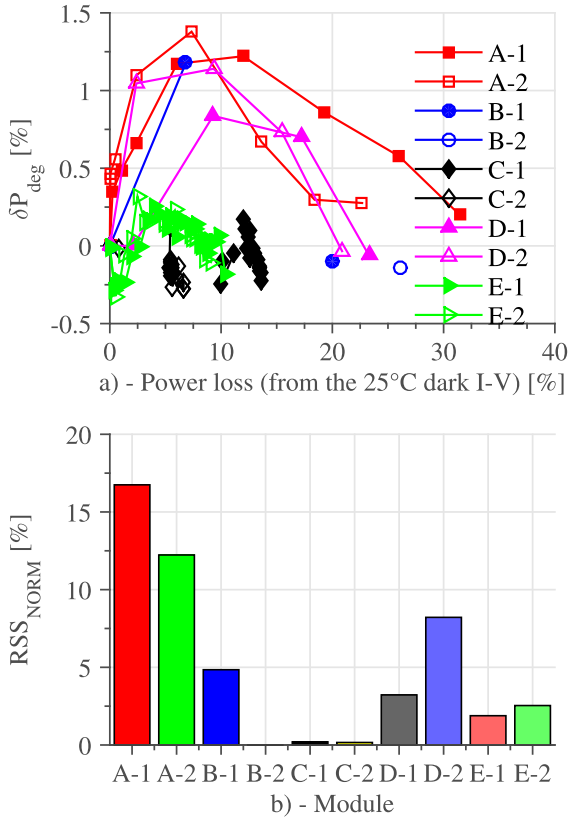

Figure 13. Summary of the relative power-loss estimation error δP_{deg} (from 60 °C to 25 °C), calculated for all photovoltaic modules, after the error compensation. (a) Upper graph is the δP_{deg} obtained after the error compensation, as a function of module power degradation. (b) Lower graph is the total (integrated) estimation error after the correction, calculated as a residual sum of squares (*RSSNORM*) and a percentage of the initial estimation error (before correction).

4. SUMMARY AND CONCLUSIONS

Potential-induced degradation studies (through environmental chamber testing or field testing) require accurate performance characterization measurements during the module degradation process, which often need to be reported at STC, which is the most often-cited benchmark for power performance of PV modules. This reporting poses difficulties, both for PID field testing and chamber testing, where modules usually operate at a temperature higher than 25 °C. Similarly, performance characterization of modules undergoing chamber PID stress testing generally involves intermittently ramping down the module temperature to 25 °C, performing *in situ* characterization of the module performance (through superposition of the dark *I–V* characteristics), or much more frequently, removing the module from the chamber and measuring power on a flash tester, which can require considerable time and effort when numerous samples are involved.

We proposed to expand the *in situ* characterization method based on the superposition of the dark *I–V* characteristics to be applied at the elevated stress temperature of the PID test, instead of 25 °C. This avoids stress transients while ramping to and from the stress temperature, and eliminates flash testing except at the initial and final data points.

For this purpose, we designed and performed a PID chamber experiment, in which five crystalline module designs with two replicates each underwent system voltage stress testing at 60 °C and 85% RH, with negative voltage bias −1000 V applied between the active material (shorted leads) and the frame of each module. Every 3 h, the dark *I–V* characteristic of each module was acquired at 60, 50, 40, 30, and 25 °C by automatically ramping down the chamber temperature and RH.

The first goal of the experiment was to determine the extent to which the temperature dependency of P_{max} is affected by the degradation of the modules through PID. The results showed there is a mismatch between the P_{max} degradation measured at the stress temperature and the P_{max} degradation measured at 25 °C; the difference depends on module design, stress temperature, and level of degradation.

Next, we attempted to correct this mismatch error using two P_{max} temperature-translation methods found in the literature. We found from experimental results that the well-known P_{max} temperature coefficient, which has been previously shown to approximate reasonably well the relationship between P_{max} and temperature for crystalline PV modules at a constant irradiance, cannot be applied in this case, because the temperature coefficient changes as the PV module degrades.

A second method we investigated for correcting the mismatch in P_{max} degradation estimates explores the capability of the two-diode model to translate dark *I–V* characteristic curves measured at the stress temperature down to 25 °C conditions as the PV module degrades through PID. From our analysis, we observed increased J_{02} diode saturation current caused by additional recombination losses occurring in the module, as well as a near-constant series resistance similar to what was reported in the literature, until the model begins to break down. Although the two-diode model has been successfully employed over the years to investigate and understand the operation of solar cells, it has limited applicability to the temperature translation of the *I–V* characteristic of a module undergoing PID, because the modeling assumption that all cells within the PV module can be lumped together may break down if the module degrades nonuniformly through PID, as occurred in this study. Extracting two-diode model parameters allows for fundamental analysis of the degradation. An increase in saturation current over the course of PID is found to correspond to a reduction in temperature dependency of P_{max} (γ_{dark} coefficient). PID may be reducing the proportion of temperature-sensitive pathways for recombination. Other constants in the model may also be changing with temperature, including the pre-exponentials and bandgap activation energy. As a consequence, the two-diode model does not lend itself to large-scale data collection and analysis because of the difficulty of curve fitting.

Finally, we proposed a simple and accurate method for compensating for the mismatch/estimation error between the P_{max} degradation measure at the stress temperature and P_{max} degradation measured at 25 °C, by taking advantage of the pseudo-linear relationship between the mismatch and P_{max} degradation, which has been observed experimentally. A mathematical formulation has been derived for the error compensation method, which requires only the initial and final P_{max} degradation data points (measured at the stress temperature and 25 °C) for parameterization. Afterwards, any P_{max} degradation point measured during the PID test at the stress temperature can be accurately translated to STC, which was validated experimentally herein for 10 crystalline silicon PV modules within five module designs tested.

Implementing the proposed method for PID chamber studies would achieve cost reductions (simpler test hardware and less laboratory personnel effort) and would lead to more rapid and greater accumulation of statistical data for future application of various statistical reliability models.

For future work, we propose to apply the error compensation method of the P_{max} degradation to PID field studies. Performance data of fielded PV modules, degrading through PID, must be reported to STC for it to be comparable with other field or chamber studies. If the module performance is measured directly in light conditions, the possible degradation of the light P_{max} temperature dependency remains unclear and has to be investigated and compensated for, if necessary. A more direct approach would be to regularly measure the dark *I–V* curves of the modules (by covering them and performing the measurements during the night), after which we can apply the superposition and the temperature-correction method proposed here to calculate the P_{max} degradation at STC, at different points during the module degradation. Thus, we would avoid having to dismount the module from the field array and characterize its performance with a solar simulator.

ACKNOWLEDGEMENTS

The authors thank Bill Marion and Sarah Kurtz for helpful discussions; Garry Babbitt for developing the hardware of the experimental setup; Greg Perrin and Kent Terwilliger for their help performing the experiments; Steve Glick and Steve Rummel for module measurements. This work was realized within the research project “Smart photovoltaic systems”, project no. 10648 supported by Energinet.dk, Aalborg University, as well as the U.S. Department of Energy under Contract No. DE-AC36-08-GO28308 with the National Renewable Energy Laboratory.

REFERENCES

1. Hacke P, Smith R, Terwilliger K, Glick S, Jordan D, Johnston S, Kempe M, Kurtz S. Testing and analysis for lifetime prediction of crystalline silicon PV modules undergoing degradation by system voltage stress. *IEEE Journal of Photovoltaics* 2013; **3**(1): 246–253. DOI: 10.1109/Jphotov.2012.2222351
2. Desharnais RA. Characterizing the Impact of Potential-Induced Degradation and Recovery on the Irradiance and Temperature Dependence of Photovoltaic Modules. in 29th European Photovoltaic Solar Energy Conference and Exhibition. 2014. Amsterdam, Netherlands. DOI: 10.4229/EUPVSEC20142014-5CO.14.4

3. Hacke P, Terwilliger K, Kurtz S. In-situ measurement of crystalline silicon modules undergoing potential-induced degradation in damp heat stress testing for estimation of low-light power performance. 2013, National Renewable Energy Laboratory (NREL), Golden, CO. p. 1-10. Report NREL/TP-5200-60044. DOI: 10.2172/1090973
4. Pingel S, Frank O, Winkler M, Daryan S, Geipel T, Hoehne H, Berghold J. Potential induced degradation of solar cells and panels. in 35th IEEE Photovoltaic Specialists Conference. 2010. Honolulu, Hawaii. DOI: 10.1109/PVSC.2010.5616823
5. Nagel H, Metz A, Wangemann K. Crystalline Si solar cells and modules featuring excellent stability against potential-induced degradation. in 26th European Photovoltaic Solar Energy Conference and Exhibition. 2011. Hamburg, Germany. DOI: 10.4229/26thEUPVSEC2011-4CO.5.6
6. Hishikawa Y, Imura Y, Oshiro T. Irradiance-dependence and translation of the I-V characteristics of crystalline silicon solar cells. In 28th IEEE Photovoltaic Specialists Conference. 2000. Anchorage, Alaska DOI: 10.1109/PVSC.2000.916169
7. Lindholm FA, Fossum JG, Burgess EL. Application of the superposition principle to solar-cell analysis. *IEEE Transactions on Electron Devices* 1979; **26**(3): 165–171. DOI: 10.1109/T-ED.1979.19400
8. Wolf M, Rauschenbach H. Series resistance effects on solar cell measurements. *Advanced Energy Conversion* 1963; **3**(2): 455–479. DOI: 10.1016/0365-1789(63)90063-8
9. Robinson SJ, Aberle AG, Green MA. Departures from the principle of superposition in silicon solar cells. *Journal of Applied Physics* 1994; **76**(12): 7920–7930. DOI: 10.1063/1.357902
10. Altermatt PP, Heiser G, Aberle AG, Wang A, Zhao J, Robinson SJ, Bowden S, Green MA. Spatially resolved analysis and minimization of resistive losses in high-efficiency Si solar cells. *Progress in Photovoltaics: Research and Applications* 1996; **4**(6): 399–414. DOI: 10.1002/(SICI)1099-159X(199611/12)4:6<399::AID-PIP148>3.0.CO;2-4
11. Breitenstein O. Understanding the current-voltage characteristics of industrial crystalline silicon solar cells by considering inhomogeneous current distributions. *Opto-Electronics Review* 2013; **21**(3): 259–282. DOI: 10.2478/s11772-013-0095-5
12. Robinson SJ, Wenham SR, Altermatt PP, Aberle AG, Heiser G, Green MA. Recombination rate saturation mechanisms at oxidized surfaces of high-efficiency silicon solar cells. *Journal of Applied Physics* 1995; **78**(7): 4740–4754. DOI: 10.1063/1.359821
13. Tarr NG, Pulfrey DL. An investigation of dark current and photocurrent superposition in photovoltaic devices. *Solid-State Electronics* 1979; **22**(3): 265–270. DOI: 10.1016/0038-1101(79)90032-7
14. Wolf M, Noel GT, Stirn RJ. Investigation of the double exponential in the current-voltage characteristics of silicon solar cells. *IEEE Transaction on Electron Devices* 1977. **24**(4): 419–428. DOI: 10.1109/T-ED.1977.18750
15. King DL, Hansen BR, Kratochvil JA, Quintana MA. Dark current-voltage measurements on photovoltaic modules as a diagnostic or manufacturing tool. *Conference Record of the Twenty-Sixth IEEE Photovoltaic Specialists Conference* 1997. DOI: 10.1109/PVSC.1997.654286
16. Gow JA, Manning CD. Development of a photovoltaic array model for use in power-electronics simulation studies. *Electric Power Applications, IEE Proceedings* 1999; **146**(2): 193–200. DOI: 10.1049/ip-epa:19990116
17. Nann S, Emery K. Spectral effects on PV-device rating. *Solar Energy Materials and Solar Cells* 1992; **27**(3): 189–216. DOI: 10.1016/0927-0248(92)90083-2
18. Brei tenstein O, Bauer J, Altermatt PP, Ramspeck K. Influence of defects on solar cell characteristics. *Solid State Phenomena* 2010; **156**: 1–10. DOI: 10.4028/www.scientific.net/SSP.156-158.1
19. Hacke P, Terwilliger K, Smith R, Glick S, Pankow J, Kempe M, Bennett SKI, Kloos M. System voltage potential-induced degradation mechanisms in PV modules and methods for test. in Photovoltaic Specialists Conference (PVSC), 2011 37th IEEE. 2011. DOI: 10.1109/PVSC.2011.6186079
20. Hacke P, Smith R, Terwilliger K, Glick S, Jordan D, Johnston S, Kempe M, Kurtz S. Acceleration factor determination for potential-induced degradation in crystalline silicon PV modules. in 2013 IEEE International Reliability Physics Symposium (IRPS). 2013. Monterey, California. DOI: 10.1109/IRPS.2013.6532009
21. Emery K, Burdick J, Caiyem Y, Dunlavy D, Field H, Kroposki B, Moriarty T, Ottoson L, Rummel S, Strand T, Wanlass MW. Temperature dependence of photovoltaic cells, modules and systems. In 25th IEEE Photovoltaic Specialists Conference. 1996. Washington, D.C. DOI: 10.1109/PVSC.1996.564365
22. King DL, Kratochvil JA, Boyson WE. Temperature coefficients for PV modules and arrays: measurement methods, difficulties, and results. In Photovoltaic Specialists Conference, 1997., Conference Record of the Twenty-Sixth IEEE. 1997. DOI: 10.1109/PVSC.1997.654300

23. Ishii T, Otani K, Takashima T, Kawai S. Estimation of the maximum power temperature coefficients of PV modules at different time scales. *Solar Energy Materials and Solar Cells* 2011; **95**(1): 386–389. DOI: 10.1016/j.solmat.2010.04.041
24. Van Dyk E, Meyer E, Leitch A, Scott B. Temperature dependence of performance of crystalline silicon photovoltaic modules. *South African Journal of Science* 2000; **96**(4): 198–200.
25. Skoplaki E, Palyvos JA. On the temperature dependence of photovoltaic module electrical performance: a review of efficiency/power correlations. *Solar Energy* 2009; **83**(5): 614–624. DOI: 10.1016/j.solener.2008.10.008
26. Fan JCC. Theoretical temperature dependence of solar cell parameters. *Solar Cells* 1986; **17**(2–3): 309–315. DOI: 10.1016/0379-6787(86)90020-7
27. Green MA. General temperature dependence of solar cell performance and implications for device modelling. *Progress in Photovoltaics: Research and Applications* 2003; **11**(5): 333–340. DOI: 10.1002/pip.496
28. Singh P, Ravindra NM. Temperature dependence of solar cell performance—an analysis. *Solar Energy Materials and Solar Cells* 2012; **101**: 36–45. DOI: 10.1016/j.solmat.2012.02.019
29. De Soto W, Klein SA, Beckman WA. Improvement and validation of a model for photovoltaic array performance. *Solar Energy* 2006; **80**(1): 78–88. DOI: 10.1016/j.solener.2005.06.010
30. Cuce E, Cuce PM, Bali T. An experimental analysis of illumination intensity and temperature dependency of photovoltaic cell parameters. *Applied Energy* 2013; **111**: 374–382. DOI: 10.1016/j.apenergy.2013.05.025
31. Singh P, Singh SN, Lal M, Husain M. Temperature dependence of I–V characteristics and performance parameters of silicon solar cell. *Solar Energy Materials and Solar Cells* 2008; **92**(12): 1611–1616. DOI: 10.1016/j.solmat.2008.07.010
32. Forero N, Hernandez J, Gordillo G. Development of a monitoring system for a PV solar plant. *Energy Conversion and Management* 2006; **47**(15-16): 2329–2336. DOI: 10.1016/j.enconman.2005.11.012
33. Aberle AG, Wenham SR, Green MA. A new method for accurate measurements of the lumped series resistance of solar cells. In 23rd IEEE Photovoltaic Specialists Conference. 1993. Louisville Kentucky DOI: 10.1109/PVSC.1993.347065
34. Radziemska E. Effect of temperature on dark current characteristics of silicon solar cells and diodes. *International Journal of Energy Research* 2006; **30**(2): 127–134. DOI: 10.1002/er.1113