Temperature-Dependent Characterization of AlGaN/GaN HEMTs: Thermal and Source/Drain Resistances

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(Invited Paper)

***Abstract*—This paper shows the application of simple dc techniques to the temperature-dependent characterization of AlGaN/GaN HEMTs in terms of the following: 1) thermal resistance and 2) ohmic series resistance (at low drain bias). Despite their simplicity, these measurement techniques are shown to give valuable information about the device behavior over a wide range of ambient/channel temperatures. The experimental results are validated by comparison with independent measurements and numerical simulations.**

***Index Terms*—Gallium compounds, microwave power transistors, MODFETs, power HEMTs, semiconductor-device measurements, semiconductor-device thermal factors, wide bandgap semiconductors, III nitrides, III–V semiconductors.**

I. Introduction

WITH UNPARALLELED output power densities such as 12 W/mm at 4 GHz (sapphire substrate) [1] or 5.1 W/mm at 18 GHz (Si substrate) [2], GaN-based HEMTs show excellent microwave power performance. High-power operation requires high power dissipation and, consequently, the need to carefully account for thermal effects when designing and modeling devices and circuits. Reliability estimates also require accurate evaluation of channel temperatures (T_C) when the accelerated life-testing data are used to extrapolate operating lifetimes.

The aim of this paper, which expands on the previous conference communications [3], [4], is to contribute to the topic of temperature characterization of AlGaN/GaN HEMTs by proposing and applying two simple dc techniques for the fast evaluation of the values and temperature dependence of the following: 1) the channel-to-base-plate (or ambient) thermal resistance R_{TH} and 2) the low-field parasitic source/drain series resistance $R_S + R_D$. While the usefulness of a simple method for extracting T_C and R_{TH} is obvious for both modeling and reliability estimation purposes, a quick experimental technique to evaluate $R_S + R_D$ is advantageous, for instance, when different process options for the ohmic contacts are to be compared with the finished HEMTs rather than with TLM or other *ad hoc* test patterns. Moreover, the source/drain parasitic resistances are tightly connected with the well-known current collapse mechanism [5], which is one of the main reliability concerns for GaN-based FETs. Finally, we will show that the extraction procedure defines a simple, yet accurate, analytical model of the drain current at low drain bias.

As far as channel-temperature or thermal-resistance measurements are concerned, several papers have been published over the years, indicating how self-heating evaluation is critical for the AlGaN/GaN HEMTs. In particular, micro-Raman spectroscopy has proven to be a powerful technique [6]–[8] for measuring temperature profiles with high spatial resolution; variants were also demonstrated, which offer time-resolved measurements [9] and 3-D mapping [10], whereas a hybrid Raman/infrared (IR) approach [11] allows for the analysis of large multimaterial structures. Other studies involved liquid crystal thermography [12], photocurrent measurements [13], and scanning thermal microscopy [14]. Each of these direct techniques has its own strengths and weaknesses; generally speaking, they offer the distinctive advantage of some degree of spatial resolution (allowing, for instance, resolution of temperature differences among different gate fingers) but often require costly equipment and time-consuming measurement sessions.

Indirect electrical techniques cannot convey any space-resolved information but are, on the other hand, simpler and cheaper than direct ones. One classical method for extracting T_C and R_{TH} is by comparing temperature-dependent fast-pulsed measurements with dc measurements; examples of application to AlGaN/GaN HEMTs can be found in [15]–[17].

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Pulsed techniques do not generally require simplifying assumptions and can provide some information on self-heating dynamics, but one must take care not to mistake electrical transients for thermal ones [15]; moreover, clean, nanosecond-scale, and temperature-dependent pulsed measurements are not easy to perform (particularly on high-power devices) and require *ad hoc* setups and significant measurement effort.

DC electrical techniques are obviously the simplest and cheapest, since they are often relying only on standard I–V measurements at different ambient temperatures. The main drawback with respect to pulsed methods is the need to rely sometimes on drastic simplifying assumptions [18], [19], including the independence of the thermal resistance with temperature and dissipated power. However, very few research works have been published in terms of simple dc electrical techniques for measuring R_{TH}.

A variant of the method developed in [20] for LDMOSFETs is applied here for the first time to extract the R_{TH} of an AlGaN/GaN HEMT. The method assumes a linear dependence of the drain current (I_D) on the channel temperature once the linear dependence of I_D on the ambient temperature (T_A) has been experimentally demonstrated. It therefore relies on the choice of suitably narrow intervals of T_A and dissipated power (P_D), wherein the drain–current temperature dependence can be linearized with good accuracy and R_{TH} can be considered constant; apart from this, no other simplifying assumption is necessary. This R_{TH} extraction procedure requires only dc I–V output curves measured at different ambient temperatures, which is a distinct advantage over classical pulse-based approaches.

As far as the parasitic source/drain resistances are concerned, it is recognized that they play a significant role in limiting the performance of microwave AlGaN/GaN FETs [21]–[25], and novel design and processing concepts have been devised for reducing them [26]–[28]. Their increase is also a serious reliability concern in the current collapse effect [5]. However, measuring these parasitics on individual FETs is not a straightforward task. The estimation is typically tackled either by numerical optimization or analytical manipulation of small-signal models [29], [30] or by relying on bias conditions that are quite far from operating conditions (e.g., the end-resistance technique [31] and its variants [32]). A disadvantage of the former approach is that it is difficult to attach a clear physical meaning to the extracted resistance values; on the other hand, the latter approach measures R_S and R_D under bias conditions where the current flow is very far from normal.

A classical technique for the measurement of compound semiconductor FET source and drain parasitic resistances at low longitudinal electric field is the one proposed by Fukui [33] for GaAs MESFETs. It rests on the assumption that the device can be divided into an intrinsic region obeying the gradual channel approximation (GCA), and therefore some simple analytical current–voltage relationship, and an extrinsic parasitic-resistance region that is not perturbed by the gate voltage. This automatically endows the extracted parasitics with a definite physical meaning; R_S and R_D measure the resistance existing between the ohmic contacts and the device region obeying the GCA (provided that one such region exists).

This paper, for the first time, applies (a modification of) Fukui's technique to the measurement of $R_S + R_D$ of an AlGaN/GaN HEMT and its temperature dependence. The validity of the underlying assumptions is discussed and supported by independent measurements.

This paper is therefore organized as follows. Section II briefly describes the HEMT under test and the additional structures measured to support the parasitic-resistance measurements. In Section III, we illustrate the procedure to measure R_{TH} and show and discuss the results it gives; Section IV does the same for the measurement of the source and drain parasitic resistances. Conclusion is given in Section V.

II. HEMTs Under Test

The devices under test were AlGaN/GaN HEMTs grown and processed at the University of California, Santa Barbara.

They were grown on a 325-μm-thick sapphire substrate. A 0.7-μm Fe-doped GaN layer is followed by 50 nm of AlN, on top of which lies the 1.7-μm-thick unintentionally doped GaN layer hosting the 2DEG; this is separated from the 29-nm Si-doped $\mathrm{Al_{0.22}Ga_{0.78}N}$ layer on top by a thin (0.6 nm) AlN interfacial layer for an improved 2DEG confinement.

The gate length is $L_G = 0.9$ μm, and the width is $W_G =$ 150 μm. The source–gate and drain–gate separations are 0.7 and 1 μm, respectively.

A long-gate HEMT with $L_G = 20$ μm, $W_G = 300$ μm, and $5 + 5$ μm-long ungated regions was also used for Hall-effect measurements of the 2DEG carrier density (n_S) and mobility (μ_n) versus gate bias, whereas temperature-dependent low-field 2DEG mobilities were extracted on a 40×400 μm ungated HEMT.

Although sapphire substrates are thermally outperformed by SiC and Si ones, sapphire wafers are much cheaper than SiC ones, and the growth of HEMT templates on sapphire is more mature than on silicon. It should also be noted that recent reports show how the problem of poor thermal conduction via the substrate can be overcome by using front-side cooling techniques [34], [35]. Moreover, the thermal performance of the substrate, which can be a serious problem in continuous-wave mode, tends to be less of a limiting factor when the HEMTs are operated in pulsed mode [36].

III. Thermal-Resistance Measurements

A. Method

Provided that the drain current I_D, at a fixed value of the gate–source voltage V_{GS0} and for a drain–source voltage V_{DS} biasing the HEMT in saturation, is experimentally observed to be a linear function of T_A, i.e.,

$$\begin{aligned} I_D(V_{\mathrm{GS0}}, V_{\mathrm{DS}}, T_A) &= I_D(V_{\mathrm{GS0}}, V_{\mathrm{DS}}, T_{\mathrm{A0}}) + h \cdot (T_A - T_{\mathrm{A0}}) \\ &= I_{\mathrm{D0}} + h \cdot (T_A - T_{\mathrm{A0}}) \end{aligned} \quad (1)$$

where T_{A0} is a reference ambient temperature, the parameter h can be measured by plotting I_D versus T_A and interpolating

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with a straight line. If it exists, the observed linear dependence (1) must be due to a linear dependence of I_D on T_C

$$I_D(V_{\mathrm{GS0}}, V_{\mathrm{DS}}, T_C) = I_{\mathrm{D0}} + h' \cdot (T_C - T_{\mathrm{C0}}) \tag{2}$$

where T_{C0} is the channel temperature determined by T_{A0}, V_{GS0}, and V_{DS}. However, by definition of the thermal resistance R_{TH}

$$T_C - T_{\mathrm{C0}} = T_A - T_{\mathrm{A0}} + R_{\mathrm{TH}} \cdot V_{\mathrm{DS}} \cdot (I_D - I_{\mathrm{D0}}) \tag{3}$$

hence substituting (3) into (2) and rearranging, one obtains

$$\frac{1}{h} = \frac{1}{h'} - R_{\mathrm{TH}} \cdot V_{\mathrm{DS}}. \tag{4}$$

By repeating this procedure at different values of V_{DS} in the saturation region, $1/h$ can be plotted versus V_{DS}. If the model is correct, the plot should be a straight line based on (4), and R_{TH} can be obtained as the slope of the best fit line.

B. Experimental Results

The HEMTs were mounted on open TO headers, and their dc output curves (together with other characteristics recorded for monitoring purposes) were measured inside a liquid He-cooled cryostat at various temperatures starting from $T_A = 74$ K, with 5-K temperature steps, up to 495 K. Each measurement point was taken after a 60-s delay to let the temperature settle. The gate–source voltage values were $V_{\mathrm{GS0}} = 0, -0.5$, and -1 V; at lower V_{GS}, self-heating is marginal, and the results become noisy. The T_A interval for R_{TH} extraction was fixed at 20 K. The section of the saturated region of the output curves used here spans from $V_{\mathrm{DS}} = 4$ to 10 V. While (4) is seen to hold well enough in the entire 4–10-V V_{DS} range for most of the temperatures, further restricting the V_{DS} range allows for a separate R_{TH} extraction in the lower (4–7 V) and upper (7–10 V) V_{DS} ranges, thus yielding information on the dependence of R_{TH} on P_D. Results are shown below for $T_A \geq 200$ K. For lower temperatures, the method gives nonphysical results, probably because the thermal conductivity of sapphire changes too much with temperature [37] for R_{TH} to be considered constant in a 20-K ambient temperature interval.

Fig. 1 shows the typical I_D versus T_A data. In all of the ambient temperature intervals probed, (1) is obeyed with good accuracy.

The values of $1/h$ obtained from the graphs similar to those in Fig. 1 have been plotted based on (4) to obtain R_{TH}. Fig. 2 shows an example of such plots.

A comprehensive plot of the results obtained for $V_{\mathrm{GS0}} = 0$ V is shown in Fig. 3. With only one exception (the 450-K data), the results are well behaved, with R_{TH} increasing as expected with ambient temperature and dissipated power. Plots corresponding to $V_{\mathrm{GS0}} = -0.5$ V and $V_{\mathrm{GS0}} = -1$ V look much like Fig. 3.

In order to have a comprehensive but readable chart showing the R_{TH} values obtained for all of the V_{GS0} values and also to check the internal consistency of the data, the thermal resistances can be used to compute the corresponding channel temperatures in each interval, and then, R_{TH} can be plotted as a function of T_C. Since the R_{TH} values have been extracted independently in several different T_A and P_D intervals, a well-behaved dependence of R_{TH} on T_C is not a self-fulfilling prophecy, and although it cannot be considered as

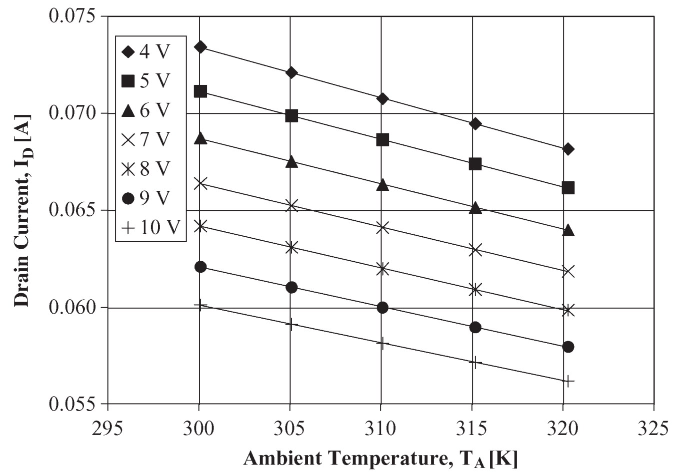

Fig. 1. Temperature dependence of I_D. Based on (1), the best fit lines yield the h value at each V_{DS} (shown in the legend). $V_{\mathrm{GS0}} = 0$ V.

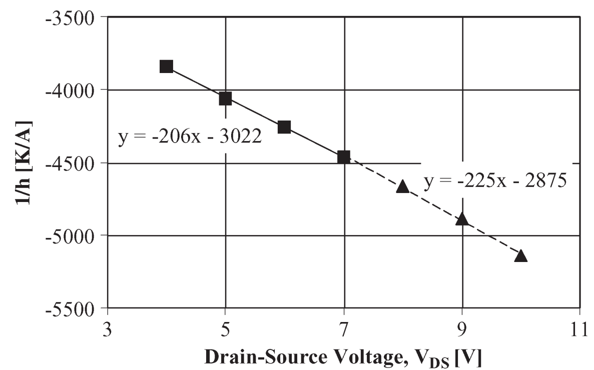

Fig. 2. Reciprocal of the h parameter [with h extracted from $I_D - T_A$ data based on (1)], which is plotted as a function of the drain–source voltage. Based on (4), the best fit line yields (solid line) $R_{\mathrm{TH}} = 206$ K/W for $V_{\mathrm{DS}} = 4$–7 V and (dashed line) $R_{\mathrm{TH}} = 225$ K/W for $V_{\mathrm{DS}} = 7$–10 V. $V_{\mathrm{GS0}} = 0$ V.

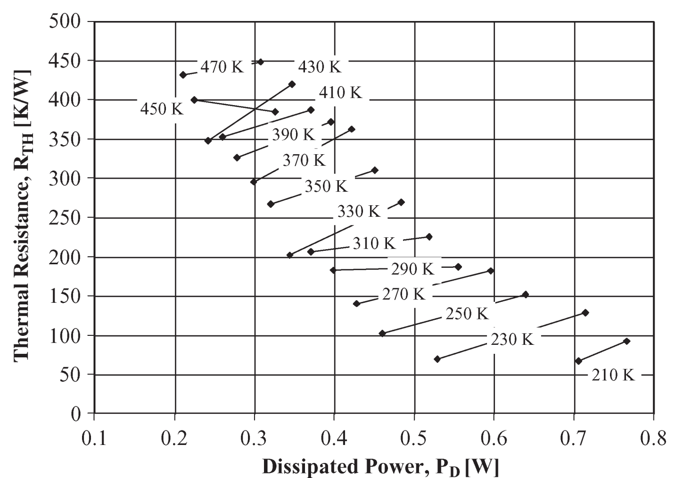

Fig. 3. Thermal resistance versus dissipated power at $V_{\mathrm{GS0}} = 0$ V. Each ambient temperature value is an average over a 20-K interval of T_A. P_D values are also averaged over the 4–7- and 7–10-V V_{DS} intervals, as shown in Fig. 2.

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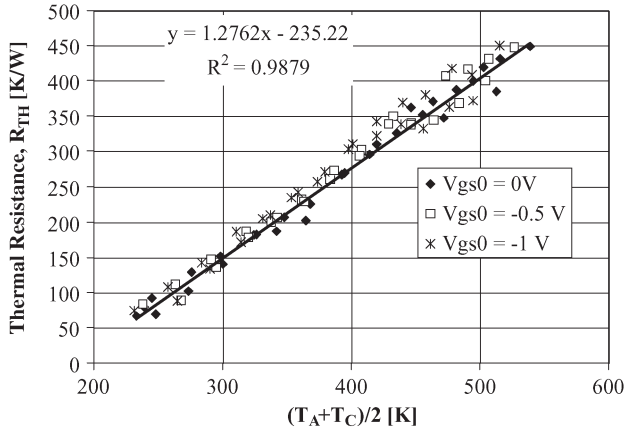

Fig. 4. Thermal resistance versus the average of ambient and channel temperature. T_C is calculated as $T_C = T_A + R_{\mathrm{TH}} P_D$, where T_A and P_D are the average values of each extraction interval.

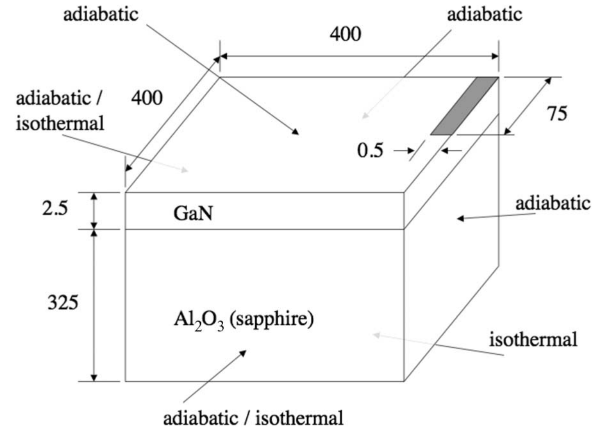

Fig. 5. Schematic view (not to scale) of the 3-D structure used in the simulations. Dimensions are expressed in micrometers. Isothermal surfaces are set at $T = 300$ K.

an independent validity check for the method, it is a necessary condition for self-consistency.

The R_{TH} versus T_C data thus obtained (not shown here) are well grouped along a straight line, indicating a good internal consistency of the method. However, the extracted R_{TH} values tend to increase slightly, at each fixed channel temperature, when V_{GS0} is decreased from 0 to -0.5 V and to -1 V, which reduces the correlation with T_C $(R^2 = 0.9733)$. A possible explanation for this behavior is the following. At lower V_{GS0}, the dissipated power P_D is also lower, and each fixed value of T_C is obtained with a combination of lower P_D and higher T_A with respect to the case of higher V_{GS0}. However, it must be considered that for a given channel temperature T_C, one can expect a larger or smaller R_{TH} depending on the higher or lower value of the ambient (i.e., back-of-the-wafer) temperature T_A since most of the thermal resistance is caused by the sapphire substrate, which sits at an average temperature somewhere between T_A and T_C. Therefore, at the same T_C, a lower V_{GS0} means a larger T_A, hence a larger R_{TH}. If this explanation is correct, one should see a better correlation by plotting R_{TH} versus the average of T_C and T_A. This is shown in Fig. 4. As anticipated, the correlation is better $(R^2 = 0.9879)$.

The excellent linear fit observed in Fig. 4 can be used to extract a compact formula to calculate the HEMT channel temperature as a function of T_A and P_D. By replacing the best fit line equation values for Fig. 4 in the formula $T_C = T_A + R_{\mathrm{TH}} P_D$ and rearranging, in our case, one obtains

$$T_C = \frac{T_A + (0.638 \cdot T_A - 235) \cdot P_D}{1 - 0.638 \cdot P_D} \tag{5}$$

where P_D is in watts, and temperatures are in kelvin.

C. Simulations

In order to check the validity of our results, channel temperatures obtained from (5) have been compared with the results of 3-D numerical heat transport simulations using Synopsys Sentaurus (formerly ISE DESSIS). The temperature dependence of the thermal conductivity of sapphire has been simulated by using quadratic fits (between 200 K and 600 K)

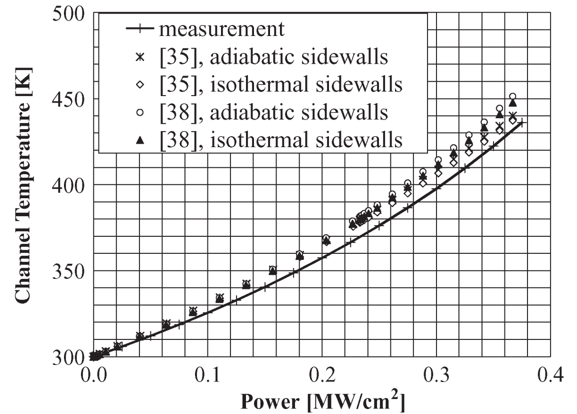

Fig. 6. Measured and simulated channel temperatures versus dissipated power density. The thermal conductivity of sapphire is taken either from [35] or [38]. Sidewalls that are not symmetry planes (see Fig. 5) are simulated either as adiabatic or isothermal (at 300 K).

to the formulas and data in [38] $(k(\mathrm{Al_2O_3}) = 5.21 \cdot 10^{-6} \cdot T^2 - 5.40 \cdot 10^{-3} \cdot T + 1.52$ W/cm/K, where T is expressed in kelvin) and [35] $(k(\mathrm{Al_2O_3}) = 2.11 \cdot 10^{-6} \cdot T^2 - 2.47 \cdot 10^{-3} \cdot T + 9.12 \cdot 10^{-1}$ W/cm/K, where T is expressed in kelvin). The thermal conductivity of the 2.5-μm-thick GaN is obviously much less critical; we used a quadratic fit to the formula found in [35] $(k(\mathrm{GaN}) = 1.54 \cdot 10^{-5} \cdot T^2 - 1.71 \cdot 10^{-2} \cdot T + 5.43$ W/cm/K, where T is expressed in kelvin).

The simulated structure is schematically shown (not to scale) in Fig. 5. The HEMT has been considered as a 150×1 μm uniform surface heating element. By using symmetry, only one-fourth of the 3-D structure needs to be simulated; the two-symmetry planes are being replaced with adiabatic surfaces, as shown in Fig. 5. The top surface is also adiabatic, whereas the bottom of the wafer is isothermal ($T = 300$ K), i.e., it is considered to be a perfect heat sink. The remaining two surfaces have been simulated as either adiabatic or isothermal ($T = 300$ K) to provide us with upper and lower bounds, respectively, to the channel temperature.

Fig. 6 shows the simulation results compared with the experimental ones, as approximated by (5). Equation (5) is seen to yield T_C values within 10 K (best case) to 20 K (worst

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case) of the maximum lattice temperatures calculated by the simulations, over a wide range of power densities and up to $T_C = 440$ K. The agreement between measurements and simulations is remarkable, considering that, as previously described, no fitting parameter has been used in the simulations. It should also be noticed that, apart from the approximation inherent with (5), the measured temperature can be expected to represent an average over the active device region; hence, it is lower than the maximum lattice temperature given by the simulations.

D. Summary

Our simple dc technique yields well-behaved temperature and dissipated power dependence of the extracted thermal resistance values, which allows the definition of a simple formula whereby the thermal resistance can be calculated for every ambient temperature and dissipated power of interest. This formula gives thermal resistance values in good agreement with those calculated by a 3-D numerical heat transport simulator.

IV. Source/Drain Parasitic-Resistance Measurements

A. Method

The method that Fukui developed for measuring $R_S + R_D$ of GaAs MESFETs [33] rests on the assumption that the device can be divided into an intrinsic region obeying the GCA, and therefore some simple analytical current–voltage relationship, and an extrinsic parasitic-resistance region that is not perturbed by the gate voltage. Under these conditions, the total drain–source resistance of the FET in the linear region can be written as

$$R_T = \frac{V_{\mathrm{DS}}}{I_D} = R_S + R_D + R_{\mathrm{CH}} = R_S + R_D + \frac{1}{f(V_{\mathrm{GS}} - V_T)} \quad (6)$$

where the channel resistance R_{CH} is expressed as the reciprocal of the intrinsic conductance, which is some function f of $(V_{\mathrm{GS}} - V_T)$. By plotting R_T as a function of $1/f(V_{\mathrm{GS}} - V_T)$, V_T is used as a fitting parameter until one obtains the linear dependence expressed by (6); the sum $R_S + R_D$ is thus determined as the intercept with the R_T axis.

In this paper, this technique will be slightly modified and applied to our HEMTs between 75 K and 400 K.

B. Long-Gate HEMT Characterization

The preliminary condition for the application of this extraction procedure is the existence of an intrinsic channel region, the conductance of which can be expressed by a simple analytical function $f(V_{\mathrm{GS}} - V_T)$. In the case of our AlGaN/GaN HEMTs, this could be verified by using the measurement of the 2DEG carrier density (n_S) and mobility (μ_n) carried out on long-gate (20×300 μm) HEMTs. Fig. 7 shows a linear gate-voltage dependence of n_S at 300 K. The channel conductance, however, is proportional to the product $n_S \cdot \mu_n$. Due to the self-shielding of the 2DEG from Coulomb scattering,

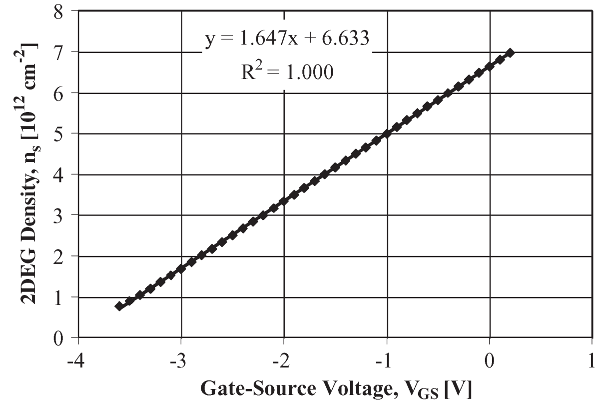

Fig. 7. Measured 2DEG density versus gate–source voltage at 300 K in the long-gate HEMT (20×300 μm).

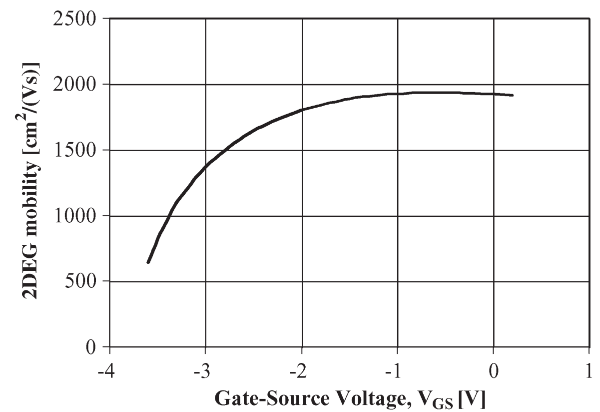

Fig. 8. Measured 2DEG mobility versus gate–source voltage at 300 K in the long-gate HEMT (20×300 μm).

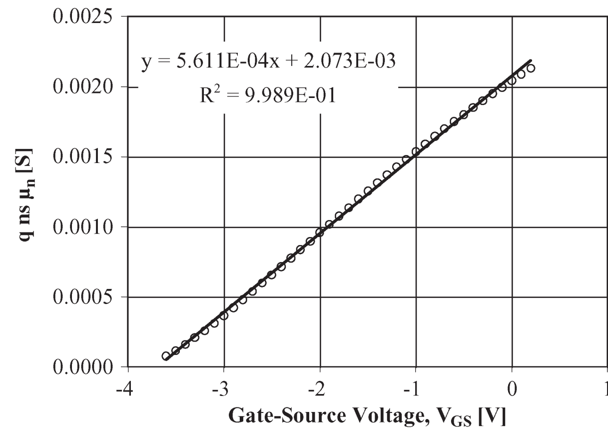

Fig. 9. Unit-(W/L) channel conductance versus gate–source voltage at 300 K in the long-gate HEMT (20×300 μm).

mobility is a nonlinear function of V_{GS}, as shown in Fig. 8. However, the change in n_S is many times the change in μ_n over the range of V_{GS} used in the measurements, so that the $n_S \cdot \mu_n$ product (as shown in Fig. 9) is, to a good approximation, linear.

The best fit line thus obtained is expressed by

$$q \cdot n_S \cdot \mu_n = 5.611 \cdot 10^{-4} \cdot (V_{\mathrm{GS}} - V_T) \quad (7)$$

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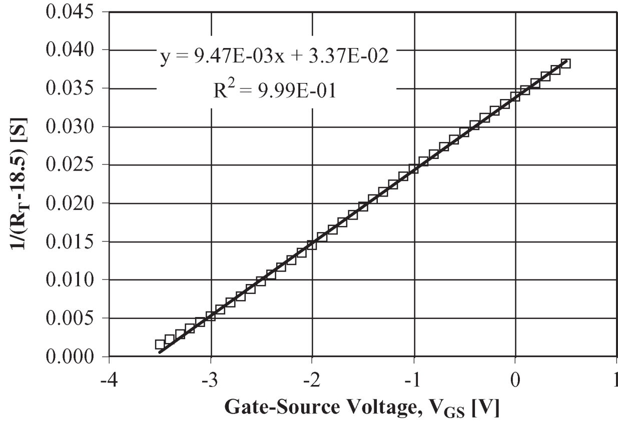

Fig. 10. Intrinsic channel conductance versus gate–source voltage at 300 K in the long-gate HEMT (20 × 300 μm). $V_{\rm DS} = 100$ mV. $R_S + R_D$ is used as a fitting parameter to obtain the linear dependence entailed by (8), resulting in $R_S + R_D = 18.5\ \Omega$.

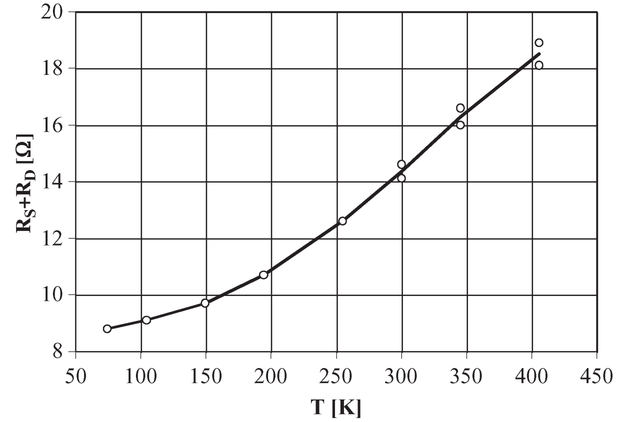

Fig. 11. Extracted parasitic resistances versus temperature in the short-gate HEMT (0.9 × 150 μm). $V_{\rm DS} = 40$ mV.

where voltages are expressed in volts, q is in coulombs, n_S is in reciprocal square centimeters, and μ_n is in square centimeters per volt second; $V_T = -3.695$ V. Based on these measurements, the resistance of the intrinsic region can be expressed as

$$R_{\rm CH} = \frac{L_G}{W_G \cdot q \cdot n_S \cdot \mu_n} = \frac{L_G}{W_G \cdot 5.611 \cdot 10^{-4} \cdot (V_{\rm GS} - V_T)} \quad (8)$$

and by plotting R_T versus $1/(V_{\rm GS} - V_T)$, as previously detailed, the value of $R_S + R_D$ can be extracted.

However, this approach [33] suffers from the sensitivity to the uncertainty of V_T because the intercept $R_S + R_D$ is much smaller than the low-$V_{\rm GS}$ R_T values in the plot. A better way to extract $R_S + R_D$ is by plotting the intrinsic conductance

$$\frac{1}{R_{\rm CH}} = \frac{1}{R_T - (R_S + R_D)} \quad (9)$$

as a function of $V_{\rm GS}$, using $R_S + R_D$ as a fitting parameter to obtain the expected linear dependence and extracting V_T from the intercept with the horizontal axis. This alternative approach is shown in Fig. 10. This procedure gives $R_S + R_D = 16.8 \div 18.5\ \Omega$ and, correspondingly, $V_T = -3.609 \div -3.563$ V (to be compared with the $V_T = -3.695$ V extracted from Fig. 9). The values of $R_S + R_D$ between 16.8 and 18.5 Ω yield the same correlation coefficient of the best fit line and are therefore indistinguishable.

The slope of the best fit line of Fig. 10 is [see (8)]

$$k = \frac{W_G}{L_G} \cdot \mu_n \cdot C = \frac{W_G}{L_G} \cdot 5.611 \cdot 10^{-4}\ \text{S/V} \quad (10)$$

where C is the AlGaN layer unit area capacitance. Therefore, from the extracted values of the slope $(8.87 \cdot 10^{-3} \div 9.47 \cdot 10^{-3}$ S/V), for $W_G = 300\ \mu$m, we obtain $L_G = 19.0 \div 17.8\ \mu$m, which is reasonably in good agreement with the 20-μm mask value.

TABLE I
TEMPERATURE DEPENDENCE OF THE EXTRACTED PARAMETERS

Temperature [K]	R_S+R_D [Ω]	V_T [V]	k [S/V]
74	8.8	-3.147	$5.23 \cdot 10^{-1}$
104	9.1	-3.185	$4.21 \cdot 10^{-1}$
149	9.7	-3.344	$2.60 \cdot 10^{-1}$
194	10.7	-3.462	$1.39 \cdot 10^{-1}$
255	12.6	-3.583	$6.13 \cdot 10^{-2}$
300	14.1 ÷ 14.6	-3.668 ÷ -3.614	$3.66 \cdot 10^{-2}$
345	16.0 ÷ 16.6	-3.692 ÷ -3.647	$2.36 \cdot 10^{-2}$
406	18.1 ÷ 18.9	-3.683 ÷ -3.648	$1.43 \cdot 10^{-2}$

For T ≥ 300 K, the entries for R_S+R_D and V_T represent a range of values yielding the same regression coefficient of the best-fit line (see Fig. 10).

Having thus gained confidence in its consistency, the extraction procedure was then applied to the short-gate HEMT.

C. Measurement of $R_S + R_D$ on the Short-Gate HEMT

The first problem to consider in moving to the short-gate ($L_G = 0.9\ \mu$m) HEMT is the possible dependence of the mobility on the longitudinal electric field, i.e., on $V_{\rm DS}$ (this was not an issue in the long-gate HEMT, where $V_{\rm DS} = 100$ mV was applied to a device with $L_G =$ 20-μm and 10-μm-long ungated regions).

The extraction procedure was therefore applied for different values of $V_{\rm DS}$, namely, 10, 40, and 100 mV. For select temperature values, R_T was also extrapolated for $V_{\rm DS} \rightarrow 0$. The results (not shown here) indicate the following: 1) There is no significant conductance degradation up to $V_{\rm DS} = 100$ mV; the average longitudinal electric field for $V_{\rm DS} = 100$ mV can be estimated to be lower than 1 kV/cm, which is a value corresponding to a marginal mobility decrease at 300 K [39]; and 2) low values, such as $V_{\rm DS} = 10$ mV, make the extraction procedure troublesome due to the disturbing effect of gate leakage at high temperatures (in spite of its impact being reduced by averaging the drain and source currents); $V_{\rm DS} = 40$ mV was therefore chosen as the best compromise value for the extraction.

The functional dependence of (8) is verified with good fidelity over the whole temperature range, the 74-K case ($R^2 = 0.996$) being the worst case observed. Fig. 11 shows the measured parasitic resistances versus temperature.

The complete set of extracted parameters, i.e., $R_S + R_D$, V_T, and k [see (10)], is given in Table I.

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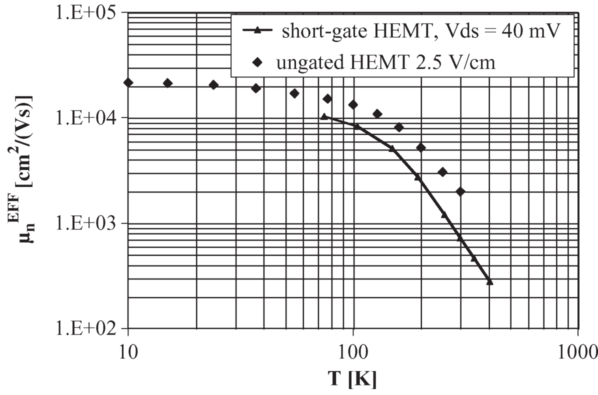

Fig. 12. Extracted (line) effective mobility versus temperature in the short-gate HEMT (0.9 × 150 μm). $V_{\mathrm{DS}} = 40$ mV. The (diamonds) measured low-field mobility of an ungated (40 × 400 μm) HEMT structure is also shown.

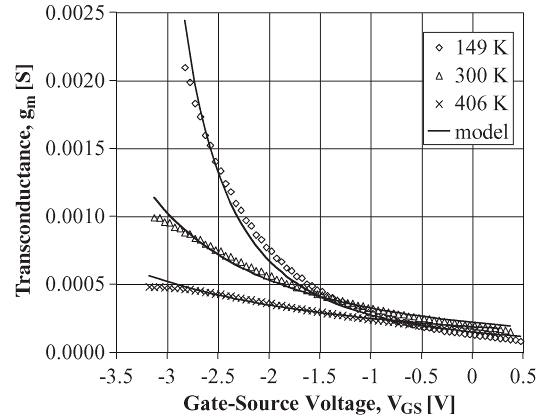

Fig. 13. HEMT transconductance measured at $V_{\mathrm{DS}} = 50$ mV and ambient temperatures of (symbols) 149 K, 300 K, and 406 K. The corresponding transconductance curves calculated by using (12) are shown by solid lines.

As (10) indicates, the slope k of the best fit line of plots such as Fig. 10 allows the extraction of an effective mobility μ_n^{EFF}

$$\mu_n^{\mathrm{EFF}} = \frac{k \cdot L_G}{W_G \cdot C} = \frac{k \cdot L_G \cdot t_{\mathrm{AlGaN}}}{W_G \cdot \varepsilon_{\mathrm{AlGaN}}} \tag{11}$$

where $\varepsilon_{\mathrm{AlGaN}}$ and t_{AlGaN} are the dielectric constant and thickness of the AlGaN layer, respectively. One must speak of an effective mobility because the true 2DEG mobility is a function of V_{GS} (Fig. 8), whereas (11) returns a single mobility value, which represents an average over the V_{GS} range used for the $R_S + R_D$ extraction (e.g., -3.5 V $< V_{\mathrm{GS}} <$ +0.5 V at 300 K). With the nominal values $L_G = 0.9$ μm, $W_G = 150$ μm, $t_{\mathrm{AlGaN}} = 30$ nm, and $\varepsilon_{\mathrm{AlGaN}} = 10.3 \cdot 8.86 \cdot 10^{-14}$ F/cm (the 0.6-nm-thick AlN layer is so thin that it can be neglected in these first-order calculations), one obtains the effective mobilities of Fig. 12 (line). The (diamonds) low-field 2DEG mobility measured on an ungated (40 × 400 μm) HEMT is also shown in Fig. 12 for comparison. The calculated μ_n^{EFF} shows the same temperature dependence as the measured low-field mobility of the ungated HEMT structure but values that are 1.5 ÷ 2.8 times lower over the 74 ÷ 406 K range. As previously discussed, this difference is unlikely to come from the effect of larger longitudinal field in the short-gate device; at $V_{\mathrm{DS}} = 40$ mV, even a very pessimistic estimate of the average field is around 400 V/cm, which is a value where the mobility degradation is minimal [39]. On the other hand, Fig. 7 shows that at 300 K, the 2DEG mobility of the long-gate HEMT changes by a factor of 3.2 between $V_{\mathrm{GS}} = -3.5$ and +0.5 V; thus, the effect of V_{GS} can easily be responsible for most of this discrepancy, together with some uncertainty in the parameters, particularly the dielectric constant and, to a smaller extent, the thickness of the AlGaN.

D. Modeling Results

It is worth pointing out that the approach we followed, besides allowing the extraction of parasitic resistance values with a clear physical meaning, represents a complete and simple, yet accurate, dc drain–current model for the HEMT biased at low V_{DS}.

By using the parameter values listed in Table I, the drain current can be calculated at each temperature as

$$I_D = \frac{V_{\mathrm{DS}}}{R_T} = \frac{V_{\mathrm{DS}}}{R_S + R_D + R_{\mathrm{CH}}} = \frac{V_{\mathrm{DS}}}{R_S + R_D + \frac{1}{k(V_{\mathrm{GS}} - V_T)}}. \tag{12}$$

As an example, we used (12) to compute the HEMT transconductance (at $V_{\mathrm{DS}} = 50$ mV) as a function of gate–source voltage, at different ambient temperatures, and compared the model with the experimental values, as shown in Fig. 13.

The model accurately describes the temperature and V_{GS} dependence of the transconductance from about 500 mV above threshold to positive gate voltage, where the lower bound is determined by the singularity of (12) for $V_{\mathrm{GS}} \rightarrow V_T$ and the upper bound is determined by the gate leakage current.

Since the temperature dependence of the parameters in Table I is smooth and well behaved, parameter values corresponding to different temperature values can be safely interpolated.

E. Summary

The extraction method described in this section yields parameter values that are physically meaningful and consistent with independent measurements; for example, the extracted channel length of the long-gate HEMT (18–19 μm) is in good agreement with the mask length (20 μm). The series resistance of the short-gate (0.9 μm × 150 μm) HEMT showed a significant increase with temperature between 74 K and 406 K, which may be correlated with the observed corresponding decrease in electron mobility. The extracted parameters define a simple analytical model of the HEMT at low drain bias that gives a good match with experimental data over bias and temperature.

V. Conclusion

This paper has shown two simple dc techniques for measuring the thermal resistance R_{TH} and the low-drain-bias ohmic parasitic resistance $R_S + R_D$ of AlGaN/GaN HEMTs. Despite

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their simplicity, these methods do not require simplifying assumptions, other than those that can be verified experimentally. The devices under test were characterized over a wide range of ambient temperatures. The main results can be summarized as follows.

1) The thermal resistance is a strong function of ambient temperature T_A and dissipated power P_D (via the channel temperature T_C). Since the channel-to-ambient thermal resistance is dominated by the thick sapphire substrate, R_{TH} is observed to be a linear function of the average temperature $(T_A + T_C)/2$, varying by as much as a factor of eight between 200 K and 500 K.
2) The measured values of T_C can be expressed accurately enough as a function of T_A and P_D by a simple formula, and these show a satisfactory agreement (within 10–20 K, depending on the choice of literature data for the thermal conductivity of sapphire) with the numerical simulations (with no fitting involved).
3) For the measurement of $R_S + R_D$, the HEMT is modeled, at low drain bias, as an intrinsic HEMT obeying the GCA and connected with the external contacts by the bias-independent parasitic resistances. This model has been discussed and validated by using the long-gate and ungated HEMT structures.
4) $R_S + R_D$ approximately doubles for ambient temperatures increasing from 75 K to 400 K, its temperature dependence mirroring that of the low-field 2DEG mobility.
5) The extracted (low drain bias) model of the HEMT accurately describes the device dc behavior over temperature and gate voltage.

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