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Temperature dependent negative capacitance behavior in (Ni/Au)/AlGaN/AlN/GaN heterostructures

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ABSTRACT

The temperature dependent capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures were investigated by considering the series resistance (R_s) effect in the temperature range of 80–390 K. The experimental results show that the values of C and G/ω are strongly functioning of temperature and bias voltage. The values of C cross at a certain forward bias voltage point (~2.8 V) and then change to negative values for each temperature, which is known as negative capacitance (NC) behavior. In order to explain the NC behavior, we drawn the C vs I and G/ω vs I plots for various temperatures at the same bias voltage. The negativity of the C decreases with increasing temperature at the forward bias voltage, and this decrement in the NC corresponds to the increment of the conductance. When the temperature was increased, the value of C decreased and the intersection point shifted towards the zero bias direction. This behavior of the C and G/ω values can be attributed to an increase in the polarization and the introduction of more carriers in the structure. R_s values increase with increasing temperature. Such temperature dependence is in obvious disagreement with the negative temperature coefficient of R or G reported in the literature. The intersection behavior of C–V curves and the increase in R_s with temperature can be explained by the lack of free charge carriers, especially at low temperatures.

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1. Introduction

In the ideal case, the capacitance of metal–semiconductor (MS) or metal–insulator–semiconductor (MIS) structures is usually frequency independent, especially at high frequency limits ($f \geqslant 1$ MHz), and shows an increase with increasing forward bias voltage [1–9]. However, this saturation is different at low and intermediate frequencies and temperatures especially in the depletion and accumulation regions, which is due to the series resistance (R_s) of the device, interface states (N_{ss}), interfacial insulator layer, and surface charges [6–13]. The performance and reliability of these devices are especially dependent on the formation barrier height at the M/S interface, R_s of devices, doping concentration, and N_{ss} [6–16]. In addition, the change in temperature has very important effects on the determination of such devices' parameters [16–20]. The existence of an interfacial insulator layer at the M/S interface and R_s of a device significantly alters the device's C–V and G/ω–V characteristics with respect to the ideal behavior. Therefore, before any analysis can take place, all of the measurements must be corrected for R_s [2].

In recent years, some investigations have reported a negative capacitance (NC) [20–37] in the forward bias C–V characteristics. These devices include p–n junctions [31], metal–semiconductor (MS) contacts/Schottky barrier diodes (SBDs) [20,22,27,30], metal–insulator–semiconductor (MIS) structures [24], quantum well infrared photodetectors (QWIPs) [29], UH photodetectors [21], far-infrared detectors [26,34], some dielectric and ferroelectric materials [35,36], and light emitting diodes (LEDs) [23,37]. The observation of negative capacitance is important because they imply that an increment of bias voltage produces a decrease in the charge on the electrodes [25]. However, NC has, so far, no meaning to us and the concept of NC is still not widely recognized because of a lack of trust in the experimental data [32]. Therefore, in many cases, the experimental NC data were not reported in the literature due to the confusion caused by the NC effect [29]. In addition, the NC effect reported in the literature has often been referred to as 'anomalous' or 'abnormal' [29]. NC measured experimentally has sometimes been attributed to instrumental problems, such as parasitic inductance [22,28] or poor measurement experiment calibration [29]. Moreover, the physical mechanism of negative capacitance in different devices is obviously different. The term 'negative capacitance' means that the material displays an inductive behavior. Sometimes, the NC that is caused by the injection

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of minority carriers can be observed only at a forward applied bias voltage [22,26,30].

In practice, NC can be explained based on the behavior of the temperature and frequency dependent admittance spectroscopy (C–V and G/ω–V) data [32]. The theory is established on the following arguments. Electrons that surmount the Schottky barrier (SB) under forward bias fill up the empty states at the interface, but because they possess excess energy, when colliding with the electrons trapped at the N_{ss}, they also knock electrons out of the traps, provided that the binding energy of these traps is less than the SB energy [22,28,34]. However, to move an electron out of the interface trap into the metal requires much less energy than to create an electron–hole pair in bulk. The strong coupling of the trap states to the metal conduction band makes the ionization energy very different on the two sides of the interface [34]. Werner et al. [22] have shown that the complete frequency dependent admittance measurements (capacitance and conductance) enable us to characterize these electrical parameters. They proposed that the observed inductive effect at a low frequency arises from the high-level injection of minor carriers into the bulk semiconductor, as demonstrated in Si SBDs. Many electronic devices comprise a semiconductor between the rectifier and ohmic contacts but with N_{ss} and bulk traps where the charges can be stored and released when the appropriate forward applied bias and the external AC oscillation voltage are applied and a large effect can be produced in the devices [21–27]. However, it is believed that the injection of charge carriers involves a process of hopping to localized interface traps/states, but a detailed physical mechanism of injection is not well understood yet.

In the present study, the origin of negative capacitance in the forward bias C–V characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures was investigated in a wide range of temperature (80–390 K) and bias voltage (±6 V) at 1 MHz. In order to explain the NC behavior, we have drawn the C vs I and G/ω vs I plots for various temperature at the same bias voltage. In addition, to obtain the real C and G/ω, the measured under reverse and forward bias capacitance (C_m) and conductance (G_m/ω) values were corrected as C_c and G_c/ω for the effect of R_s.

2. Experimental

$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures were grown on c-plane (0 0 0 1) double-polished 2 inch diameter Al_2O_3 substrate in a low pressure metalorganic chemical-vapor deposition (MOCVD) reactor (Aixtron 200/4 HT-S) by using trimethylgallium (TMGa), trimethylaluminum (TMAl), and ammonia as Ga, Al, and N precursors, respectively. Prior to epitaxial growth, Al_2O_3 substrate was annealed at 1100 °C for 10 min in order to remove surface contamination. The buffer structures consisted of a 15 nm thick, low temperature (650 °C) AlN nucleation layer, and high temperature (1150 °C) 420 nm AlN templates. A 1.5 μm nominally undoped GaN layer was grown on an AlN template layer at 1050 °C, followed by a 2 nm thick high temperature AlN (1150 °C) barrier layer. The AlN barrier layer was used to reduce the alloy disorder scattering by minimizing the wave function penetration from the two-dimensional electron gas (2DEG) channel into the $Al_xGa_{1-x}N$ layer. After the deposition of these layers, a 23 nm thick undoped $Al_{0.22}Ga_{0.78}N$ layer was grown on an AlN layer at 1050 °C. Finally, a 5 nm thick GaN cap layer growth was carried out at a temperature of 1085 °C and a pressure of 50 mbars. Since the sapphire substrate is insulating, the ohmic and Schottky/rectifier contacts were made on top of the sample, respectively, in the high vacuum coating system at approx. 10^{-7} Torr. The ohmic contacts were formed as a square van der Pauw shape and the Schottky contacts were formed as 1 mm diameter circular dots (Fig. 1). Prior to ohmic contact formation, the samples were cleaned with acetone in an ultrasonic bath. Then, a sample was treated with boiling isopropyl alcohol for 5 min and rinsed in de-ionized (DI) water at 18 MΩ resistivity. After cleaning, the samples were dipped in a solution of HCl/H_2O (1:2) for 30 s in order to remove the surface oxides, and then rinsed in DI water again for a prolonged period. Ti/Al/Ni/Au (17.5/175/40/80 nm) metals were thermally evaporated on the sample and were annealed at 850 °C for 30 s in N_2 ambient in order to form the ohmic contact. Schottky contacts were formed by Ni/Au (40/80 nm) evaporation.

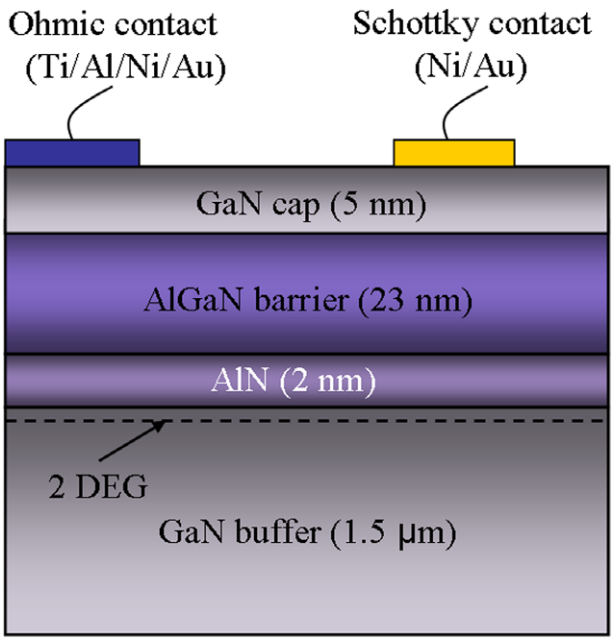

Fig. 1. Schematic diagram of the Ohmic and Schottky contacts on the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure.

The temperature dependence of the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures were performed by using an HP 4192 A LF impedance analyzer (5 Hz–13 MHz) at 1 MHz. The measurements were performed under the sweep of bias voltage from (−6 V) to (+6 V) and the test signal of 40 mV peak to peak in the temperature range of 80–390 K. The sample temperature was controlled with a Janes vpf-475 cryostat. Furthermore, the sample temperature was continually monitored by using a copper-constant thermocouple close to the sample and was measured with a Keithley model 199 dmm/scanner and a Lake Shore model 321 auto-tuning temperature controller with sensitivity better than ±0.1 K.

3. Results

The plots of the measured capacitance $C(V,T)$ and the conductance $G(V,T)$ of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures are shown in Fig. 2(a) and (b), respectively. As shown in Fig. 2(a) and (b), both C–V and G/ω–V characteristics exhibit accumulation, depletion, and inversion regions. The C and G/ω values decrease with increasing temperature especially in the accumulation and depletion regions for each bias voltage. The forward bias C–V curves show a nearly common intersection point of all the curves at bias voltage. The forward bias C–V curves show an abnormal behavior that changes to negative values after a certain forward bias voltage (~2.8 V) and after the crossing point, and the C values increases with increasing temperature. Contrary to the C–V curves,

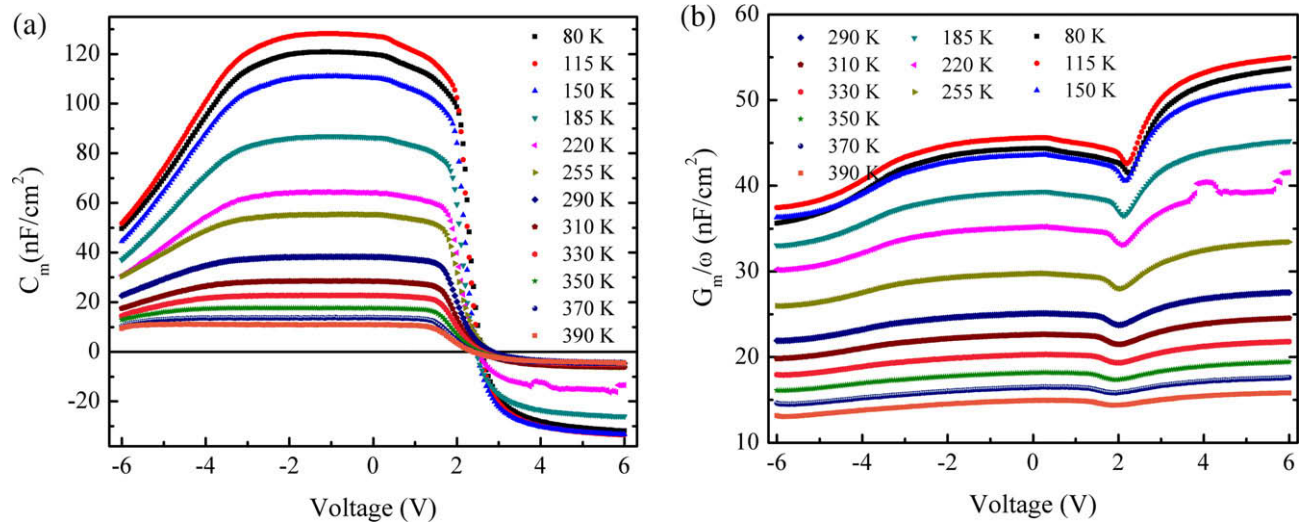

Fig. 2. (a) The measured capacitance $C_m(V,T)$ and (b) conductance $G_m/\omega(V,T)$ at various temperatures for (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures, respectively.

the values of G/ω increase with increasing bias voltage from the −6 V to 6 V and have a minimum of approx. 2 V for each temperature. As can be seen from Fig. 2(a) and (b), the NC values appear at every temperature and correspond to the maximum of the device conductance. In order to explain the effect of the bias voltage, both the capacitance and conductance values are shown in Figs. 3 and 4 in the depletion region as a function of temperature with steps of 0.1 V, respectively. Both the C and G/ω values show a weak dependence on the bias voltage at high temperatures.

Several methods have been suggested in the literature for the calculation of R_s of MIS and MOS type structures, but the theoretical expression of R_s is still unclarified and has not been clearly disclosed in the literature [2,38,39]. However, to extract the series resistance of these structures, the method that was developed by Nicollian and Brews [2] is thought to be generally the most accurate. This method provides the determination of R_s for the reverse and forward bias regions. In this method, the R_s values are given as,

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2}. \quad (1)$$

The real series resistance of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures were obtained from the measured capacitance (C_m) and conductance (G_m) at various temperatures and 1 MHz for each bias voltage. The series resistances that are calculated from the data in Fig. 2(a) and (b) at various temperatures and the various forward biases are shown in Figs. 5 and 6, respectively. These very significant values demanded special attention to be given to the effects of the R_s in the application of the admittance-based measured methods (C–V and G/ω–V).

As shown in Fig. 5, the value of R_s increases with increasing temperature. In addition, the bias voltage dependent of R_s is shown in Fig. 6. It is clearly seen in Fig. 6 that the change in the R_s with bias voltage is less significant around room temperature, which is contrary to low and high temperatures. Figs. 5 and 6 show that the value of R_s is strongly dependent on the bias voltage and temperature, and it increases with increasing temperature.

In order to determine the real C and G/ω of the heterostructures, the measured capacitance (C_m) and conductance (G_m/ω) values, under reverse and forward bias, were corrected as C_c and G_c/ω for the effect of R_s according to,

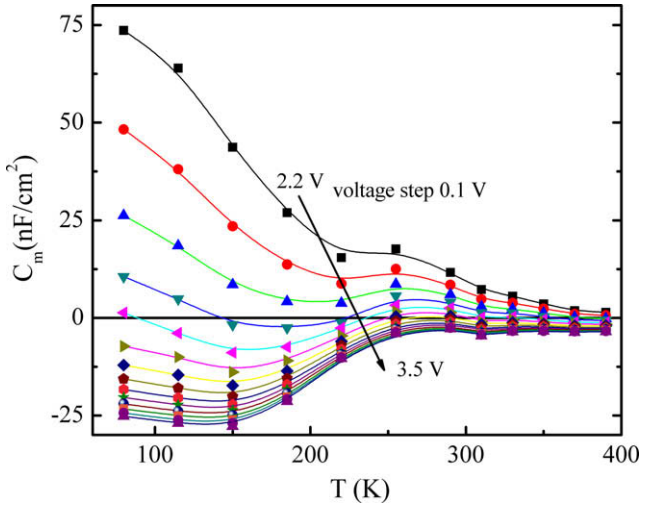

Fig. 3. The experimental C_m–V characteristics of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures in the voltage range of 2.2–3.5 V with steps of 0.1 V.

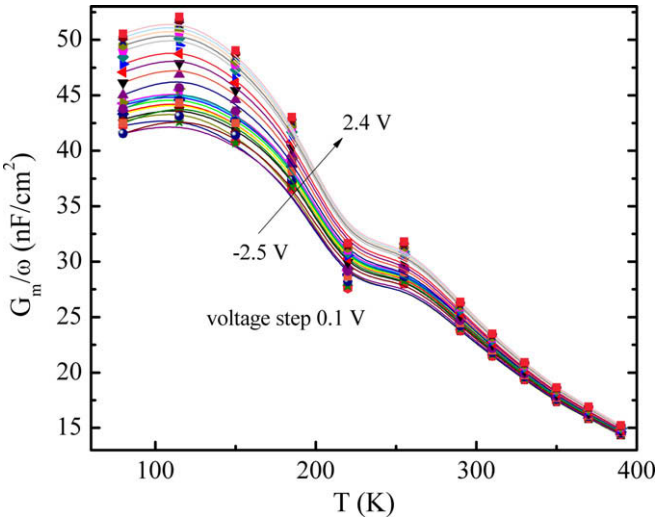

Fig. 4. The experimental G_m/ω–T characteristics of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures in the voltage range of −2.5–2.8 V steps of 0.1 V.

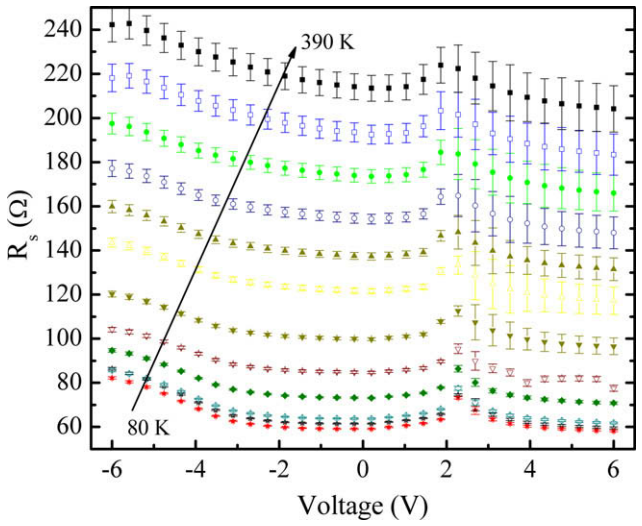

Fig. 5. R_s vs V plots for (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures at various temperatures.

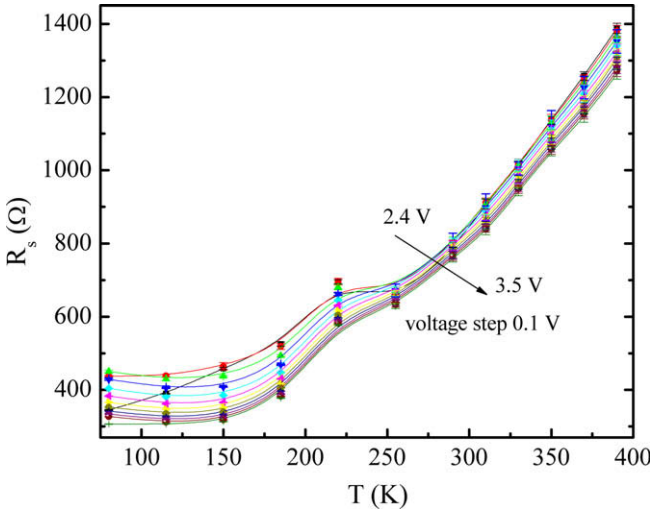

Fig. 6. The experimental temperature dependence of R_s for (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures at the voltage range 2.4–3.5 V steps of 0.1 V.

$$C_c = \frac{\left[G_m^2 + (\omega C_m)^2\right] C_m}{a^2 + (\omega C_m)^2} \tag{2}$$

and

$$G_c = \frac{[G_m^2 + (\omega C_m)^2]\, a}{a^2 + (\omega C_m)^2}, \tag{3}$$

where a is given in the following form

$$a = C_m - \left[G_m^2 + (\omega C_m)^2\right] R_s. \tag{4}$$

The corrected capacitance (C_c) and conductance (G_c/ω), under forward and reverse bias, were obtained by using Eqs. (3) and (4) and are shown in Fig. 7(a) and (b), respectively. After the correction, the values of the C_c increase with increasing voltage, especially in the accumulation region.

To compare the variation of C and G/ω in the same bias voltage, the C–V and G/ω–V plots for the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure are shown in Fig. 8 at room temperature. As can be seen in Fig. 8, the value of C nearly decreases with increasing bias voltage in the depletion and inversion regions. On the contrary, the values of conductance increase with increasing bias voltage in the same regions, and pass from a valley at ~2.5 V. It is clear that the decrease of the capacitance corresponds to an increase of the conductance. On the other hand, the minimum of the C values coincides with the maximum of the conductance.

To compare the NC and corresponding conductance (G/ω) in the same bias voltage and current, we have drawn both the C vs I and G/ω vs I plots of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure at four different temperatures and are shown in Fig. 9(a) and (b), respectively. As shown in Fig. 9(a), the value of C changes to negative at a critic bias voltage (V_c) for each temperature. These values of V_c, NC or C_{min} and corresponding maximum conductance (G_{max}/ω) are shown in Table 1. It can be seen in Fig. 9 and Table 1 that the negativity of the C (C_{min}) value decreases with increasing temperature. When the temperature decreases from 390 to 80 K, the value of C_{min} and the G_{max}/ω vary, respectively, from −0.016 nF to −0.201 nF and from 0.778 nF to 2.505 nF. Fig. 9(a) and (b) clearly shows that the decrease of the capacitance corresponds to an increase of the conductance.

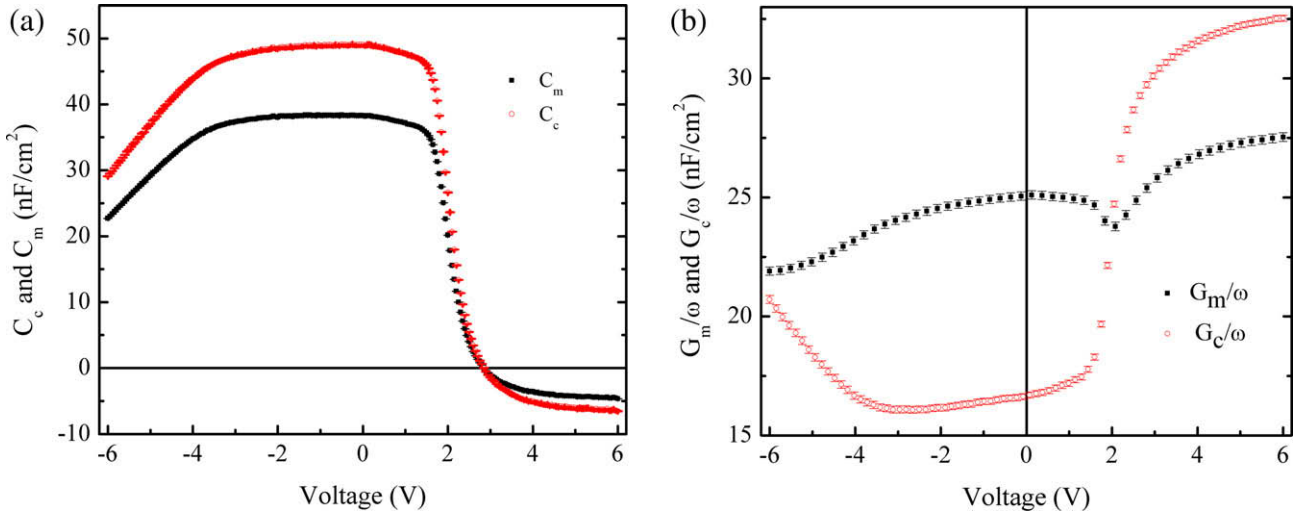

Fig. 7. The voltage dependent plot of the corrected (a) C_c–V and C_m–V (b) G_c/ω–V and G_m/ω–V of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures.

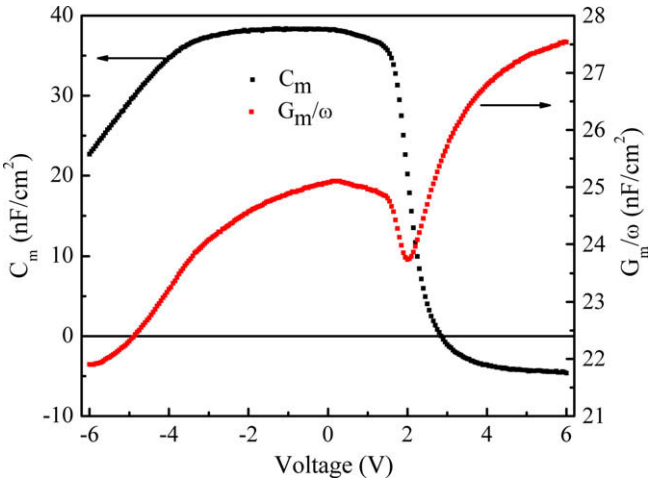

Fig. 8. The variation of the C_m–V and G_m/ω–V for the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures as a function of bias voltage at room temperature.

4. Discussion

It is well known that the analysis of the C–V and G/ω–V measurements of semiconductor devices such as MS, MIS, or MOS and high electron mobility transistors (HEMTs) only at a room or narrow temperature range and one bias voltage cannot give us detailed information about the conduction mechanisms, barrier formation at the M/S interface, or interface charges. Contrarily, in the wide temperature and bias voltage regions (under forward and reverse bias) of the C–V and G/ω–V measurements of these devices can enable us to understand the different aspects of conduction mechanisms or the temperature and bias voltage dependence behavior of the main electrical parameters. Therefore, the C–V and G/ω–V characteristics of (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures have been investigated in the wide temperature range of 80–390 K and at 1 MHz. This is because, at sufficiently high frequencies ($f \geqslant 1$ MHz), the interface states cannot follow the AC signal [1–5].

Since the temperature is increased, the generation of thermal carriers (electrons or holes) in a semiconductor is enhanced at positive and negative biased conditions. Therefore, the increase of C with the temperature for all the applied bias levels can be understood due to charge storage (=Q/V), (Fig. 2a).

Table 1
The C_{min} and G_{max}/w values of the (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN heterostructures at various temperatures.

T (K)	$V_c \pm 0.1$ (mV)	$C_{min} \pm 0.001$ (nF)	$G_{max}/\omega \pm 0.001$ (nF)
80	21.8	−0.201	2.505
220	15.6	−0.118	1.939
290	14.0	−0.034	1.357
390	7.1	−0.016	0.778

These behaviors of C–V–T and G/ω–V–T show that the material displays an inductive behavior [21,32,33,35]. The origin of this is believed to be due to the carrier capture of an emission at the interface states. This observation of negative capacitance is important because it implies that an increment of bias voltage produces a decrease in the charge on the electrodes [25]. It is believed that the negative capacitance that is caused by the injection of minority carriers can be observed only at a forward applied bias voltage [22,26,30]. On the other hand, it is believed that the injection of charge carriers involves a process of hopping to localized interface traps/states, but the detailed physical mechanisms of an injection are not well understood yet. The trap charges have enough energy to escape from the traps that are located between the metal and semiconductor interface in the $Al_{0.22}Ga_{0.78}N$ band gap.

The temperature dependence of R_s, as shown in Fig. 6, is in obvious disagreement with the reported negative temperature coefficient of R_s for ideal MS and MIS type Schottky diodes. This variation of R_s with the temperature can be expected for semiconductors in the temperature region where there is no freezing behavior of the carriers. Trap charges have enough energy to escape from the traps that are located between the metal and semiconductor interface in the $Al_{0.22}Ga_{0.78}N$ band gap.

The contrary behavior in the C–V and G/ω–V plots that are shown in Fig. 8 can be explained by the existence of localized interface states at the metal and semiconductor interface and results in a charge dipole at the interface. Under forward bias, most of the applied bias voltage is shared by the semiconductor and interfacial dipole [32]. Therefore, the capacitance value decreases with increasing polarization and more carriers are introduced in the structure.

The high value of NC in Fig. 9, at high temperatures, in the forward bias region can be attributed to the low value of R_s at low temperatures, which is due to an inductive contribution to the impedance that is believed to arise from the high-level injection of minority carriers into the bulk semiconductor [35].

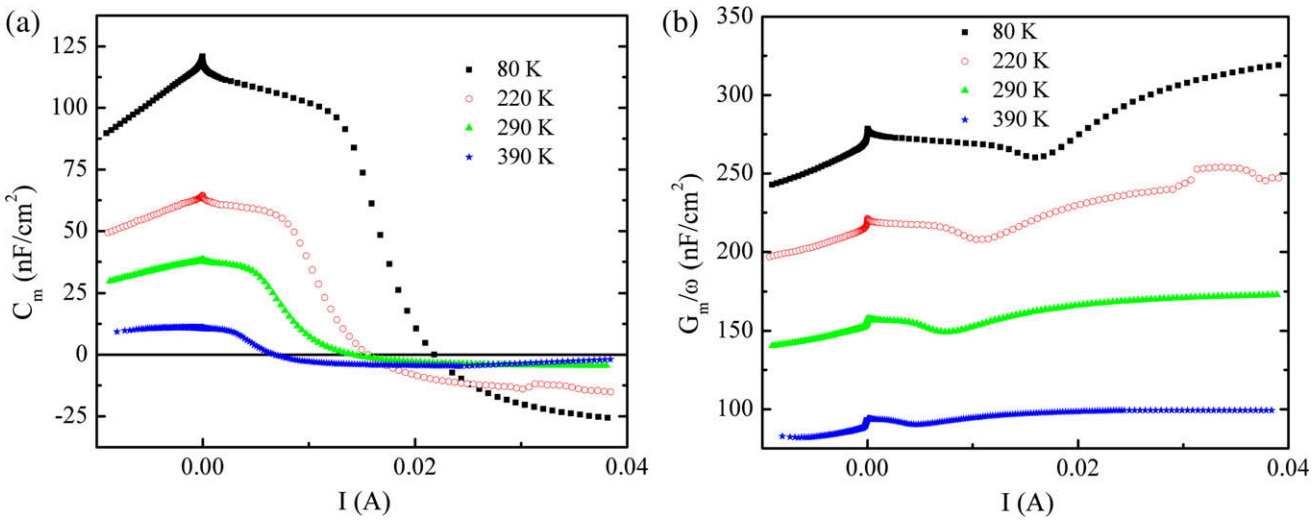

Fig. 9. C_m vs I, and G_m/ω vs I characteristics of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures at various temperatures, respectively.

5. Conclusion

The forward and reverse bias C–V and G/ω–V characteristics of the (Ni/Au)/$Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures were investigated by considering the series resistance (R_s) at 1 MHz and in the temperature range of 80–390 K. The experimental results show that C and G/ω were quite sensitive to temperature and bias voltage. The C–V plots cross at a nearly common forward bias voltage point ($\sim$2.8 V) and then change to negative values. The intersection behaviors of the C–V curves and the increase in R_s with temperature were attributed to the lack of free charge, especially at low temperatures. In order to explain this negative behavior of capacitance (NC) at the forward bias region, we have drawn the C vs I and G/ω vs I plots for various temperatures at the same bias voltage. It is clear that the negativity of the C values decrease with increasing temperature at the forward bias voltage, and this decrease of the NC corresponds to an increase of the conductance. When the temperature was increased, the values of C increased and shifted towards the zero bias direction. Such behavior of the C and G/ω can be attributed to the increments of the polarization and more carriers in the structure. In addition, to obtain the real values of heterojunction C and G/ω, both under reverse and forward bias, the measured capacitance (C_m) and conductance (G_m/ω) values were corrected as C_c and G_c/ω for the effect of R_s.

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