Temperature Sensitive Electrical Parameters for Condition Monitoring in SiC Power MOSFETs

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Abstract

This paper presents an analysis of the turn ON transient for SiC power MOSFETs and defines a Temperature Sensitive Electrical Parameter (TSEP) which is suitable for condition monitoring. The drain current switching rate dI_{DS}/dt and its temperature dependency have been measured and analysed for commercially available 1.2 kV/10 A, 1.2 kV/24 A and 1.2 kV/42 A SiC MOSFETs from Wolfspeed showing that at lower switching speeds, i.e. using high gate resistances, it can be a suitable TSEP for condition monitoring. The impact of temperature on the switching speed indicates that the current switching rate is a more effective TSEP for higher current rated devices and the evaluation of the switching losses suggests that the sacrifice in switching speed for enabling the ability of estimating the junction temperature is not a major trade-off.

1 Introduction

Semiconductor devices are subjected to numerous power and temperature cycles during their lifetime. Due to the thermo-mechanical stresses resulting from mismatch in the coefficients of thermal expansion at critical interfaces like the semiconductor/die-attach/substrate interfaces [1], they may exhibit higher thermal resistances, resulting from solder pad de-lamination and die attach voiding, and gate-wirebond degradation. Power devices may also exhibit higher source and gate contact resistance resulting from increased contact resistance. The rate of heat extraction from the device becomes impeded due to higher interfacial thermal resistances; hence, the device operates at a higher junction temperature. An effective method of condition monitoring during on-line operation, where it is not possible to integrate a temperature/current sensor directly on the chip, is using a TSEP to estimate the junction temperature indirectly through the known temperature dependence of the electrical parameter [2]. Several TSEPs have been proposed for both online and offline condition monitoring of silicon power devices [2]. These TSEPs include the threshold voltage [4], the switching transients [5] and recently, the temperature dependency of the gate current as a TSEP for Si MOSFETs and Si IGBTs has shown promising results [6].

SiC power MOSFETs are now widely and commercially available hence, for maximising their potential; the question of condition monitoring becomes an important topic. Due to the material properties of silicon carbide, SiC MOSFETs are not as temperature sensitive as silicon devices hence, the use of TSEPs for condition monitoring is challenging. The temperature dependence of the on-state voltage is not linear and despite the improvements in the channel resistance for the last generation of SiC MOSFETs, it is not as temperature sensitive as it is for Si MOSFETs [7]. The Miller capacitance of SiC devices is small because of the reduced die size, hence using the discharging time of the Miller capacitance is more difficult than for Si devices. Moreover, the fast switching rate of SiC coupled with the parasitic inductances of the power modules causes electromagnetic oscillations. The oscillations in the drain-source voltage resulting from the source inductance are transmitted back to gate voltage through the Miller capacitance making the monitoring of the gate voltage more difficult.

In [8], the authors analyse the impact of temperature and the gate resistance value in dynamic characteristics of SiC devices. The temperature dependency of the current commutation rate (dI_{DS}/dt) can be an effective TSEP for SiC MOSFETs if the devices are driven with lower commutation rates, as the analytical and experimental results of section 2 and 3 suggest. The turn ON transient is defined by the size (rating) of the die and the operating conditions of the device. The impact of these factors on the implementation of effective condition monitoring is studied in section 4. The impact of reduced MOSFET switching rates on the overall losses is investigated for SiC and silicon devices. Section 5 concludes the paper.

2 Analysis of the Impact of Temperature on the Turn ON Transient of SiC Power MOSFETs

The turn ON of a SiC MOSFET has different stages that can be explained by analysing the gate current [9-10]. The total gate current that has to be supplied by the gate driver has 3 components that are time shifted and follow equation (1), where I_G is the gate current, C_{GS} is the gate source capacitance, $C_{GD\text{-}HV}$ is the Miller capacitance at high drain voltage, $C_{GD\text{-}LV}$ is the Miller capacitance at low drain voltage,

V_{GG} is the gate drive voltage, R_G is the gate resistance and V_{GP} is the plateau voltage.

$$I_G = \begin{cases} \dfrac{C_{GS}}{(C_{GS}+C_{GD-HV})} \dfrac{V_{GG}}{R_G} e^{-\frac{t}{R_G(C_{GS}+C_{GD-HV})}} & for\ 0 < t < t_1 \\ \dfrac{V_{GG}-V_{GP}}{R_G} & for\ t_1 < t < t_2 \\ \dfrac{C_{GS}}{(C_{GS}+C_{GD-LV})} \dfrac{V_{GG}-V_{GP}}{R_G} e^{-\frac{t}{R_G(C_{GS}+C_{GD-LV})}} & for\ t_2 < t < t_3 \end{cases} \quad (1)$$

Figure 1 shows the idealised waveforms for the turn ON for two different junction temperatures where the dashed line represents the turn ON at a higher junction temperature. Between 0 and t_1, the gate current charges C_{GS} while C_{GD} is constant and no current flows through the MOSFET. The load current starts to rise at t_0 when the gate voltage reaches the threshold voltage (V_{TH}) and it reaches its maximum at t_1, causing the V_{DS} across the MOSFET to fall to its on-state value thereby charging the Miller capacitance between t_1 and t_2. At the end of t_2, the V_{DS} transient is complete and the V_{GS} resumes its exponential rise to V_{GG} but with a larger time constant since the Miller capacitance has increased due to its dependency on the V_{DS}.

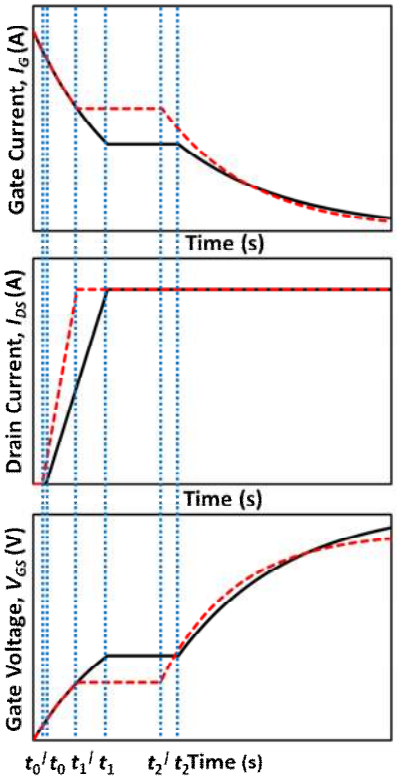


Figure 1: Generic Turn ON waveforms for a SiC MOSFET

At the time instant that the MOSFET is switched ON ($t = 0$ in Figure. 1), the gate current is at its maximum and it charges only C_{GS}. Between 0 and t_1, the V_{GS} is on an exponential rise and I_G is in an exponential decay. If the MOSFET has a higher junction temperature, the negative temperature coefficient of V_{TH} has two effects: the load current starts to rise sooner because of the lower threshold voltage and there is an increase in the current commutation rate (dI_{DS}/dt) [8]. The higher dI_{DS}/dt means that the device with the higher T_J requires less time to conduct the full load current. As a result, the V_{DS} transient charges the Miller capacitance at a faster rate in the hotter device thereby causing the gate current to reach the plateau sooner and at a higher gate current. Observing the V_{GS} characteristics, it can be seen that V_{GP} decreases with increasing temperature, hence, the current through C_{GD} increases with temperature since the current is equal to $(V_{GG}-V_{GP})/R_G$. In other words, referring to (1), the transition from the first component of the gate current to the second component occurs sooner in time and at a higher gate current value

The time to threshold (t_0) as shown in Figure 1, depends on the value of the threshold voltage and hence on temperature. The temperature sensitivity of this time value can be determined analytically with the equations below. The time-to-threshold (t_0) is given by equation (2).

$$V_{GS}(t_0) = V_{GG}\left(1 - e^{-\frac{t_0}{R_G(C_{GS}+C_{GD-HV})}}\right) = V_{TH} \quad (2)$$

Solving for t_0 yields

$$t_0 = R_G(C_{GS}+C_{GD-HV}) \ln\left(\frac{V_{GG}}{V_{GG} - \left(V_{TH}\big|_{25°C} - \frac{dV_{TH}}{dT}(T_j - 25)\right)}\right) \quad (3)$$

As the temperature increases and the threshold voltage decreases, the value of t_0 decreases and the drain current starts to rise sooner. The time taken for V_{GS} to change from the threshold voltage (V_{TH}) to the gate voltage plateau (V_{GP}) is also the time required for the current to change from 0 to the full load current. The rate of change of V_{GS} and I_{DS} with time can be expressed as

$$\frac{dV_{GS}}{dt} = \frac{V_{GG}}{R_G(C_{GS}+C_{GD-HV})} e^{-\frac{t}{R_G(C_{GS}+C_{GD-HV})}} \quad (4)$$

$$\frac{dI_{DS}}{dt} = B(V_{GS}-V_{TH}) \frac{V_{GG}}{R_G(C_{GS}+C_{GD-HV})} e^{-\frac{t}{R_G(C_{GS}+C_{GD-HV})}} \quad (5)$$

where $B = \dfrac{W\mu C_{OX}}{L}$.

The time required for V_{GS} to change from the threshold voltage to the plateau voltage can be expressed as the ratio of the load current to the current commutation rate.

$$t_{RISE} = t_1 - t_0 = \frac{I}{dI_{DS}/dt} \quad (6)$$

The current commutation rate (dI_{DS}/dt) has a temperature dependency according to equation (7).

$$\frac{d^2 I_{DS}}{dt \cdot dT_J} = B\left|\frac{dV_{TH}}{dT}\right| \frac{V_{GG}}{R_G(C_{GS}+C_{GD-HV})} e^{-\frac{t}{R_G(C_{GS}+C_{GD-HV})}} \quad (7)$$

Note that the temperature dependency of the effective mobility is neglected here, since the MOSFET is not fully turned-on, hence, the channel resistance is still very high and the temperature dependency of the threshold voltage has a much greater effect on the commutation rate of the drain current. Equation (7) is always positive thereby affirming the fact that the current commutation rate reduces with increasing temperature. Equation (6) can be expressed as

$$t_{RISE} = \frac{I}{B\left|\frac{dV_{TH}}{dT}\right| \frac{V_{GG}}{R_G(C_{GS}+C_{GD-HV})} e^{-\frac{t}{R_G(C_{GS}+C_{GD-HV})}(T_J-25)} + \left.\frac{dI_{DS}}{dt}\right|_{25°C}} \quad (8)$$

It can be observed that increasing the junction temperature reduces both t_{RISE} and t_0, causing the reduction of t_1 (time to plateau). The time taken for V_{GS} to rise to the plateau voltage can be expressed as

$$t_1 = t_0 + t_{RISE} \quad (9)$$

By substituting the value given by (9) into the first gate current component in (1), the gate current plateau can be determined as a function of temperature.

3 Experimental Results

The impact of temperature on the turn ON characteristics of a Si MOSFET as TSEP was proposed in [7]. However, the results in [10] suggest that the impact of the gate resistance and temperature on the dynamic characteristics of SiC devices could redefine dI_{DS}/dt as a TSEP for SiC MOSFETs. Commercially available 10A, 24A and 42A 1.2kV SiC MOSFETs from Wolfspeed have been characterised under clamped inductive switching conditions at different temperatures. The electrical schematic is shown in Figure 2 and the test rig configuration is shown in Figure 3.

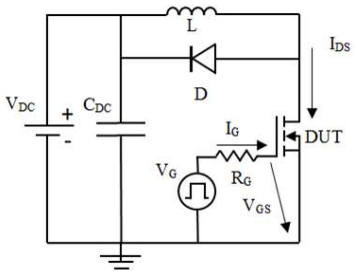
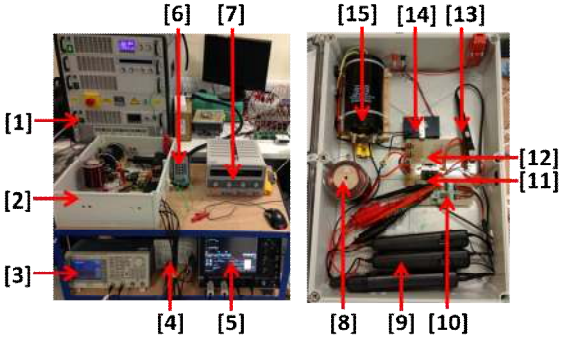


Figure 2: Schematic of the clamped inductive switching test rig

A small heater was used to set the temperature of the device. By leaving enough time to achieve thermal equilibrium, the junction temperature of the device under test (DUT) can be assumed equal to the case temperature set by the heater. The value for the inductor is 2 mH, the freewheeling diode is a SiC Schottky C4D10120A from Wolfspeed, the gate driver voltage output is 0/18 V and the DC link capacitor value is 470 µF.

Figure 4 shows the V_{DS}, I_{DS}, V_{GS} and I_{GS} transients during the SiC MOSFET turn-on for the 1.2kV/42A SiC MOSFET switched with R_G=220 Ω at T_J=25 °C while Figure 5 shows the turn ON for T_J=150 °C. By comparing the measurements at the different temperatures, it can be seen that the average dI_{DS}/dt at 150 °C is higher than at 25 °C.



[1] DC Power Supply, [2] Test Enclosure, [3] Function Generator, [4] Current Probe Amplifier, [5] Oscilloscope, [6] Thermometer, [7] DC Power Supply for the Heater, [8] Inductor, [9] Differential Voltage Probes, [10] Gate Driver [11] DUT, [12] Heater, [13] Current Probe, [14] Freewheeling Diode, [15] DC Link Capacitor

Figure 3: Test rig configuration

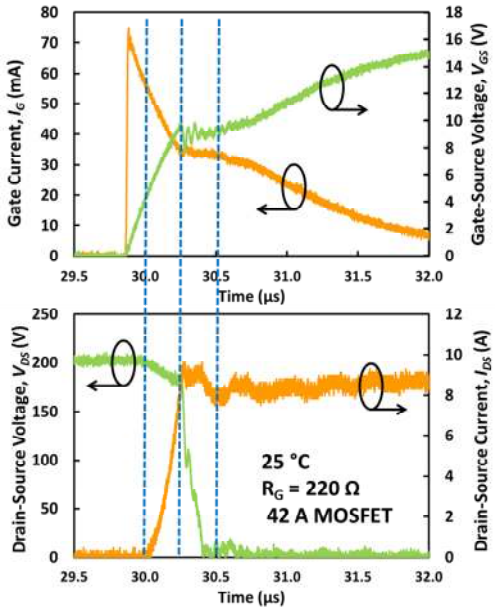


Figure 4: Measured V_{DS}, I_{DS}, V_{GS} and I_{GS} transients during the turn-on for the 1.2kV/42A SiC MOSFET switched with R_G=220 Ω and V_{DC}=200 V at T_J=25 °C

As shown analytically in equations (1) to (9), it can be seen by comparing Figure 4 and Figure 5 that the gate current plateau occurs at a higher current level when T_J=150 °C and the gate voltage plateau occurs at a slightly lower voltage. The reason for this, as explained previously, is that the gate voltage transient enters the plateau region and it starts charging the Miller capacitance sooner: the device begins to conduct current sooner because of the lower threshold voltage and the load current is reached sooner at higher junction temperatures because the rate of change of current with time increases with temperature.

The impact of the temperature on the drain-source current during the turn ON of the device is shown in Figure 6 and Figure 7.

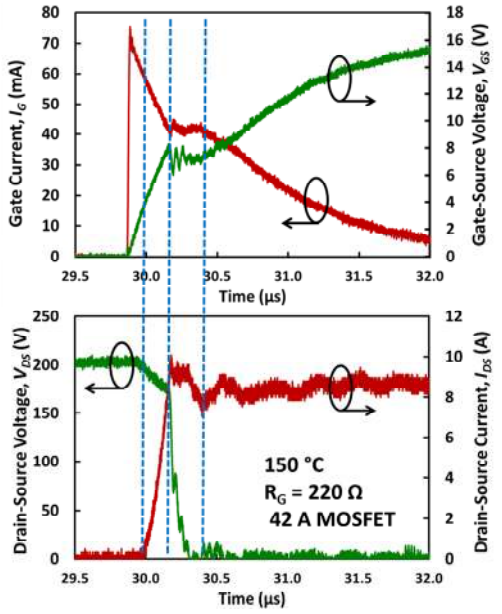


Figure 5: Measured V_{DS}, I_{DS}, V_{GS} and I_{GS} transients during the turn-on for the 1.2kV/42A SiC MOSFET switched with R_G=220 Ω and V_{DC}=200 V at T_J=150 °C

It can be seen from Figure 6 and Figure 7 that the hotter devices turn on faster and sooner. This effect is more easily observable for the larger devices. The time constant defined by the gate resistance and the gate-source and gate drain capacitances determines switching speed. Since parasitic capacitances are proportional to die size/current rating, the capacitances for the large devices are significantly higher according to the datasheet values. The variation of the threshold voltage with temperature (dV_{TH}/dT) is also higher for the 42 A MOSFET, according to the datasheet values which affects both t_0 and t_{RISE} according to equations (3) and (8). The impact of this is clearly visible in case of the 42 A SiC MOSFET, Figure 6(b), compared to the 10 A SiC MOSFET, Figure 7(b).

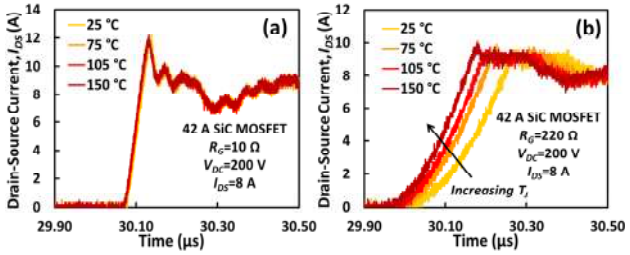


Figure 6: I_{DS} during the turn ON transition of the 42 A SiC MOSFET. V_{DC}=200V. (a) R_G=10 Ω and (b) R_G=220Ω

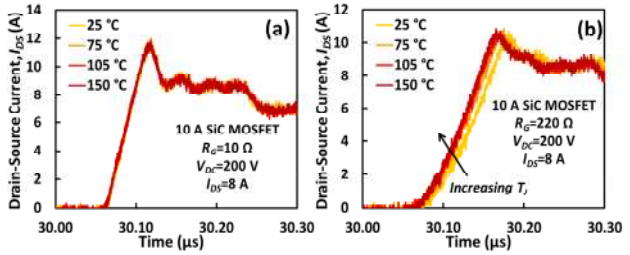


Figure 7: I_{DS} during the turn ON transition of the 10 A SiC MOSFET. V_{DC}=200V. (a) R_G=10 Ω and (b) R_G=220Ω

The dependency of the maximum turn-ON dI_{DS}/dt on the gate resistances and junction temperature for the SiC MOSFETs studied in this paper are shown in Figure 8. The impact of the internal gate resistance, which is higher for the smaller device since it is inversely proportional to the die size, reduces the effect of the variation of the external gate resistance on dI_{DS}/dt. In other words, as the current rating is decreased, the impact of R_G on dI_{DS}/dt also decreases. For the 10 A rated SiC MOSFETs, the impact of increasing the gate resistance on the switching rate is not as observable as for the 42 A SiC MOSFET.

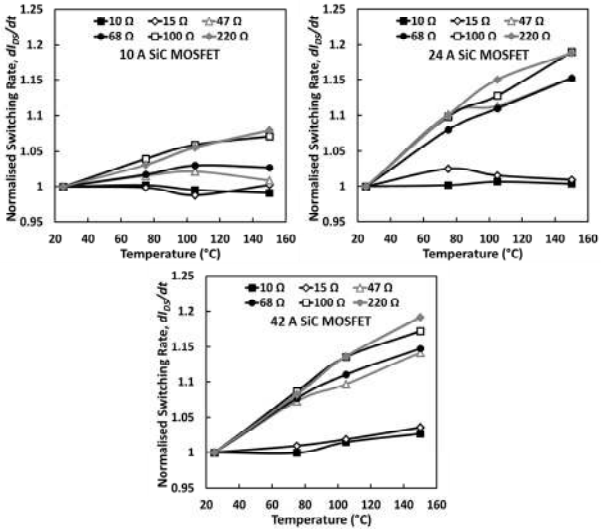


Figure 8: Maximum dI_{DS}/dt for the SiC MOSFETs. I_{DS}=8A, V_{DC}=200V at different temperatures and different R_G values

The gate current during the turn ON transient of the 10 A, 24 A and 42 A SiC MOSFETs is shown in Figure 9, Figure 10 and Figure 11 respectively. Figure 9(a) shows the measured gate current of the 10 A SiC MOSFET switched with a 10 Ω gate resistance over junction temperatures ranging from 25 °C to 150 °C. Figure 9(b) shows a similar plot for the same device but switched with a 220 Ω gate resistance. As expected, the peak gate current measured when the MOSFET is switched with R_G=10 Ω (700 mA) is much higher than that when the MOSFET is switched with R_G=220 Ω (65 mA).

Since the total gate charge is constant, the higher peak current in the R_G=10 Ω case occurs over a much smaller duration compared with the case of R_G=220 Ω. It can also be seen that the temperature dependency of the gate current in In case of the 24 A SiC MOSFET, Figure 10(a) is not clear because the different components of the gate current are not clearly delineated. In Figure 10(b), the different components are clearly delineated hence, the temperature dependency is clear and the results follow the behaviour predicted by equations (1) to (10). The results for the 42 A SiC MOSFET are shown in Figure 11. Using a R_G=220 Ω, the 3 current components are clearly defined and the plateau resolution is better than for the 10 A SiC MOSFET. The effect of temperature on V_{TH} and dI_{DS}/dt is more observable for the larger dies, hence the temperature sensitivity of the gate current plateau is better, especially when a large external R_G is used i.e. the time

constants that define the transient response increase. The impact of the internal gate resistance can be seen in the peak gate current values. The higher internal gate resistance causes a lower value of the peak gate current for the 10 A SiC MOSFET compared with the 42 A SiC MOSFET.

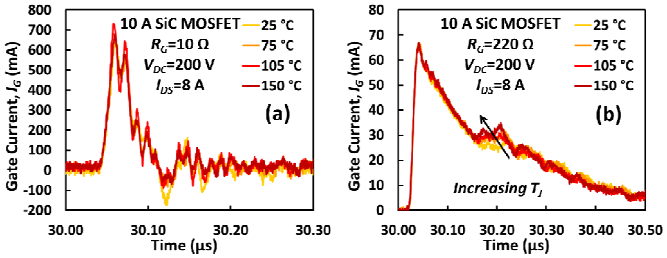


Figure 9: 10 A SiC MOSFET - I_G during turn ON (a) R_G=10Ω (b) R_G=220Ω

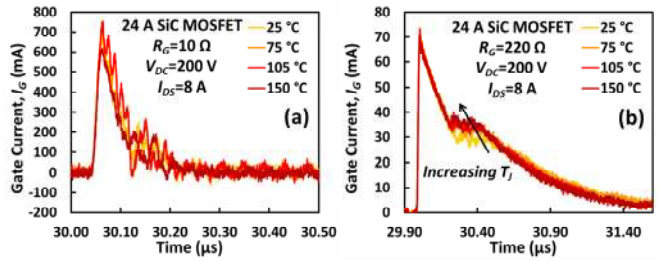


Figure 10: 24 A SiC MOSFET - I_G during turn ON (a) R_G=10Ω (b) R_G=220Ω

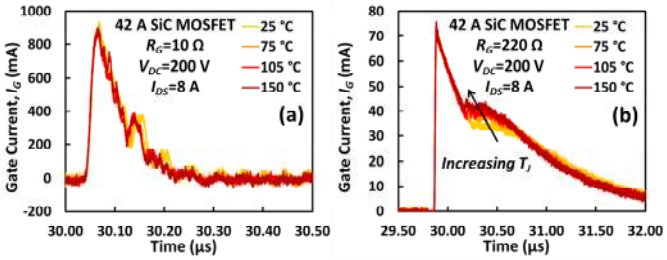


Figure 11: 42 A SiC MOSFET - I_G during turn ON (a) R_G=10Ω (b) R_G=220Ω

4 Condition Monitoring Implementation and Impact on the Switching Losses

If the switching rate is to be used as a TSEP for condition monitoring in SiC power MOSFETs, then its relationship with other parameters on the circuit must be characterised. An effective TSEP must show a strong temperature correlation and not change excessively with other circuit parameters [2]. To investigate this, measurements were performed to determine the dependency of the switching rate and gate current plateau on the load current. Figure 12 shows the turn-on drain-source current characteristics of the 42A SiC power MOSFET switched with R_G=220 Ω for 3 different load currents namely, 9, 18 and 27 A and V_{DS}=400 V. The results shown in Figure 12 suggest that the gate current plateau has a strong dependence on the load current value but the drain current switching rate during turn ON seems not to be affected by the load current value.

The turn-ON current of a MOSFET is comprised of the saturation current at low V_{GS} and the linear mode current at high V_{GS}. The saturation current is proportional to $(V_{GS}\text{-}V_{TH})^2$ [10], while the linear current is proportional to V_{GS}. Hence, the switching rate is not constant during the turn ON of the MOSFET as the current moves from saturation to linear. Using a large external R_G not only makes the turn ON slower but it also increases the time that the device is in the saturation stage of the turn ON (where the load current is parabolic in the vicinity of V_{TH} [10]). The analysis of the dI_{DS}/dt for the 42 A SiC MOSFET during the turn ON transient for different load current values at V_{DS}=400 V is shown in Figure 13. The average slope of I_{DS} has been calculated from the measured data using an 80 ns window shifted every 200 ps i.e. dI_{DS}/dt is calculated using a moving window, but for practical implementation it would be possible to use analogue electronics. The results show that dI_{DS}/dt does not change with the load current during the turn ON transient but the maximum dI_{DS}/dt can be affected by the value of the load current due to its parabolic nature before going into linear.

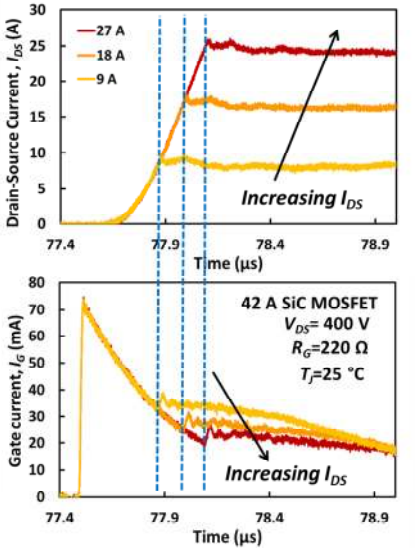


Figure 12: Drain-Source current and gate current during the turn ON transient of the 42 A SiC MOSFET at different load current values

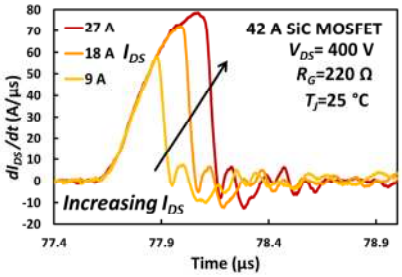


Figure 13: dI_{DS}/dt during turn ON at different I_{DS} values

The impact of the junction temperature on the dynamic dI_{DS}/dt during the turn ON has been analysed for the 10 A and 42 A SiC MOSFETs shown in Figure 6 and Figure. 7. The calculated dI_{DS}/dt is shown in Figure 14 and Figure 15. The use of large gate resistances increases the time that the device is in the saturation mode where the dI_{DS}/dt has a high temperature sensitivity in the areas close to V_{TH}, especially for the higher current rating device.

The use of the drain current switching rate and the gate current transient as TSEPs for SiC MOSFETs has several trade-offs. Slowing down the device using a higher gate resistance allows higher temperature sensitivity for the current switching rate but with a penalty of increasing the switching losses [9].

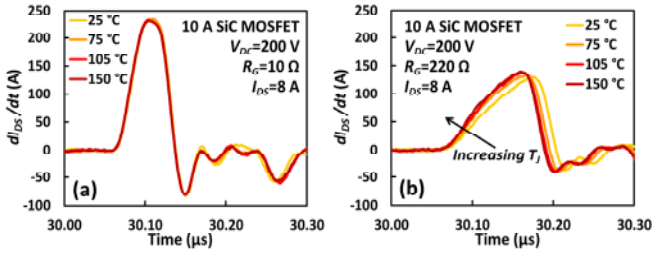


Figure 14: 10 A SiC MOSFET dI_{DS}/dt during turn ON at different temperatures. a) R_G=10Ω (b) R_G=220Ω

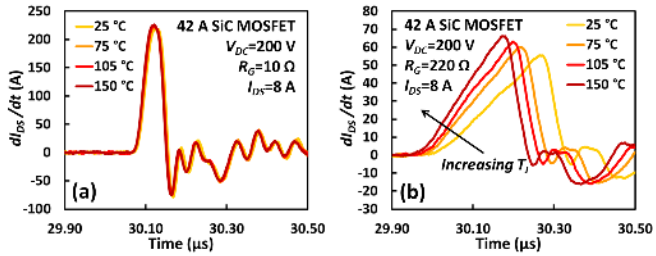


Figure 15: 42 A SiC MOSFET dI_{DS}/dt during turn ON at different temperatures. a) R_G=10Ω (b) R_G=220Ω

The analysis of the losses for different gate resistors has been done for the 24 A SiC MOSFET and a 30 A Si IGBT. The results are shown in Figure 16(a). The switching energy as a function of temperature for the 24 A SiC MOSFET and a 30 A IGBT, using a 220 Ω gate resistor is shown in Figure. 16(b) and it can be seen that the superior switching efficiency of the SiC MOSFET compensates the impact of increasing the gate resistance for enabling condition monitoring.

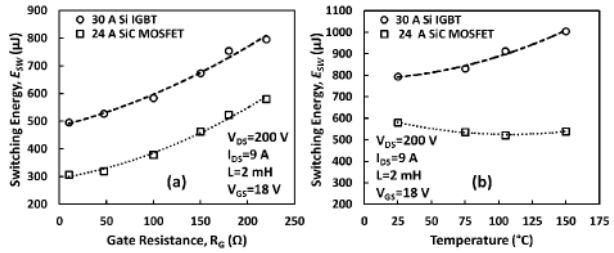


Figure 16: Switching energy comparison of a 24 A SiC MOSFET and a 30 A Si IGBT as a function of R_G (a) as a function of temperature (b)

Conclusion

In this paper two TSEPs for condition monitoring of SiC MOSFETs (by measuring the operating junction temperature) have been analysed. These TSEPs are based on reducing the switching speed of the device, by means of increasing the external gate resistance.

The use of dI_{DS}/dt as TSEP is promising for applications where a high switching rate is not required. The temperature sensitivity of both the maximum dI_{DS}/dt and dI_{DS}/dt at low V_{GS}, in the vicinity of V_{TH}, can be used.

The gate current plateau has a strong dependency on both temperature and the load current; hence its use requires decoupling the effect of the load current on the gate current plateau.

The gate current and turn-ON switching rate are more suitable as TSEPs for high current rated devices, since they are highly influenced by the value of the parasitic capacitances and internal R_G of the devices.

Increasing the gate resistance causes higher switching losses, but the lower switching energy of SiC MOSFETs compared with silicon IGBTs and the temperature independence of the switching losses means a minor sacrifice for enabling the ability of sensing the junction temperature online.

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