

TEMPERATURE-STABLE HIGH-Q ALN-ON-SILICON RESONATORS WITH EMBEDDED ARRAY OF OXIDE PILLARS

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ABSTRACT

This paper reports on a new temperature compensation technique for high- Q AlN-on-Silicon bulk acoustic wave resonators. A uniform array of silicon dioxide (SiO_2) pillars are formed in the silicon body of the resonator to generate a composite resonator with a near-zero temperature coefficient of frequency (TCF). At a resonance frequency of 24MHz, a total frequency drift of 90 ppm over the temperature range of -20°C to 100°C was measured while Q exceeded 10,000 at all temperatures. This compensation technique is applicable to bulk acoustic resonators with thick silicon substrate that demonstrate high Q as well as good power handling and linearity.

INTRODUCTION

AlN-on-Silicon resonators are characterized by low insertion loss and a high Q [3]. However, a major drawback of silicon resonators is in their high TCF, which is in the range of -20 to -30 ppm/ $^\circ\text{C}$ for uncompensated resonators [1] [2]. In order to compensate for this large negative TCF, a layer of a material with positive temperature coefficient of elasticity (typically SiO_2) can be added to the resonator stack [1-3]. However, in order to achieve full temperature compensation in length-extensional resonators, the thicknesses of the SiO_2 and Si layers should be comparable. This creates several problems, given that a relatively thick layer of silicon (20-60 μm) is required in AlN-transduced resonators to achieve a high Q as well as good power handling and linearity. One problem is that the addition of a comparably thick SiO_2 layer will result in a considerable drop in the device Q . Secondly, a thick SiO_2 layer makes the fabrication process challenging. In order to address these challenges, we present a new method of passive material compensation. Instead of adding a thick layer of oxide, a uniform array of SiO_2 pillars are formed in the silicon body of the resonator to generate a composite structure with a near zero TCF. The pillars are formed by filling square-shaped trenches etched in the body of the resonator with high-temperature LPCVD SiO_2 . In contrast to oxide-compensated capacitive resonators, the presented resonators do not require a DC electric field for operation and are hence immune from dielectric charging effects that cause frequency drift [4].

RESONATOR DESIGN

A silicon resonator with a two-dimensional array of uniformly distributed oxide pillars can be modeled as a network of series and parallel finite-mass springs. Figure 1 shows a typical array of oxide pillars and its equivalent mass-spring network model.

The equivalent mass and stiffness of the springs, which determine the resonance frequency of the system and its variation with temperature, depend on the distribution and configuration of the oxide pillars. Assuming a totally uniform pattern, the overall amount of oxide required to fully compensate the negative TCF of the silicon resonator can be estimated from the following equation:

$$\frac{1}{2} \left(\frac{\rho_{ox}^{1/2} E_{si}^{1/2}}{\rho_{si}^{1/2} E_{ox}^{1/2}} + \frac{E_{ox}}{E_{si}} \right) \left(\frac{TCE_{ox}}{TCE_{si}} \right) \left(\frac{V_{ox}}{V_{si}} \right) = -1 \quad (1)$$

Here V_{ox} and V_{si} are the overall volume of oxide pillars and silicon in the resonator, E_{ox} and E_{si} are Young's Modulus and ρ_{ox} and ρ_{si} are density of oxide and silicon respectively.

ANSYS simulations were used to adjust the dimensions and distribution of the oxide pillars and the thickness of the top oxide layer in order to achieve zero TCF over the desired range of temperature at a specific resonance frequency.

RESONATOR FABRICATION

To fabricate the resonators, trenches with slightly tapered sidewalls are first etched into the device layer of an SOI wafer and subsequently filled with LPCVD SiO_2 deposited at 850°C . A smooth top surface is obtained by short wet etching and subsequent deposition of SiO_2 . A nearly smooth surface is required for the deposition of Mo electrodes and high-quality AlN. The rest of the fabrication process is similar to the one reported in [3] with some minor modifications. Figure 2 shows an SEM picture of a fabricated temperature-stable 24MHz resonator with uniformly distributed array of oxide pillars.

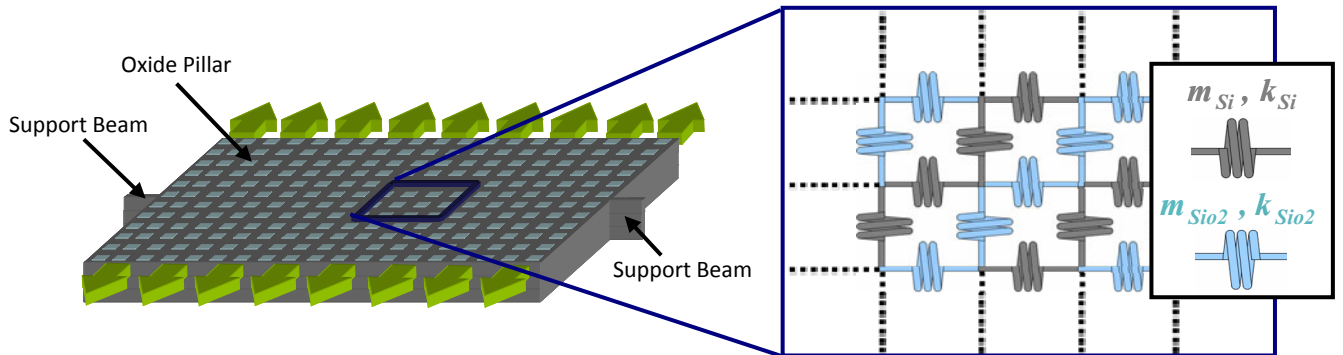


Figure 1: A typical array of oxide pillars in resonator and simplified equivalent mass-spring model. Arrows show resonance direction.

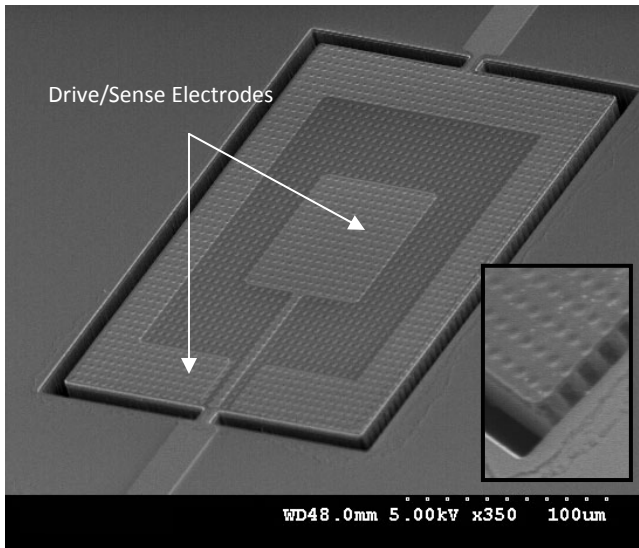


Figure 2: SEM picture of a temperature compensated 24MHz resonator with SiO_2 pillars. Inset shows the oxide pillars.

CHARACTERIZATION RESULTS

Figure 3 is the measured frequency response of the temperature stable resonator of Figure 2 showing very high Q .

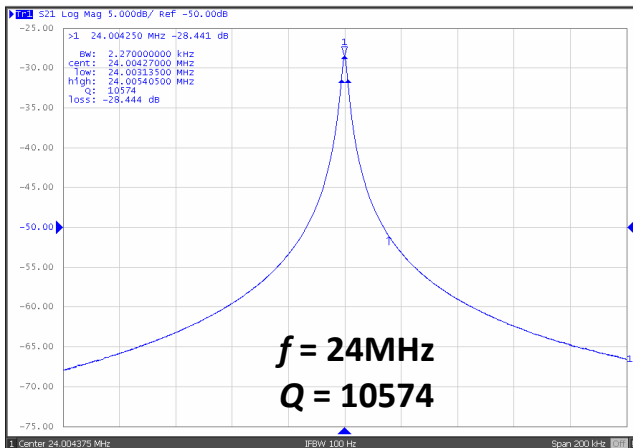


Figure 3: Frequency response of the 24MHz temperature compensated resonator of Figure 2.

Figure 4 shows the temperature characteristics of three identical samples of compensated 24MHz resonators from across the wafer with a $1.4 \mu\text{m}$ of surface LPCVD oxide layer deposited between a $20 \mu\text{m}$ layer of silicon body and Mo/AlN/Mo layers. A resonance frequency drift of 90-180 ppm over the range -20°C to 100°C was measured for these three samples while Q exceeded 10,000 at all temperatures (in vacuum). Figure 5 shows the temperature characteristic of Q for the resonator of Figure 2.

ACKNOWLEDGMENT

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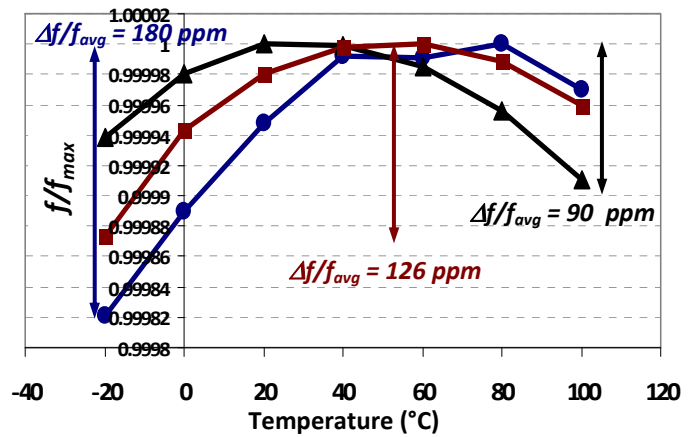


Figure 4: Temperature characteristic of three 24MHz temperature compensated AlN-on-Si resonators with oxide pillars.

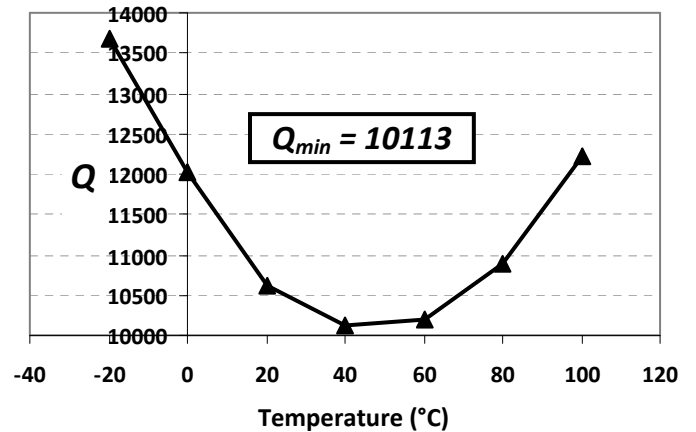


Figure 5: Temperature characteristic of Q for the resonator of Figure 2.

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