Temporal Readout Noise Analysis and Reduction Techniques For Low Light CMOS Image Sensors

Assim Boukhayma, Arnaud Peizerat and Christian Enz

***Abstract*—In this paper, an analytical noise calculation is presented to derive the impact of process and design parameters on 1/f and thermal noise for a low noise CIS readout chain. It is shown that dramatic noise reduction is obtained by using a thin oxide transistor as the source follower of a typical 4T pixel. This approach is confirmed by a test chip designed in a 180nm CIS CMOS process, and embedding small arrays of the proposed new pixels together with state-of-the-art 4T pixels for comparison. The new pixels feature a pitch of 7.5μm and a fill factor of 66%. A 0.4e- RMS input-referred noise and a 185μV/e- conversion gain are obtained. Compared to state-of-the-art pixels, also present onto the test chip, the RMS noise is divided by more than 2 and the conversion gain is multiplied by 2.2.**

I. Introduction

THE development of pinned photo diodes has been crucial for enhancing the sensitivity of CMOS image sensors (CIS) through lower dark current and efficient reset noise cancellation. Since then, efforts have been concentrated on reducing the temporal noise of the readout chain. The implementation of column level amplification and correlated double sampling (CDS) reduces the input-referred readout noise to just a few electrons [1] [2] [3] by reducing 1/f and thermal noise of the readout chain and noise contributions of the next stages such as the buffers and the analog-to-digital converters. After performing these noise reduction techniques, 1/f and RTS like noise originating from the in-pixel amplifying transistor become the dominant noise sources. During the last few years, many works focused on reducing the input-referred temporal noise below the limit of one electron by implementing high column level gain and correlated multiple sampling (CMS) [4] [5].Yet works based on these techniques reported temporal noise ranging between 1 and 2 electrons RMS. The combination of these techniques with device optimization like using in-pixel buried channel source followers [6] [7] or in-pixel PMOS amplifier [8] showed that the noise can be reduced slightly below the one electron RMS barrier.

Both the pixel conversion gain and the $1/f$ noise depend on the in-pixel source follower design and technological parameters. Therefore finding the exact relationship between the source follower gate size, the oxide thickness and the input-referred noise leaves some room for further optimization. In order to address this problem, this paper presents an analytical temporal noise calculation in a CIS readout chain with pinned photo diode, column amplification and correlated sampling. The obtained expressions of the input-referred noise show the impact of the source follower gate dimensions and oxide thickness as well as other design parameters and suggest that the reduction of the gate oxide thickness of the source follower leads to lower noise and better conversion gain. However, the image sensor process flow is not yet compatible with gate oxide thickness reduction, thus, a pixel, based on a state-of-the-art CIS process, where only the source follower transistor features a thin gate oxide is introduced. Compared to a state-of-the-art pixel with an optimized source follower embedded on the same chip, the new pixel shows more than 50% less noise confirming the theoretical results.

This paper is organized as follows: Section II recalls the operation principle of a CIS readout chain. In Section III the analytical noise calculation of the input-referred thermal and 1/f noise is presented. The noise reduction strategy and the new pixel design are detailed in Section IV. Sections V and VI describe the test and measurement results.

II. Operation of CIS readout chain

State-of-the-art low light CMOS image sensors readout chains are based on pixels with pinned photodiodes and column level amplification. Fig. 1 shows a schematic of a classical CIS readout chain with the corresponding timing diagram. When the row selector switch is turned on (RS high), the sense node is first reset to a voltage V_{RST} higher than the pinning voltage of the buried photo diode. After auto-zeroing of the column amplifier, the reset voltage level is sampled at the output of the column amplifier. Then, the transfer gate is pulsed to allow charge transfer from the pinned photodiode to the sense node. The voltage drop in the sense node is amplified and sampled at the column level amplifier output. The first (reset) and second (transfer) samples are then differentiated using analog circuitry or after analog-to-digital conversion of both samples. Correlated multiple sampling (CMS) can also be used at the output of the readout chain. It consists of differentiating the average values of multiple samples during the reset and transfer phase. The double sampling readout scheme of the CIS readout chain cancels the reset $\frac{kT}{C}$ noise as well as the column amplifier and pixel source follower offset. The noise performance of the classical read-out chain is analyzed in details in the next Section.

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Assim Boukhayma is with the CEA-LETI, Grenoble, France and Ecole Polytechnique Federale de Lausanne (EPFL), Lausanne, Switzerland.(e-mail: assim.boukhayma@epfl.ch).

Arnaud Peizerat is with the CEA-LETI.

Christian Enz is the diredtor of the IMT institute of EPFL, Neuchatel, Switzerland.

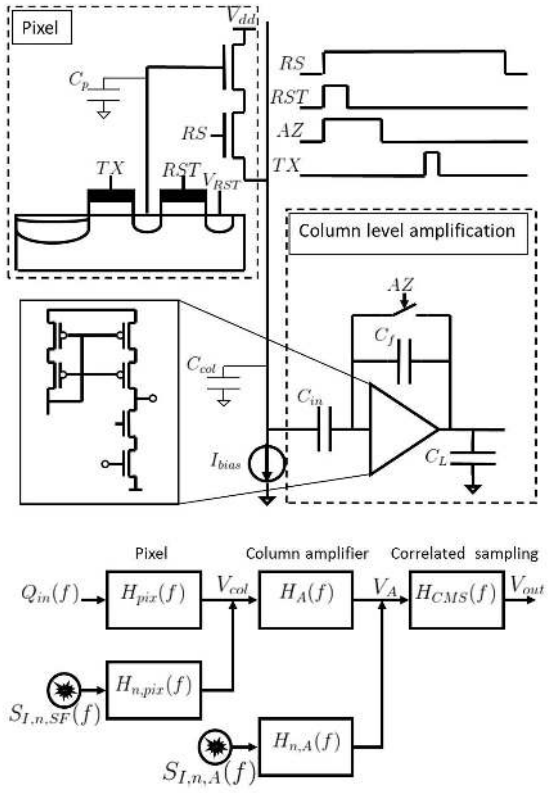


Fig. 1. CIS readout chain with its timing diagram and a schematic depicting the signal path togetehr with the source follower and the column amplifier noise paths

III. Noise analysis of the CIS readout chain

In the following analysis, it is assumed that the noise sources of the different devices are statistically independent and hence uncorrelated. The transfer function from each noise source to the output is first calculated. The total output referred noise variance is then given by the sum of all variances corresponding to each noise source. The 1/f and thermal noise are analyzed separately in order to clarify their relative impact on the output-referred noise. In this readout chain, only two dominant noise sources are considered, namely, one from the in-pixel source follower transistor, and one from the column amplifier as depicted in Fig. 1. The noise originating from the bias circuits and from the power supply are neglected at this point since they can be designed to be negligible compared to the noise sources directly affecting the signal-path.

The input signal of the CIS readout chain is the charge transferred to the sense node. For the readout circuit, the noise mechanism is better described as a current or voltage fluctuation. Thus, the readout noise is calculated at the output of the signal path as a voltage using the noise transfer functions, then referred to the input as a charge after division by the gain of the signal path, namely the pixel conversion gain A_{CG} and column level amplifier gain G_A.

For noise calculation, we consider the noisy model of a MOS transistor in saturation where the drain noise current PSD including thermal and $1/f$ noise is given by [9]

$$S_{I,n}(f) = 4kT\gamma g_m + \frac{K}{C_{ox}^2 WL}\frac{g_m^2}{f}, \tag{1}$$

where k is the Boltzmann constant, T the absolute temperature, g_m the gate transconductance, γ the excess noise factor given by $\frac{2n}{3}$, for a transistor biased in strong inversion, where n is the slope factor [9], K is a process dependent parameter related to the flicker noise, C_{ox} is the gate oxide capacitance per unit area. W and L are respectively the width and length of the transistor gate.

A. Signal transfer functions

The pinned photo diode is modeled with a current source $I_{in}(t)$ injecting a charge $Q_{in} = I_{in} \cdot \triangle t$ in the sense node. The transfer function of the pixel giving the expression of the column level voltage induced by a charge injected in the sense node can be expressed using the simplified small-signal circuit of Fig. 2a. Assuming that $g_{out,SF} \ll g_{m,SF}$, where $g_{out,SF}$ is output conductance of the source follower and $g_{m,SF}$ its gate transconductance. The pixel transfer function is given by

$$H_{pix}(f) = \frac{V_{col}}{Q_{in}} = \frac{A_{CG}}{1 + j\frac{f}{f_{c,pix}}}, \tag{2}$$

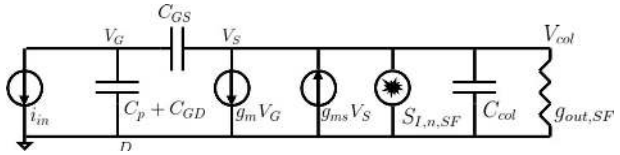
where $f_{c,pix} = \frac{1}{2\pi}\frac{g_{m,SF}}{C_{col}\cdot A_{CG}\cdot(C_{GS}+C_{GD}+C_P)}$ is the cut-off frequency of the in-pixel source follower stage, C_{col} is the column level capacitance, C_{GS} and C_{GD} are the gate-to-source and gate-to-drain source follower capacitances, C_P is the sum of parasitic capacitances due to wiring, transfer gate, reset transistor and the n^+ junction, and n is the slope factor of the source follower transistor [9]. In saturation, $n = \frac{g_{ms,SF}}{g_{m,SF}}$ where $g_{ms,SF}$ is the source transconductance of the source follower transistor. The value of n ranges from 1.2 to 1.6. The conversion gain corresponds to the dc gain of the pixel transfer function $H_{pix}(f)$. It is given by

$$A_{CG} = \frac{\frac{1}{n}}{C_P + C_{GD} + (1-\frac{1}{n})C_{GS}}. \tag{3}$$

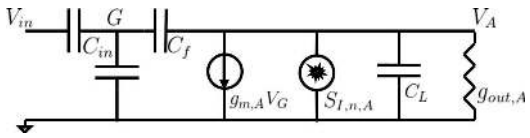
The transfer function of the column amplifier when the auto-zeroing switch is opened is calculated based on the small-signal circuit shown in Fig. 2b. The column level gain is given by $G_A = \frac{C_{in}}{C_f}$, where C_{in} and C_f are respectively the integrating and feedback capacitors of the column level amplifier. In order to simplify the noise calculations, it is assumed that $G_A \ll \frac{g_{m,A}}{g_{out,A}}$, where $g_{out,A}$ and $g_{m,A}$ are the output conductance and the transconductance of the column level operational transconductance amplifier (OTA). The zero frequency of the column amplifier transfer function numerator $\frac{g_{m,A}}{C_{in}}$ has been neglected. The column amplifier transfer function is then expressed as

$$H_A(f) = \frac{-G_A}{1 + j\frac{f}{f_{c,A}}}, \tag{4}$$

where $f_{c,A} = \frac{1}{2\pi}\frac{g_{m,A}}{(G_A+1)C_L+C_{in}}$, C_{in} and C_L are the column amplifier integrating and load capacitors.



(a) In-pixel source follower stage



(b) Column level amplifier

Fig. 2. Simplified small-signal circuit

The transfer function of the CMS has been derived in previous works [10] [11] its squared magnitude is given by

$$|H_{CMS}(f)|^2 = \frac{4}{M^2} \frac{sin^4(\pi M \cdot T_{CMS} \cdot f)}{sin^2(\pi T_{CMS} \cdot f)}, \tag{5}$$

where M is the number of the equally spaced samples and T_{CMS} is the duration between them.

B. Noise transfer functions

Based on the small-signal circuit depicted in Fig. 2a, the transfer function of the noise originating from the in-pixel source follower referred to the column level is given by

$$H_{n,pix}(f) = \frac{\frac{1}{g_{m,SF}} A_{CG} \cdot (C_{GS} + C_{GD} + C_P)}{1 + j\frac{f}{f_{c,pix}}}. \tag{6}$$

The column level amplifier operates in two phases, auto-zeroing and amplification. After auto-zeroing, the noise frozen in the integrating capacitor C_{in} is transferred to the feedback capacitor and to the output during the amplification phase. This frozen noise is canceled thanks to the action of the correlated double sampling at the output of the column amplifier. Thus, for noise calculation, we only need to consider the direct noise at the output of the column amplifier during the amplification phase. Using the small-signal circuit of Fig. 2b, the transfer function for the noise originating from the column level amplifier and referred to its output is given by

$$H_{n,A}(f) = \frac{\frac{G_A+1}{g_{m,A}}}{1 + j\frac{f}{f_{c,A}}}. \tag{7}$$

C. Thermal noise analysis

The current PSD of the thermal noise originating from the in-pixel source follower is expressed based on (1). The output referred source follower thermal noise voltage PSD is then calculated using the pixel noise transfer function $H_{n,pix}(f)$ and the signal transfer functions of the column amplifier and CMS as

$$S_{n,th,SF,out}(f) = 4kT\gamma_{SF} g_{m,SF} |H_{n,pix}(f) H_A(f) H_{CMS}(f)|^2 \tag{8}$$

In the same way, the expression of the output referred PSD of thermal noise originating from the column amplifier is given by

$$S_{n,th,A,out}(f) = 4kT\gamma_A g_{m,A} |H_{n,A}(f) H_{CMS}(f)|^2. \tag{9}$$

In (8) and (9), γ_{SF} and γ_A are noise excess factors of the source follower and the column amplifier respectively. The total output thermal noise PSD is then given by the sum of $S_{n,th,A,out}(f)$ and $S_{n,th,SF,out}(f)$. The input referred noise charge variance is then calculated using the total gain of the signal path. It is expressed as

$$\overline{Q^2_{n,th}} = \frac{1}{A^2_{CG} \cdot G^2_A} \int_0^\infty S_{n,th,SF,out}(f) + S_{n,th,A,out}(f) df. \tag{10}$$

It is not easy to find the analytical expression of $\overline{Q^2_{n,th}}$ because of the $H_{CMS}(f)$ term. But the impact of CMS on thermal noise has been studied numerically in previous works [11] [10]. When the readout chain cutoff frequency is sufficiently larger than the sampling frequency, the thermal noise variance after CMS is simply multiplied by a factor $\frac{2}{M}$. Using this assumption, the variance of the total input-referred thermal noise charge can be expressed as

$$\overline{Q^2_{n,th}} = \frac{2kT}{M \cdot G_A \cdot C} \left(\frac{\gamma_{SF} g_{m,A} (C_{GS} + C_{GD} + C_P)^2}{g_{m,SF}} + \frac{\gamma_A}{A^2_{CG}} \right), \tag{11}$$

where $C = C_L + \frac{C_{in}}{G_A+1}$. This equation is discussed in more details in Section IV.

D. 1/f noise analysis

Since the $1/f$ noise PSD is inversely proportional to the transistor gate area $W \cdot L$, the $1/f$ noise contribution of all the readout chain transistors could be made negligible at the cost of a larger area and parasitic capacitances. However, this unfortunately doesn't hold for the source follower transistor. Indeed, as will be shown in more details in Section IV, its equivalent input-referred $1/f$ noise charge contribution actually increases when increasing the gate area. This is due the fact that the conversion gain is roughly inversely proportional to $W \cdot L$. Referring the $1/f$ noise to the input by dividing the noise PSD by the square of the conversion gain makes the input-referred noise charge roughly proportional to $W \cdot L$. It is therefore crucial to correctly model the dominant $1/f$ noise contribution of the source follower. Following the same steps used above for the thermal noise calculation, the output referred PSD of the $1/f$ noise originating from the pixel is given by

$$S_{n,1/f,out}(f) = \frac{K g^2_{m,SF}}{C^2_{ox} W L f} |H_{n,pix}(f) H_A(f) H_{CMS}(f)|^2(f), \tag{12}$$

and the input referred $1/f$ noise charge variance can be expressed as

$$\overline{Q^2_{n,1/f}} = \frac{1}{A^2_{CG} \cdot G^2_A} \int_0^\infty S_{n,1/f,out}(f) df. \tag{13}$$

We introduce the parameter α_{CMS} given by

$$\alpha_{CMS} = \int_0^\infty \frac{|H_A(f)^2|}{G^2_A} \frac{|H_{CMS}(f)^2|}{f} df. \tag{14}$$

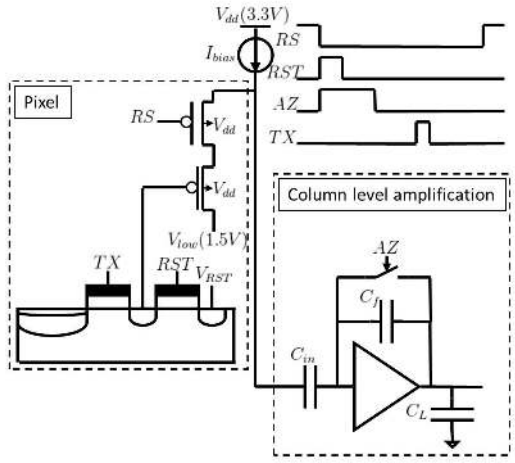


Fig. 3. CIS readout chain based on a thin oxide source follower with its timing diagram

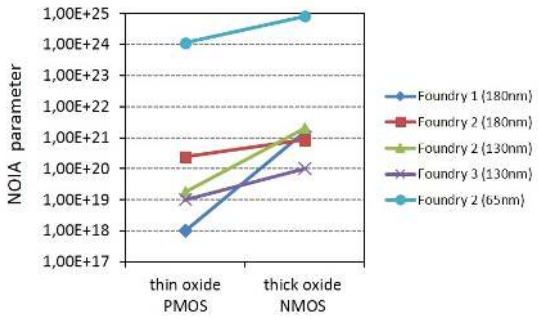


Fig. 4. NOIA parameter proportional of thin oxide PMOS and NMOS for different foundries and technology nodes

α_{CMS} has been studied numerically in [10]. It depends only on the ratio between the column amplifier cutoff frequency and the sampling frequency of the CMS as well as the CMS order M. When the column amplifier cutoff frequency is much larger than the sampling frequency and the order M is higher than 4, $\alpha_{CMS} \simeq 3$ [10]. The input referred $1/f$ noise charge variance is then given by

$$\overline{Q^2_{n,1/f}} = \frac{K(C_P + C_{GS} + C_{GD})^2}{C_{ox}^2 WL}\alpha_{CMS}. \qquad (15)$$

This result is discussed in more detail in Section IV.

IV. Noise reduction techniques for CIS readout chains

Based on (11), the input-referred thermal noise charge variance can be reduced using parameters independent from the pixel design, namely, the column amplification (G_A), correlated multiple sampling (M) and bandwidth control (C). CMS and bandwidth control play the same role in the thermal noise reduction. In fact, increasing the number of samples M increases the readout time by a factor of M. Reducing the bandwidth by a factor of M by using $M.C$ instead of C has exactly the same effect. Simulation results detailed in [10] show that the combination of these design parameters makes

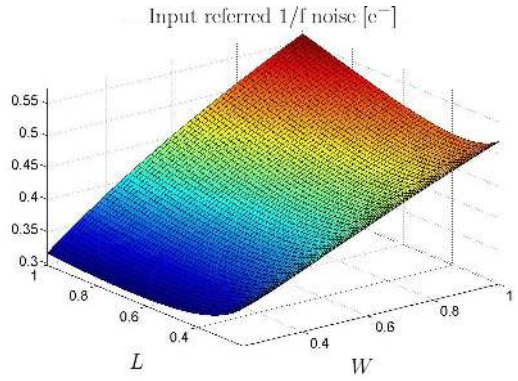


Fig. 5. Calculated input referred $1/f$ noise (16) as a function of the in-pixel source follower width W and length L for a thin oxide PMOS in a $180nm$ technology where $C_P = 0.6fF$, $C_{gse} = C_{gde} = 0.95fF/\mu m$, $C_{ox} = 9.5fF/\mu m^2$, $K = 10^{-12}F^2V^2/m^2$ and $\alpha_{CMS} = 3$.

$1/f$ noise originating from the in-pixel source follower the dominant noise source.

Equation (15) determines the impact of design and technological parameters on the input-referred $1/f$ noise charge variance. But still, the expression of $C_{GD} + C_{GS}$ as a function of the source follower gate width and length is to be determined. The gate-to-source C_{GS} and gate-to-drain C_{GD} capacitances include both intrinsic and extrinsic components. The intrinsic component is proportional to the gate area WL and depends on the transistor biasing. The extrinsic component, including overlap and fringing field parasitic capacitances , is less dependent on the transistor biasing and is proportional to the gate width W. When the source follower transistor operates in strong inversion, the intrinsic component of $C_{GD}+C_{GS}$ is dominated by C_{GS}, and is approximately equal to $\frac{2}{3}C_{ox}WL$. The extrinsic component of $C_{GD} + C_{GS}$ can be expressed as $(C_{gde} + C_{gse})W$. Thus the expression of the input-referred $1/f$ noise becomes

$$\overline{Q^2_{n,1/f}} = \frac{K\left(C_P + (C_{gse} + C_{gde})W + \frac{2}{3}C_{ox}WL\right)^2}{C_{ox}^2 WL}\alpha_{CMS}. \qquad (16)$$

Equation (16) suggests that the input-referred $1/f$ noise can be reduced by increasing the gate oxide capacitance per unit area C_{ox} and reducing the source follower gate size. C_{ox} can be increased by reducing the gate oxide thickness. CIS image sensors process flow uses thick oxide transistors to support high voltages used to reduce leakage currents and difficulties to downscale the pinning voltage of buried photodiodes. A way to overcome this limitation is by using a thin oxide transistor only for the source follower. But still, it is important to verify that reducing the gate oxide thickness does not come with a negative impact on the $1/f$ noise K factor. Intuitively, since the gate control over the channel increases when the gate oxide thickness is reduced, the K factor should be smaller for thin oxide transistors. In order to verify this assumption, data from different foundries design kits are investigated. Design kits are based on the BSIM3V3 model for all compared technology nodes except for the $65nm$ technology where the design kit is based on BSIM4. For BSIM3V3 [12], the NOIA

parameter is proportional to the spice model K factor, the BSIM4 NOIA parameter is converted using the following equation [13]: $NOIA_{BSIM3V3} = 1.6.10^{-17} NOIA_{BSIM4}$. Fig. 4 shows, for each foundry, that the NOIA parameter for thick oxide NMOS is higher than for thin oxide PMOS and therefore that the $1/f$ noise K factor is lower for the thin oxide PMOS. Moreover, based on (11), the contribution of the in-pixel source follower to the input-referred thermal noise is proportional to $C_P + (C_{gse} + C_{gde})W + \frac{2}{3}C_{ox}WL$. Thus, this contribution is also expected to decrease by reducing the gate oxide thickness if both the width W and length L of the source follower gate are reduced by at least by the same factor, especially when $\frac{2}{3}C_{ox}WL$ dominates.

The optimal sizing of the source follower transistor for low $1/f$ noise can also be calculated analytically [10] or numerically using (16) as shown in Fig. 5.

The new readout chain based on the thin oxide PMOS source follower is depicted in Fig. 3. In the $180nm$ process used for this work, the voltage difference between the four thin oxide source follower transistor terminals (gate, source, drain and bulk) must not exceed $1.8V$. In this work a "digital" thin oxide PMOS source follower is used to meet this condition.

V. Test description

In order to confirm the theoretical results presented in the previous sections, a test chip has been designed to compare a state-of-the-art pixel, already optimized for low noise, with the new pixel based on the thin oxide PMOS source follower introduced in Fig. 3. Both pixels are based on 4 transistors and a classical pinned photo diode. The new pixel features a pitch of $7.5\mu m$ and a fill factor of 66%. The reference pixel used for comparison features a pitch of $6.5\mu m$. The $5mm \times 1mm$ test chip presented in Fig. 6 is designed in a $180nm$ CMOS process dedicated to image sensors and includes a total of 24 columns connected to small arrays of new and reference pixels, each surrounded by 8 dummy pixels for proper characterization. Both pixels are implemented with the same column level amplifier limiting the bandwidth to $265kHz$ and offering a gain adjustable between 8 and 64 in order to check its impact on noise. The internal amplifier consists of a common source fully cascoded amplifier as shown in Fig. 1. The column amplifier is followed by a voltage buffer to drive the signal to the input of an external 14 bits ADC.

The test follows the same path than the one used for the noise calculation: the overall conversion gain ($A_{CG} \times G_A$) of each readout chain is measured first, then the output noise is measured and referred to the input using the overall conversion gain. The source follower and column amplification voltage gain is measured using the reset voltage as an input while opening the reset switch.

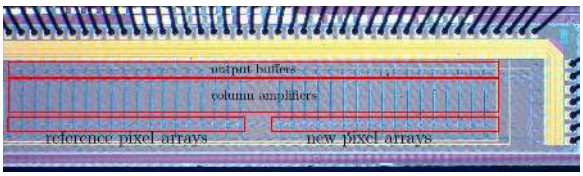


Fig. 6. Test chip micrograph

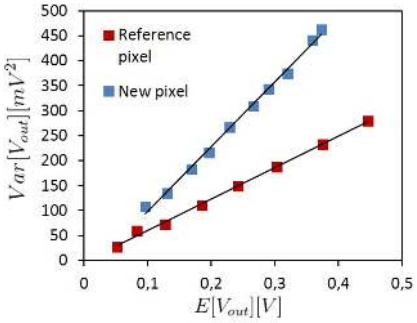


Fig. 7. Conversion gain measurement using the photon transfer curve

VI. Measurement results

In order to measure the conversion gain, the photon transfer curve (PTC) method [14] is used. Photon shot noise dominates the readout noise when the pixel receives an amount of photons between the noise floor and saturation. For an average number N of received photons, the variance of the corresponding shot noise is given by N. On the one hand, the mean value of the signal at the output of the readout chain is given by

$$E[V_{out}] = N \times A_{CG} \times G_A. \tag{17}$$

On the other hand, the variance of the output voltage when the photon shot noise dominates is given by

$$Var[V_{out}] = N \times (A_{CG} \times G_A)^2. \tag{18}$$

Thus, the readout chain conversion gain can be obtained without knowing the exact value of N combining equations (17) and (18)

$$A_{CG} \times G_A = \frac{Var[V_{out}]}{E[V_{out}]}. \tag{19}$$

Therefore, the plot of $Var[V_{out}]$ as a function of $E[V_{out}]$ should correspond to a line for which the slope matches with the value of $CG \times G_A$. This technique is used for both pixels by illuminating them with a voltage controlled LED to obtain different points. For each LED voltage value, a 100 readouts are operated in order to obtain statistically

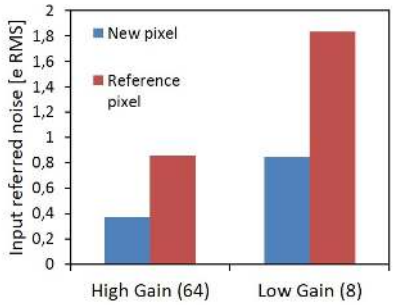


Fig. 8. Measured input-referred noise for two column gains

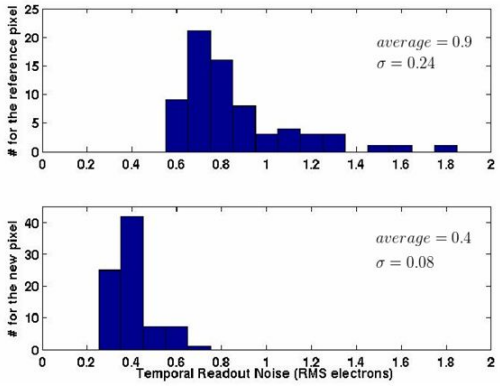


Fig. 9. Histograms of input-referred noise of readout chains based on both pixels for a column level gain of 64

the corresponding values of $Var[V_{out}]$ and $E[V_{out}]$. Fig. 7 shows the results obtained for both pixels. The points of both curves are well aligned, which confirms the validity of this measurement method. The conversion gain is then calculated by estimating the slope factor of both curves. The conversion gain of the new pixel is equal to $185\mu V/e^-$ whereas for the reference pixel, it is equal to $85\mu V/e^-$.

The output noise variance and RMS value are measured for all pixels by using a 14 bits ADC. The noise is measured by operating 1000 readouts for each pixel without activating the transfer gate. Fig. 9 shows the histograms of the input-referred noise charge obtained with all the new and reference pixels (85 of each) with a column gain of 64. The new pixel shows a lower average input-referred noise below $0.4e^-_{RMS}$. The reference NMOS source follower based pixel features an average input referred noise of $0.9e^-_{RMS}$. In addition, the histograms show that the standard deviation corresponding to the noise measurement of the new pixels is three times smaller than that of the reference pixel. The impact of the column level gain on the average value of the input-referred noise for both pixels is shown in Fig. 8. The new pixel shows more than 50% less noise than the reference pixel even at low gain ($G_A = 8$) when $1/f$ noise is not dominating. This confirms that reducing the gate dimensions and choosing a thin gate oxide also reduces the input-referred thermal noise of the readout chain as shown theoretically in Section IV.

An overview of the recently reported sensitive CMOS image sensors is summarized in Table I. It shows that the reduction of the temporal read noise to below $1e^-_{RMS}$ has been made at the cost of a large pixel pitch and a low fill factor. A comparison of the presented readout chain based on the new pixel with state-of-the-art CMOS image sensors shows that the proposed noise reduction technique is very promising. Indeed, the new pixel features lower noise with higher fill factor and lower pixel pitch. In addition, these results are obtained using a "digital" thin oxide PMOS which leaves some room for more optimization at the process level.

VII. Conclusion

A detailed noise analysis of a CIS readout chain showing the impact of the in-pixel source follower gate size and oxide thickness together with design and technological parameters is presented. Analytical noise calculation shows that the input-referred noise can be significantly reduced by, on one hand reducing the gate oxide thickness of the in-pixel source follower (choosing a thin oxide transistor instead of a traditional thick oxide transistor) and on the other hand reducing its gate area, assuming that the 1/f noise factor K of the thin oxide device remains equal or smaller than that of the thick oxide transistor. A new pixel, based on a thin oxide PMOS source follower with a pitch of $7.5\mu m$ and a fill factor of 66 % has been designed in a standard $180nm$ CIS CMOS process to verify the theoretical results. The new pixel is implemented on the same chip together with a state-of-the-art pixel based on an thick oxide NMOS source follower already optimized for low noise. Test and characterization of the new pixel and the reference pixel shows that the noise reduction technique proposed in this work is very promising. Indeed, the new proposed pixel achieves an input-referred noise of $0.4e^-_{RMS}$ corresponding to a noise reduction of more than 50 % compared to the classical reference pixel.

TABLE I
Overview of recently reported sensitive CMOS image sensors

Technique	Noise $[e^-_{rms}]$	Conversion gain $[\mu V/e^-]$	Pixel pitch $[\mu m]$	Fill-factor [%]	Reference
Multiple Sampling, Folding Integration/ Cyclic ADC	1.2	67	7.5	52	ISSCC 2011 [5]
Pseudo Multiple Sampling with SSADC	1.1	110	1.4		ISSCC 2010 [4]
PMOS Common-Source Pixel Amplifier	0.86	300	11	50	ISSCC 2011 [8]
Buried Channel NMOS source follower, Multiple Sampling with SSADC	0.7	45	10	33	ISSCC 2012 [7]
Thin oxide PMOS source follower	**0.4**	**185**	**7.5**	**66**	**This work**

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Assim Boukhayma was born in Rabat, Morocco, on February 5, 1988. He received the graduate engineering degree (D.I.) in information and communication technology and the M.Sc. in microelectronics and embedded systems architecture from Telecom-Bretagne, Brest, France, in 2013. He is currently working toward the Ph.D. at École Polytechnique Fédérale de Lausanne (EPFL), Neuchâtel, Switzerland and Commissariat a l'Energie Atomique (CEA-LETI), Grenoble, France with Prof. Christian Enz on the subject of CMOS image sensors.
From 2011 to 2012, he worked with Bouygues-Telecom as a Telecommunication Radio Junior Engineer. In 2013, he did his M.Sc. Internship at Commissariat a l'Energie Atomique (CEA-LETI) on the design of a low noise CMOS THz camera.

Arnaud Peizerat was born in Nice, France, in 1975. He received the M.Sc. degree in electronic engineering from Institut National Polytechnique de Grenoble, Grenoble, in 1998, the Agregation degree from Education Nationale, Cachan, in 1999 and the Ph.D. degree in microelectronics from Institut National Polytechnique de Grenoble, Grenoble, in 2006.
He is currently a Research engineer in the Image Sensor design Laboratory at the CEA-LETI, Grenoble. His research interests include solid-state image sensors and low-noise mixed-signal design for IR, visible or X-ray applications. He is the author or co-author of 17 papers and 8 patents in the field of image sensors.

Christian Enz (M'84, S'12) received the M.S. and Ph.D. degrees in Electrical Engineering from the EPFL in 1984 and 1989 respectively. From 1984 to 1989 he was research assistant at the EPFL, working in the field of micro-power analog IC design. In 1989 he was one of the founders of Smart Silicon Systems S.A. (S3), where he developed several low-noise and low-power ICs, mainly for high energy physics applications. From 1992 to 1997, he was an Assistant Professor at EPFL, working in the field of low-power analog CMOS and BiCMOS IC design and device modeling. From 1997 to 1999, he was Principal Senior Engineer at Conexant (formerly Rockwell Semiconductor Systems), Newport Beach, CA, where he was responsible for the modeling and characterization of MOS transistors for the design of RF CMOS circuits. In 1999, he joined the Swiss Center for Electronics and Microtechnology (CSEM) where he launched and lead the RF and Analog IC Design group. In 2000, he was promoted Vice President, heading the Microelectronics Department, which became the Integrated and Wireless Systems Division in 2009. He joined the EPFL as full professor in 2013, where he is currently the director of the Institute of Microengineering (IMT) and head of the Integrated Circuits Laboratory (ICLAB). He is lecturing and supervising undergraduate and graduate students in the field of Analog and RF IC Design at EPFL. His technical interests and expertise are in the field of very low-power analog and RF IC design, semiconductor device modeling, and inexact and error tolerant circuits and systems. He has published more than 200 scientific papers and has contributed to numerous conference presentations and advanced engineering courses. Together with E. Vittoz and F. Krummenacher he is one of the developer of the EKV MOS transistor model and the author of the book "Charge-Based MOS Transistor Modeling - The EKV Model for Low-Power and RF IC Design" (Wiley, 2006). He has been member of several technical program committees, including the International Solid-State Circuits Conference (ISSCC) and European Solid-State Circuits Conference (ESSCIRC). He has served as a vice-chair for the 2000 International Symposium on Low Power Electronics and Design (ISLPED), exhibit chair for the 2000 International Symposium on Circuits and Systems (ISCAS) and chair of the technical program committee for the 2006 European Solid-State Circuits Conference (ESSCIRC). He has been elected as member of the IEEE Solid-State Circuits Society (SSCS) Administrative Commmittee (AdCom) from 2012 to 2014. He is also Chair of the IEEE SSCS Chapter of Switzerland.