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Ternary and quaternary logic to binary bit conversion CMOS integrated circuit design using multiple input floating gate MOSFETs

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TERNARY AND QUATERNARY LOGIC TO BINARY BIT CONVERSION CMOS INTEGRATED CIRCUIT DESIGN USING MULTIPLE INPUT FLOATING GATE MOSFETS

A Thesis

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by
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Abstract

Multiple-input floating gate MOSFETs and floating gate potential diagrams have been used for conversion of ternary-valued input and quaternary-valued input into corresponding binary-valued output in CMOS integrated circuit design environment. The method is demonstrated through the design of a circuit for conversion of ternary inputs 00 to -1-1 (decimal 0 to -4) and 00 to 11 (decimal 0 to +4) into the corresponding binary bits and for conversion of quaternary inputs (decimal 0 to 3) into the corresponding binary bits (binary 00 to 11) in a standard 1.5 µm digital CMOS technology. The physical design of the circuits is simulated and tested with SPICE using MOSIS BSIM3 model parameters. The conversion method is simple and compatible with the present CMOS process. The circuits could be embedded in digital CMOS VLSI design architectures.

The conversion circuit for ternary inputs into corresponding binary outputs has maximum propagation delay of 8 ns with 0.1 pF simulated capacitive load. The physical layout design occupies an area of 432×908 µm^2.

The conversion circuit for quaternary inputs to corresponding binary outputs has maximum propagation delay of 6 ns with 0.1 pF simulated capacitive load. The physical layout design occupies an area of 130×175 µm^2. The conversion circuit achieved significant improvement in the number of devices. A reduction of more than 75% in transistor count was obtained over the previous designs. Measurements of the fabricated devices for the conversion of quaternary input into binary output agree with simulated values.

Chapter 1

Introduction

The performance of two level binary logic is limited due to interconnects which occupy a large area on a VLSI chip. In a VLSI circuit, approximately 70 percent of the area is devoted to interconnection, 20 percent to insulation, and 10 percent to device [1]. One can achieve a more cost-effective way of utilizing interconnections by using a larger set of signals over the same area in multiple-valued logic (MVL) devices [2,3], allowing easy implementation of circuits. In MVL devices, the noise advantage of binary logic is retained. The higher radix in use is the ternary (radix-3) and the quaternary (radix-4). Two logic systems are available in ternary logic, balanced ternary logic -1, 0 and 1 and simple ternary logic 0, 1 and 2. The quaternary logic uses 0, 1, 2 and 3 logic levels. Figure 1.1 shows ternary logic with a 3 V supply voltage. Figure 1.2 shows quaternary logic levels.

In any numerical system, the smaller the radix the larger the number of digits required to present a given quantity. The number necessary to express a range N is given by $N = R^d$ where R is the radix and d is the necessary number of digits, rounded up to the next highest integer. The cost and complexity C of system hardware is proportional to the digit capacity R×d [3], then

$$C = k(R \times d) = k \left[R \frac{\log N}{\log R} \right] \tag{1.1}$$

where k is constant. Differentiating with respect to R will show that for minimum cost C, R should be equal to e = 2.718. Since in practice R must be an integer, this suggests that R = 3 (ternary) would be more economical than R = 2 (binary) [3].
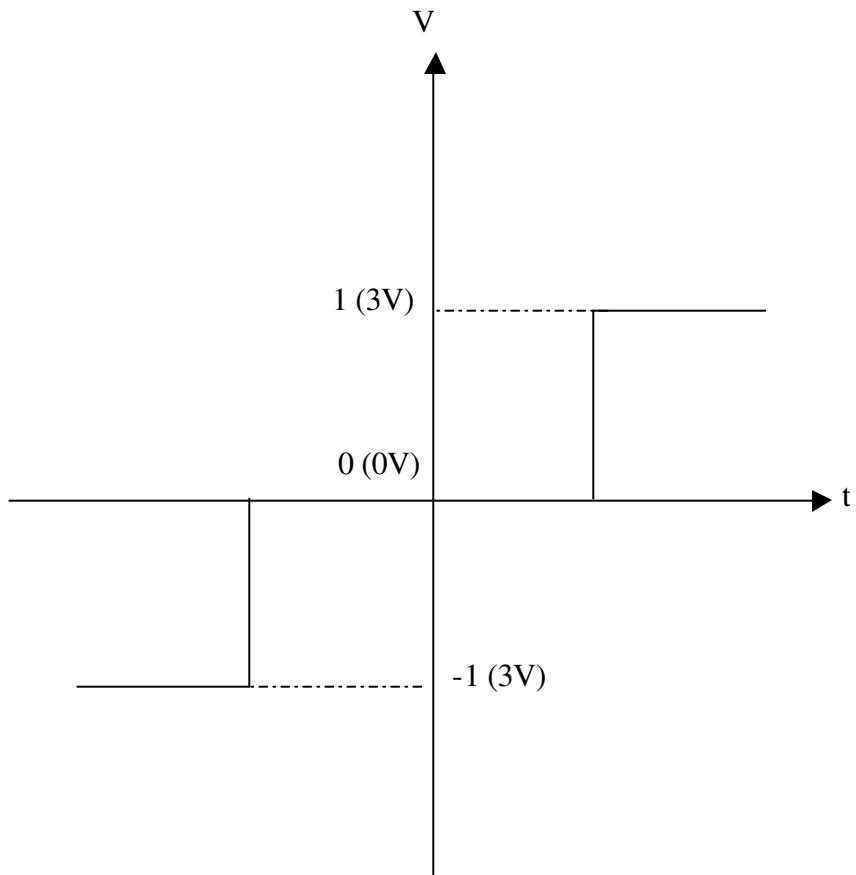
Fig. 1.1: Logic levels used for a ternary logic.
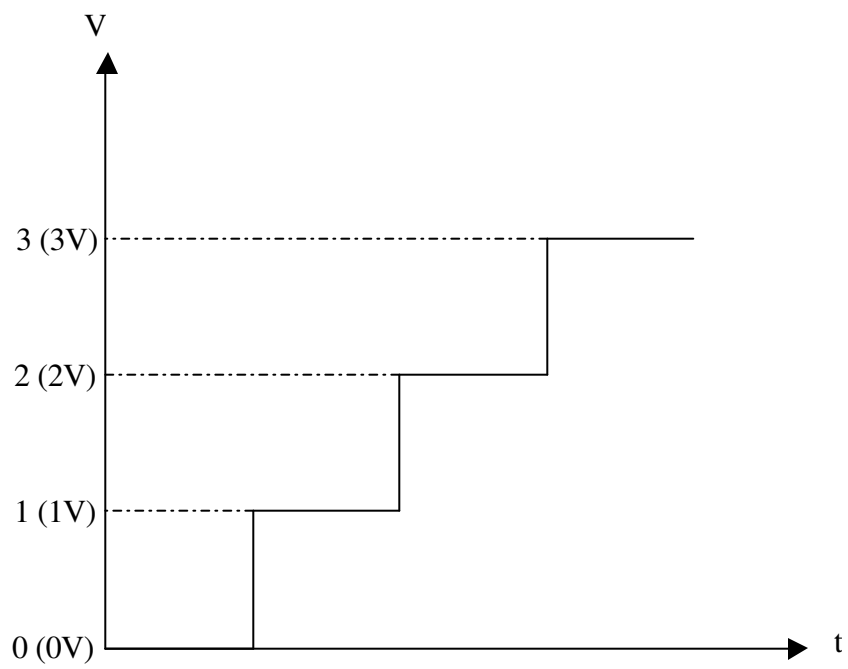
Fig. 1.2: Logic levels used for a quaternary logic.

If it is assumed that circuit cost and complexity C for processing one signal line remains constant irrespective of radix, then total system cost C is merely proportional to d. In this case

$$C = kd = k \left\lceil \frac{\log N}{\log R} \right\rceil \tag{1.2}$$

which is a gradually decreasing cost with increasing radix R.

The ternary logic system is represented in two different logic levels; simple (or "unsigned") ternary logic levels 0, 1 and 2 and balanced (or "signed") ternary logic levels -1, 0 and $+1$. The balanced ternary logic level system has added mathematical advantages in numerical representation and in arithmetic operations over the simple ternary logic system [3,4]. It can represent both positive and negative numbers without using an unary minus. The negative of a number is obtained by interchanging $+1$ and -1. Addition and multiplication are almost as simple as for the binary, cases with no digits larger than 1 in the tables. It follows that addition and subtraction may be performed with the same hardware in balanced ternary system by sign changes of the addend or subtractend, respectively as required. Simple algorithms are available for division. The operation of rounding to the nearest integer is identical to truncation (i.e., deleting everything to the right of the radix point). Ternary arithmetic with both unsigned and balanced (signed) encoding is found in [5]. It is shown that the balanced ternary provides a significant reduction in the gate count in comparison to binary and unsigned ternary systems, but at the expense of an increased logic delay.

In a standard CMOS process with supply voltage of 3 V, the logic level -1, 0 and 1 is defined as -3 V, 0 V and 3 V, respectively. The advantage of an odd valued radix in a complex number multiplier suitable for applications such as discrete Fourier transform has been demonstrated [6]. Wu [7] has listed the advantages and disadvantages of using multi-valued logic implemented with in integrated circuits. He discussed the reasons for focusing on the ternary logic over quaternary logic in terms of cost and complexity, characteristics and additional hardware required. The ternary logic has better noise margin and noise immunity when compared to quaternary logic because of the use of two different voltage sources. The power dissipation is higher in ternary logic circuits, as the peak-to-peak voltage of ternary logic is twice that of binary logic circuits. Srivastava and Venkatapathy [8] have demonstrated that ternary logic circuits could be implemented in standard CMOS process with voltage supply as low as 1 V.

In order to make use of the advantages of multi-valued logic, the structure of mixed radix system using multi-valued and binary logic is more appropriate than use of only multi-valued logic [9,10]. Therefore, it will be necessary to provide encoding and decoding circuitry to perform the required conversion between multi-valued logic signaling on the bus and the binary logic processing circuits. The usage of multi-valued circuits over binary circuits deals with the circuit complexity of encoder and decoder and other circuits for the same case. Lack of simple encoder and decoder schemes for the multi-valued system reduces the effective usage of MVL circuits in VLSI circuits. In the present work, floating gate MOSFETs are used to simplify the design of conversion circuits.

1.1 Literature Review

The encoder and decoder circuits to convert binary logic to multivalued logic and multivalued logic to binary logic have been reported in literature [10-24]. Few of those circuits are discussed below.

The radix conversion circuit is designed using a radix converting read only memory (RCROM) [11]. The RCROM behaves very similar to a binary read only memory (ROM), except that the differential drivers and level shifters used in RCROM drives proper voltage levels to transistors of memory array. The block diagram showing the implementation of the radix conversion is shown in the Fig. 1.3.

The value to be converted from source radix (S'r') to destination radix (D'r') is applied to RCROM, which acts as an address to the memory. The address is decoded to produce row and column select signals. The row select signal turns ON a column line of the required D'r' logic level. Then column select signal turns ON a transmission gate and connects the column line to an output node. Thus an n-place source S'r' value is converted to the equivalent m-place destination D'r' value. The conversion circuit was implemented in 1.2-μm technology. The ternary logic uses 0, 1 and 2 logic levels with supply voltages of 0 V, 2.5 V and 5 V, respectively. The supply voltages of 2.5 V and 5 V were applied externally to the circuit.

Wu [7] implemented ternary logic circuits (ternary NAND, ternary AND, ternary NOR, ternary OR, ternary NOT) using resistors, using logic levels of (0,1,2). The encoder and decoder circuits for conversion between binary logic to ternary logic and ternary logic to binary logic were presented utilizing different design

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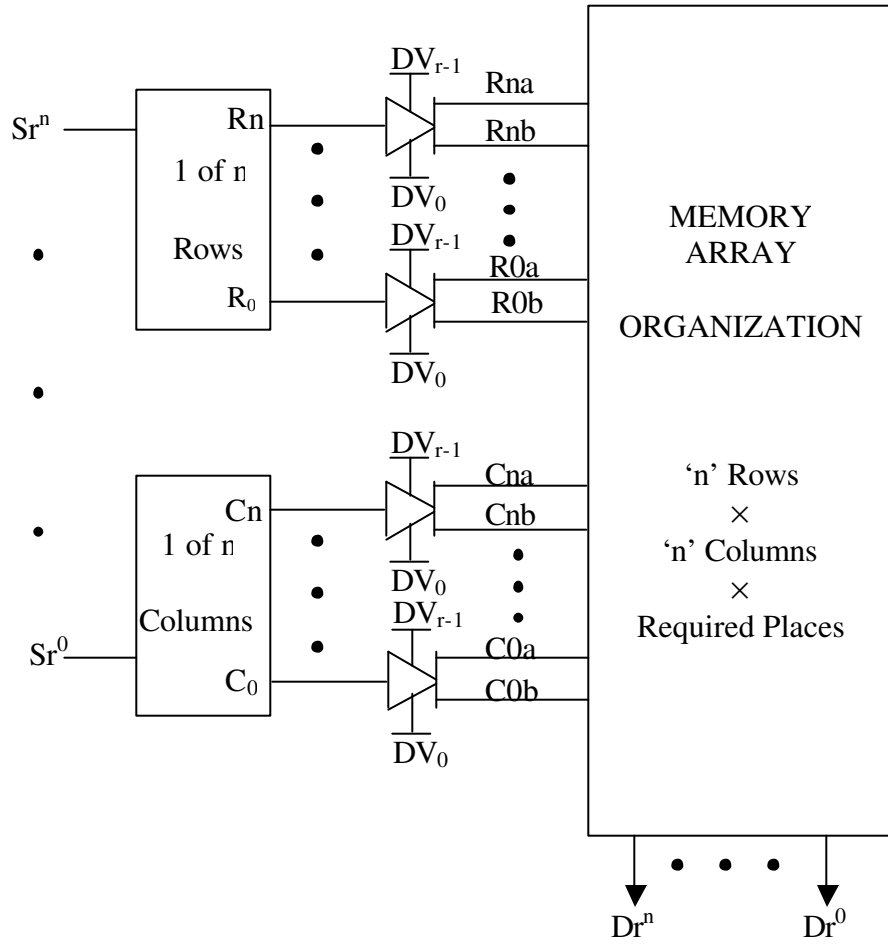
Fig. 1.3: The block diagram for radix converting read only memory (RCROM).

techniques. The decoder circuits were designed by i) altering the width to length ratio of CMOS transistors, by ii) using pad MOS transistors and by iii) using multi-threshold CMOS transistors. In i), the width to length ratio is adjusted such that the threshold voltage of inverter is set to obtain the binary outputs. In ii), stacking an nMOS transistor at ground or pMOS transistor at power supply changes the threshold voltage, which gives the binary output. In iii), MOSFETs with different threshold voltages are designed.

Wu and Huang [12] presented a parallel-pipelined multiplier using dynamic ternary logic circuits. The multiplier is reported to have lesser device count, increased operating frequency, lesser latency, power dissipation and chip area. The basic design of multiplier uses a block, which converts radix-2 redundant positive digit number (0,1,2) to binary (0,1). The converter is implemented using dynamic logic with clock Φ, and by adjusting the threshold voltages such that binary output is produced at clock edges.

Ueno *et. al.*[13] designed conversion circuits from binary to multi-valued and multi-valued to binary using switched capacitor array technique. The basic design presented can be extended to any radix. The block diagram of the converter from multi-valued to binary is shown in Fig. 1.4. As shown in Fig. 1.4, the threshold voltages $V_{th}(k)$ are generated using the equation,

$$V_{th}(k) = \left\{1 - \frac{2k-1}{2(n-1)}\right\}V_{ref} \, , (k = 1,2,3..., n-1) \tag{1.3}$$

where V_{ref} is the reference voltage and n is the radix. The threshold voltages are sampled and held in hold circuits. Multi-valued input voltage is compared with these threshold voltages. The outputs of the comparators are fed as inputs to the
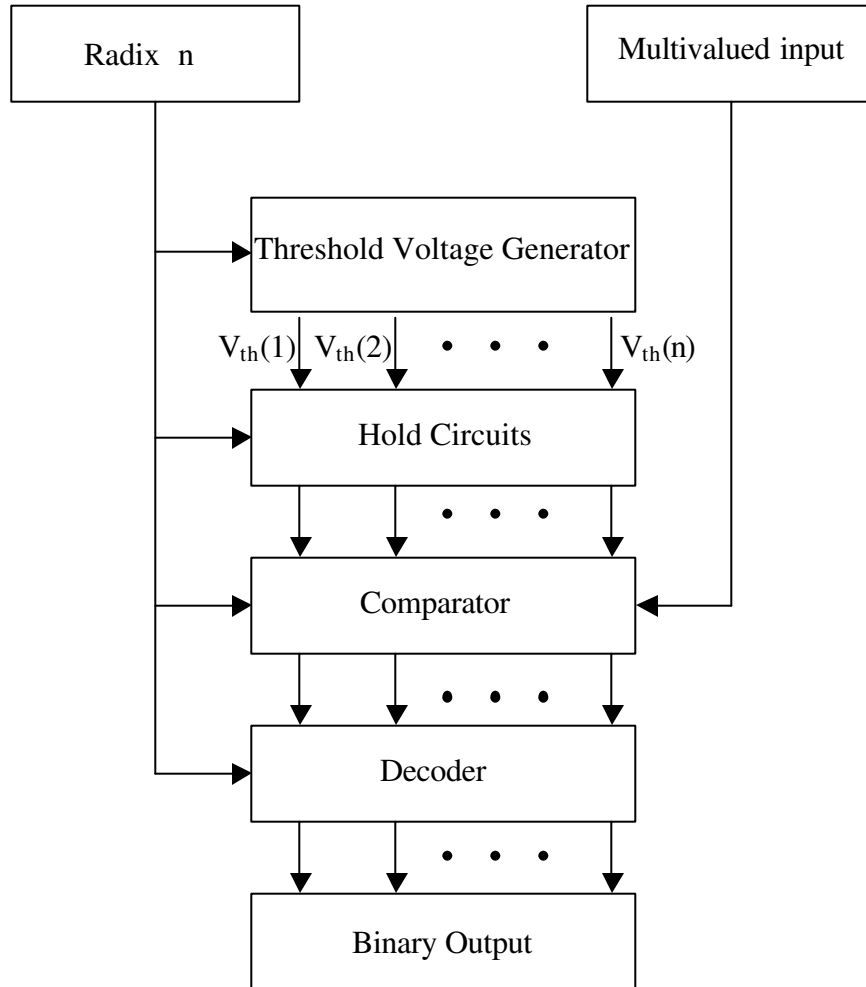
Fig. 1.4: Block diagram for the conversion from multivalued to binary logic using switched capacitor array technique.

decoding circuit, which generates binary output. The accuracy of the decoder depends on the generation of threshold voltages. The circuit configuration uses capacitors to generate the threshold voltage, which allows the design to be extended for large radices without loosing accuracy.

The above design is applied for the conversion from ternary logic (n=3) to binary logic (n=2). Using equation (1.3), the threshold voltages to be generated are $V_{th}(1) = 3/4V_{ref}$ and $V_{th}(2) = 1/4V_{ref}$. The ternary input 0 (0V), 1 ($1/2V_{ref}$) or 2 (V_{ref}) when applied to the circuit are compared with the thresholds $1/4V_{ref}$ and $3/4V_{ref}$ and decoded to give binary output.

Li *et. al.* [14] proposed conversion technique from binary to balanced ternary logic (-1,0,1) based on Josephson technology. They converted an eight bit binary number to six bit ternary number. The schematic diagram of binary to ternary converter for 8-bit binary number constructed using six cells is shown in Fig. 1.5. The basic structure of the cell used in Fig. 1.5 is shown in Fig. 1.6, where (I_{b0}, …, I_{b7}) is 8 bit binary input. The symbol SG is sum circuit to produce ternary output '*t*' and CG is carry circuit to produce C_{01} or C_{02}. The SG and CG circuits are constructed with Josephson complementary ternary logic (JCTL), which exhibits symmetrical I-V characteristics. In summary, the decoder circuits found in literature converted ternary logic (0, 1, 2) to binary logic (0, 1). Few encoder and decoder [8,13-21] circuits for conversion from binary to quaternary (0, 1, 2, 3) and quaternary to binary are found in literature. The present work focuses on conversion from balanced ternary logic (-1, 0, 1) to binary logic using floating gate MOSFETs.
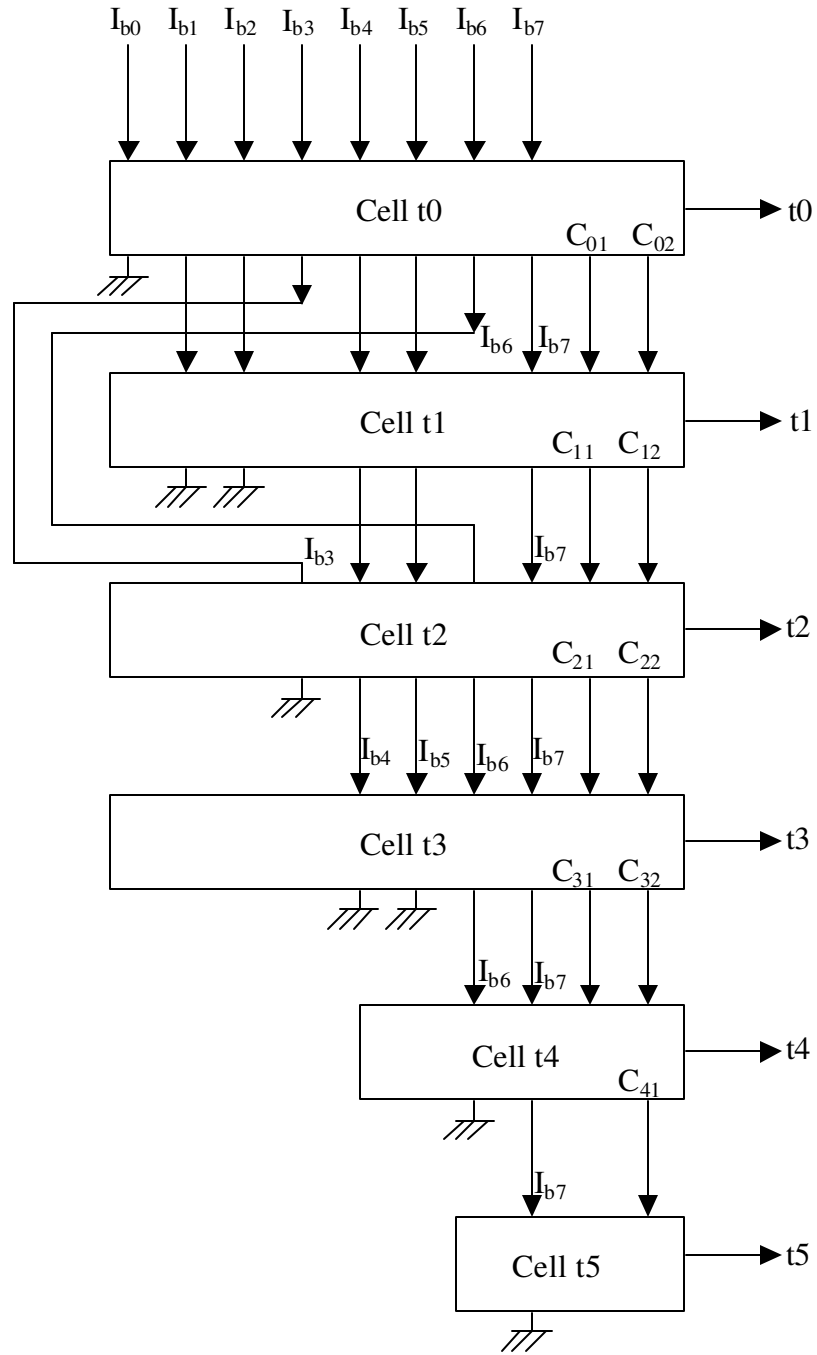
Fig. 1.5: Block diagram for conversion from eight bit binary number to six bit ternary number using Josephson junction technology.

I_{b2} I_{b1}

I_{b0} I_{b3}

SG   SG

S   S

I_{b6} I_{b5}

I_{b4} I_{b7}

SG

I_{b0} I_{b2} I_{b1} I_{b3} I_{b4} I_{b6} I_{b5} I_{b7}

S   t0

CG

C

C_{01}

CG   CG

C   C

C_{02}
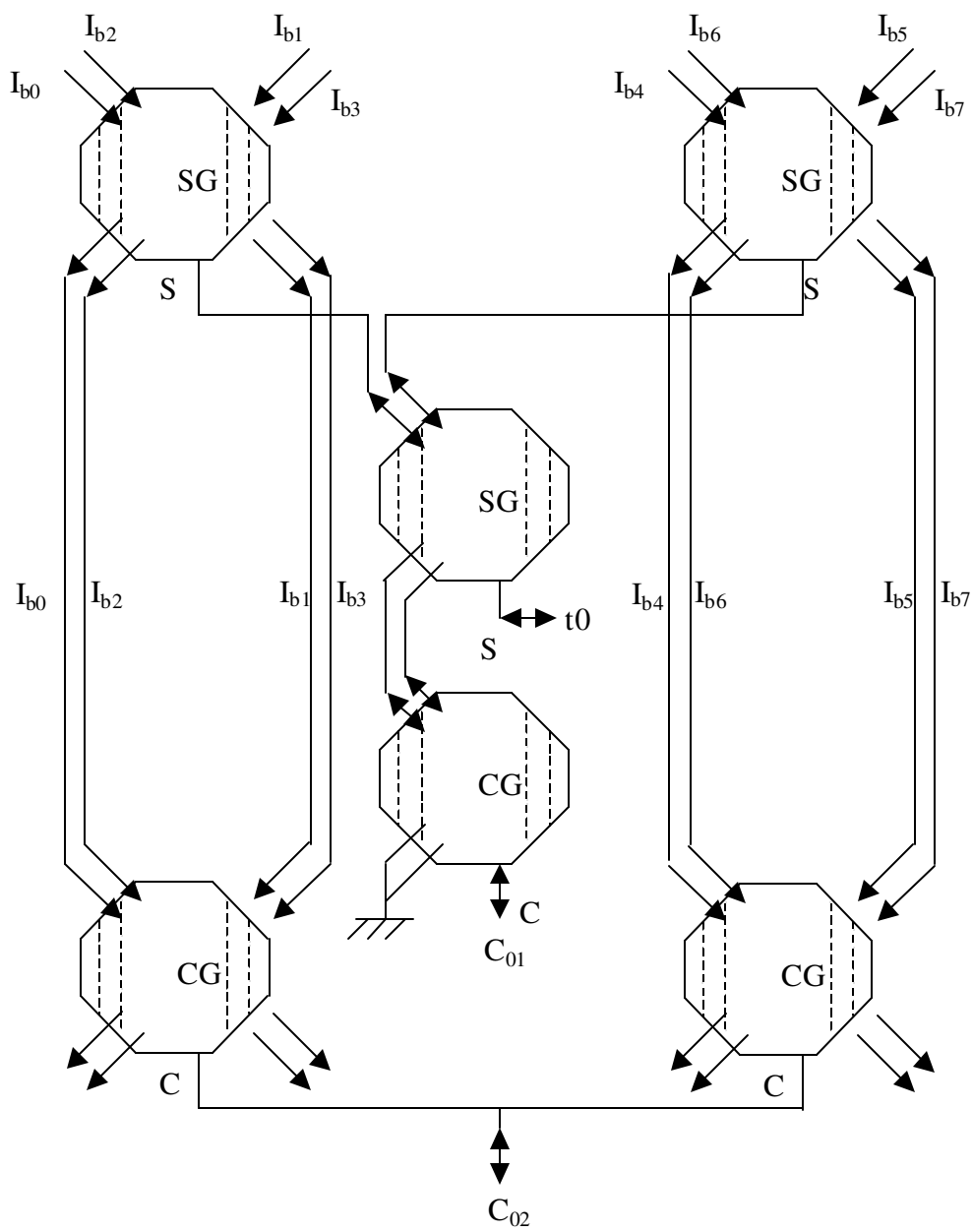
Fig. 1.6: Schematic diagram of cell shown in Fig. 1.5.

1.2   Chapter Organization

The basic structure and operation of floating gate devices is discussed in Chapter 2. The design flow with simulation results obtained from SPICE, for conversion from balanced ternary to binary logic is presented in Chapter 3. In Chapter4, a scheme to convert quaternary to binary bit is presented. Chapter 5 concludes the present work. The circuit files used for simulations to obtain the I-V characteristic curves of floating gate MOSFETs are listed in Appendix A. The MOS model parameters used for design is presented in Appendix B. The MOS model parameters of the fabricated chip are presented in Appendix D. Techniques used to simulate floating gate devices in SPICE is presented in Appendix C.

Chapter 2

Multiple-Input Floating Gate MOSFET (MIFG MOSFET)

2.1 Introduction

The multiple-input floating gate devices are well known for EPROMs, EEPROMs, and flash memories [24,25,26]. The primary principle is that the polysilicon floating gate of MOS transistor, is insulated with silicon dioxide, and hence, maintains stored charge for a long time. The floating gate devices are implemented in a standard analog CMOS process. The floating gate MOSFETs are used not just in digital memories but also in capacitive based circuits, in adaptive circuit elements and in analog memory elements as well [27,28,29]. The floating gate devices occupy a small layout area, have a high reliability for data computation and have low power dissipation of the logic functions [30,31].

2.2 Basic Structure and Operation

The basic structure of the multiple-input floating gate MOSFET [32,33] is shown in the Fig. 2.1. It consists of n-channel MOS transistor having a gate electrode, which is electrically floating. The floating gate in the MOSFET extends over the channel and the field oxide. Array of control gates, which are inputs to the transistor, are formed over the floating gate using the second polysilicon layer. Fig. 2.2 shows the capacitive coupling between the multiple input gates and the floating gate and the channel. In Fig. 2.2, C_1, C_2, C_3,…,C_n are the coupling capacitors between the floating gate and the input corresponding to terminal voltages V_1, V_2, V_3,…,V_n, respectively. C_0 is the capacitance between floating gate and substrate.

V$_1$ V$_2$ V$_3$ V$_n$

Input Gates

Thin Oxide

Floating Gate

Gate Oxide

n$^+$ n$^+$

p-Si
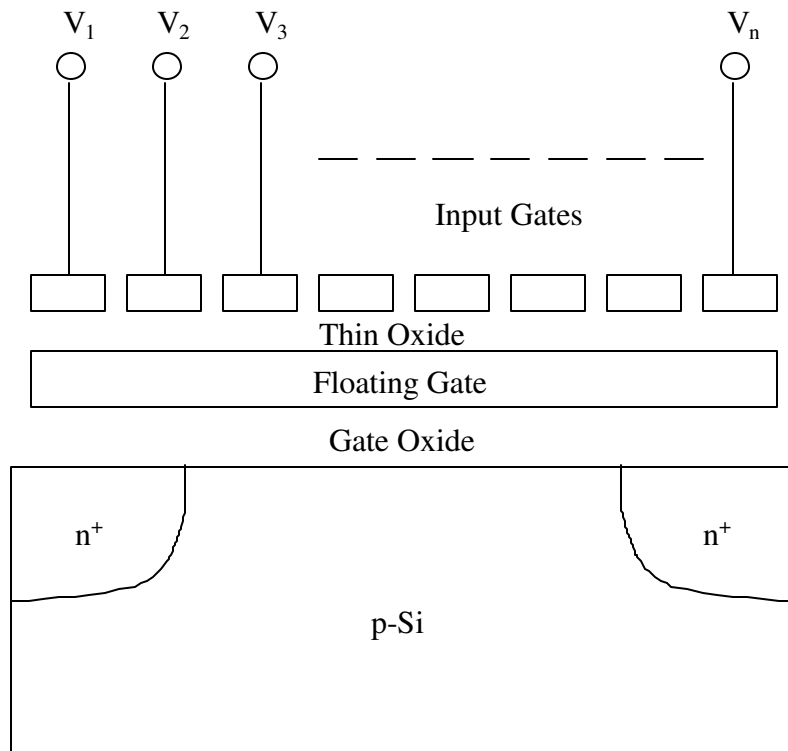
Fig. 2.1: Basic structure of a multiple-input floating gate MOSFET.
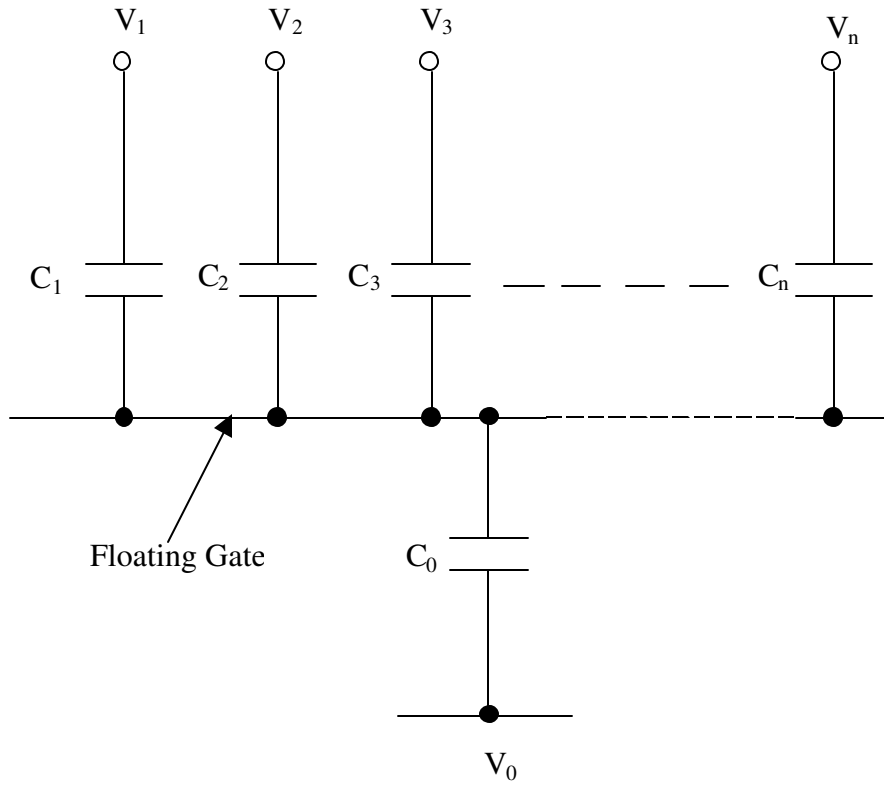
Fig. 2.2: Relationship among terminal voltages and coupling capacitances of a multiple-input floating gate MOSFET.

Q_1, Q_2, Q_3,...Q_n are the charges stored in corresponding capacitors C_1, C_2, C_3,...,C_n, respectively. At any given time 't', the net charge on the floating gate $Q_F(t)$ is given by [33],

$$Q_F(t) = Q_0 + \sum_{i=1}^{n}(-Q_i(t)) = \sum_{i=0}^{n}C_i(\Phi_F(t) - V_i(t)) \qquad (2.1)$$

or $\qquad Q_F(t) = \Phi_F(t)\sum_{i=0}^{n}C_i - \sum_{i=0}^{n}C_iV_i(t) \qquad (2.2)$

where n is the number of inputs, Q_0 is the initial charge present on the floating gate, $Q_i(t)$ is the charge present in the capacitor C_i at time 't' and $\Phi_F(t)$ is the potential at the input of the floating gate. The law of conservation of charge states that the net charge of an isolated system remains constant. Set $V_0 = 0$ V and assuming that area of capacitance is constant with time, applying conservation of charge at floating gate, equation (2.2) can be expressed as follows,

$$\Phi_F(0)\sum_{i=0}^{n}C_i - \sum_{i=1}^{n}C_iV_i(0) = \Phi_F(t)\sum_{i=0}^{n}C_i - \sum_{i=1}^{n}C_iV_i(t) \qquad (2.3)$$

or $\qquad \Phi_F(t)\sum_{i=0}^{n}C_i - \Phi_F(0)\sum_{i=0}^{n}C_i = \sum_{i=1}^{n}C_iV_i(t) - \sum_{i=1}^{n}C_iV_i(0) \qquad (2.4)$

or $\qquad \Phi_F(t) = \Phi_F(0) + \dfrac{\sum_{i=1}^{n}C_iV_i(t) - \sum_{i=1}^{n}C_iV_i(0)}{\sum_{i=0}^{n}C_i}. \qquad (2.5)$

Assuming zero initial charge on the floating gate, at equilibrium equation (2.5) reduces to

$$\Phi_F(t) = \dfrac{\sum_{i=1}^{n}C_iV_i(t)}{\sum_{i=0}^{n}C_i}. \qquad (2.6)$$

The nMOS transistor is switched ON or OFF depending on whether $\Phi_F(t)$ is greater than or less than threshold voltage of the transistor. The symbol of nMOS and pMOS floating gate transistors are shown in Figs. 2.3 and 2.4, respectively. The voltage on the floating gate of the transistor is given by the equation (2.6). If V_s is the voltage on the source of pMOS transistor then, the transistor is ON if

$$(\Phi_F - V_s) < V_{thp}$$

and the transistor is OFF if

$$(\Phi_F - V_s) > V_{thp}$$

where V_{thp} is threshold voltage of pMOSFET.

If V_s is the voltage on the source of nMOS transistor then, the transistor is ON if

$$(\Phi_F - V_s) > V_{thn}$$

and the transistor is OFF if

$$(\Phi_F - V_s) < V_{thn}$$

where V_{thn} is threshold voltage of nMOSFET.

2.3   I–V Characteristics of MIFG Transistors

The circuits used for obtaining the I–V characteristics of floating gate MOS transistors are shown in Fig. 2.5 and Fig. 2.6, respectively. The circuits shown in Figs. 2.5 and 2.6 have capacitors of 500 fF at the gate of the transistor. The capacitor value 500 fF is the unit capacitance used in circuits here to plot the characteristics of the floating gate transistors. While performing a DC analysis, SPICE open circuits the capacitor, resulting in no input applied to the gate of the transistor for a given value of V_{gs}. Hence, instead of performing DC analysis; transient   analysis   is   performed   to   obtain   the   characteristics.

Drain (V_d)

Floating
gate

V_n

Substrate

V_3

V_2

V_1

Source (V_s)
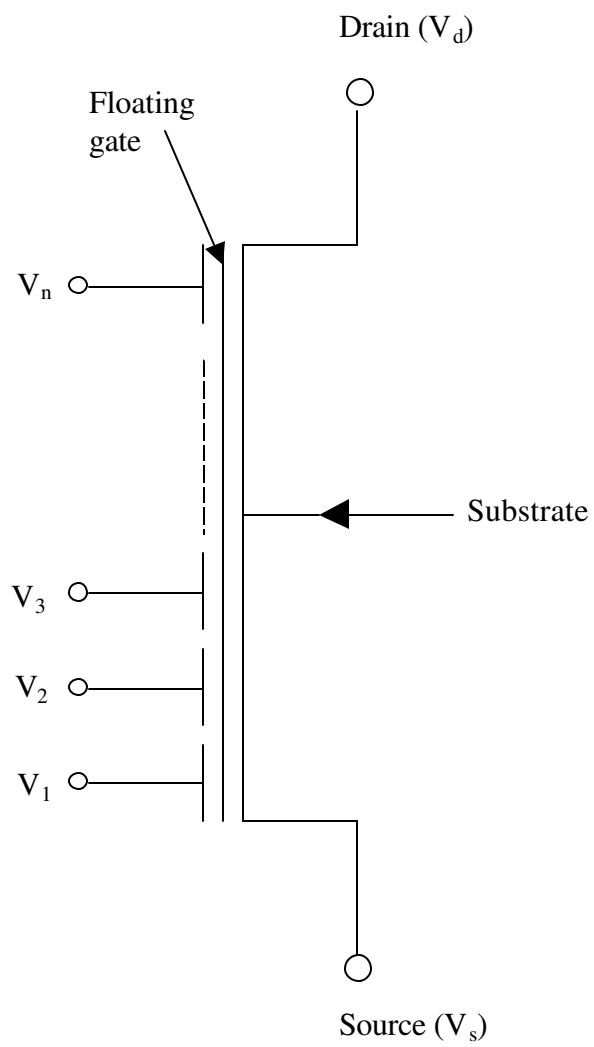
Fig. 2.3: Symbol representing a multiple-input floating gate nMOS device.

Source (V_s)

Floating
gate

V_n ○

Substrate

V_3 ○

V_2 ○

V_1 ○

Drain (V_d)
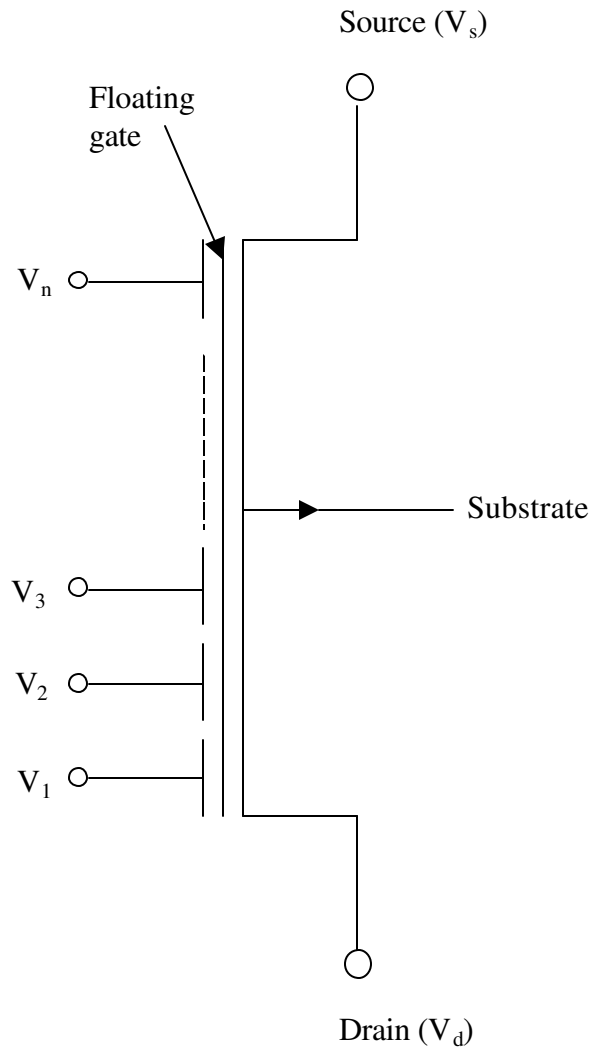
Fig. 2.4: Symbol representing a multiple-input floating gate pMOS device.
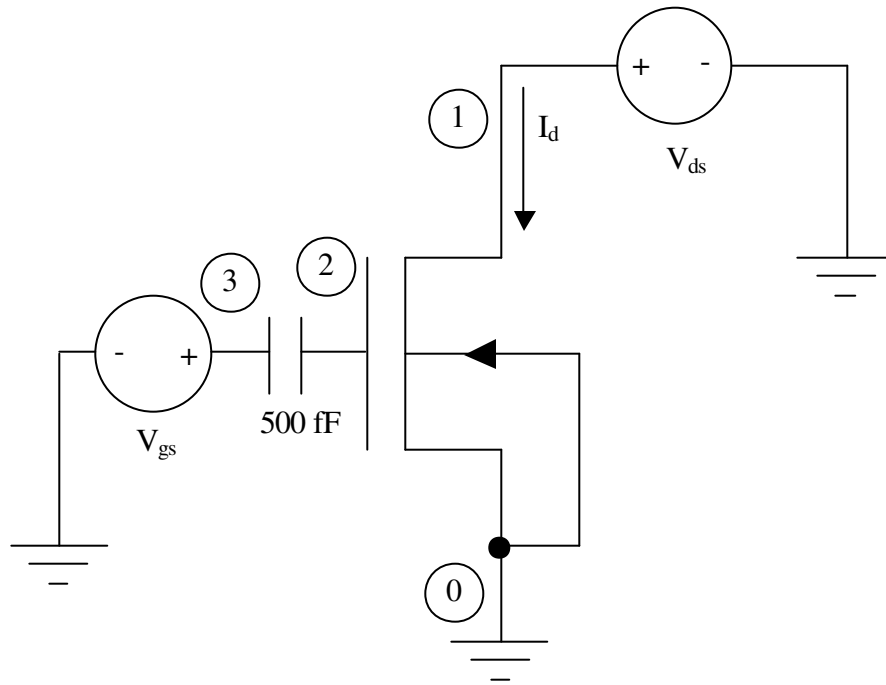
Fig. 2.5: Circuit diagram to obtain I-V characteristics of a floating gate nMOS transistor.
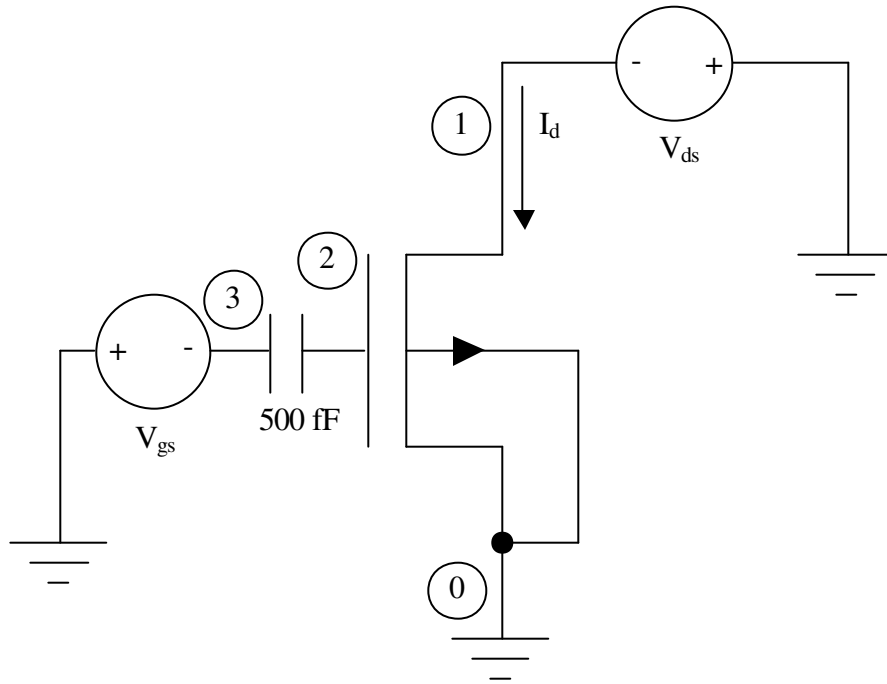
Fig. 2.6: Circuit diagram to obtain I-V characteristics of a floating gate pMOS transistor.

Following changes are made in the circuit. The DC voltage source V_{ds} applied at the drain of the transistor is changed to a ramp voltage source (0 - 3 V) that would give same result as when DC analysis is performed and the circuit is simulated for various values of V_{gs}. The plots obtained for various values of V_{gs} are appended to obtain the I–V characteristics.

The I–V characteristics of n-channel and p-channel multi-input floating gate MOSFETs are plotted in Figs. 2.7 and 2.8, respectively. The current I_d is plotted as function of V_{ds} (from 0 V to 3 V) for different values of gate voltage, V_{gs}. Figures 2.9 and 2.10 show transfer curves I_d as function of V_{gs} from 0 V to 3 V for different values of drain voltage V_{ds} in steps of 1 V. The input circuit files used to obtain the characteristics are included in Appendix A. BSIM3 MOS transistor model parameters used are shown in Appendix B.

2.4   MIFG CMOS Inverter

The multiple-input floating gate MOS inverter is shown in Fig. 2.11, where V_1, V_2, V_3,…,V_n are input voltages and C_1, C_2, C_3,…,C_n are corresponding capacitors. Equation (2.6) is used in finding the voltage on the floating gate of the inverter. A weighted sum of all inputs is performed at the gate and is converted into a multiple-valued voltage V_M at the floating gate. Switching of the floating gate CMOS inverter depends on whether V_M obtained from the weighted sum is greater than or less than the threshold voltage or switching voltage (Φ_t) of the CMOS inverter [34,35]. The switching voltage Φ_t is defined as the average of Φ_{g0}, the input voltage to obtain perfect logic 1 (3 V) at the output and Φ_{s1}, the input voltage to obtain perfect logic 0 (0 V) at the output.
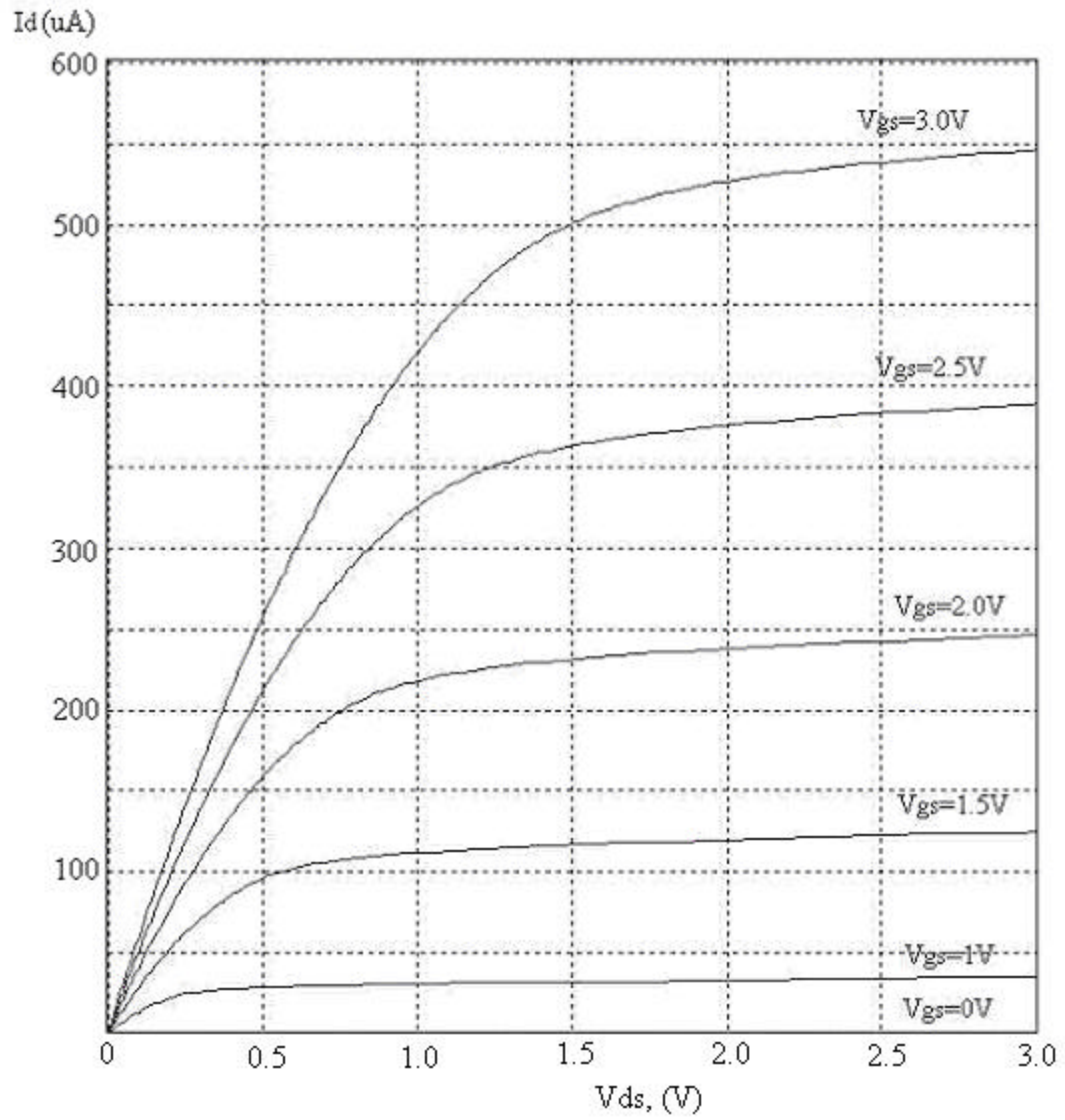
Fig. 2.7: I-V characteristics of a floating gate nMOS transistor (W/L= 4µm/1.6 µm).
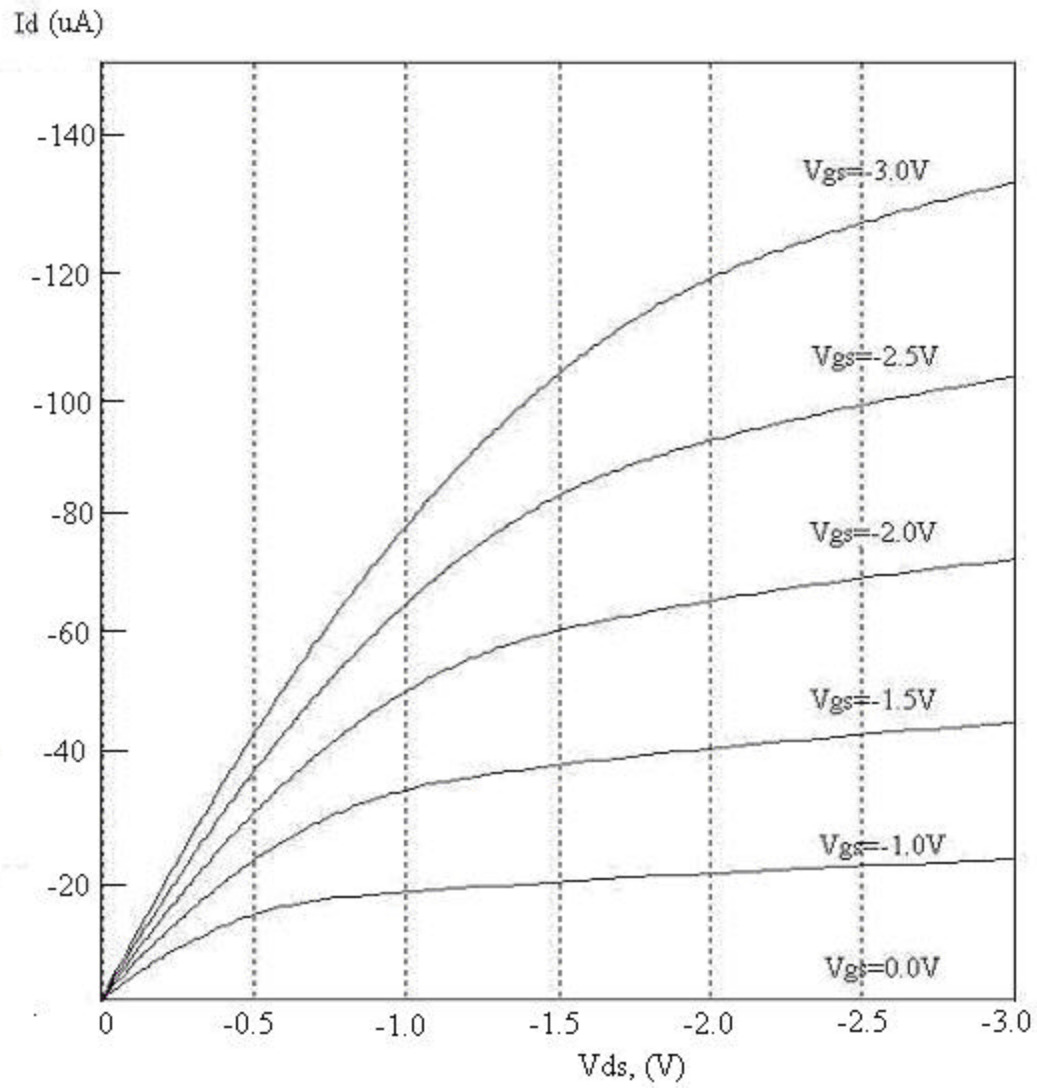
Fig. 2.8: I-V characteristics of a floating gate pMOS transistor (W/L= 4μm/1.6 μm).
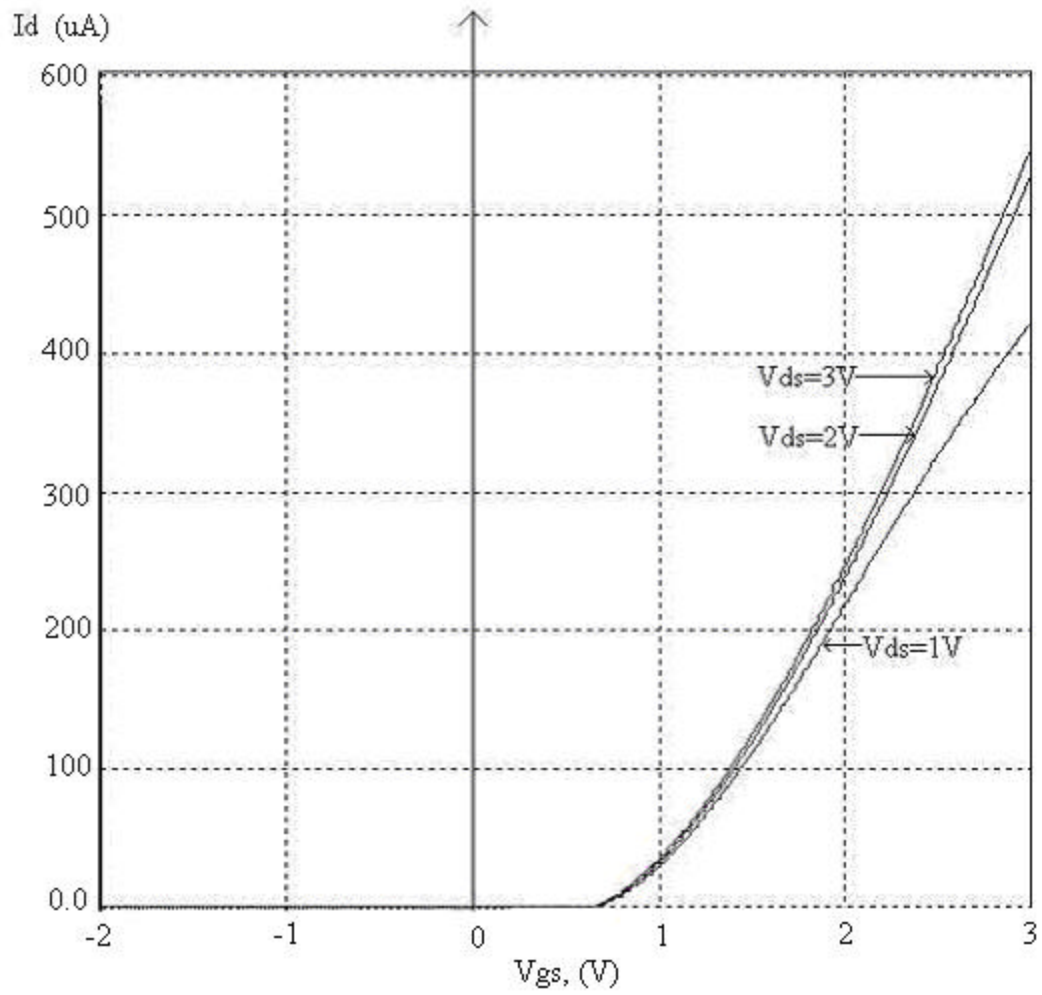
Fig. 2.9: Transfer curves for floating gate nMOS transistor (I_d vs V_{gs}) as a function of $V_{ds.}$
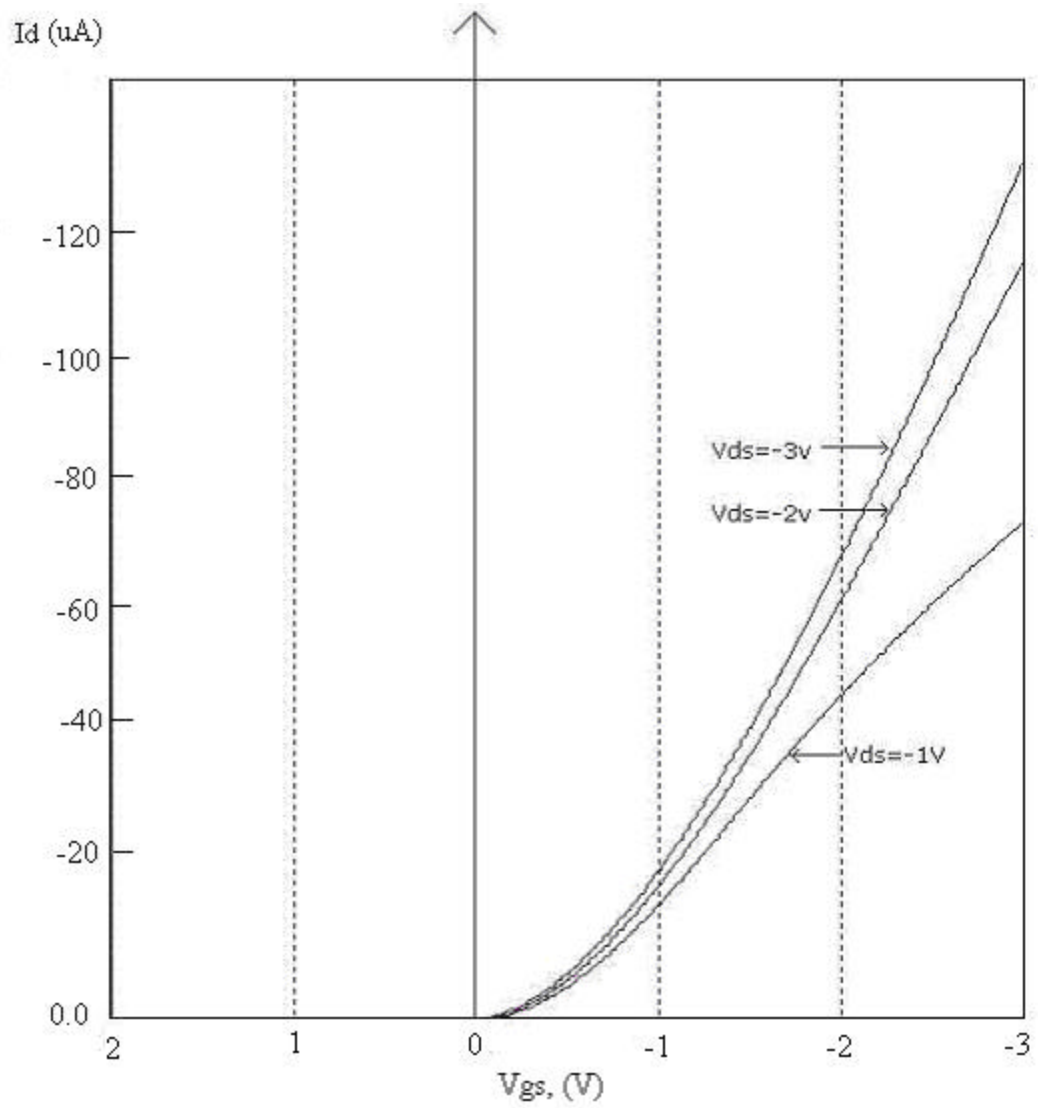
Fig. 2.10: Transfer curves for a floating gate pMOS transistor (I_d vs V_{gs}) as a function of $V_{ds.}$
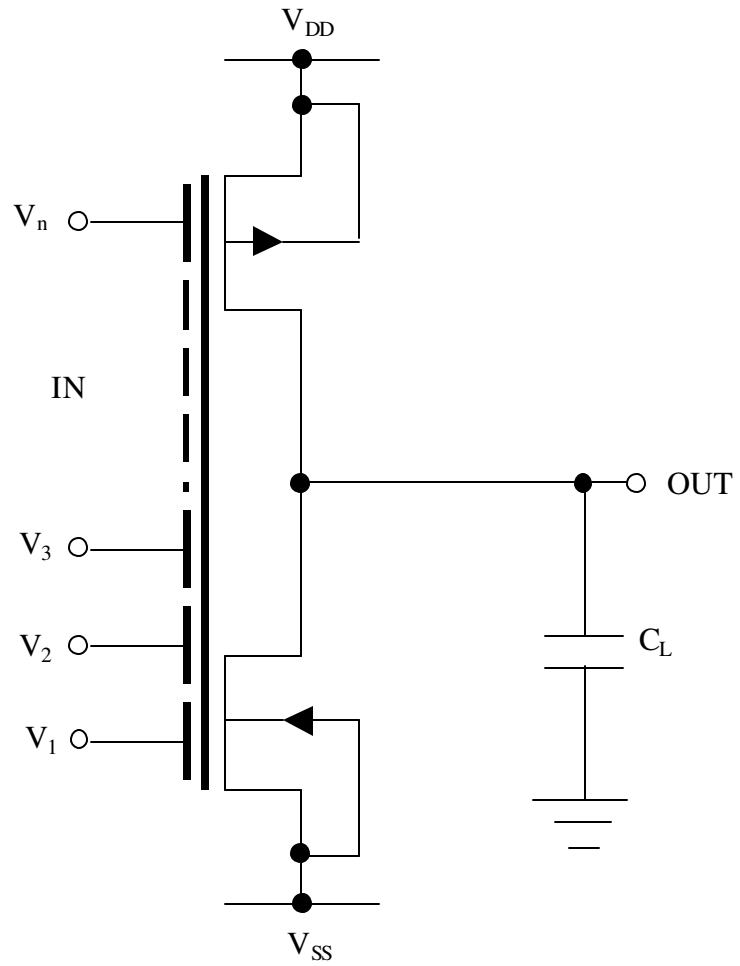
Fig. 2.11: CMOS inverter using MIFG MOSFETs.

$$\Phi_t = \frac{\left(\Phi_{g0} + \Phi_{s1}\right)}{2}. \tag{2.7}$$

Hence, the output (V_{out}) of floating gate CMOS inverter is given by,

V_{out} = HIGH (3 V)   if $\Phi_F < \Phi_t$

       = LOW (0 V)   if $\Phi_F > \Phi_t$ (2.8)

Φ_{g0} and Φ_{sl} are obtained from voltage transfer characteristic of a CMOS inverter. The latter is shown in Fig. 2.12 for W/L=8.0 µm/1.6 µm. The values of Φ_{g0} and Φ_{s1} are also shown in the Fig 2.12. Φ_{g0} and Φ_{sl} are the input voltages at which the output V_{out} is V_{DD}-0.1V and 0.1 V, respectively.

The capacitor network formed for the n-input floating gate inverter is shown in Fig. 2.13. The gate oxide capacitance of pMOS transistor C_{oxp} is between the floating gate and N-well, which is connected to V_{DD} and C_{oxn} is between the floating gate and substrate, which is connected to V_{SS}. The capacitance C_p is the parasitic capacitance formed between polysilicon floating gate, which is on field oxide and substrate, which is connected to V_{SS}. From Fig 2.13, the voltage on the floating gate is given by,

$$\Phi_F = \frac{V_1 \times C_1 + V_2 \times C_2 + V_3 \times C_3 + ... + V_n \times C_n + V_{DD} \times C_{oxp} + V_{SS} \times (C_p + C_{oxn})}{C_1 + C_2 + C_3 + ... + C_n + C_{oxn} + C_{oxp} + C_p}.$$

Set V_{SS} = 0 V, voltage on floating gate is given by,

$$\Phi_F = \frac{V_1 \times C_1 + V_2 \times C_2 + V_3 \times C_3 + ... + V_n \times C_n + V_{DD} \times C_{oxp}}{C_1 + C_2 + C_3 + ... + C_n + C_{oxn} + C_{oxp} + C_p}. \tag{2.9}$$

In order to facilitate a logic design procedure employing floating gate transistors, a graphical technique called floating gate potential diagram (FPD) has been developed [36,37]. In FPD, Φ_F is plotted as a function of multi-input voltage,
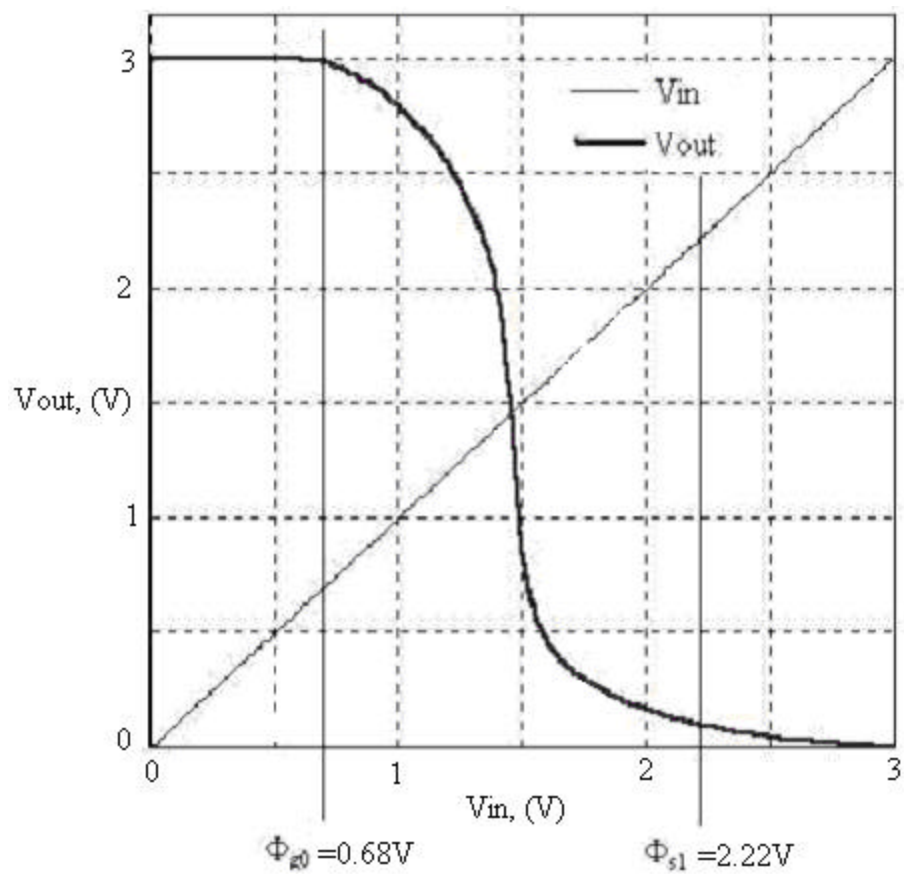
Fig. 2.12: Voltage transfer characteristics of a CMOS inverter with W/L = 8μm/1.6 μm (Note: Φ_{g0} = 0.68 V and Φ_{s1} = 2.22 V).
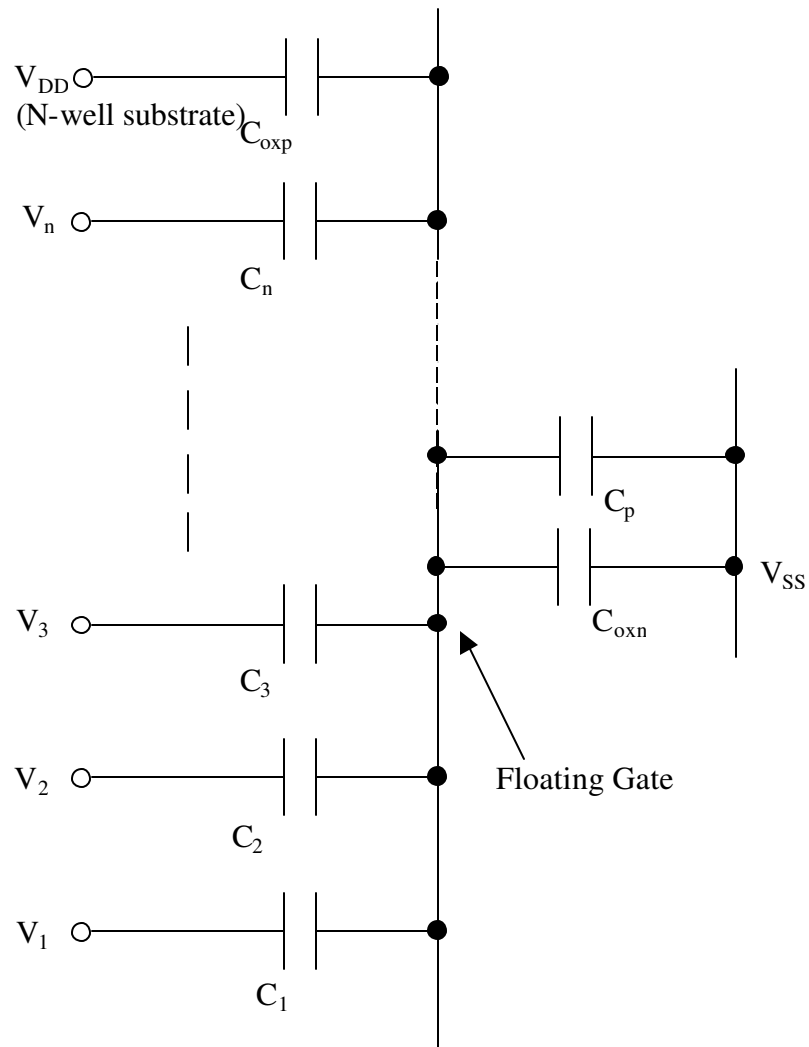
Fig. 2.13: Capacitive network formed for a multiple input floating gate CMOS inverter.

V_p. In reference [33], the switching threshold of MIFG inverter is set to $\gamma V_{DD}/2$, which they considered it to be a standard value, where γ is defined as floating gate gain and given by,

$$\gamma = \frac{\sum\limits_{i=1}^{n} C_i}{\sum\limits_{i=0}^{n} C_i} \tag{2.10}$$

where n is the number of inputs to the floating gate CMOS inverter and C_0 is the capacitance from floating gate to substrate and is sum of C_{oxn}, C_{oxp} and C_p. The switching voltage of a floating gate inverter is independent of the value of capacitors at the input. Hence, dependence of switching voltage of the inverter on γ as explained in [33] is not appropriate. Instead the appropriate value of inversion threshold of floating gate inverter is Φ_t calculated from equation (2.7).

Following example would explain the above discussion. Consider two MIFG inverters with W/L = 8.0 μm/1.6 μm for pMOS and nMOS transistors with a supply voltage of 3 V. The first MIFG inverter has one input capacitor of 100fF and second MIFG inverter has four input capacitors of 100 fF each. Calculating the value of γ using equation (2.10), we get $\gamma = 0.77$ and $\gamma V_{DD}/2 = 1.15$ V for first MIFG CMOS inverter and $\gamma = 0.93$ and $\gamma V_{DD}/2 = 1.39$ V for the second MIFG CMOS inverter. The value of C_0 is approximated to be 30 fF for this case. That is for this inverter, the switching threshold voltage varies when $\gamma V_{DD}/2$ is considered the switching voltage. But the voltage transfer characteristics for the MIFG inverters do not change with the values of input capacitors as shown in Fig. 2.12. Hence Φ_t is considered more appropriate value for the switching threshold voltage.

2.5   Variable Threshold Voltage

In general, logic circuits need different switching voltage values for Φ_t for better performance. This is obtained by varying the W/L ratio of either the nMOS or the pMOS transistor [38]. The voltage transfer characteristics of MIFG CMOS inverter with varying W_p/W_n ratios and a constant L are shown in Fig. 2.14. When the switching point needs to be shifted by more than 0.6 V, circuits can be designed easily as shown in Fig. 2.15. Input to capacitor C_1 is logic HIGH (3 V) and input to capacitor C_3 is logic LOW (0 V). The values of capacitors C_1 or C_3 are calculated depending on the shift required for the switching point. Either the capacitor C_1 or C_3 is designed as per the requirement. The voltage transfer characteristics for the circuit shown in Fig. 2.15 are plotted in Fig. 2.16 with various values of C_1 and C_3. The voltage transfer characteristics of MIFG CMOS inverter can be obtained using SPICE by performing DC analysis. As explained in section 2.3, DC analysis would open circuit all capacitors and short-circuit all inductors. Such a situation is overcome by performing transient analysis instead, by using ramp input voltage source (0 V to 3 V) instead of a DC voltage source at the input of the MIFG inverter.

2.6   Implementation of MIFG CMOS Transistor

The multiple input floating gate transistors could be implemented in standard analog CMOS process [39,40]. The following section presents the implementation of capacitors for the floating gate MOSFETs. A top view of parallel plate capacitor is shown in Fig. 2.17. The value of capacitance excluding parasitic capacitances is given by,
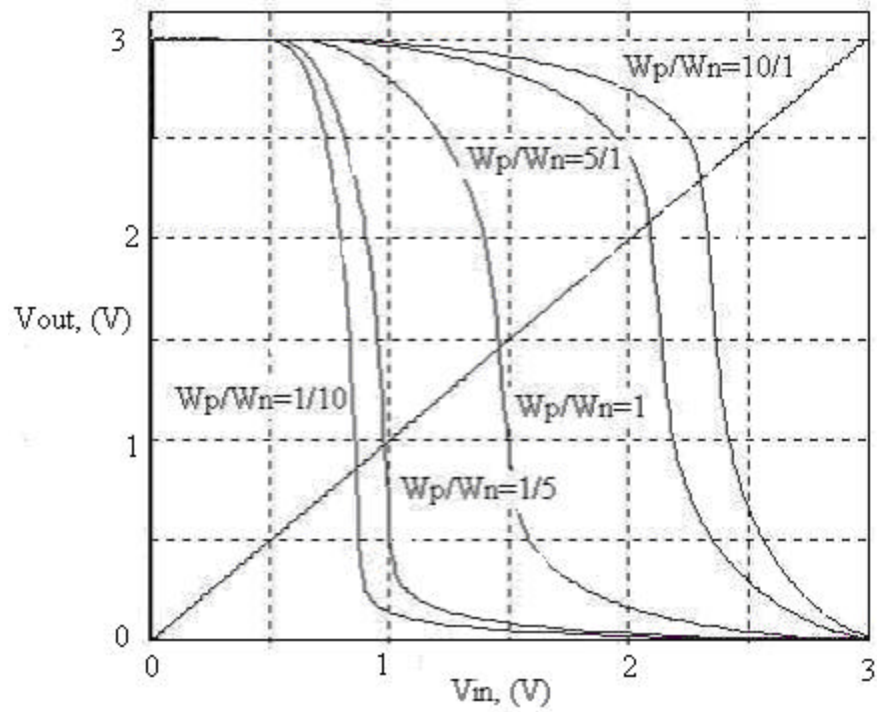
Fig. 2.14: Voltage transfer characteristics for various W_p/W_n ratios of CMOS inverter. (Note: Channel length $L_p = L_n = 1.6$ µm).
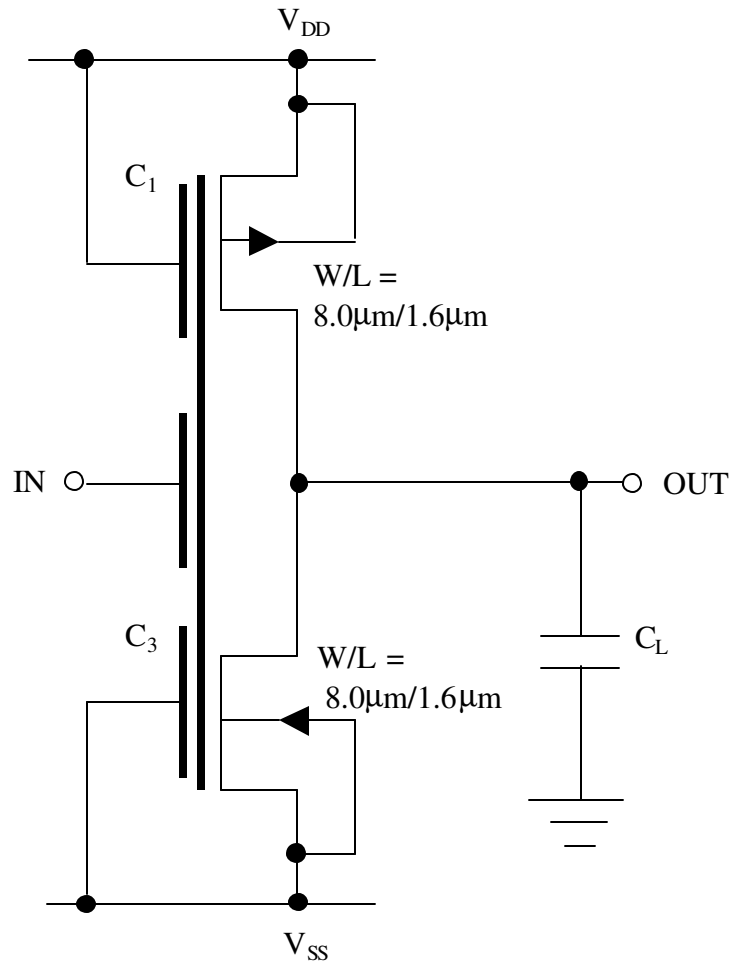
Fig. 2.15: Circuit diagram for variable threshold voltage using floating gate devices.
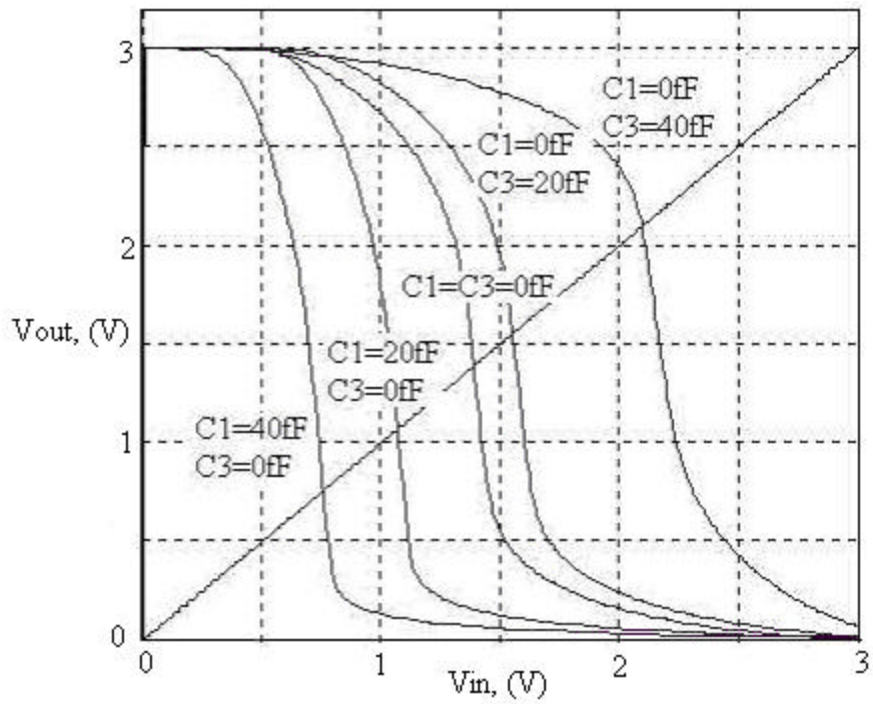
Fig. 2.16: Voltage transfer characteristics of Fig. 2.15 for various capacitor values.
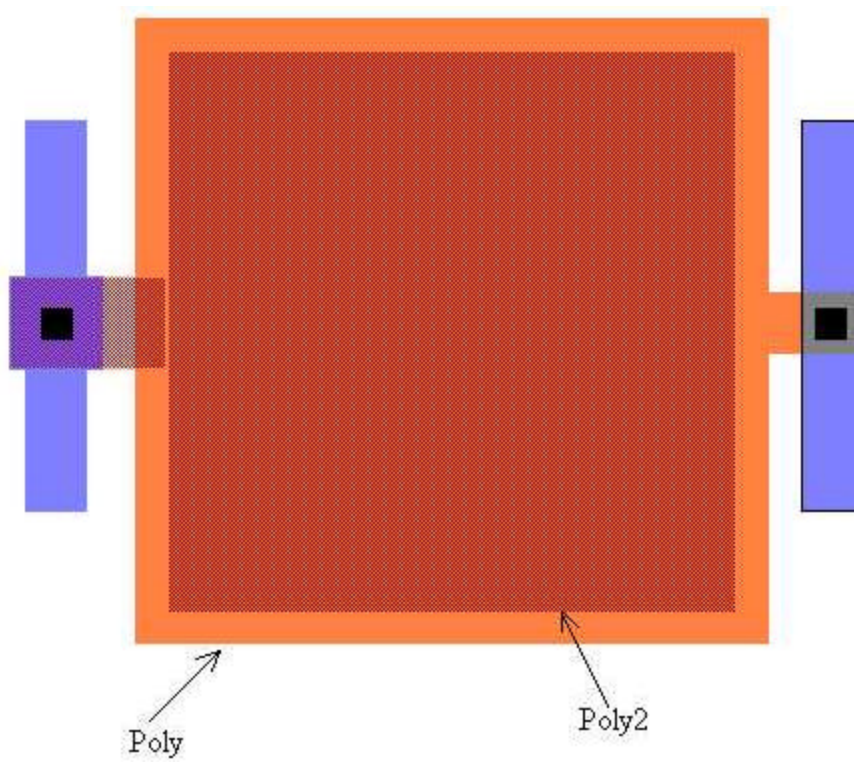
Fig. 2.17: Layout for a parallel plate capacitor. (C=500 fF).

Note: Area of top plate (Poly2) $29 \times 29 \ \mu m^2$ and bottom plate (Poly) $32.2 \times 32.2 \ \mu m^2$ and oxide thickness between two plates = 575 Å.

$$C = AC'$$
(2.10)

where A is the total area of top plate and C' is capacitance per unit area. The insulator between the parallel plates of the capacitor in standard CMOS process is usually thicker than transistor gate oxide. For a typical $1.5\ \mu m$ technology CMOS process, the gate oxide thickness is $300\ \text{Å}$ and the oxide thickness between parallel poly S_i plates it is $575\ \text{Å}$. To obtain a capacitor of 500 fF, the area of top plate $29 \times 29\ \mu m^2$ and that of bottom plate of $32.2 \times 32.2\ \mu m^2$ is used.

There are several ways in which capacitors can be implemented [41]. A popular one uses double-polysilicon technology in which two poly levels are available. The top plate and the bottom plate of the capacitor are made of polysilicon. In a single polysilicon technology, the top plate of the capacitor is made of metal. A high quality thin oxide is formed as insulator before the top plate is formed.

Two parasitic capacitances are associated with the main capacitor as shown in Fig. 2.18. The main one C_{p1} is between the bottom plate and the substrate. It contributes most to the parasitic capacitance. The capacitance due to wiring of the bottom plate augments this capacitance. The metal wiring used to contact the top plate results in second small parasitic capacitance C_{p2}. Another parasitic shown in Fig. 2.18 by a broken line is resistance R_p of the polysilicon plate. This parasitic is ignored except at high frequencies. The capacitor of Fig. 2.17 is susceptible to interference. Any noise signal on substrate can be coupled to the capacitor through the parasitic capacitances. Also, any voltage variation on the bottom plate of the capacitor can be coupled to the substrate and through that to other components on
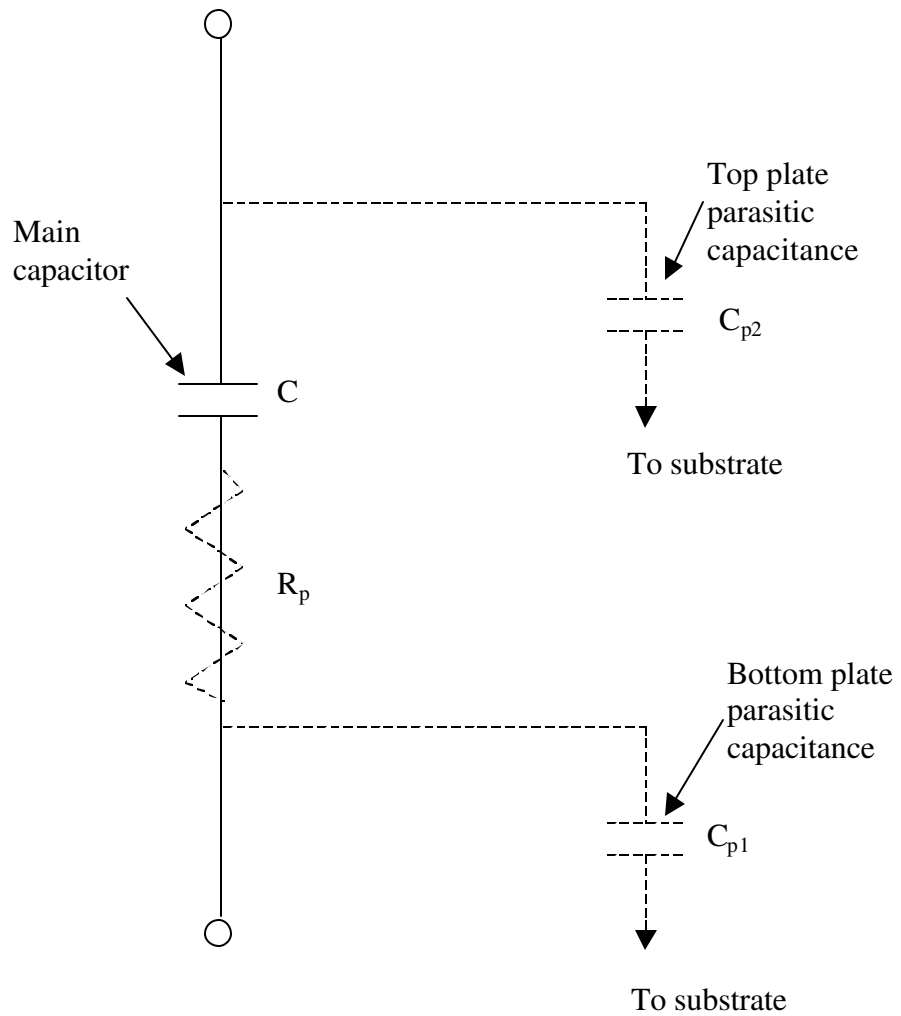
Fig. 2.18: An integrated capacitor with its associated parasitics.

the chip. Hence if the capacitor is too large, then it should be shielded from the substrate by an n‑well under it, which is connected to a DC potential (V_{DD}).

2.7   Unit Capacitance

Due to shortcomings in fabrication process, the edges of capacitor plates are shorter than intended. To maintain constant capacitor ratio, unit size capacitors are used as explained in reference [41]. An important step in designing floating gate circuits is setting the value of unit capacitance. As stated earlier, the shorter edges and variation in thickness of oxide between the plates would change the value of the capacitance. The MOSIS provides the area capacitance C′ values between the poly and poly2 layer, which varies from 580 aF/μm^2 to 620 aF/μm^2 for different runs. An average value of 596 aF/μm^2, which was observed in most of the runs, is used in the present work. Table 2.1 shows required area for different values of unit capacitance. The table provides minimum and maximum capacitance values obtained for variation in area capacitance C′. The table also includes the value of the capacitance with edges shorted by 0.5 μm and 1.0 μm on each side. The percentage change from the desired capacitance to worst‑case variation in the capacitance is calculated.

For 10 fF $\%change = \dfrac{9.536 - 2.32}{9.536} \times 100 = 76\%$

For 20 fF $\%change = \dfrac{21.456 - 9.28}{21.456} \times 100 = 57\%$

For 100 fF $\%change = \dfrac{100.724 - 70.18}{100.724} \times 100 = 30\%$

For 500 fF $\%change = \dfrac{501.236 - 364.5}{501.236} \times 100 = 27\%$

Table 2.1: Variation in unit capacitance with respect to area and area capacitance

Unit Capacitance	Area Required	C' 580 aF/μm^2	C' 596 aF/μm^2	C' 620 aF/μm^2
10 fF	4 μ $\times$ 4 μ	9.280 fF	9.536 fF	9.920 fF
	3 μ $\times$ 3 μ	5.220 fF	5.364 fF	5.580 fF
	2 μ $\times$ 2 μ	2.320 fF	2.384 fF	2.480 fF
20 fF	6 μ $\times$ 6 μ	20.880 fF	21.456 fF	22.320 fF
	5 μ $\times$ 5 μ	14.5 fF	14.9 fF	15.5 fF
	4 μ $\times$ 4 μ	9.28 fF	9.536 fF	9.920 fF
100 fF	13 μ $\times$ 13 μ	98.020 fF	100.724 fF	104.780 fF
	12 μ $\times$ 12 μ	83.520 fF	85.824 fF	89.280 fF
	11 μ $\times$ 11 μ	70.180 fF	72.116 fF	75.020 fF
500 fF	29 μ $\times$ 29 μ	487.78 fF	501.236 fF	521.420 fF
	28 μ $\times$ 28 μ	454.72 fF	467.264 fF	486.080 fF
	27 μ $\times$ 27 μ	364.5 fF	434.484 fF	451.980 fF
1000 fF	41 μ $\times$ 41 μ	974.980 fF	1001.876 fF	1042.22 fF
	40 μ $\times$ 40 μ	928.00 fF	953.6 fF	992.00 fF
	39 μ $\times$ 39 μ	882.18 fF	906.516 fF	943.00 fF

For 1000 fF $\quad\%change = \dfrac{1001.876 - 882.18}{1001.876} \times 100 = 12\%$

Since designing floating circuits is based on capacitor ratios, variation in capacitor values does not affect the functionality of the circuit, so long as the unit capacitance is large compared to the gate oxide capacitance. Hence unit capacitance of 500 fF is used in the present work. The circuits should be re-simulated with worst-case value of unit capacitance to ensure that variation in the value wouldn't affect the functionality of the circuit. The parasitic capacitance C_{p1} associated with unit capacitor of 500 fF, explained in previous section is found to be 40 fF. If 'C' is the unit capacitance and input capacitors are multiples of 'C' then the value of C_p used in the equation (2.9) is given by,

$$C_p = k \times C_{p1} \tag{2.11}$$

where k is given by

$$k = \dfrac{C_1 + C_2 + C_3 + ... + C_n}{C}. \tag{2.12}$$

2.8   Design Issues

Floating gate CMOS inverter, on the other hand has degraded output for a particular set of inputs, when the calculated sum of input voltages on the floating gates lies between Φ_{g0} and Φ_{s1}. Hence the need for generation of output signal using a CMOS inverter at the end of the circuit. Consider an MIFG inverter with W/L = 8.0 μm/1.6 μm with supply voltage of 3 V and three input capacitors of 500 fF each. When inputs to the three capacitors are logic LOW (0 V) and logic HIGH (3 V), the voltage on floating gate using equation (2.9) is 0 V and 2.75 V, respectively for value of C_0 approximated at 30 fF. A full output swing of 3 V and 0 V is expected at

the output. When one of the three inputs is logic HIGH or two of the three inputs are logic HIGH then the voltage on floating gate given by equation (2.9) is 0.94 V and 1.85 V, respectively. In these cases, a full swing of the output is not expected. Hence the output needs to be buffered to generate full logic voltage swing.

Initial charge present on the floating gate due to reasons like fabrication may shift the threshold condition and would result in logical error of the circuit. The initial charge on the floating gate is to be erased by UV radiation or by using additional devices for resetting the charge. An nMOS transistor is connected between the floating gate and ground, to eliminate the charge present on the floating gate in reset phase. Kotani *et.al.* [42] proposed a new technique to balance the charge on the floating gate by connecting the floating gate to the inverter output.

Simulation of floating gate devices with standard CMOS models provided by the manufacturer requires, new simulation techniques. The major problem of simulating floating-gate devices is the inability of the simulator to converge floating nodes. To avoid the problem of floating nodes at the gate of a transistor, different approaches have been reported in reference [43-46]. These techniques include use of additional networks like resistors and voltage controlled voltage sources (VCVS) for establishing initial floating-gate voltage value. These simulation techniques are explained in Appendix C.

Chapter 3

Conversion from Ternary Logic to Binary Logic

3.1 Overview

The balanced ternary logic is expressed as (-1,0,1). In a standard 3 V CMOS process, the logic -1, 0, 1 is defined as -3 V, 0 V, 3 V, respectively. The benefits of using ternary logic system are explained in Chapter 1. In spite of these benefits ternary logic system has not gained importance in the area of integrated circuit design. This is due to lack of efficient interfacing circuits with binary logic. Hence an attempt to design an interface circuit from ternary logic to binary logic has been made. The circuits are designed using multiple-input floating gate MOS transistors. The basic structure and operation of floating gate MOSFETs is explained in Chapter 2. Table 3.1 provides ternary logic with corresponding binary bits. The corresponding decimal number is also included in the table. The representation of ternary and binary bits for corresponding decimal number is explained using an example.

Consider a decimal number "-2", for which the corresponding binary bits are $(1010)_2$. The left most bit is the sign bit, which is "1" represents the number is negative and next three bits "010" represents "2". For decimal number "-2", the corresponding ternary bits are $(-1,1)_3$. The conversion from ternary logic to decimal number is given by,

$$(-1 \times 3^1) + (1 \times 3^0) = (-3) + (1) = -2.$$

The remaining ternary and binary bit representing corresponding decimal number is obtained.

Table 3.1: Decimal number, ternary and binary bits

Decimal	Ternary	Binary
-4	$(-1-1)_3$	$(1100)_2$
-3	$(-10)_3$	$(1011)_2$
-2	$(-11)_3$	$(1010)_2$
-1	$(0-1)_3$	$(1001)_2$
0	$(00)_3$	$(0000)_2$
+1	$(01)_3$	$(0001)_2$
+2	$(1-1)_3$	$(0010)_2$
+3	$(10)_3$	$(0011)_2$
+4	$(11)_3$	$(0100)_2$

Note: Ternary bits representation is $(MSB, LSB)_3$
Binary bits representation is $(Sign\ bit, MSB, SSB, LSB)_2$

The chapter explains design for the conversion circuits from ternary logic to binary logic. The circuit block has two ternary logic inputs, a MSB and a LSB and four binary logic outputs, a sign bit (SB), a most significant bit (MSB), a second significant bit (SSB) and a least significant bit (LSB). The design of SB, MSB, SSB and LSB are explained in separate sections. The design of pre-input gate inverter stages needed to control the main inverter stage is explained in respective subsections.

3.2   Circuit Design for Sign Bit

The procedure for designing circuits using floating gate devices is mentioned in Chapter 2. The circuits are designed for 1.5 µm CMOS VLSI technology. The switching threshold voltage Φ_t is found first from the voltage transfer characteristics of the inverter. The standard CMOS inverter with W/L ratio = 8.0 µm/1.6 µm for MOSFETs is shown in Fig. 3.1. The voltage transfer characteristics of the inverter obtained by performing DC analysis is shown in Fig. 3.2. The values of Φ_{g0} and Φ_{s1} are obtained from the voltage transfer characteristic of the inverter. Φ_{g0} and Φ_{s1} are the input voltages for which the output is V_{DD}-0.1 V and 0.1 V, respectively. The values of Φ_{g0} and Φ_{s1} are found to be 0.68 V and 2.22 V. The values of Φ_{g0} and Φ_{s1} are marked on the voltage transfer characteristics. The switching threshold voltage of the inverter is found using the equation (2.7),

$$\Phi_t = \frac{0.68 + 2.22}{2} = 1.45V. \tag{3.1}$$

The floating gate potential diagrams (FPD) are drawn as next step in designing the circuits. From Table 3.1 the sign bit is logic HIGH (3 V) for inputs
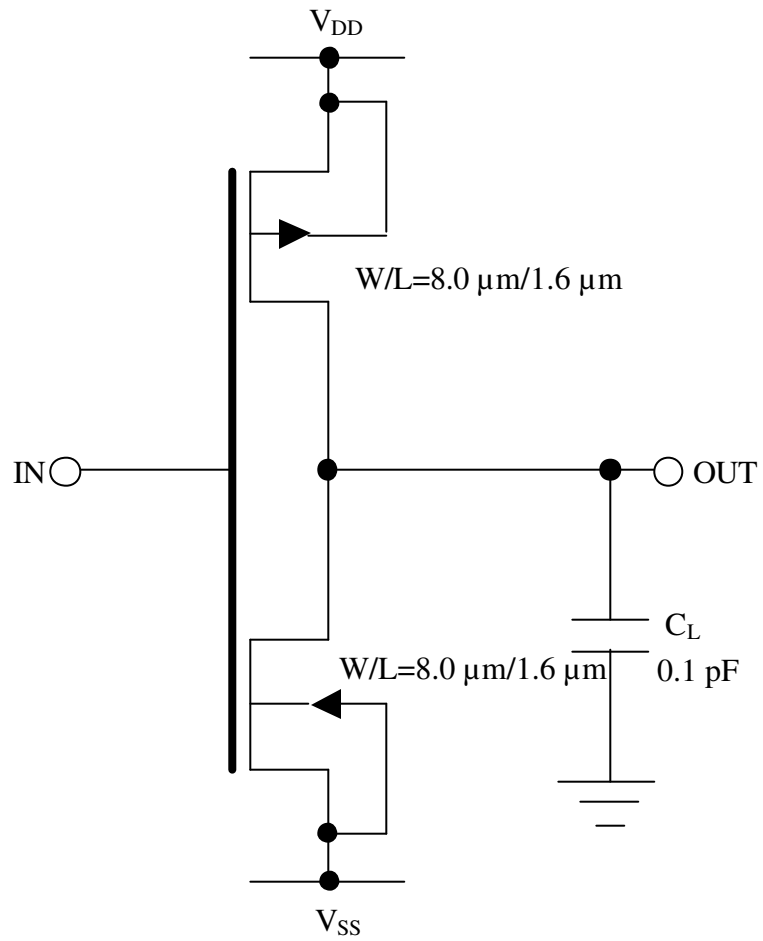
Fig. 3.1: Standard CMOS inverter with W/L ratio = 8.0 μm/1.6 μm.
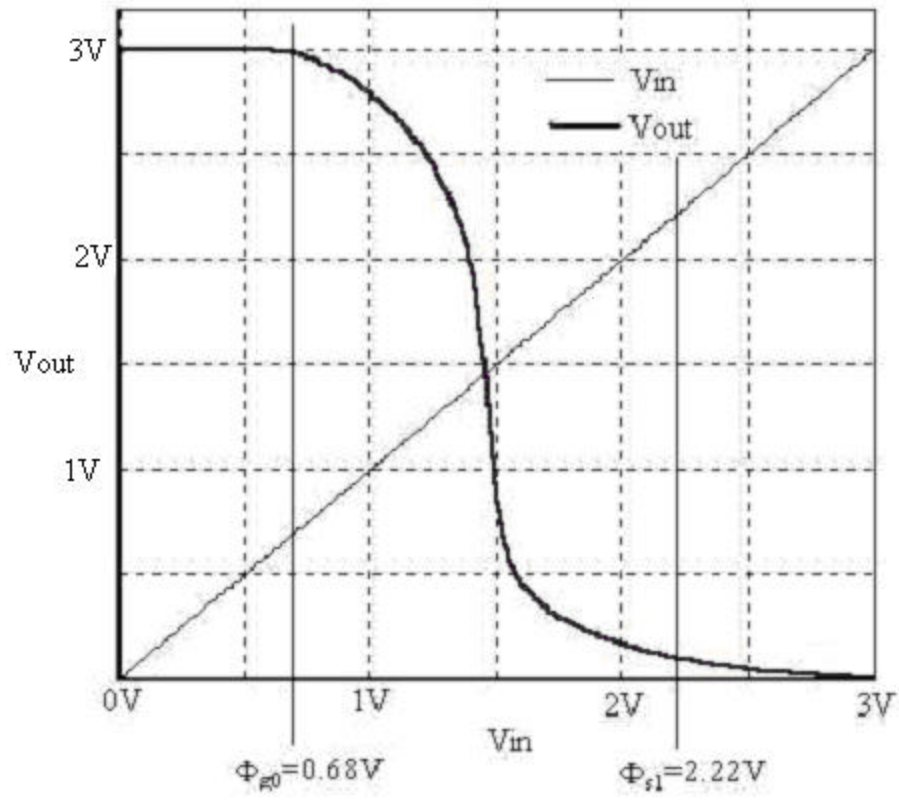
Fig. 3.2: Voltage transfer characteristics of a CMOS inverter. (W/L= 8.0μm/1.6 μm).

$(-1,-1)_3$ to $(0,1)_3$ and logic LOW (0 V) for inputs $(0,0)_3$ to $(1,1)_3$. Hence the voltage on floating gate Φ_F of inverter should be below switching voltage Φ_t for inputs $(-1,-1)_3$ to $(0,-1)_3$ and above the switching voltage for inputs $(0,0)_3$ to $(1,1)_3$. The FPD for the sign bit is shown in Fig. 3.3. The switching threshold line is marked in the figure.

The circuit is realized with two input capacitors C_1 and C_2 controlled by the two ternary inputs V_A and V_B. The sizes of the capacitors are set to 3:1 according to the weights of MSB and LSB in ternary bits. Using equations (2.7-2.9) for inputs $(-1,-1)_3$ to $(0,-1)_3$,

$$\frac{V_A \times C_1 + V_B \times C_2 + V_{DD} \times C_{oxp}}{C_1 + C_2 + C_{oxn} + C_{oxp} + C_p} < \Phi_t \tag{3.2}$$

and for inputs $(0,0)_3$ to $(1,1)_3$,

$$\frac{V_A \times C_1 + V_B \times C_2 + V_{DD} \times C_{oxp}}{C_1 + C_2 + C_{oxn} + C_{oxp} + C_p} > \Phi_t \tag{3.3}$$

where C_{oxn} and C_{oxp} are the gate oxide capacitance (C_{ox}) of nMOS and pMOS transistor, respectively, of the inverter and C_p is the parasitic capacitance due to capacitors C_1 and C_2. The gate oxide capacitance C_{ox} is given by,

$$C_{ox} = \frac{\epsilon_0 \epsilon_{SiO_2}}{t_{ox}} \times (WL) \tag{3.4}$$

where W and L are width and length of the transistors, ϵ_0 (8.854×10^{-8} F/cm) is the permittivity of free space, ϵ_{SiO2} (3.9) is the permittivity of silicon dioxide and t_{ox} is the thickness of gate oxide. The thickness of gate oxide is obtained from model parameters given by MOSIS and is 300 Å. For W/L = 8.0 µm/1.6 µm, using equation (3.4) C_{ox} is given by,
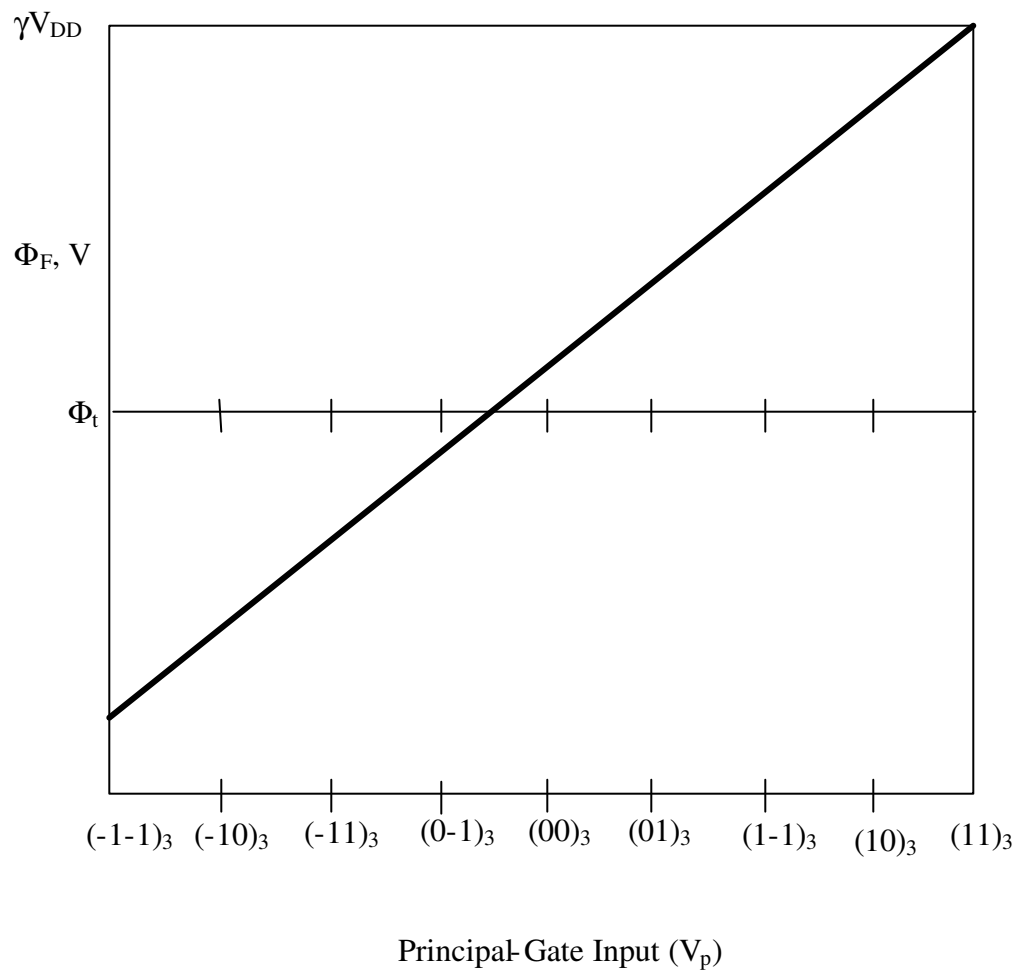
Fig. 3.3: Floating gate potential diagram for the sign bit.
(Note: Figure is not drawn to scale).

$$C_{ox} = \frac{8.0\,\mu m \times 1.6\,\mu m \times 3.9 \times 8.854 F\,/\,cm}{300 \times 10^{-8}\,cm} \approx 15\,fF. \tag{3.5}$$

A unit capacitance "C" of 500 fF is considered, taking layout constraints into consideration. The capacitors C_1 and C_2 are set to 1500 fF and 500 fF, respectively, in the ratio of 3:1. For input $(0,0)_3$, the inequality (3.3) will not hold good. It is observed that the numerator on LHS is negligible when compared to RHS of the inequality. Hence a third capacitor C_3 is introduced which is connected to supply voltage. The size of capacitor C_3 is designed such that the voltage on floating gate is greater than switching threshold voltage of the inverter for inputs $(0,0)_3$. The inequality (3.3) is rewritten as,

$$\frac{V_A \times C_1 + V_B \times C_2 + 3V \times C_3 + 3V \times C_{oxp}}{C_1 + C_2 + C_3 + C_{oxn} + C_{oxp} + C_p} > \Phi_t. \tag{3.6}$$

The value of C_p is calculated using equation (2.11),

$$C_p = k \times C_{p1}$$

where C_{p1} is parasitic capacitance generated due to unit capacitance "C" (500 fF). C_{p1} is found to be 40 fF from layout extraction and k is given by,

$$k = \frac{C_1 + C_2 + C_3}{C}. \tag{3.7}$$

Substituting C_1 equal to 3C and C_2 as C in equation (3.7),

$$k = \frac{3C + C + C_3}{C} = 4 + \frac{C_3}{C}.$$

Substituting the value of k, C_p is calculated as,

$$C_p = (4 + \frac{C_3}{500\,fF}) \times 40\,fF = 160\,fF + C_3 \times 40\,/\,500. \tag{3.8}$$

Substituting values for input $(0,0)_3$, C_{oxn}, C_{oxp}, C_p in inequality (3.6),

$$\frac{0V \times (1500\,fF) + 0V \times (500\,fF) + 3V \times C_3 + 3V \times (15\,fF)}{1500\,fF + 500\,fF + C_3 + 15\,fF + 15\,fF + \underbrace{(160\,fF + C_3 \times 40/500)}_{C_P}} > \Phi_t\,(1.45V). \quad (3.9)$$

The smallest value of C_3 that satisfies the inequality (3.9) is found to be 3000 fF, which is a multiple of 500 fF (unit capacitance). Substituting the value of C_3 in equation (3.8) value of C_p is found to be 400 fF.

To verify the design, the capacitor values are substituted for input $(0,-1)_3$,

$$\frac{0V \times (1500\,fF) + (-3V) \times (500\,fF) + 3V \times 3000\,fF + 3V(15\,fF)}{1500\,fF + 500\,fF + 3000\,fF + 15\,fF + 15\,fF + (160\,fF + 240\,fF)} < \Phi_t\,(1.45V). \quad (3.10)$$

The voltage on floating gate Φ_F for ternary inputs is calculated and tabulated in Table 3.2. The voltage on floating gate Φ_F from table is found to be less than switching threshold voltage for inputs $(-1,-1)_3$ to $(0,-1)_3$ and greater than switching threshold voltage for inputs $(0,0)_3$ to $(1,1)_3$. The FPD for the SB to scale is shown in Fig. 3.4. The circuit diagram for sign bit is shown in Fig. 3.5.

3.3 Circuit Design for MSB

The most significant bit is found to be logic HIGH (3V) for inputs $(-1,-1)_3$ and $(1,1)_3$ and logic LOW (0 V) for rest of inputs from Table 3.1. The FPD for the MSB is shown in Fig. 3.6. The potential on floating gate is below switching threshold voltage Φ_t for inputs $(-1,-1)_3$, $(1,1)_3$ and above switching threshold voltage for inputs $(-1,0)_3$ to $(1,0)_3$. Voltage on floating gate falls below switching threshold voltage once, hence one pre-input gate inverter stage is required to control voltage on floating gate. Figure 3.7 shows circuit level implementation for MSB. In Fig. 3.7, the main inverter stage (#3) has three input capacitors C_6, C_7 and C_8. The capacitors C_6 and C_7 are controlled by ternary inputs V_A and V_B, respectively and capacitor C_8

Table 3.2: Voltage on the floating gate Φ_F for the sign bit for corresponding ternary inputs (Φ_t for the MIFG inverter is 1.45 V)

Ternary Inputs	Voltage on Floating Gate Φ_F	
$(-1-1)_3$	0.316	$\Phi_F < \Phi_t$
$(-10)_3$	0.623	$\Phi_F < \Phi_t$
$(-11)_3$	0.929	$\Phi_F < \Phi_t$
$(0-1)_3$	1.236	$\Phi_F < \Phi_t$
$(00)_3$	1.543	$\Phi_F > \Phi_t$
$(01)_3$	1.849	$\Phi_F > \Phi_t$
$(1-1)_3$	2.156	$\Phi_F > \Phi_t$
$(10)_3$	2.463	$\Phi_F > \Phi_t$
$(11)_3$	2.769	$\Phi_F > \Phi_t$

Fig. 3.4: Floating gate potential diagram for the sign bit.
(Note: Figure is drawn to scale).

V_DD

C_3
3000 fF

W/L=8.0 μm/1.6 μm

#1

C_1
1500 fF

V_A ○ ────────── ●────────● ○ Sign Bit

C_2
500 fF

V_B ○

W/L=8.0 μm/1.6 μm   C_L   0.1 pF

V_SS
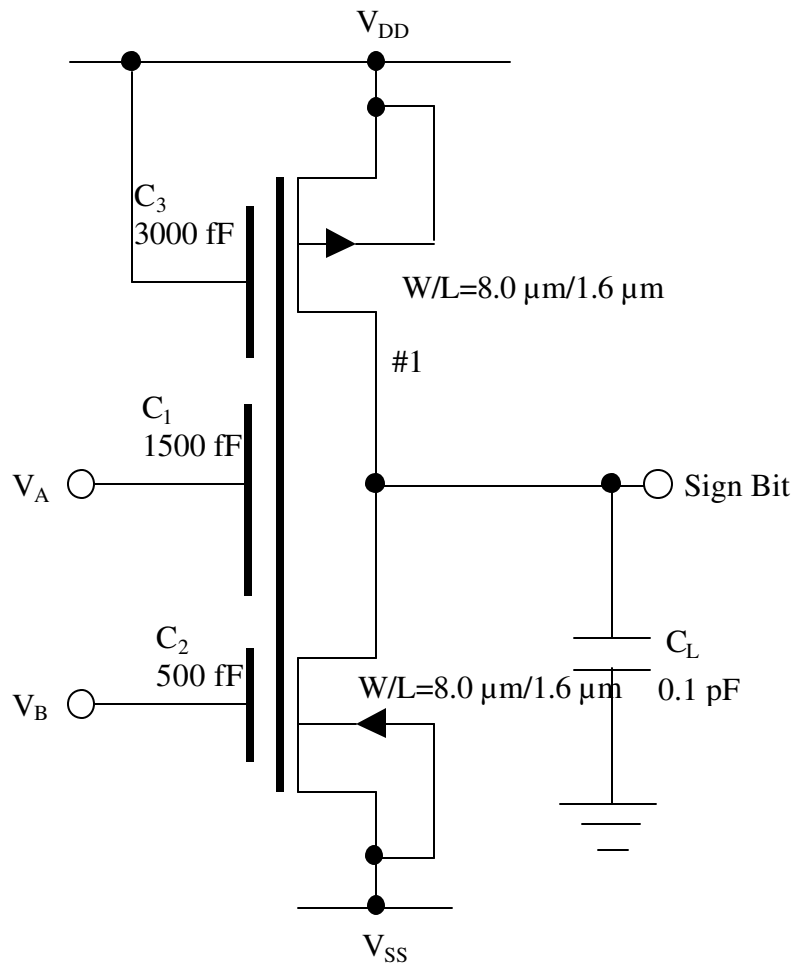
Fig. 3.5: Circuit diagram for implementation of ternary to binary logic (Sign Bit) using floating gate MOSFETs.

Fig. 3.6: Floating gate potential diagram for the most significant bit
(Note: Figure not drawn to scale).

Fig. 3.7: Circuit diagram for implementation of ternary logic to binary logic (MSB bit) using floating gate MOSFETs.

is controlled by the output V_2 of pre-input gate inverter stage (#2). Using equations (2.7-2.9), the inequalities for the MSB can be written as follows. For input $(-1,-1)_3$,

$$\frac{(-3V) \times C_6 + (-3V) \times C_7 + V_2 \times C_8 + 3V \times C_{oxp}}{C_6 + C_7 + C_8 + C_{oxn} + C_{oxp} + C_p} < \Phi_t(1.45V) \qquad (3.11)$$

and for $(1,1)_3$,

$$\frac{(3V) \times C_6 + (3V) \times C_7 + V_2 \times C_8 + 3V \times C_{oxp}}{C_6 + C_7 + C_8 + C_{oxn} + C_{oxp} + C_p} < \Phi_t(1.45V) . \qquad (3.12)$$

The inequality (3.10) can be satisfied only if V_2 is LOW (0 V) for input $(1,1)_3$. Hence the output of pre-input inverter stage (#2) is LOW (0 V) for input $(1,1)_3$ and HIGH (3 V) for rest of the inputs. For inputs $(-1,0)_3$ to $(1,0)_3$, voltage on floating gate should be greater than switching threshold voltage. Considering the extreme input $(-1,0)_3$, the inequality is given by,

$$\frac{(-3V) \times C_6 + (0V) \times C_7 + (3V) \times C_8 + (3V) \times C_{oxp}}{C_6 + C_7 + C_8 + C_{oxn} + C_{oxp} + C_p} > \Phi_t(1.45V) . \qquad (3.13)$$

The sizes of capacitors C_6 and C_7 is set to 3:1 in the ratio of MSB and LSB as in ternary bits. The minimum size of the capacitance of C_6 and C_7 is 1500 fF and 500fF, respectively.

The value of C_p is obtained from equation (2.11), where C_{p1} = 40 fF and k is given by,

$$k = \frac{C_6 + C_7 + C_8}{C} . \qquad (3.14)$$

Substituting C_6 equal to 3C, C_7 equal to C in equation (3.14),

$$k = \frac{3C + C + C_8}{C} = 4 + \frac{C_8}{C} .$$

Substituting the value of k, C_p is calculated as,

$$C_p = (4 + \frac{C_8}{500\,fF}) \times 40\,fF = 160\,fF + C_8 \times 40/500.$$

Substituting the values for input $(-1,0)_3$, C_{oxn}, C_{oxp}, C_p in inequality (3.13),

$$\frac{(-3V) \times (1500\,fF) + (0V) \times (500\,fF) + 3V \times C_8 + 3V \times (15\,fF)}{1500\,fF + 500\,fF + C_8 + 15\,fF + 15\,fF + \underbrace{(160\,fF + C_8 \times 40/500)}_{C_P}} > \Phi_t.(1.45V) \quad (3.15)$$

The minimum value of capacitor C_8 that satisfies inequality (3.15) is 5000 fF, which is a multiple of unit capacitance. High value of capacitance C_8 resulted in high propagation delay, hence the capacitor ratio of C_6 and C_7 is reconsidered. The sizes of capacitors are set in the ratio of 1:1 and a minimum value of 500 fF is considered.

The value of C_p is obtained from equation (2.11), where $C_{p1} = 40$ fF and k is given by,

$$k = \frac{C_6 + C_7 + C_8}{C}. \qquad (3.16)$$

Substituting C_6 equal to C and C_7 equal to C in equation (3.16),

$$k = \frac{C + C + C_8}{C} = 2 + \frac{C_8}{C}.$$

Substituting the value of k, C_p is calculated as,

$$C_p = (2 + \frac{C_8}{500\,fF}) \times 40\,fF = 80\,fF + C_8 \times 40/500.$$

The inequality (3.13) is rewritten,

$$\frac{(-3V) \times 500\,fF + (0V) \times 500\,fF + (3V) \times C_8 + (3V) \times 15\,fF}{500\,fF + 500\,fF + C_8 + 15\,fF + 15\,fF + (80\,fF + C_8 \times 40/500)} > \Phi_t(1.45V). \quad (3.17)$$

The minimum value of capacitor C_8 that satisfies the inequality (3.17) is 2500 fF. Substituting the value of C_8, the value of C_p is found to be 280 fF.

The voltage on floating gate Φ_F of the main inverter stage (#3) of MSB, for ternary inputs is calculated and tabulated in Table 3.3. The voltage on floating gate Φ_F is less than switching threshold voltage for inputs $(-1,-1)_3$ and $(1,1)_3$ and greater than switching threshold voltage for inputs $(-1,0)_3$ to $(1,0)_3$ satisfying the conditions. The FPD for the MSB to scale is shown in Fig. 3.8. The FPD shown in Fig. 3.8 is different when compared to Fig. 3.6, as the capacitor ratio of C_6 to C_7 is set to 1:1, instead of 3:1.

3.3.1 Circuit Design for #2 Stage

The output of stage #2 is LOW (0 V) for input $(1,1)_3$ and HIGH(3V) for test of the inputs. The circuit can be realized with two input capacitors C_4 and C_5. For input $(1,1)_3$, the inequality is written using equations (2.7-2.9),

$$\frac{(3V) \times C_4 + (3V) \times C_5 + (3V) \times C_{oxp}}{C_4 + C_5 + C_{oxn} + C_{oxp} + C_p} > \Phi_t(1.45V). \tag{3.18}$$

The capacitors C_4 and C_5 are equal and minimum size unit capacitors (500 fF) satisfy the inequality (3.18). The voltage on the floating gate Φ_F is calculated and tabulated in Table 3.4. The output of stage (#2) is buffered which controls the capacitor C8 of the main inverter stage. The transistor widths used in buffer are $W_p/W_n = 16\ \mu m/16\ \mu m$ and $W_p/W_n = 40\ \mu m/40\ \mu m$. The circuit diagram for most significant bit is shown in Fig. 3.7. The non-inverting buffer at the output of #2 stage is not shown in the figure.

Table 3.3: Voltage on floating gate Φ_F of MSB for corresponding ternary inputs (Φ_t for MIFG inverter is 1.45 V)

Ternary Inputs	Output of #2 V_2	Voltage on Floating Gate Φ_F	
$(-1-1)_3$	HIGH (3 V)	1.192	$\Phi_F < \Phi_t$
$(-10)_3$	HIGH (3 V)	1.586	$\Phi_F > \Phi_t$
$(-11)_3$	HIGH (3 V)	1.980	$\Phi_F > \Phi_t$
$(0-1)_3$	HIGH (3 V)	2.374	$\Phi_F > \Phi_t$
$(00)_3$	HIGH (3 V)	1.980	$\Phi_F > \Phi_t$
$(01)_3$	HIGH (3 V)	2.374	$\Phi_F > \Phi_t$
$(1-1)_3$	HIGH (3 V)	1.980	$\Phi_F > \Phi_t$
$(10)_3$	HIGH (3 V)	2.374	$\Phi_F > \Phi_t$
$(11)_3$	LOW (0 V)	0.799	$\Phi_F < \Phi_t$

Note: Output of #2 stage V_2 controls the capacitor C_8 of the main inverter stage.
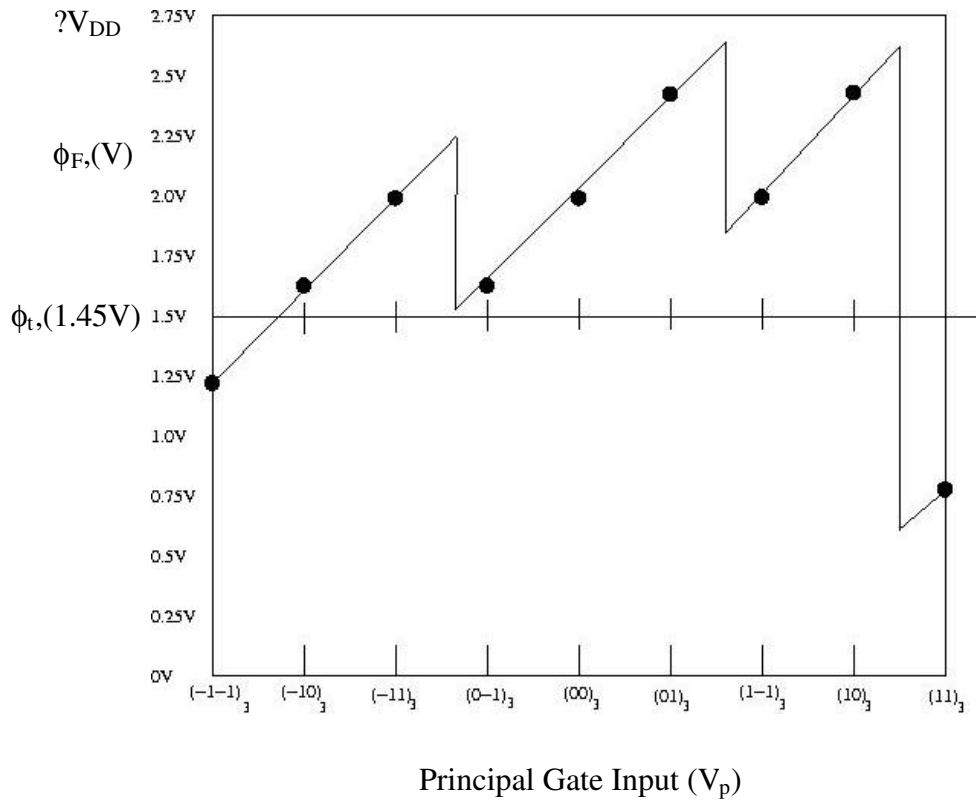
Fig. 3.8: Floating gate potential diagram for the most significant bit.
(Note: Figure drawn to scale).

Table 3.4: Voltage on floating gate Φ_F of V_2 for corresponding ternary inputs (Φ_t for MIFG inverter is 1.45 V)

Ternary Inputs	Voltage on Floating Gate Φ_F	
$(-1-1)_3$	-2.662	$\Phi_F < \Phi_t$
$(-10)_3$	-1.310	$\Phi_F < \Phi_t$
$(-11)_3$	0.004	$\Phi_F < \Phi_t$
$(0-1)_3$	-1.310	$\Phi_F < \Phi_t$
$(00)_3$	0.004	$\Phi_F < \Phi_t$
$(01)_3$	0.490	$\Phi_F < \Phi_t$
$(1-1)_3$	0.004	$\Phi_F < \Phi_t$
$(10)_3$	0.490	$\Phi_F < \Phi_t$
$(11)_3$	2.743	$\Phi_F > \Phi_t$

3.4   Circuit Design for SSB

From Table 3.1, the output of second significant bit (SSB) is logic LOW (0 V) for inputs $(-1,-1)_3$, $(1,1)_3$ and from inputs $(0,-1)_3$ to $(0,1)_3$ and is logic HIGH (3 V) for rest of the inputs. The FPD for the SSB is shown in Fig. 3.9, the voltage on floating gate is below switching threshold voltage for inputs $(-1,-1)_3$, $(1,1)_3$ and from inputs $(0,-1)_3$ to $(0,1)_3$. That is voltage on floating gate falls below switching threshold voltage twice and hence two pre-input gate inverter stages (#4, #5) are required to control the main inverter stage as shown in Fig. 3.10. The main inverter stage (#6) has four input capacitors C_{12}, C_{13}, C_{14} and C_{15}. The capacitors C_{12} and C_{13} are controlled by two ternary inputs V_A and V_B, respectively. The capacitors C_{14} and C_{15} are controlled by output of pre-input inverter stages V_4 (#4) and V_5 (#5), respectively. The output of the pre-input inverter stage V_4 (#4) goes LOW (0 V) from inputs $(0,-1)_3$ to $(1,1)_3$ and output of the pre-input gate inverter stage V_5 (#5) goes LOW (0V) for input $(1,1)_3$.

Designing the main inverter stage (#6), for input $(-1,-1)_3$, the inequality is given by,

$$\frac{(-3V) \times C_{12} + (-3V) \times C_{13} + 3V \times C_{14} + 3V \times C_{15} + 3V \times C_{oxp}}{C_{12} + C_{13} + C_{14} + C_{15} + C_{oxn} + C_{oxp} + C_p} < \Phi_t (1.45V). \qquad (3.19)$$

For inputs $(-1,0)_3$ and $(-1,1)_3$, the inequality is

$$\frac{V_A \times C_{12} + V_B \times C_{13} + 3V \times C_{14} + 3V \times C_{15} + 3V \times C_{oxp}}{C_{12} + C_{13} + C_{14} + C_{15} + C_{oxn} + C_{oxp} + C_p} > \Phi_t (1.45V). \qquad (3.20)$$

The output of pre-input inverter stage (#4) goes LOW (0 V) for inputs $(0,-1)_3$ to $(1,1)_3$, hence for inputs $(0,-1)_3$ to $(0,1)_3$ the inequality is,

$$\frac{V_A \times C_{12} + V_B \times C_{13} + 0V \times C_{14} + 3V \times C_{15} + 3V \times C_{oxp}}{C_{12} + C_{13} + C_{14} + C_{15} + C_{oxn} + C_{oxp} + C_p} < \Phi_t (1.45V). \qquad (3.21)$$
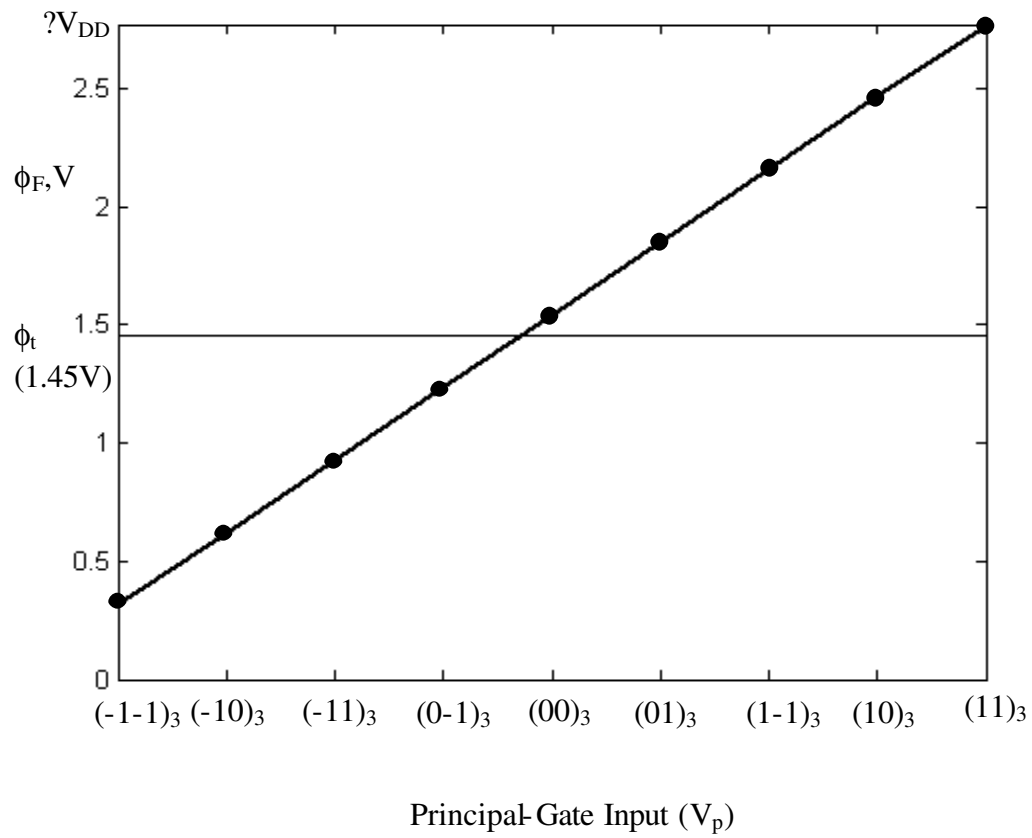
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Fig. 3.9: Floating gate potential diagram for the second significant bit.
(Note: Figure not drawn to scale).
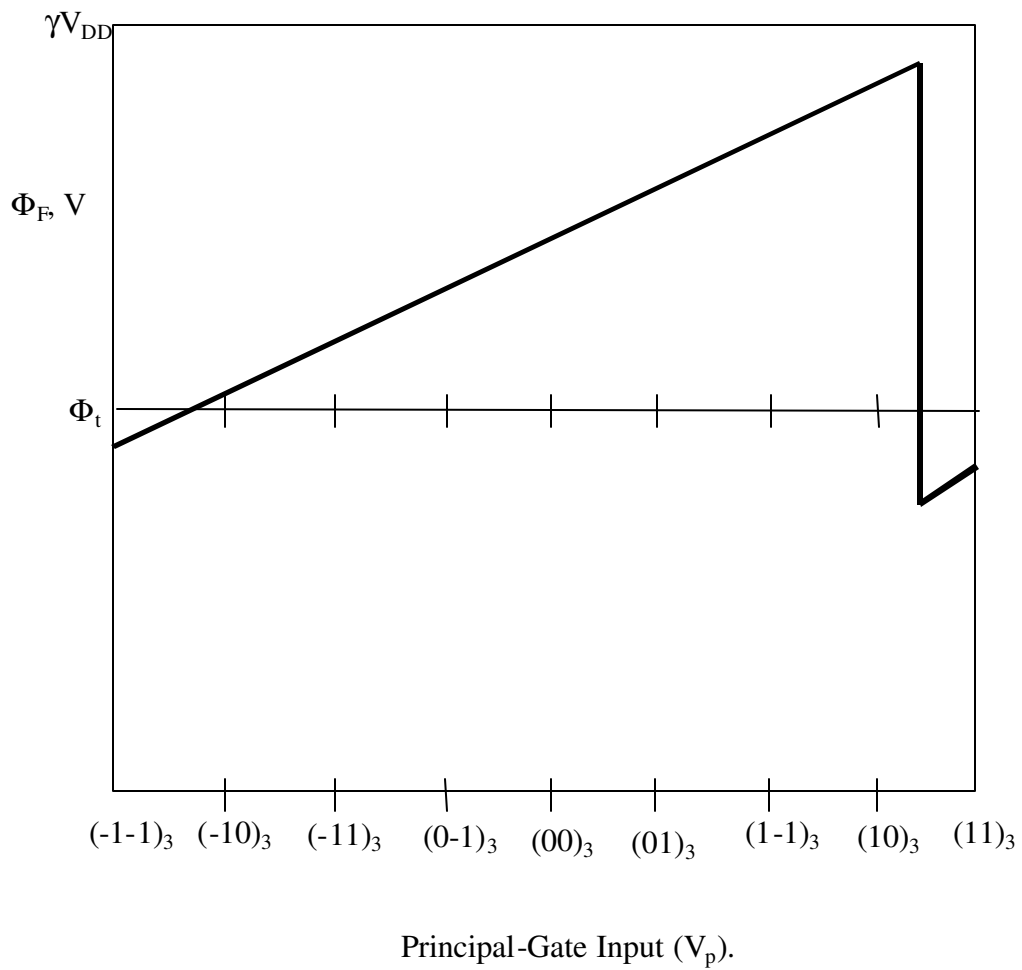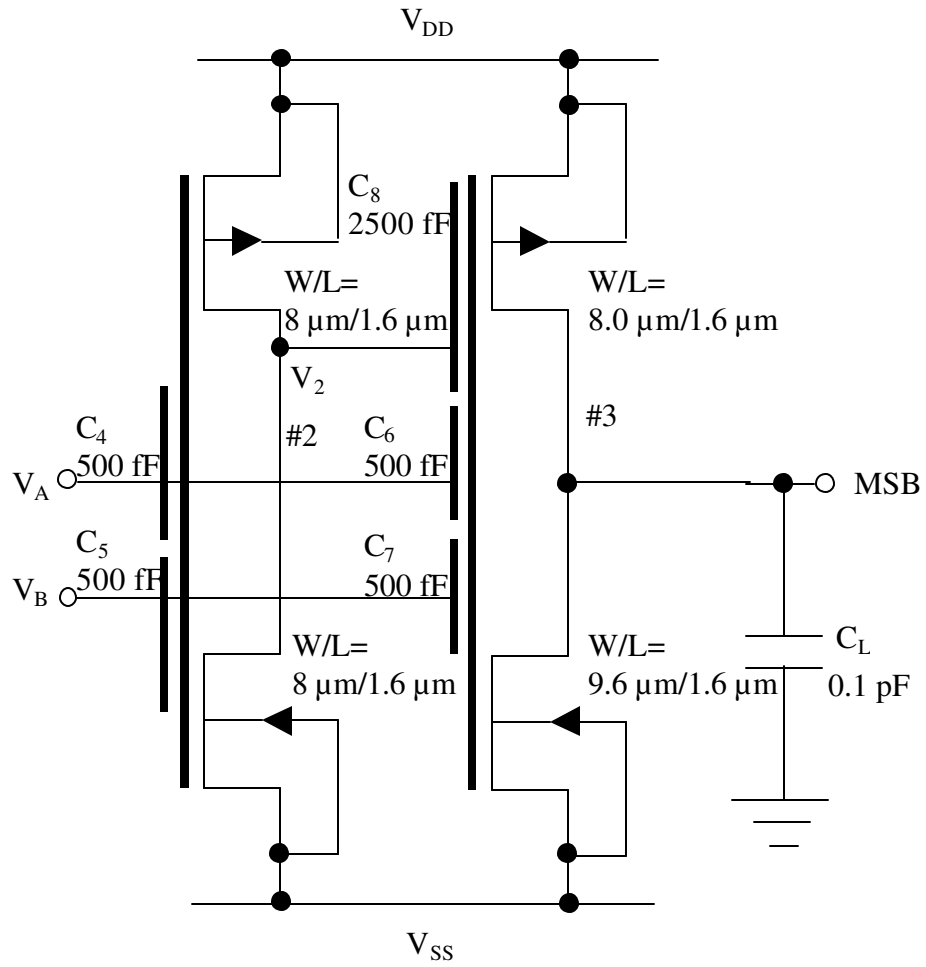
Fig. 3.10: Circuit diagram for implementation of ternary logic to binary logic (SSB bit) using floating gate MOSFETs.
Note: Pre-input inverter stage #5 produces same output as #2, hence output V_2 controls the capacitor C_{15}.

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For inputs $(1,-1)_3$ and $(1,0)_3$, the inequality is,

$$\frac{V_A \times C_{12} + V_B \times C_{13} + 0V \times C_{14} + 3V \times C_{15} + 3V \times C_{oxp}}{C_{12} + C_{13} + C_{14} + C_{15} + C_{oxn} + C_{oxp} + C_p} > \Phi_t (1.45V). \qquad (3.22)$$

The output of pre-input inverter stage (#5) goes LOW (0 V) for input $(1,1)_3$, hence for input $(1,1)_3$ the inequality is,

$$\frac{V_A \times C_{12} + V_B \times C_{13} + 0V \times C_{14} + 0V \times C_{15} + 3V \times C_{oxp}}{C_{12} + C_{13} + C_{14} + C_{15} + C_{oxn} + C_{oxp} + C_p} < \Phi_t (1.45V). \qquad (3.23)$$

The sizes of capacitors C_{12} and C_{13} are set to 3:1 in the ratio of weights of MSB and LSB in ternary bits and minimum sized capacitance of 1500 fF and 500 fF, respectively are considered. The value of C_p is calculated using equation (2.11), where $C_{p1} = 40$ fF and k is given by,

$$k = \frac{C_{12} + C_{13} + C_{14} + C_{15}}{C}.$$

Substituting C_{12} equal to 3C, C_{13} equal to C,

$$k = \frac{3C + C + C_{14} + C_{15}}{C} = 4 + \frac{C_{14} + C_{15}}{C}.$$

Substituting the value of k, C_p is calculated as,

$$C_p = (4 + \frac{C_{14} + C_{15}}{500\,fF}) \times 40\,fF = 160\,fF + (C_{14} + C_{15}) \times 40/500.$$

The values of C_{12} and C_{13} are substituted in above inequalities (3.19)-(3.23). The values of C_{14} and C_{15} that satisfy above inequalities are found to be 2500 fF and 1500 fF, respectively. Substituting the value of C_{14} and C_{15} the value of C_p is found to be 480 fF.

The width of nMOS transistor is adjusted to change switching threshold voltage to meet the inequality (3.23). The switching threshold voltage is shifted

Table 3.5: Voltage on floating gate Φ_F of SSB for corresponding
ternary inputs (Φ_t for MIFG inverter is 1.05 V)

Ternary Inputs	Output of #4 V_4	Output of #5 V_5	Voltage on Floating Gate Φ_F	
$(-1-1)_3$	HIGH (3 V)	HIGH (3 V)	0.925	$\Phi_F < \Phi_t$
$(-10)_3$	HIGH (3 V)	HIGH (3 V)	1.155	$\Phi_F > \Phi_t$
$(-11)_3$	HIGH (3 V)	HIGH (3 V)	1.385	$\Phi_F > \Phi_t$
$(0-1)_3$	LOW (0 V)	HIGH (3 V)	0.466	$\Phi_F < \Phi_t$
$(00)_3$	LOW (0 V)	HIGH (3 V)	0.696	$\Phi_F < \Phi_t$
$(01)_3$	LOW (0 V)	HIGH (3 V)	0.925	$\Phi_F < \Phi_t$
$(1-1)_3$	LOW (0 V)	HIGH (3 V)	1.155	$\Phi_F > \Phi_t$
$(10)_3$	LOW (0 V)	HIGH (3 V)	1.385	$\Phi_F > \Phi_t$
$(11)_3$	LOW (0 V)	LOW (0 V)	0.925	$\Phi_F < \Phi_t$

Note: Output of #4 stage V_4 controls the capacitor C_{14} of the main inverter stage.
Output of #5 stage V_5 controls the capacitor C_{15} of the main inverter stage.
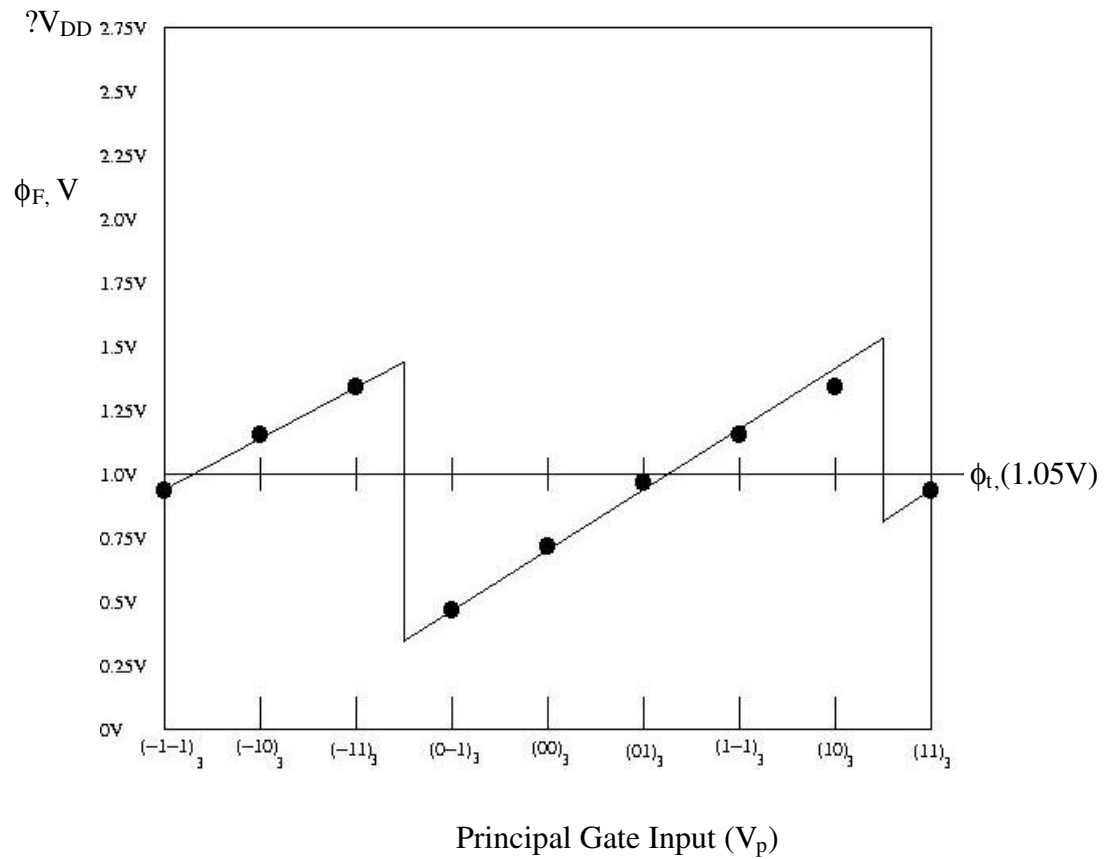
Fig. 3.11: Floating gate potential diagram for the second significant bit.
(Note: Figure drawn to scale).

from 1.45 V to 1.05 V by changing the width of nMOS transistor from $W_n = 8.0\ \mu m$

to $W_n = 24\ \mu m$. The voltage on the floating gate is calculated and tabulated in Table

3.5. The FPD for the SSB to scale is shown in Fig. 3.11. The output of the circuit

needs to be inverted to get the correct output. Hence a CMOS inverter is inserted at

the output, which would invert and as well buffer the output. The width of the

transistors used in the buffer is $16\ \mu m$ ($W_p = W_n = 16\ \mu m$).

3.4.1 Circuit Design for #4 Stage

The output of the pre-input inverter stage V_4 goes LOW (0 V) from inputs

$(0,-1)_3$ to $(1,1)_3$. The inverter stage (#4) can be designed with three input capacitors

C_9, C_{10} and C_{11}. The capacitors C_9 and C_{10} are controlled by ternary inputs V_A and

V_B, respectively and capacitor C_{11} is connected to supply voltage V_{DD} (3 V). Using

equations (2.7-2.9) the inequalities for inverter stage (#4) is found.

For inputs $(-1,-1)_3$ to $(-1,1)_3$,

$$\frac{V_A \times C_9 + V_B \times C_{10} + 3V \times C_{11} + 3V \times C_{oxp}}{C_9 + C_{10} + C_{11} + C_{oxn} + C_{oxp} + C_p} < \Phi_t\,(1.45V). \qquad (3.24)$$

For inputs $(0,-1)_3$ to $(1,1)_3$,

$$\frac{V_A \times C_9 + V_B \times C_{10} + 3V \times C_{11} + 3V \times C_{oxp}}{C_9 + C_{10} + C_{11} + C_{oxn} + C_{oxp} + C_p} > \Phi_t\,(1.45V). \qquad (3.25)$$

The sizes of capacitors C_9 and C_{10} are set to 3:1 in the ratio of weights of

MSB and LSB in ternary bits and minimum sized capacitance of 1500 fF and 500 fF

are considered. The value of C_p is calculated using equation (2.11), where C_{p1}=40 fF

and k is given by,

$$k = \frac{C_9 + C_{10} + C_{11}}{C}.$$

Substituting C_9 equal to $3C$, C_{10} equal to C,

$$k = \frac{3C + C + C_{11}}{C} = 4 + \frac{C_{11}}{C}.$$

Substituting the value of k, C_p is calculated as,

$$C_p = (4 + \frac{C_{11}}{500\,fF}) \times 40\,fF = 160\,fF + (C_{11}) \times 40/500.$$

Substituting the value of C_9, C_{10} and C_p in the inequalities (3.24,3.25) the minimum value of C_{11} is 3500 fF, which is a multiple of 500 fF. For better timing response, the value of C_{11} can be reduced and still meet the inequalities by increasing the W/L ratio of nMOS transistor, in other words shifting switching threshold voltage. The width of nMOS transistor W_n = 20 µm is used and value of C_{11} reduces to 2500 fF and is shown in Fig. 3.10. Substituting the value of C_9, C_{10} and C_{11}, the value of C_p is found to be 360 fF.

3.4.2 Circuit Design for #5 Stage

The output of the pre-input gate inverter stage (#5) is same as the output of pre-input gate inverter stage (#2). Hence the output V_2 of (#2) is used to control the capacitor C_{15}.

3.5 Circuit Design for LSB

The least significant bit is designed on similar lines. The output of the LSB bit is HIGH (3 V) for odd decimal numbers (-3, -1, 1, 3) and LOW (0 V) for even decimal numbers (-4, -2, 0, 2, 4). From Table 3.1 the FPD for LSB is drawn and is shown in Fig. 3.12. From FPD, the voltage on floating gate falls below switching threshold voltage four times, hence four pre-input gate inverter stages are used to control the voltage on floating gate as shown in Fig. 3.13. The main inverter stage
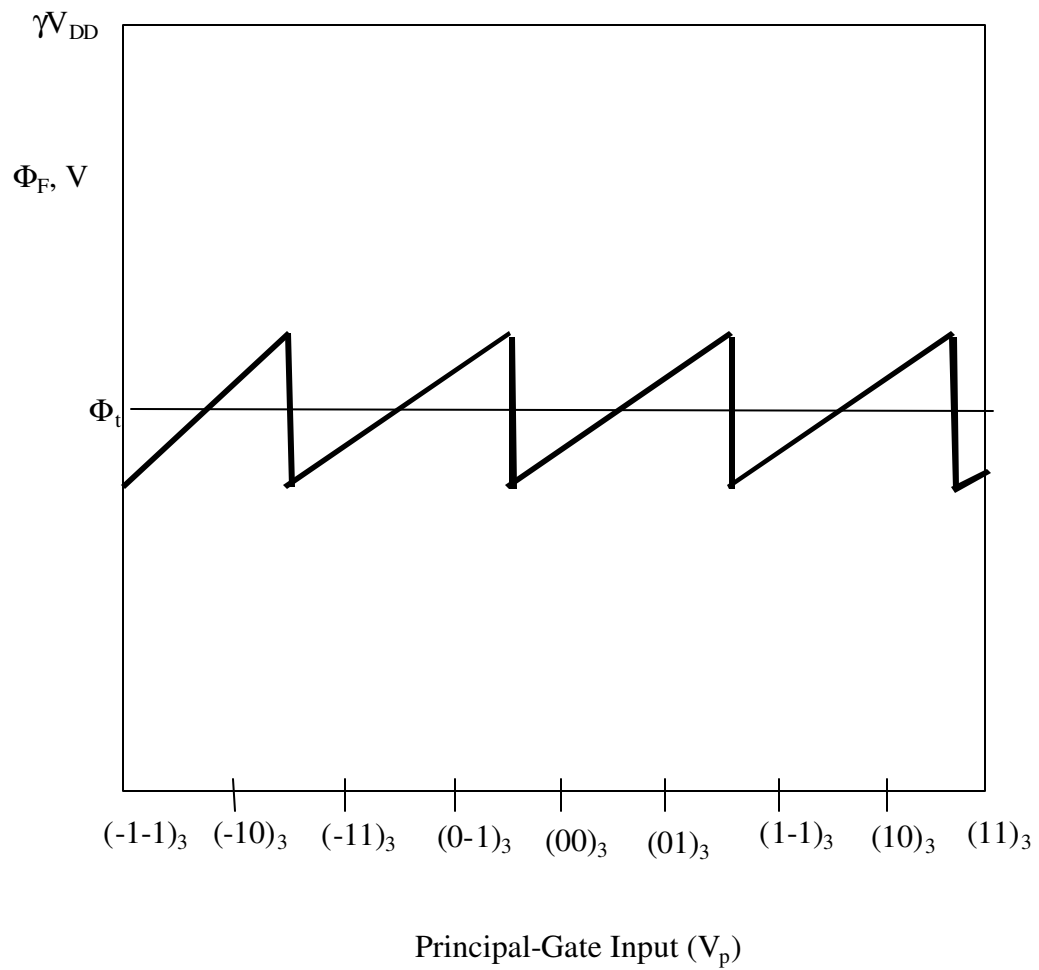
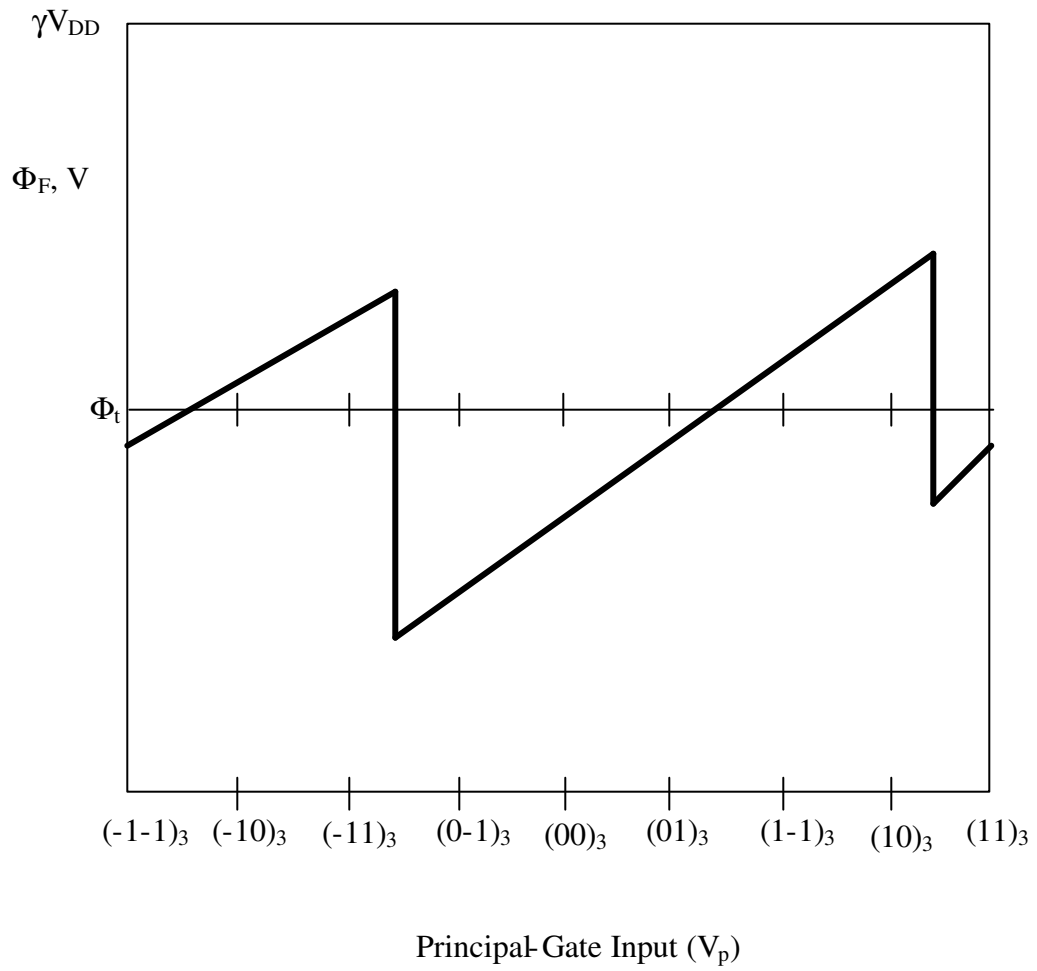Fig. 3.12: Floating gate potential diagram for the least significant bit.
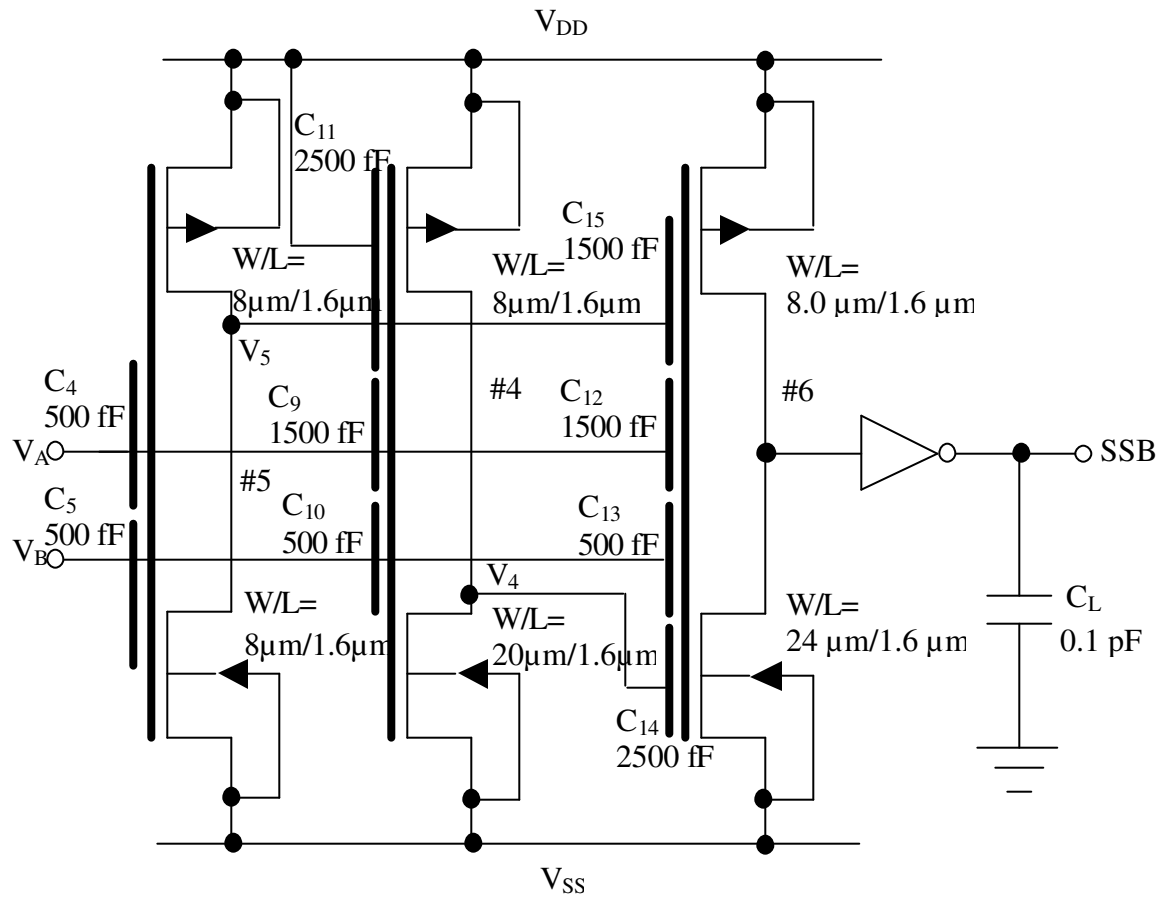(Note: Figure not drawn to scale).
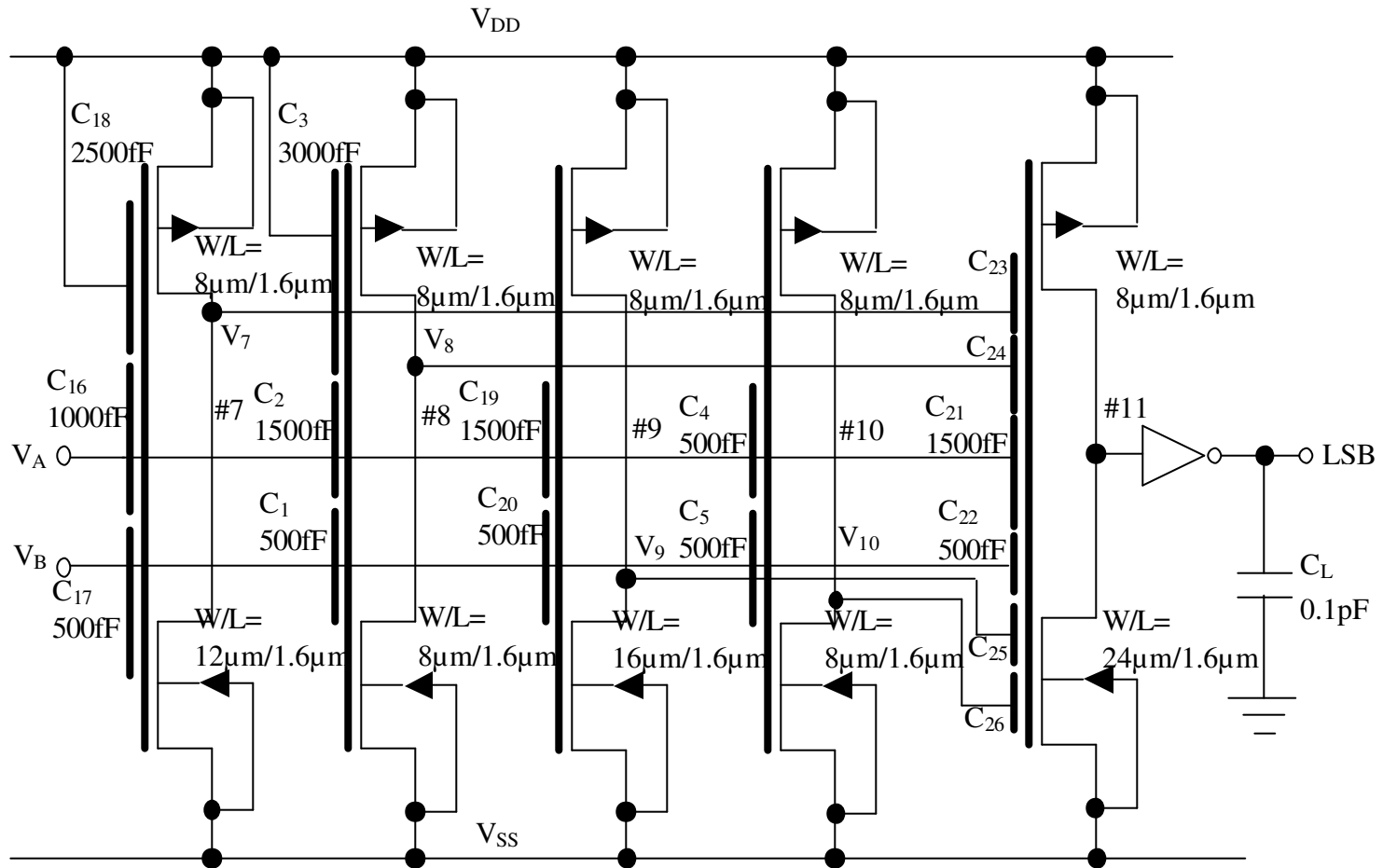
Fig. 3.13: Circuit diagram for implementation of ternary logic to binary logic (LSB bit) using floating gate MOSFETs.
Note: Pre-input gate inverter stage #8, #10 produce same output as sign bit and #2, respectively, hence the sign bit and V_2 are used to control capacitors C_{24} and C_{26}.

has six input capacitors C_{21}, C_{22}, C_{23}, C_{24}, C_{25} and C_{26}. The capacitors C_{21} and C_{22} are controlled by ternary inputs V_A and V_B, respectively. The capacitors C_{23}, C_{24}, C_{25} and C_{26} are controlled by outputs V_7, V_8, V_9 and V_{10} of pre-input inverter stages (#7), (#8), (#9) and (#10), respectively. The output of pre-input gate inverter stage (#7) goes LOW (0 V) from input $(-1,1)_3$ to $(1,1)_3$, the output of (#8) goes LOW (0V) from inputs $(0,0)_3$ to $(1,1)_3$, the output of (#9) goes LOW (0V) from inputs $(1,-1)_3$ to $(1,1)_3$ and the output of (#10) goes LOW for input $(1,1)_3$.

The voltage on floating gate Φ_F of the main inverter stage is given by equation (2.7),

$$\Phi_F = \frac{V_A \times C_{21} + V_B \times C_{22} + V_7 \times C_{23} + V_8 \times C_{24} + V_9 \times C_{25} + V_{10} \times C_{26} + V_{DD} \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p}.$$

Using equations (2.7-2.9), for input $(-1,-1)_3$,

$$\frac{(-3V) \times C_{21} + (-3V) \times C_{22} + 3V \times C_{23} + 3V \times C_{24} + 3V \times C_{25} + 3V \times C_{26} + 3V \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p} < \Phi_t.$$

For input $(-1,0)_3$,

$$\frac{(-3V) \times C_{21} + (0V) \times C_{22} + 3V \times C_{23} + 3V \times C_{24} + 3V \times C_{25} + 3V \times C_{26} + 3V \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p} > \Phi_t.$$

For input $(-1,1)_3$,

$$\frac{(-3V) \times C_{21} + (3V) \times C_{22} + 0V \times C_{23} + 3V \times C_{24} + 3V \times C_{25} + 3V \times C_{26} + 3V \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p} < \Phi_t.$$

For input $(0,-1)_3$,

$$\frac{(-3V) \times C_{21} + (0V) \times C_{22} + 0V \times C_{23} + 3V \times C_{24} + 3V \times C_{25} + 3V \times C_{26} + 3V \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p} > \Phi_t.$$

For input $(0,0)_3$,

$$\frac{(0V) \times C_{21} + (0V) \times C_{22} + 0V \times C_{23} + 0V \times C_{24} + 3V \times C_{25} + 3V \times C_{26} + 3V \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p} < \Phi_t.$$

For input $(0,1)_3$,

$$\frac{(0V) \times C_{21} + (3V) \times C_{22} + 0V \times C_{23} + 0V \times C_{24} + 3V \times C_{25} + 3V \times C_{26} + 3V \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p} > \Phi_t.$$

For input $(1,-1)_3$,

$$\frac{(3V) \times C_{21} + (-3V) \times C_{22} + 0V \times C_{23} + 0V \times C_{24} + 0V \times C_{25} + 3V \times C_{26} + 3V \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p} < \Phi_t.$$

For input $(1,0)_3$,

$$\frac{(3V) \times C_{21} + (0V) \times C_{22} + 0V \times C_{23} + 0V \times C_{24} + 0V \times C_{25} + 3V \times C_{26} + 3V \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p} > \Phi_t.$$

For input $(1,1)_3$,

$$\frac{(3V) \times C_{21} + (3V) \times C_{22} + 0V \times C_{23} + 0V \times C_{24} + 0V \times C_{25} + 0V \times C_{26} + 3V \times C_{oxp}}{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26} + C_{oxn} + C_{oxp} + C_p} < \Phi_t.$$

The input capacitors C_{21} and C_{22} of the main inverter stage are controlled by ternary inputs and are set to 3:1 as in the ratio of weights of MSB and LSB in ternary bits. The minimum size capacitance of 1500 fF and 500 fF are considered. The value of C_p is calculated using equation (2.11), where C_{p1}=40 fF and k is given by,

$$k = \frac{C_{21} + C_{22} + C_{23} + C_{24} + C_{25} + C_{26}}{C}.$$

Substituting C_{21} equal to 3C, C_{22} equal to C,

$$k = \frac{3C + C + C_{23} + C_{24} + C_{25} + C_{26}}{C} = 4 + \frac{C_{23} + C_{24} + C_{25} + C_{26}}{C}.$$

Substituting the value of k, C_p is calculated as,

$$C_p = (4 + \frac{C_{23} + C_{24} + C_{25} + C_{26}}{500\,fF}) \times 40\,fF = 160\,fF + (C_{23} + C_{24} + C_{25} + C_{26}) \times 40/500.$$

The minimum sizes of the capacitors C_{23}, C_{24}, C_{25} and C_{26} controlled by output of pre-input inverter stages, which satisfy above equations are equal and is found to be 1000 fF. Substituting the value of C_{21}, C_{22}, C_{23}, C_{24}, C_{25} and C_{26} the value of C_p is found to be 480 fF. The switching threshold voltage of the main inverter stage is changed from 1.45 V to 1.05 V by changing the width of nMOS transistor from W_n=8 μm to W_n = 24 μm. The voltage on floating gate is calculated and tabulated in Table 3.6. The FPD for LSB is drawn to scale and is shown in Fig. 3.14. The output of the main inverter stage needs to be inverted to obtain the LSB. Hence a CMOS inverter is inserted at the output, which also acts as a buffer. The width of transistors used in the buffer is $W_n = W_p = 16$ μm.

3.5.1 Circuit Design for #7 Stage

The pre-input gate inverter stage (#7) goes LOW (0 V) from inputs $(-1,1)_3$ to $(1,1)_3$, hence using equations (2.7-2.9), the inequalities would be,

$$\frac{V_A \times C_{16} + V_B \times C_{17} + 3V \times C_{18} + 3V \times C_{oxp}}{C_{16} + C_{17} + C_{18} + C_{oxn} + C_{oxp} + C_p} > \Phi_t (1.45V). \tag{3.24}$$

The capacitor ratio C_{16} and C_{17} are set 3:1 in the ratio of MSB and LSB as in the ternary bits. The minimum value of 1500 fF and 500 fF is considered. The value of C_p is calculated using equation (2.11), where C_{p1}=40 fF and k is given by,

$$k = \frac{C_{16} + C_{17} + C_{18}}{C}.$$

Substituting C_{16} equal to 3C, C_{17} equal to C,

$$k = \frac{3C + C + C_{18}}{C} = 4 + \frac{C_{18}}{C}.$$

Table 3.6: Voltage on floating gate Φ_F of LSB for corresponding ternary inputs (Φ_t for MIFG inverter is 1.05 V)

Ternary Inputs	Output of #7 V_7	Output of #8 V_8	Output of #9 V_9	Output of #10 V_{10}	Voltage on Floating Gate Φ_F	
$(-1-1)_3$	HIGH (3V)	HIGH (3V)	HIGH (3V)	HIGH (3V)	0.924	$\Phi_F < \Phi_t$
$(-10)_3$	HIGH (3V)	HIGH (3V)	HIGH (3V)	HIGH (3V)	1.153	$\Phi_F > \Phi_t$
$(-11)_3$	LOW (0V)	HIGH (3V)	HIGH (3V)	HIGH (3V)	0.924	$\Phi_F < \Phi_t$
$(0-1)_3$	LOW (0V)	HIGH (3V)	HIGH (3V)	HIGH (3V)	1.153	$\Phi_F > \Phi_t$
$(00)_3$	LOW (0V)	LOW (0V)	HIGH (3V)	HIGH (3V)	0.924	$\Phi_F < \Phi_t$
$(01)_3$	LOW (0V)	LOW (0V)	HIGH (3V)	HIGH (3V)	1.153	$\Phi_F > \Phi_t$
$(1-1)_3$	LOW (0V)	LOW (0V)	LOW (0V)	HIGH (3V)	0.924	$\Phi_F < \Phi_t$
$(10)_3$	LOW (0V)	LOW (0V)	LOW (0V)	HIGH (3V)	1.153	$\Phi_F > \Phi_t$
$(11)_3$	LOW (0V)	LOW (0V)	LOW (0V)	LOW (0V)	0.924	$\Phi_F < \Phi_t$

Note: Output of #7 stage V_7 controls the capacitor C_{23} of the main inverter stage.
Output of #8 stage V_8 controls the capacitor C_{24} of the main inverter stage.
Output of #9 stage V_9 controls the capacitor C_{25} of the main inverter stage.
Output of #10 stage V_{10} controls the capacitor C_{26} of the main inverter stage.
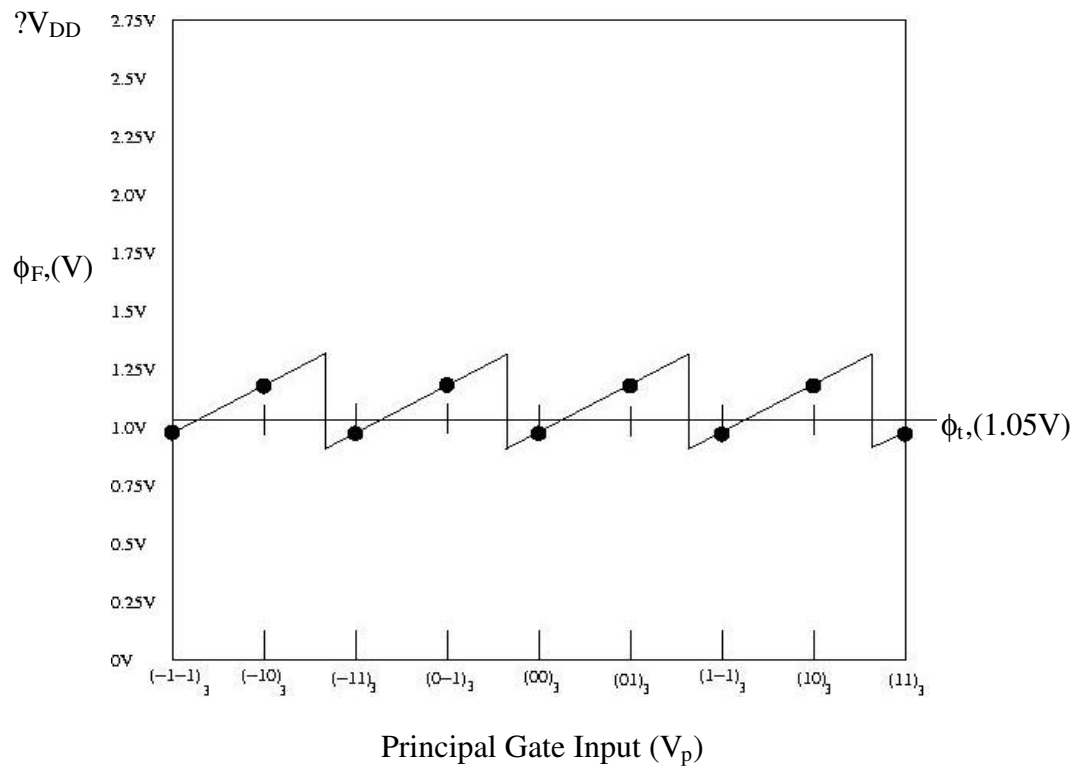
Fig. 3.14: Floating gate potential diagram for the least significant bit.
(Note: Figure drawn to scale).

Substituting the value of k, C_p is calculated as,

$$C_p = (4 + \frac{C_{18}}{500\,fF}) \times 40\,fF = 160\,fF + (C_{18}) \times 40/500.$$

Substituting the values of C_{16} and C_{17} in inequality (3.24), for input $(-1,1)_3$, the minimum value of C_{18} is found to be 4000 fF. High value of capacitance C_{18} resulted in high propagation delay, hence the capacitor ratio of C_{16} and C_{17} is reconsidered. The capacitor ratio of C_{16} to C_{17} is set to 2:1 and minimum size of 1000 fF and 500 fF is considered. Substituting the values of C_{16} and C_{17} in inequality (3.24), for input $(-1,1)_3$, the minimum value of C_{18} is found to be 2500 fF. Substituting the value of C_9, C_{10} and C_{11} the value of C_p is found to be 320 fF.

3.5.2 Circuit Design for #8 Stage

The output of pre-input gate inverter stage (#8) goes LOW (0 V) from inputs $(0,0)_3$ to $(1,1)_3$. The output of pre-input gate inverter stage (#8) is same as the output of sign bit, hence output of sign bit is used to control the input capacitor C_{24}.

3.5.3 Circuit Design for #9 Stage

The pre-input gate inverter stage (#9) goes LOW (0 V) from input $(1,-1)_3$ to $(1,1)_3$. Using equations (2.7-2.9) the inequality would be,

$$\frac{V_A \times C_{19} + V_B \times C_{20} + 3V \times C_{27} + 3V \times C_{oxp}}{C_{19} + C_{20} + C_{21} + C_{oxn} + C_{oxp} + C_p} > \Phi_t (1.45V). \tag{3.25}$$

The capacitors C_{19} and C_{20} are set to 3:1 in the ratio of MSB and LSB in ternary bits and a minimum size of 1500 fF and 500 fF is considered. Substituting the values of C_{19} and C_{20} in inequality (3.25), for input $(1,-1)_3$, the value of C_{27} is found to be 0 fF. Hence capacitor C_{27} is not used for the pre-input inverter stage

(#9). For faster output the width of nMOS transistor is adjusted from its minimum value of $W_n = 8\ \mu m$ to $W_n = 16\ \mu m$ and is shown in Fig. 3.13.

3.5.4 Circuit Design for #10 Stage

The output of pre-input gate inverter stage (#10) goes LOW (0V) for input $(1,1)_3$. The output of the pre-input inverter stage (#10) is same as output of the pre-input gate inverter stage (#2), hence output V_2 is used to control input capacitor C_{26}.

3.6 Simulation Results

The output of SB, MSB, SSB, LSB is buffered which drives the pad. The transistor widths used for the buffer are $W_p/W_n = 16\ \mu m/16\ \mu m$ and $W_p/W_n = 40\ \mu m/40\ \mu m$. Fig. 3.15 shows the full CMOS circuit to convert ternary logic to binary logic using floating gate MOSFETs. The circuit in Fig. 3.15 is simulated for 1.5 μm technology with 3 V supply voltage. BSIM3 MOS model parameters have been used for simulation and are listed in Appendix B. The ternary inputs to the circuit are piece-wise linear voltage sources, which verifies all inputs mentioned in Table 3.1. A pulse width of 20 ns with rise and fall times of 0.1 ns is given as input to the circuit. The parasitic capacitance C_p from floating gate to substrate on field oxide is estimated and is considered in designing circuits at pre-layout level. The output of floating gate inverters is buffered to obtain full logic levels. The pre-layout simulation output of the circuit shown in Fig. 3.15, the SB, MSB, SSB and LSB are shown in Fig. 3.16. The voltage on floating gate of the main inverter stage for these bits is shown in Fig. 3.17. The outputs of pre-input inverter stage V_2, V_4, V_7 and V_9, which controls the main inverter stage, are shown in Fig. 3.18. The propagation delay of the circuit is listed in Table 3.7. The blank columns in Table 3.7 correspond
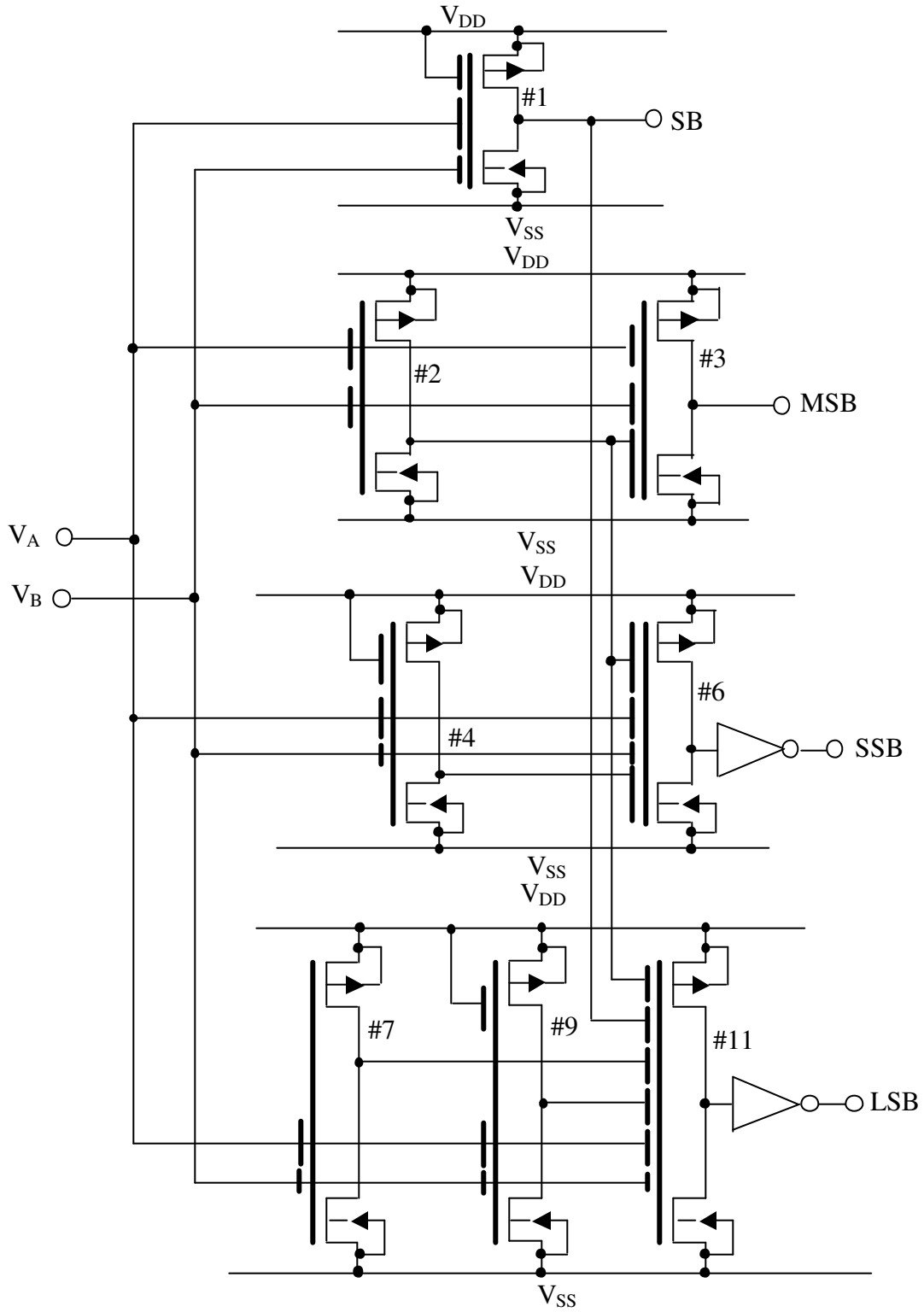
Fig. 3.15: Circuit diagram for implementation of conversion from ternary logic to binary logic.
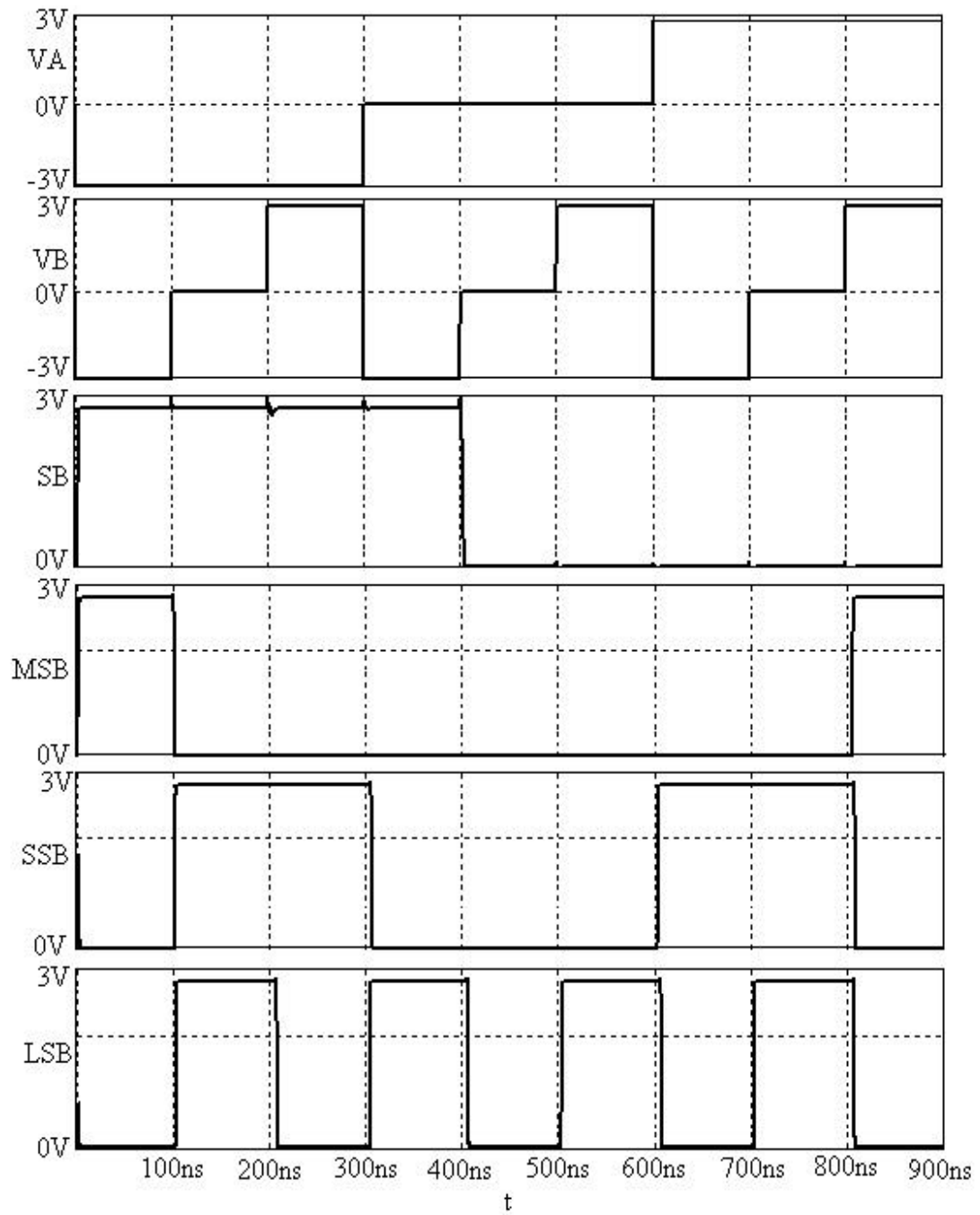
Fig. 3.16: Ternary inputs and SPICE simulated output of the circuit in Fig. 3.15.
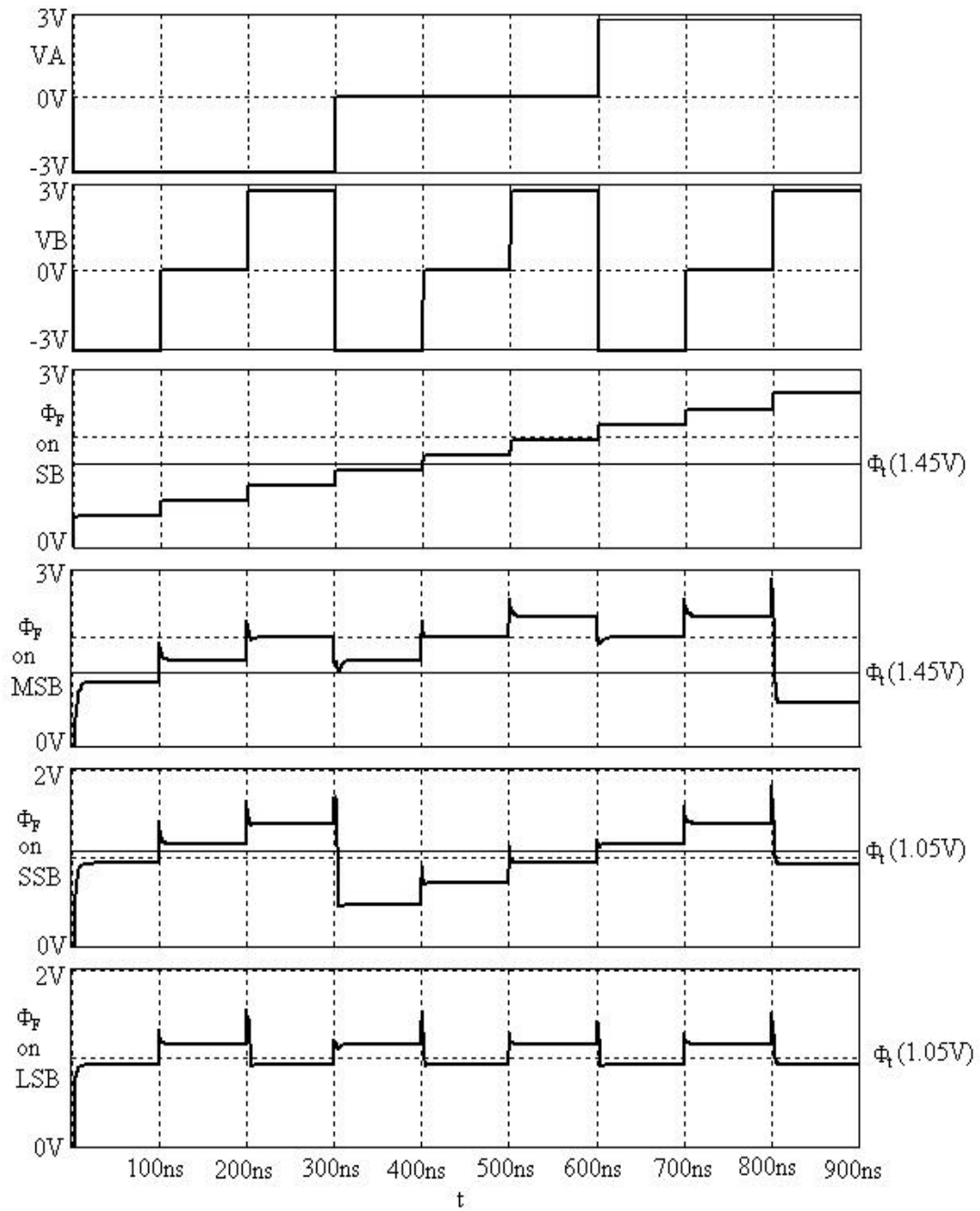
Fig. 3.17: Ternary input and SPICE simulated voltage on floating gate of main inverter gate stages shown in Fig. 3.15.
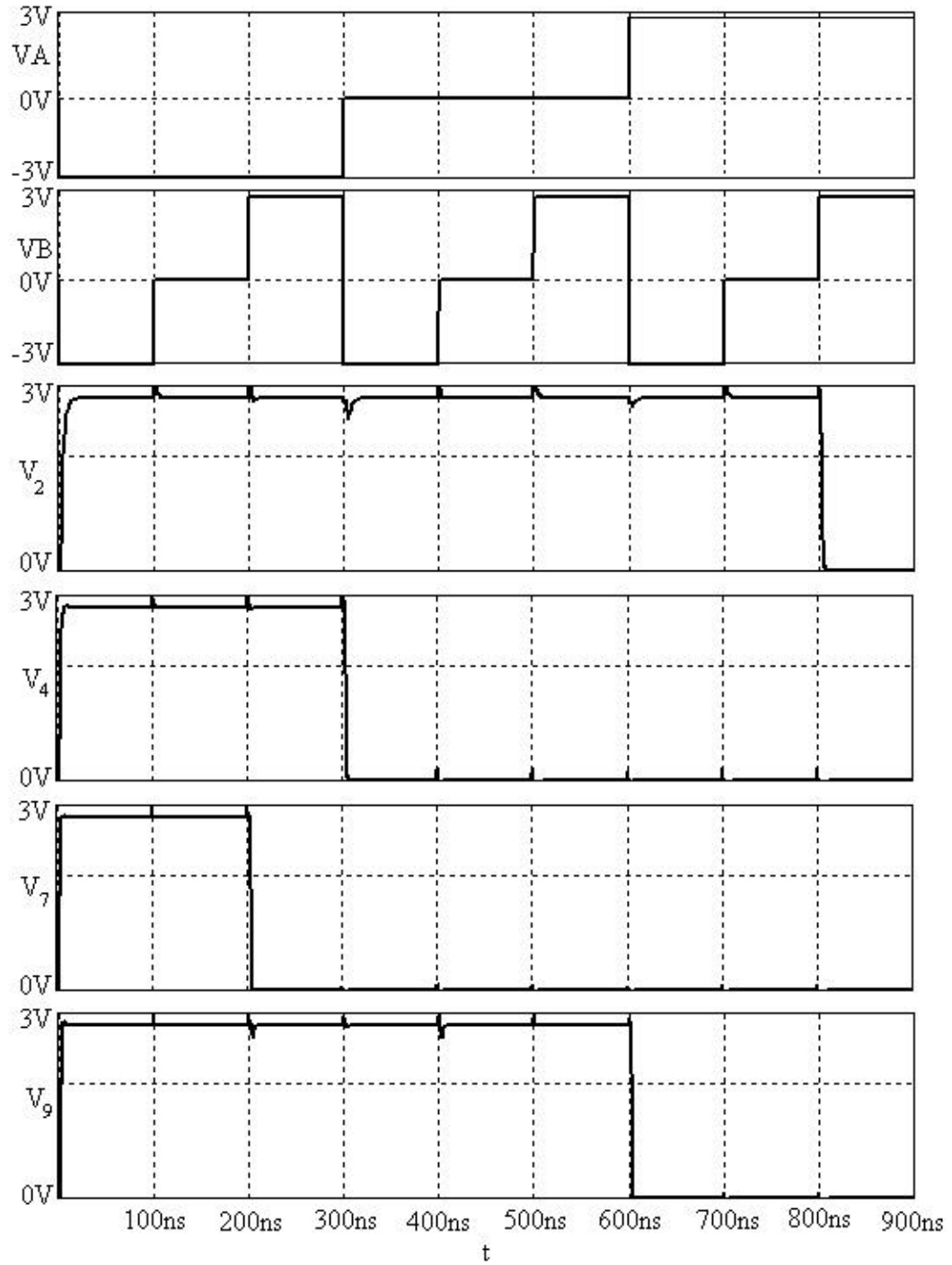
Fig. 3.18: Ternary input and output of pre-input gate inverter stages V_2, V_4, V_7 and V_9 shown in Fig. 3.15.

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Table 3.7: Propagation delay time from the layout in Fig. 3.19 with 0.1 pF load capacitance

Logic Level Transition (Ternary Logic)	SB (ns)	MSB (ns)	SSB (ns)	LSB (ns)
-4 →-3	-	1.70	1.97	3.04
-3→-2	-	-	-	8.11
-2→-1	-	-	6.78	5.04
-1→0	3.09	-	-	6.70
0→1	-	-	-	3.42
1→2	-	-	3.40	6.74
2→3	-	-	-	3.57
3→4	-	6.68	8.32	7.72
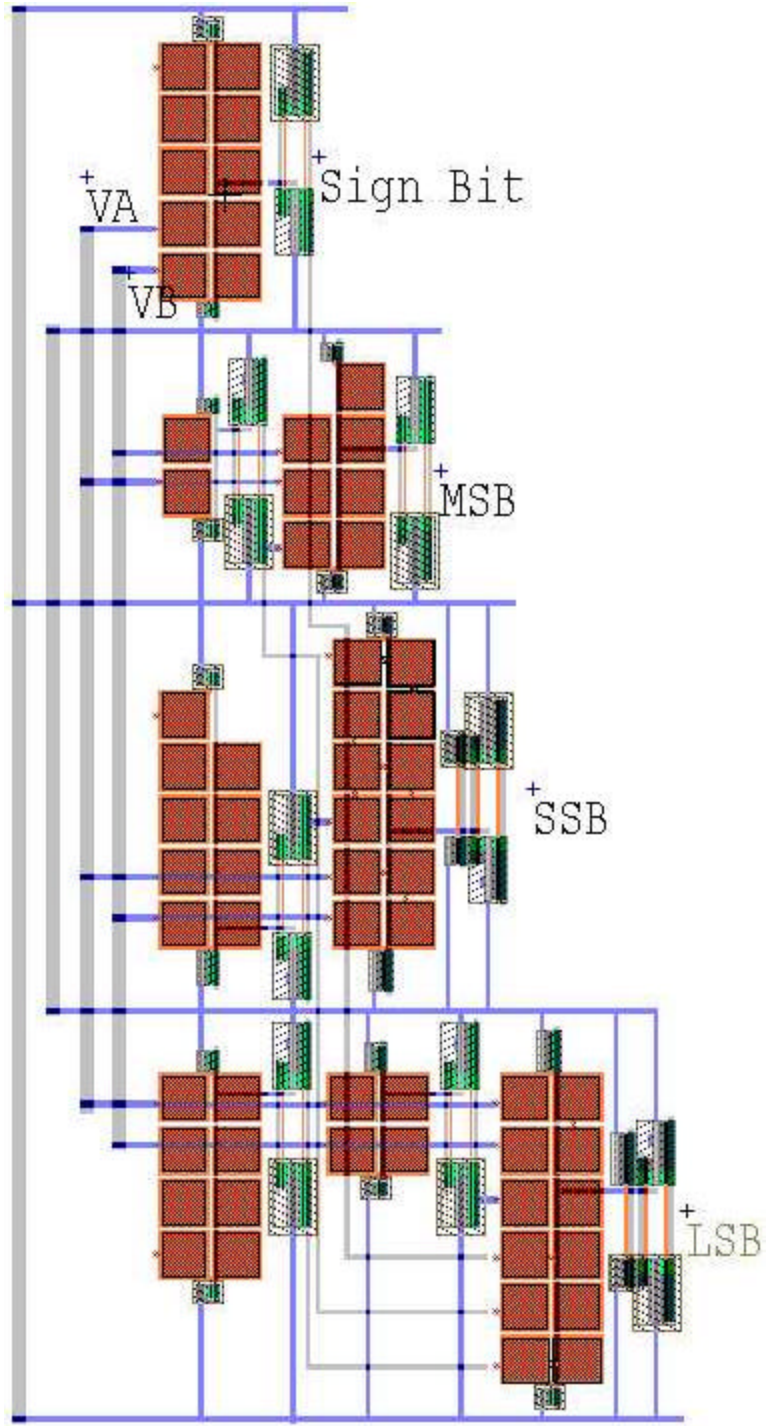
Fig. 3.19: Physical layout for the conversion circuit from ternary logic to binary logic shown in Fig. 3.15.

to no output change condition. The physical layout of the circuit in Fig. 3.15 is drawn using Tanner Tools and is shown in Fig. 3.19. The layout occupies an area of 432 μm x 908 μm.

The layout for the circuit with padframe is shown in Fig. 3.20. The post-layout simulation outputs of circuit with 0.1 pF load are shown in Figs. 3.21. At testing level, capacitance offered by probes of oscilloscope and breadboard are added to the pad pin, which is estimated to be 15 pF. Hence the circuit is also simulated with 15 pF load and is shown in Fig. 3.22. The expected propagation delay is presented in Table 3.8.

The worst-case variation in unit capacitance of 500 fF would be 365 fF from Table. 2.1. The circuit is simulated using 365 fF as unit capacitance and outputs are shown in Fig. 3.23.

3.7   Experimental Results

The conversion circuit is fabricated at MOSIS for 1.5 μm technology. The MOS model parameters of the fabricated chip are listed in Appendix D. The microphotograph of the fabricated design is shown in Fig. 3.24. The ternary inputs V_A and V_B are connected to pin11 and pin12, respectively. The input/output pads has protection devices from electro static discharge ESD, which are back-to-back diodes connected to V_{DD} and V_{SS}. Whenever the input voltage is above V_{DD} (3 V) or below V_{SS} (0 V), the respective diode is forward biased and input signal is pulled towards V_{DD} or V_{SS}. In the present case, whenever logic -1 (-3 V) is given as input to the circuit, diode connected to V_{SS} is forward biased and is pulled towards ground. Hence testing was limited and few transitions, which did not use logic -1 (-3
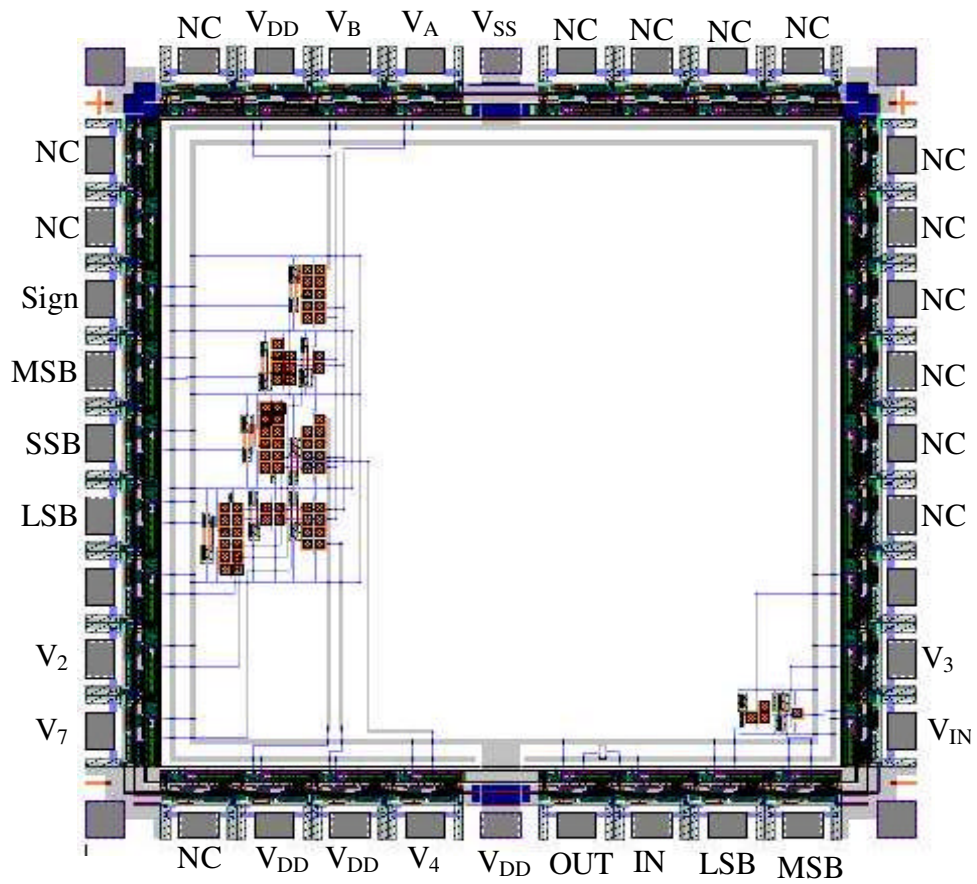
Fig. 3.20: Ternary logic to binary logic conversion layout with padframe.
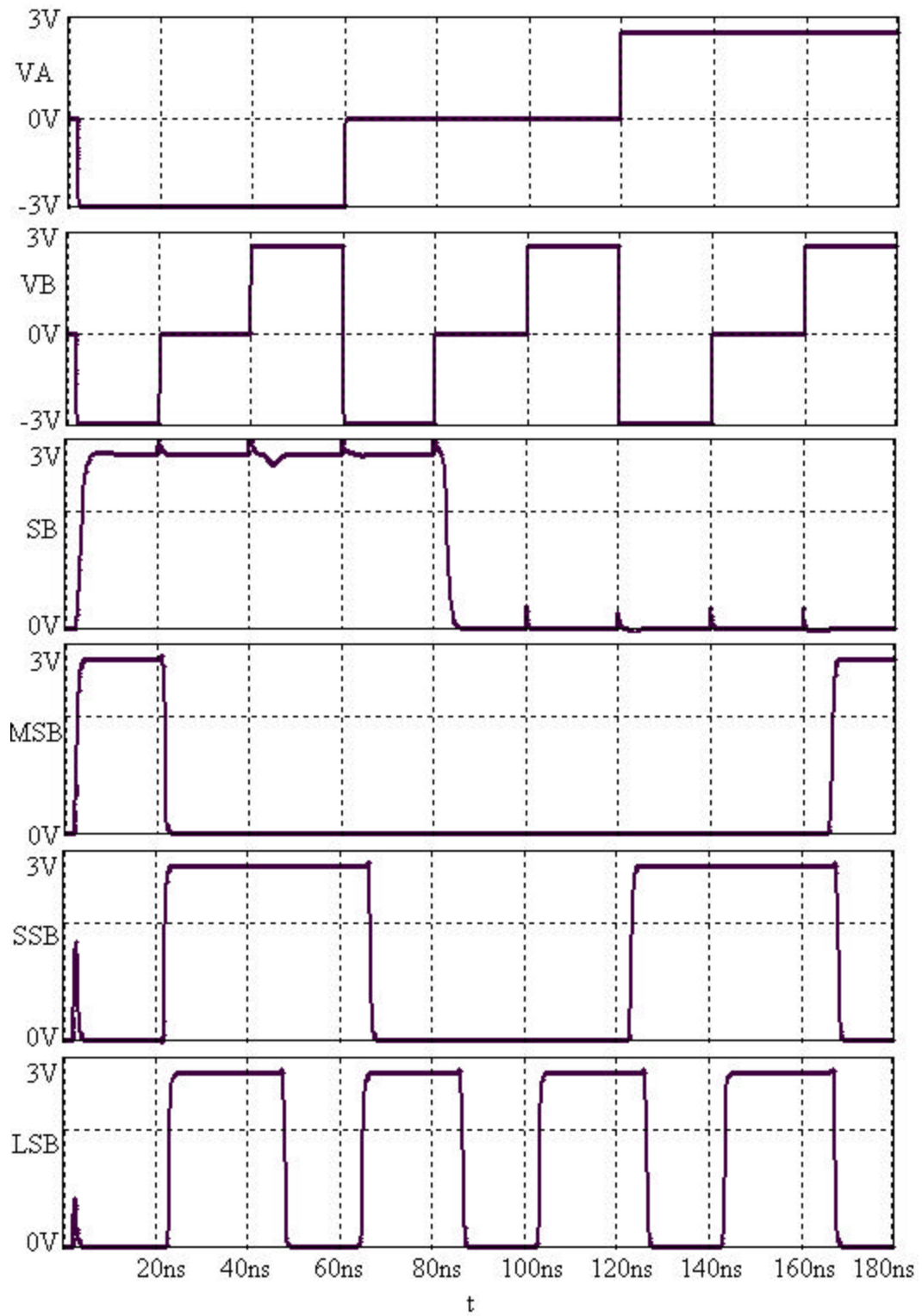
Fig. 3.21: Post-layout simulation outputs of circuit with 0.1 pF load capacitance.
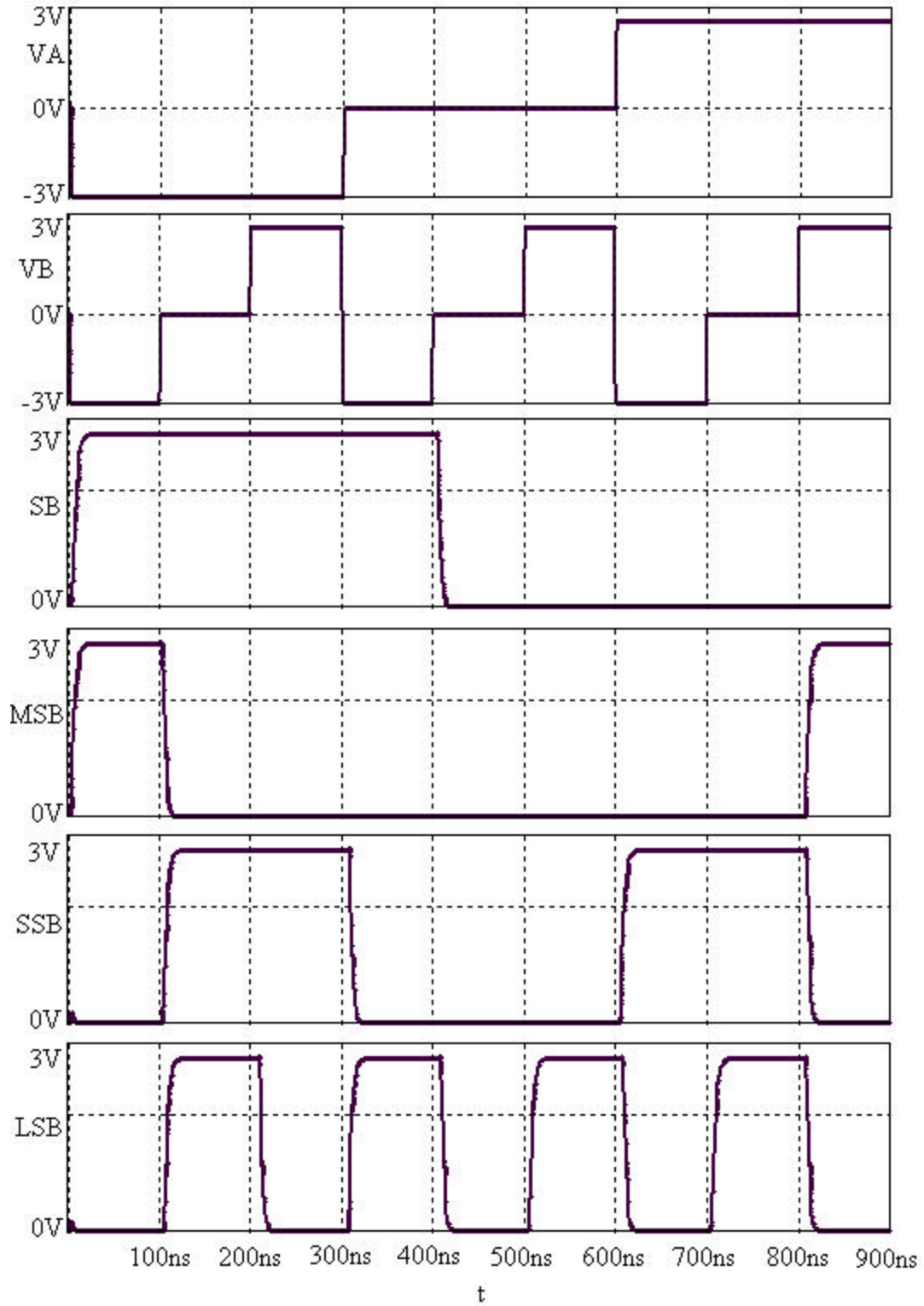
Fig. 3.22: Post-layout simulation outputs of circuit with 15 pF load capacitance.

Table 3.8: Propagation delay time from the layout in Fig. 3.19 with 15 pF load capacitance

Logic Level Transition (Ternary Logic)	Sign Bit (ns)	MSB (ns)	SSB (ns)	LSB (ns)
-4 →-3	-	6.63	7.34	8.42
-3→-2	-	-	-	13.02
-2→-1	-	-	11.726	10.37
-1→0	8.11	-	-	11.79
0→1	-	-	-	8.80
1→2	-	-	8.77	11.71
2→3	-	-	-	8.93
3→4	-	11.88	13.10	12.52
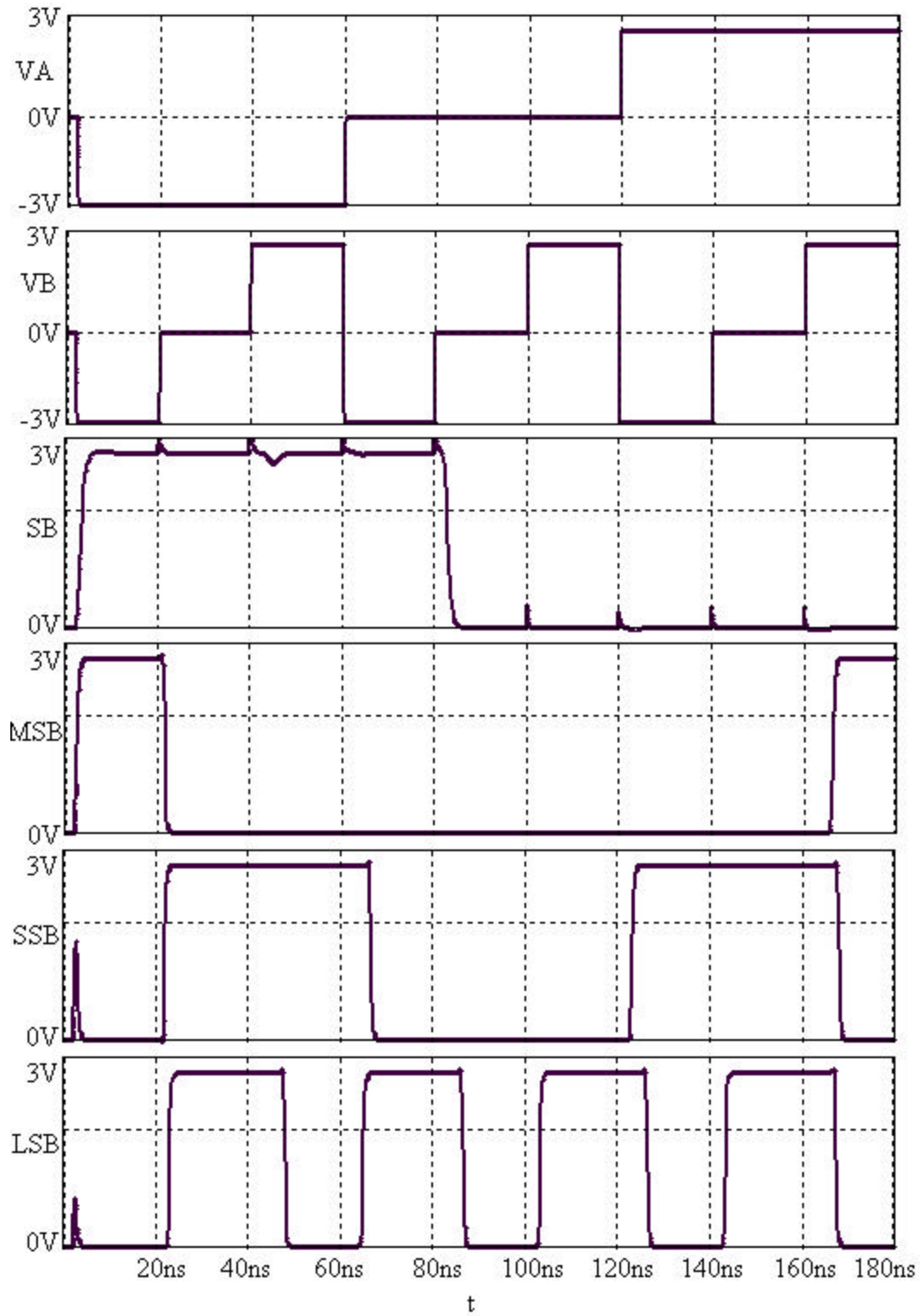
Fig. 3.23: Ternary inputs and SPICE simulated output of the circuit in Fig. 3.15 with unit capacitance of 365 fF.
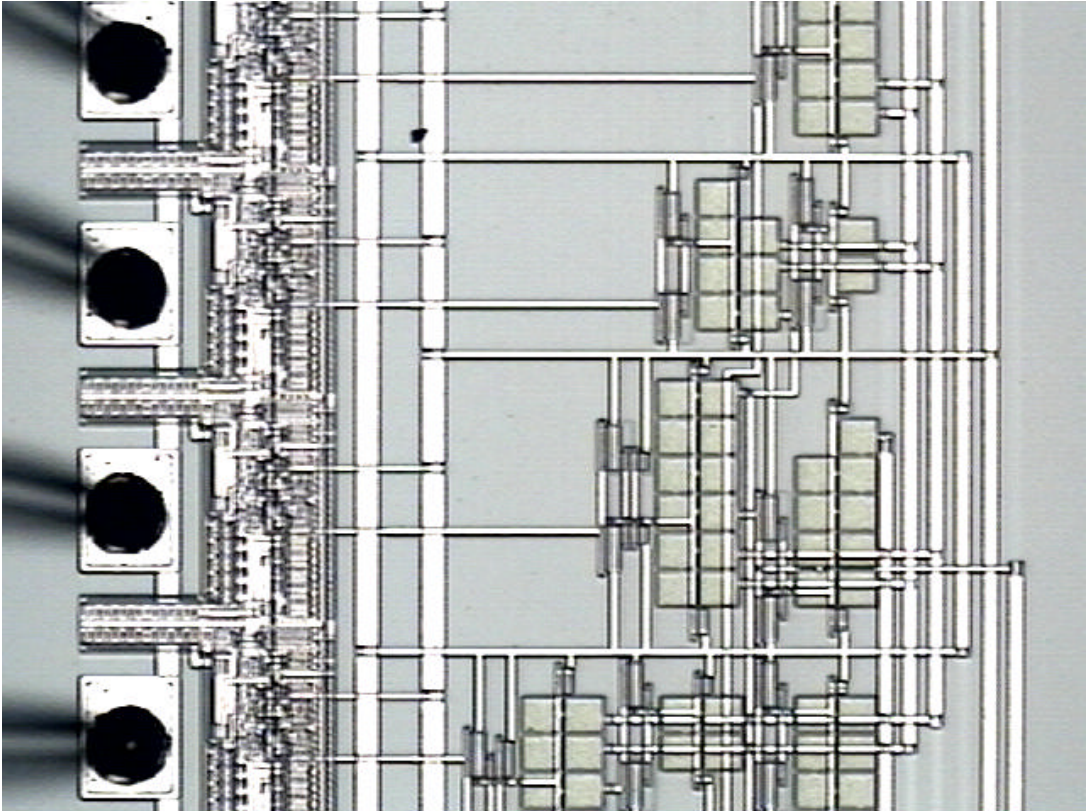
Fig. 3.24: Chip photograph of ternary to binary bit conversion device.

V) could be tested on the fabricated device. The padframe design is being investigated and revised for balanced ternary logic implementation and is left as scope for future work.

The capacitors C_3, C_{11} and C_{18} are used to adjust the threshold voltage for sign bit, V_4 and V_7, respectively. The capacitors C_3, C_{11} and C_{18} are connected to V_{DD} in the design. The inputs to these capacitors can be controlled at pin13, pin27 and pin28. The voltage at these pins is controlled using external voltage sources to adjust threshold voltage of the MIFG inverters.

Chapter 4

Conversion from Quaternary Logic to Binary Logic

4.1 Overview

The quaternary logic system is expressed in the form of (0,1,2,3). In a standard 3 V CMOS process, logic levels 0, 1, 2 and 3 are defined as 0 V, 1 V, 2 V and 3 V, respectively. Table 4.1 shows quaternary logic levels and corresponding binary bits. Corresponding decimal number is also included in Table 4.1. The conversion circuits from quaternary logic to binary logic presented here uses MIFG MOSFETs. The principle of transistor switching ON or OFF depending on the calculated weighted sum of all inputs on floating gate greater than or less than switching threshold voltage is utilized in designing the conversion circuits.

4.2 Circuit Design for MSB

The circuits are designed for 1.5 µm technology with a 3 V supply voltage. The switching threshold voltage of a CMOS inverter is found from voltage transfer characteristics. The standard CMOS inverter shown in Fig. 4.1 is simulated with W/L=16.0 µm/1.6 µm for a 3 V supply voltage. The W/L ratio of the transistors is taken more than the minimum values to obtain faster timing response. DC analysis is performed to obtain voltage transfer characteristics (VTC). The VTC is shown in Fig. 4.2, and Φ_{g0} and Φ_{s1} are marked. Φ_{g0} and Φ_{s1} are input voltages at which the output of inverter is V_{DD}-0.1 V and 0.1 V, respectively. Φ_{g0} is 0.53 V and Φ_{s1} is 2.37 V. The switching threshold voltage Φ_t is obtained using equation (2.7),

$$\Phi_t = \frac{0.53 + 2.37}{2} = 1.45V. \tag{4.1}$$

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Table 4.1 Decimal number, quaternary logic levels and binary logic levels

Decimal Number	Quaternary Logic	Binary Logic
0	0	00
1	1	01
2	2	10
3	3	11
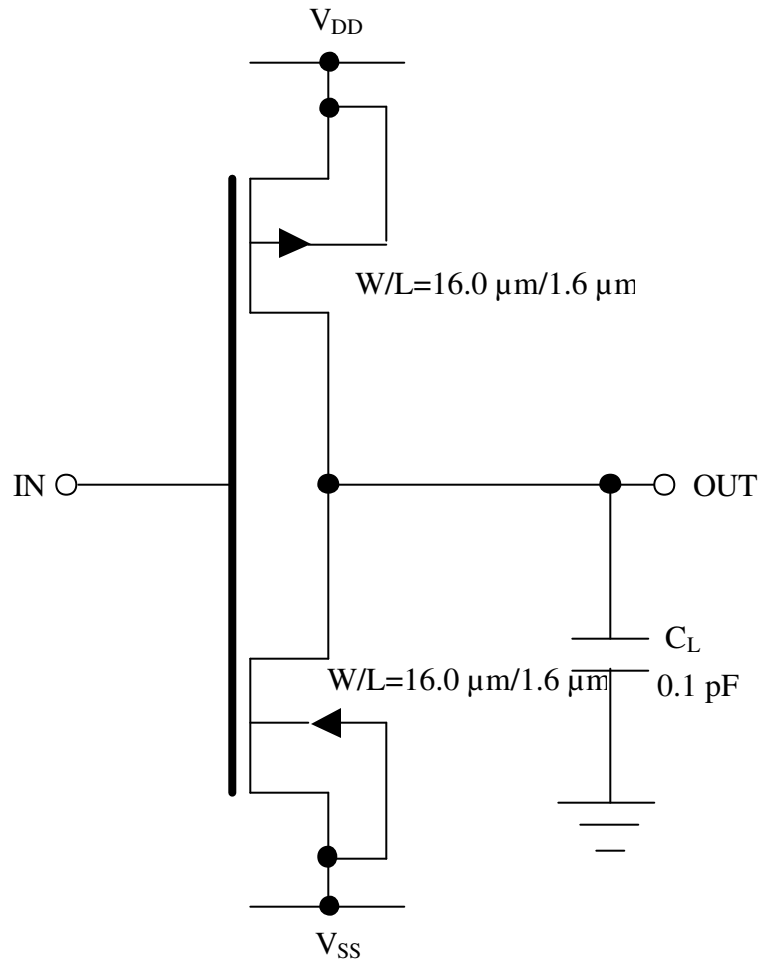
Fig. 4.1: Standard CMOS inverter with W/L ratio = 16.0 μm/1.6 μm.
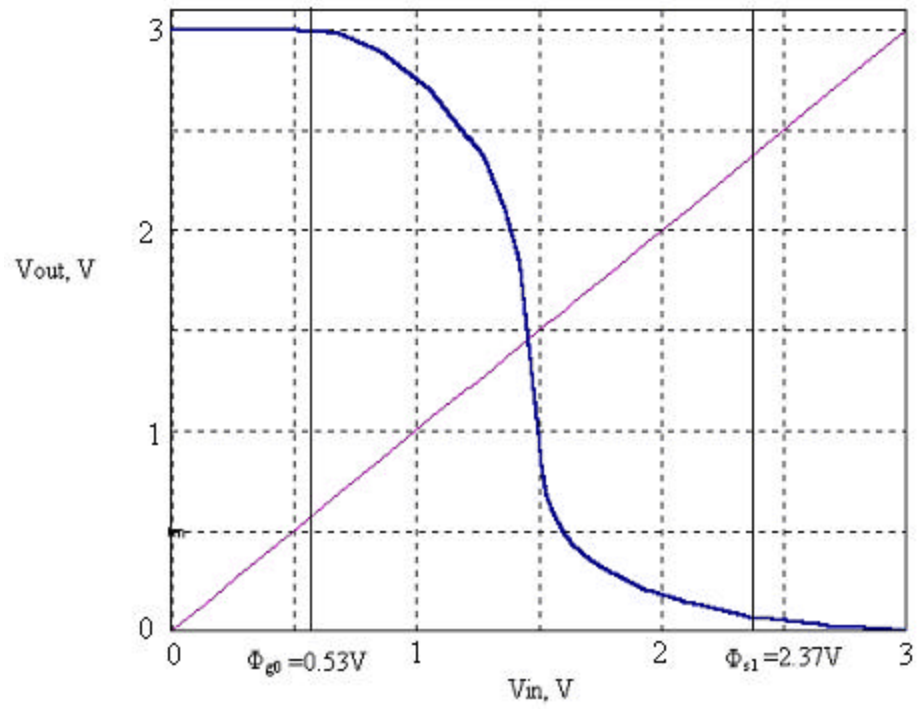
Fig. 4.2: Voltage transfer characteristics of a CMOS inverter. (W/L= 16.0μm/1.6 μm).

We observe that Φ_t remains same for W_p/W_n = 8.0 μm/8.0 μm and W_p/W_n = 16.0 μm/16.0 μm. We obtain greater drive strength in the latter case.

The next step in design flow of floating gate circuits is drawing floating gate potential diagrams (FPD). The circuit has single quaternary input (V_{IN}) and two binary outputs, a MSB and a LSB. Using Table 4.1, the FPD for MSB and LSB are drawn. The design for the MSB is considered first. From Table 4.1, we observe that the MSB is logic LOW (0 V) for quaternary inputs 0 (0 V) and 1 (1 V) and is logic HIGH (3 V) for logic inputs 2 (2 V) and 3 (3 V). Hence the potential on the floating gate is to be below the switching threshold voltage for inputs 0 (0 V) and 1 (1 V) and above the switching threshold voltage for inputs 2 (2 V) and 3 (3 V). The FPD for the MSB is shown in Fig. 4.3. The switching threshold line is also shown in the figure.

From Fig. 4.3, the output MSB is designed with a single capacitor C_1 at the input of the floating gate CMOS inverter. Using equations (2.7-2.9), we obtain for quaternary input 0 (0 V),

$$\frac{0V \times C_1 + 3V \times C_{oxp}}{C_1 + C_{oxn} + C_{oxp} + C_p} < \Phi_t(1.45V). \tag{4.2}$$

For quaternary input 1 (1 V),

$$\frac{1V \times C_1 + 3V \times C_{oxp}}{C_1 + C_{oxn} + C_{oxp} + C_p} < \Phi_t(1.45V). \tag{4.3}$$

For quaternary input 2 (2 V),

$$\frac{2V \times C_1 + 3V \times C_{oxp}}{C_1 + C_{oxn} + C_{oxp} + C_p} > \Phi_t(1.45V). \tag{4.4}$$
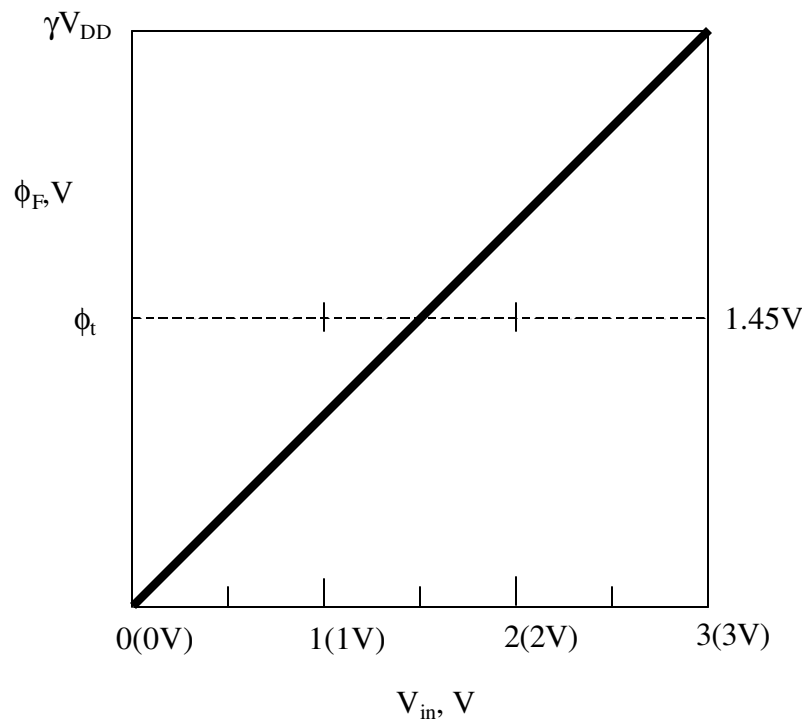
Fig. 4.3: Floating gate potential diagram for conversion of quaternary
to binary logic for MSB.

And for quaternary input 3 (3 V)

$$\frac{3V \times C_1 + 3V \times C_{oxp}}{C_1 + C_{oxn} + C_{oxp} + C_p} > \Phi_t (1.45V). \tag{4.5}$$

For W/L = 16.0 μm/1.6 μm, using equation (3.4) C_{ox} is given by,

$$C_{ox} = \frac{16.0 \mu m \times 1.6 \mu m \times 3.9 \times 8.854 F/cm}{300 \times 10^{-8} cm} \approx 30\,fF. \tag{4.6}$$

Taking layout constraints into consideration, as explained in Chapter 2, section 2.7, a unit capacitance of 500 fF is considered. Hence the capacitors in circuit design need to be in multiples of 500 fF. From layout extraction, a unit capacitance of 500 fF gives 40 fF of parasitic capacitance (C_{p1}).

$$\therefore C_p = \frac{40\,fF \times C_1}{500\,fF}. \tag{4.7}$$

Substituting the values of C_{oxn} (30 fF), C_{oxp} (30 fF) and C_p using equations (4.6) and (4.7) in equations (4.2), (4.3), (4.4) and (4.5), value of C_1 is obtained. The smallest value of C_1 that satisfies the above inequalities is 500 fF. Substituting the value of C_1 in equation (4.7), the value of C_p is found to be 40 fF. The voltage on floating gate is calculated and tabulated in Table 4.2. The output of MIFG CMOS inverter needs to be inverted to get required output as shown in Table 4.1. Hence a CMOS inverter #2 is introduced at the output of MIFG inverter, which inverts the output as well as buffers, the signal generated by MIFG inverter. The circuit for MSB is shown in Fig. 4.4.

4.3 Circuit Design of LSB

From Table 4.1, the LSB is LOW (0 V) for quaternary inputs 0 (0 V) and 2 (2V) and is HIGH (3 V) for inputs 1 (1 V) and 3 (3 V). Hence the potential on

Table 4.2 Voltage on floating gate of MSB for corresponding quaternary inputs (Φ_t = 1.45 V)

Quaternary Input	Voltage on Floating Gate (Φ_F), V	
0	0.15	$\Phi_F < \Phi t$
1	0.983	$\Phi_F < \Phi t$
2	1.816	$\Phi_F > \Phi t$
3	2.65	$\Phi_F > \Phi t$

V_DD

W/L=16.0 μm/1.6 μm

#1

C_1
500 fF

V_{IN}

#2

MSB

C_L
0.1 pF

W/L=16.0 μm/1.6 μm

V_{SS}
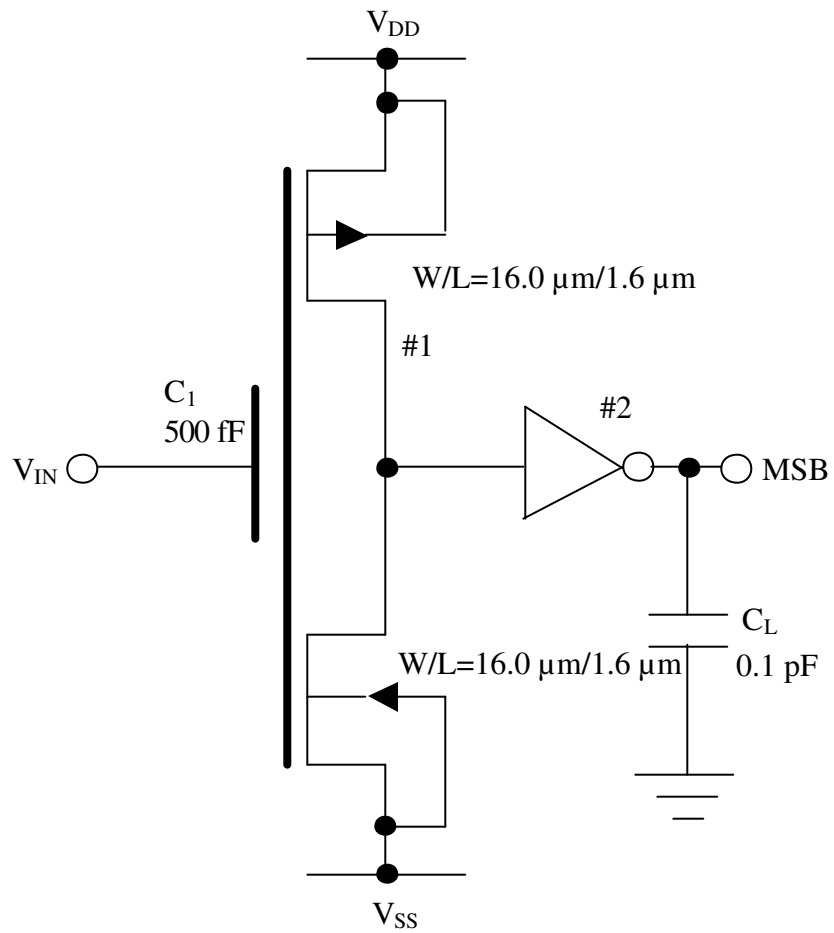
Fig. 4.4: Circuit diagram for implementation of quaternary to binary logic (MSB) using floating gate MOSFETs.

floating gate should be below the switching threshold voltage for inputs 0 (0 V) and 2 (2 V) and above the switching threshold voltage for inputs 1 (1 V) and 3 (3 V). The FPD for LSB is shown in Fig. 4.5. We observe that the voltage on floating gate falls below switching threshold voltage for input 2 (2 V). A pre-input gate inverter stage (#3) is required to control the voltage on floating gate, such that the output of the pre-input inverter stage goes LOW (0 V) for inputs 2 (2 V) and 3 (3 V). Fig. 4.6 shows the circuit diagram for LSB output. The capacitors C_2 and C_3 are the input capacitors for the MIFG inverter. Capacitor C_3 is controlled by quaternary input and capacitor C_2 is controlled by output of pre-input gate inverter stage. The voltage on floating gate of MIFG inverter is given by equation (2.9),

$$\Phi_F = \frac{V_{IN} \times C_3 + V_3 \times C_2 + 3V \times C_{oxp}}{C_2 + C_3 + C_{oxn} + C_{oxp} + C_p}. \tag{4.8}$$

Again using equations (2.7-2.9) the inequalities for four quaternary inputs can be obtained. For quaternary input 0 (0 V),

$$\frac{0V \times C_3 + 3V \times C_2 + 3V \times C_{oxp}}{C_2 + C_3 + C_{oxp} + C_{oxn} + C_p} < \Phi_{inv}(1.45V). \tag{4.9}$$

For quaternary input 1 (1 V),

$$\frac{1V \times C_3 + 3V \times C_2 + 3V \times C_{oxp}}{C_2 + C_3 + C_{oxp} + C_{oxn} + C_p} > \Phi_{inv}(1.45V). \tag{4.10}$$

For quaternary input 2 (2 V),

$$\frac{2V \times C_3 + 0V \times C_2 + 3V \times C_{oxp}}{C_2 + C_3 + C_{oxp} + C_{oxn} + C_p} < \Phi_{inv}(1.45V) \tag{4.11}$$

For quaternary input 3 (3 V),
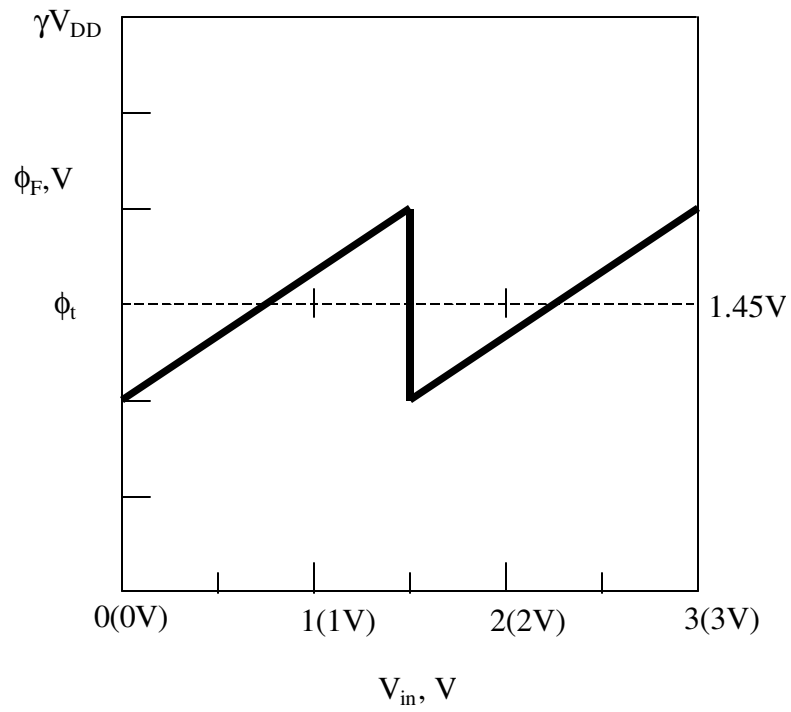
Fig. 4.5: Floating gate potential diagram for conversion of quaternary to binary logic for LSB.
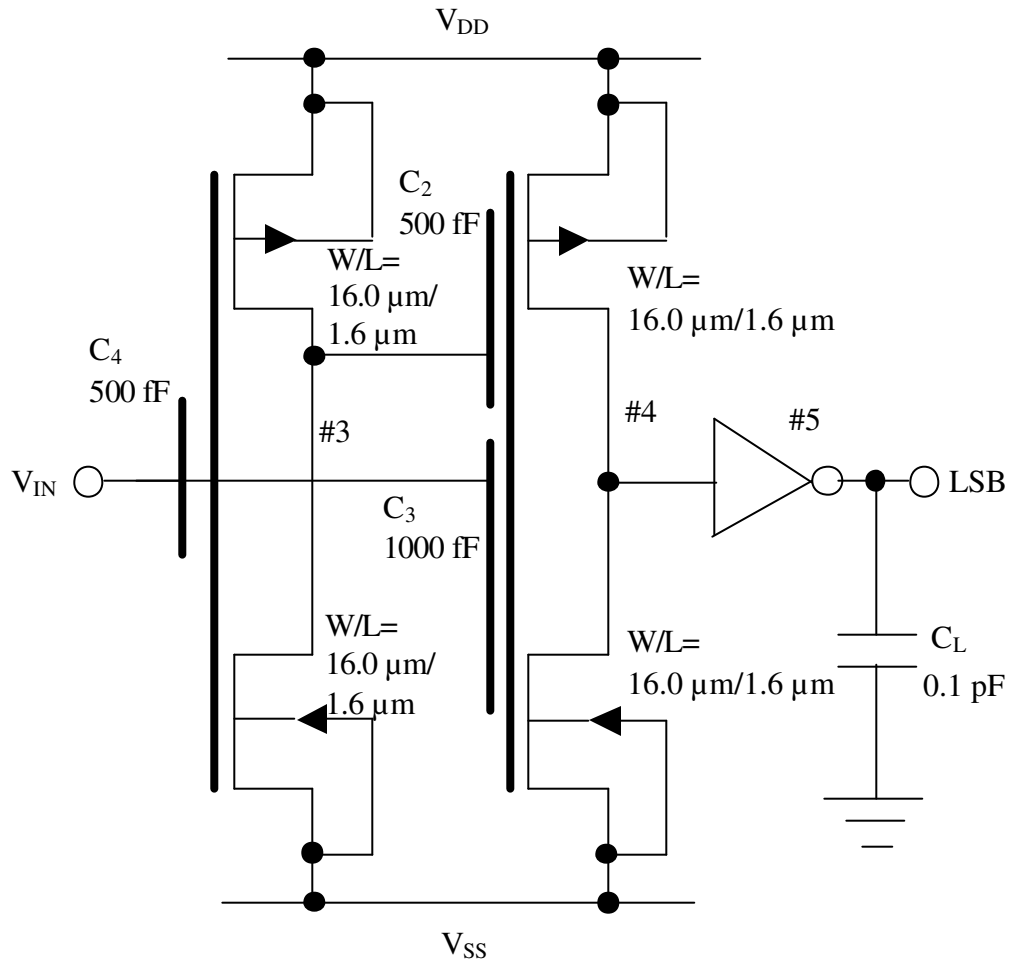
Fig. 4.6: Circuit diagram for implementation of quaternary logic to binary logic (LSB) using floating gate MOSFETs.

$$\frac{3V \times C_3 + 0V \times C_2 + 3V \times C_{oxp}}{C_2 + C_3 + C_{oxp} + C_{oxn} + C_p} > \Phi_{inv}(1.45V). \tag{4.12}$$

Again 500 fF of unit capacitance gives 40 fF of parasitic capacitance (C_{p1}). The value of C_p is given by,

$$\therefore C_p = \frac{40fF \times (C_2 + C_3)}{500fF}. \tag{4.13}$$

Substitute the value of C_{oxn} (30 fF), C_{oxp} (30 fF) and C_p using equations (4.6) and (4.13) in equations (4.9), (4.10), (4.11) and (4.12) to obtain the values of C_2 and C_3. For the above inequalities to satisfy, the value of capacitor C_3 should be more than the value of capacitor C_2. Plug in the values for C_2 and C_3, which are multiples of 500 fF. Capacitors C_2 and C_3 are found to be 500 fF and 1000 fF, which satisfy the above inequalities. Substituting the value of C_2 and C_3 in equation (4.13), the value of C_p is found to be 120 fF. The voltage on floating gate is calculated and tabulated in Table 4.3. The output of MIFG CMOS inverter (#4) needs to be inverted to get the required output as shown in the Table 4.1. Hence a CMOS inverter #5 is introduced at the output of MIFG CMOS inverter.

4.3.1 Circuit Design for #3 Stage

The pre-input inverter stage (#3) in Fig. 4.6 controlling the capacitor C_2 is to be designed such that the output of the inverter stage is HIGH (3 V) for inputs 0 (0 V) and 1 (1 V) and is LOW (0 V) for inputs 2 (2 V) and 3 (3 V). Using equations (2.7-2.9) the inequalities for (#3) inverter stage are obtained. For quaternary input 0

$$\frac{0V \times C_4 + 3V \times C_{oxp}}{C_4 + C_{oxn} + C_{oxp} + C_p} < \Phi_{inv}(1.45V). \tag{4.14}$$

For quaternary input 1 (1 V),

Table 4.3 Voltage on floating gate of LSB for corresponding
quaternary inputs (Φ_t = 1.45 V)

Quaternary Input	Output of #3	Voltage on Floating Gate (Φ_F),V	
0	HIGH (3 V)	0.964	$\Phi_F < \Phi_t$
1	HIGH (3 V)	1.541	$\Phi_F > \Phi_t$
2	LOW (0 V)	1.244	$\Phi_F < \Phi_t$
3	LOW (0 V)	1.839	$\Phi_F > \Phi_t$

$$\frac{1V \times C_4 + 3V \times C_{oxp}}{C_4 + C_{oxn} + C_{oxp} + C_p} < \Phi_{inv}(1.45V). \tag{4.15}$$

For quaternary input 2 (2 V),

$$\frac{2V \times C_4 + 3V \times C_{oxp}}{C_4 + C_{oxn} + C_{oxp} + C_p} > \Phi_{inv}(1.45V). \tag{4.16}$$

And for quaternary input 3 (3 V),

$$\frac{3V \times C_4 + 3V \times C_{oxp}}{C_4 + C_{oxn} + C_{oxp} + C_p} > \Phi_{inv}(1.45V). \tag{4.17}$$

The value of C_p is given by,

$$C_p = \frac{40\,fF \times C_4}{500\,fF}. \tag{4.18}$$

For the above inequalities to satisfy, the value of C_4 is 500 fF. The circuit for the LSB using MIFG inverters is shown in Fig. 4.6. The pre-input inverter stage (#3) for the LSB is observed to be same as the MIFG inverter (#1) in MSB circuit. Hence the output of MIFG inverter of MSB can be used to control the capacitor C_2 instead of a pre-input inverter stage. The resulting circuit with MSB and LSB is shown in Fig. 4.7. The conversion circuit shown in Fig. 4.7 has a total of eight transistors, four MIFG transistors and four CMOS transistors. An approximate of 75% reduction in transistor count is obtained, when compared to previous circuits found in literature [15,16,18].

4.4 Simulation Results

The circuits are simulated for 1.5 μm technology with BSIM3 model parameters obtained from MOSIS. The MOS model parameters used for nMOS and pMOS transistors are listed in Appendix B. The circuits are initially simulated to
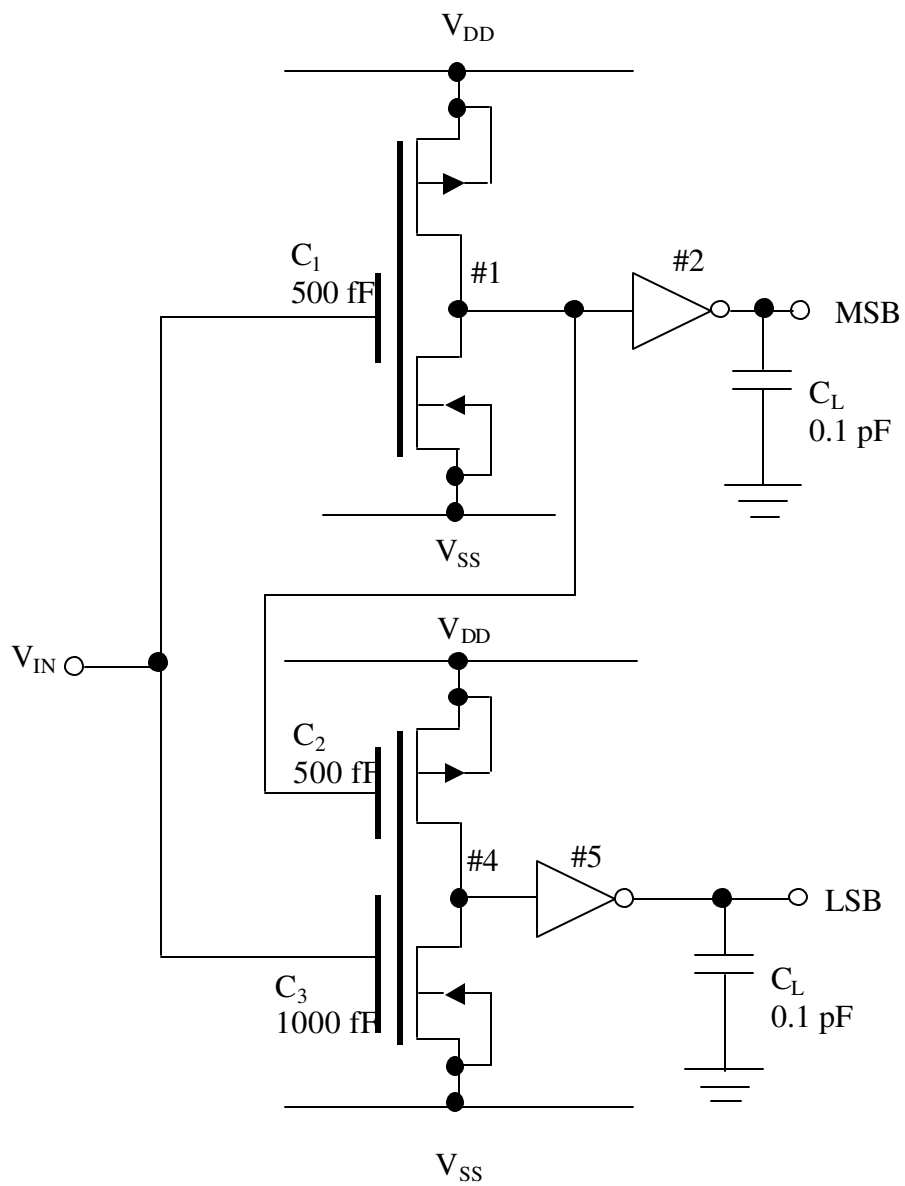
Fig. 4.7: Circuit diagram for implementing conversion of quaternary logic to binary logic using floating gate MOSFETs.

verify proper functionality of the circuit. A ramp input from 0 V to 3 V is given as input to the circuit. The output of MSB and LSB are shown in Figs. 4.8 and 4.9. The voltage on floating gate of MSB and LSB are shown in Figs. 4.10 and 4.11. The circuit is verified for all possible transitions of quaternary input [18]. A piece-wise-linear voltage source with 0.1 ns rise and fall time with 40 ns pulse width is given at input of the circuit. The output of MSB and LSB is shown in Fig. 4.12. The physical design for the circuit in Fig. 4.7 is shown in Fig. 4.13. The layout occupies an area of $130 \times 175 \ \mu m^2$. The post-layout simulation includes the extracted parasitic capacitances and a load capacitance of 0.1 pF is added at the output. The post-layout simulation output is shown in Fig. 4.14. The propagation delay is measured from 50 percent point of input to 50 percent point of output. For example, when input transits from logic 2 (2 V) to 3 (3 V), the delay is considered from 50 percent between 2 (2 V) and 3 (3 V) i.e. 2.5V (2 V + 0.5×(3 V-2 V) = 2.5 V) to 50 percent of output i.e. at 1.5 V. Table 4.4 provides the propagation delays. The worst-case delay of t_{pLH} ~ 6 ns for input transitions 2(2 V) $\rightarrow$ 1(1 V) and t_{pHL} ~ 5 ns for input transition of 1(1 V) $\rightarrow$ 2(2 V) are noted. Few columns in Table 4.4 are not filled; this is accounts for no change in the output of circuit for the given change in input. The present work is compared with previous works [15,16,18], to date and is summarized in Table 4.5. The worst-case value of unit capacitance due to discrepancies in the fabrication is 365 fF. The circuit was simulated with unit capacitance of 365 fF and the outputs are shown in Fig. 4.15. The capacitance formed between floating gate and substrate on field oxide was estimated and taken into account in pre-layout simulations.
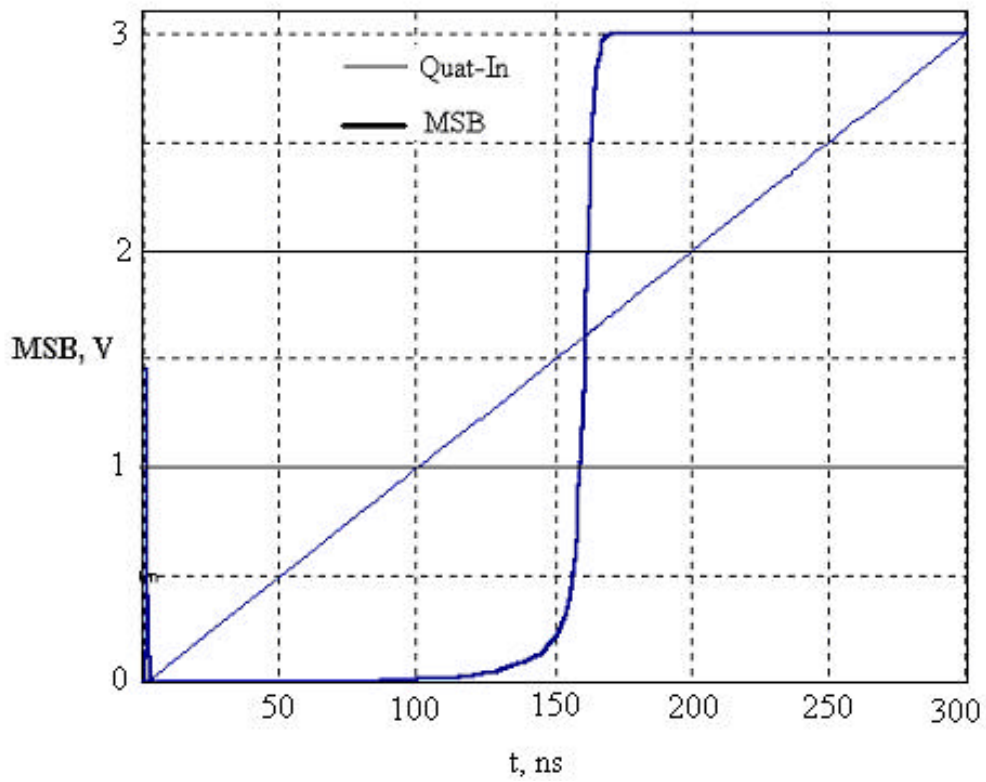
Fig. 4.8: Quaternary input and SPICE simulated output (MSB) for the circuit in Fig. 4.4.
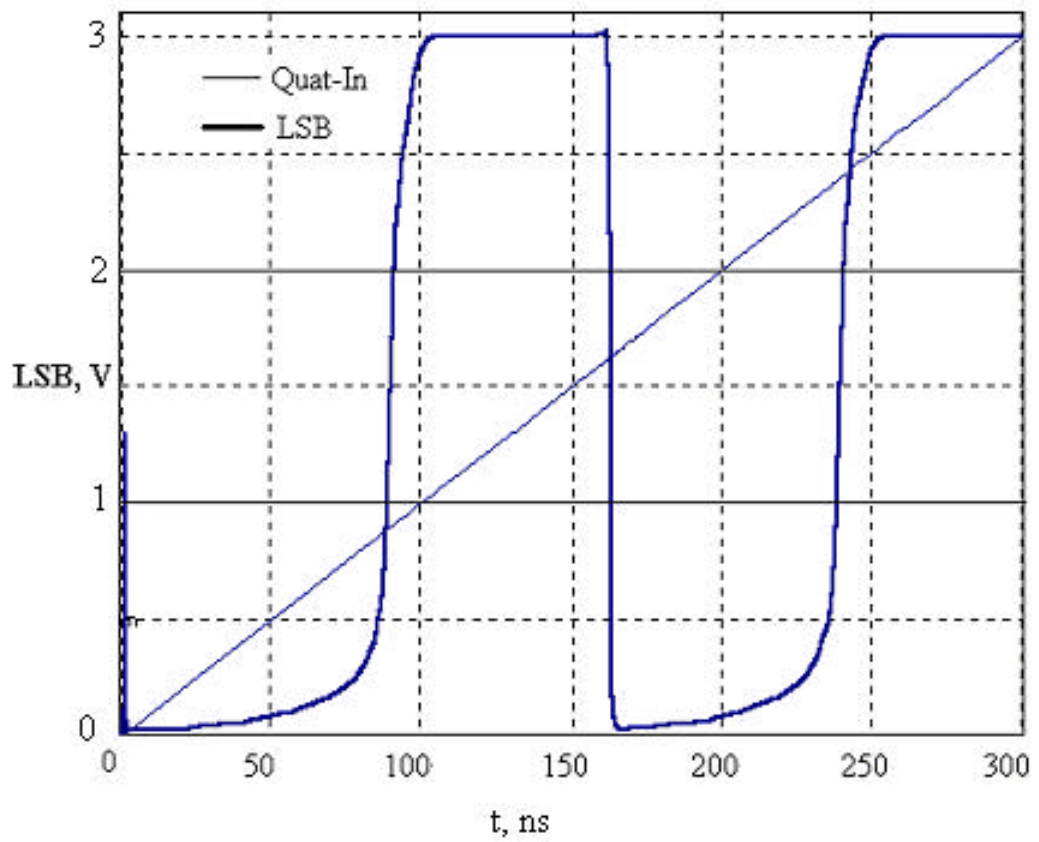
Fig. 4.9: Quaternary input and SPICE simulated output (LSB) for the circuit in Fig. 4.6.
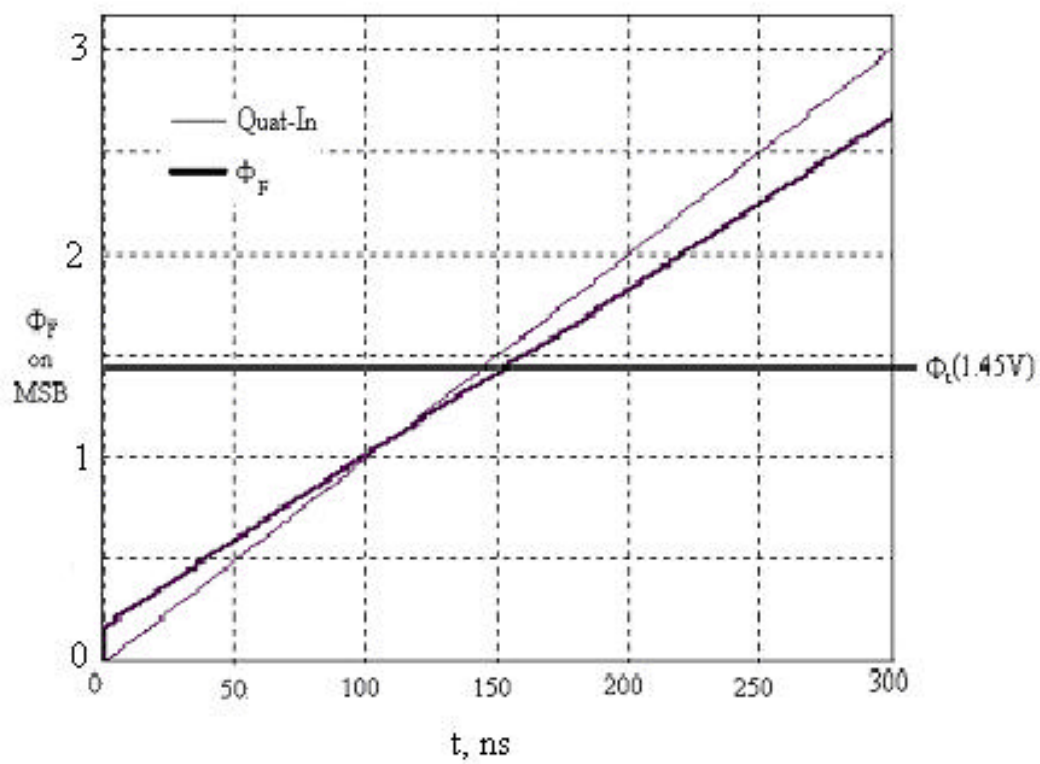
Fig. 4.10: Voltage on floating gate of MSB in Fig. 4.4 from SPICE simulations.
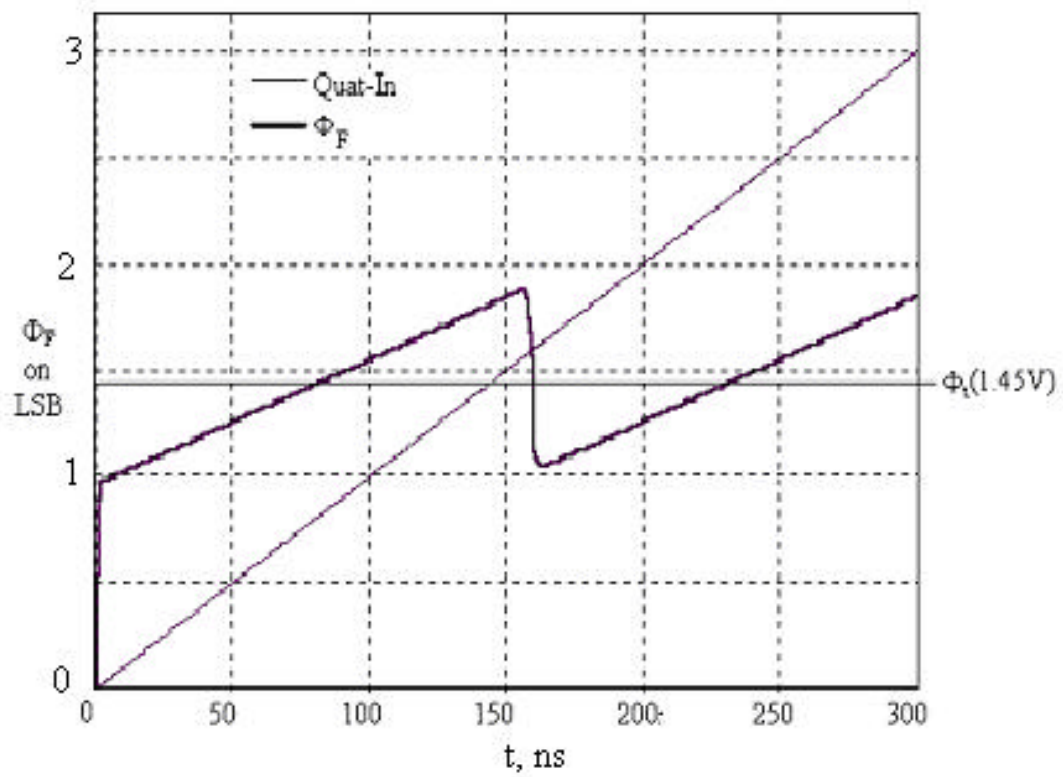
Fig. 4.11: Voltage on floating gate of LSB of Fig. 4.6 from SPICE simulations.
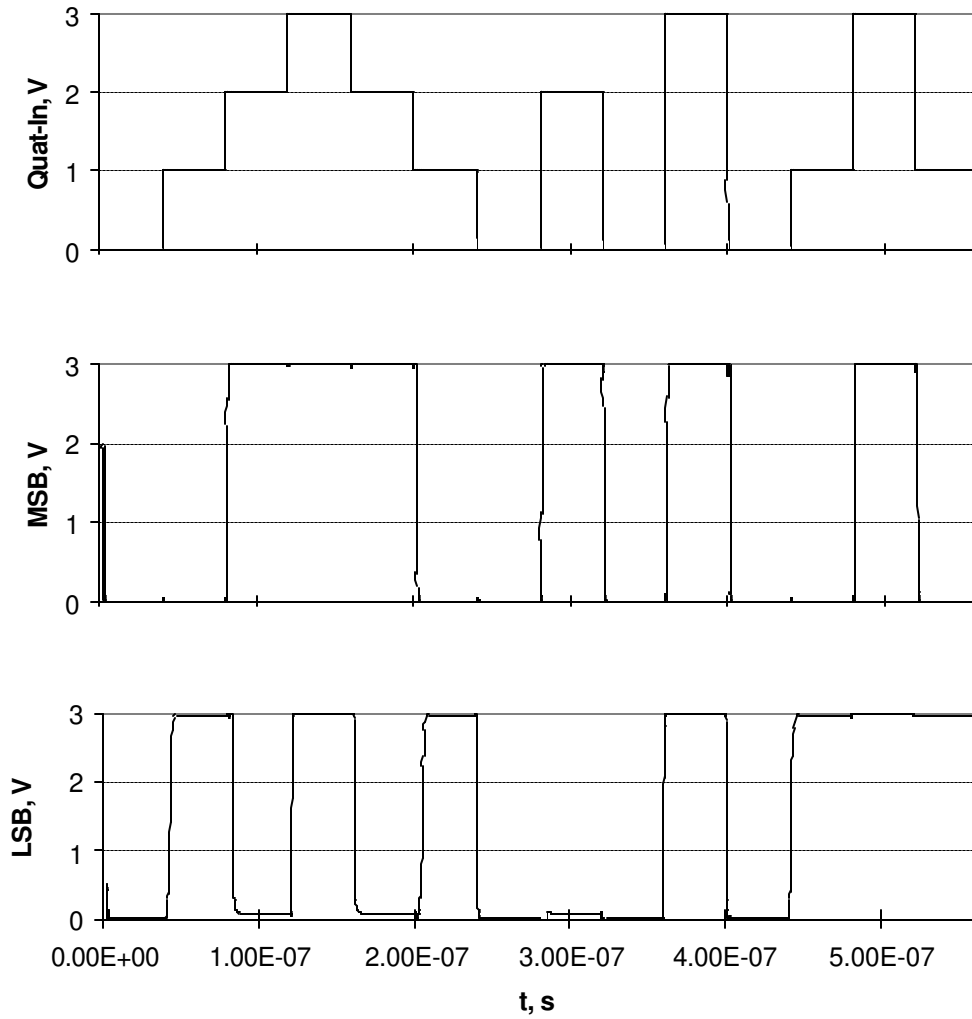
Fig. 4.12: Pre-layout SPICE simulated output of circuit in Fig. 4.7 for all possible combinations of quaternary input.
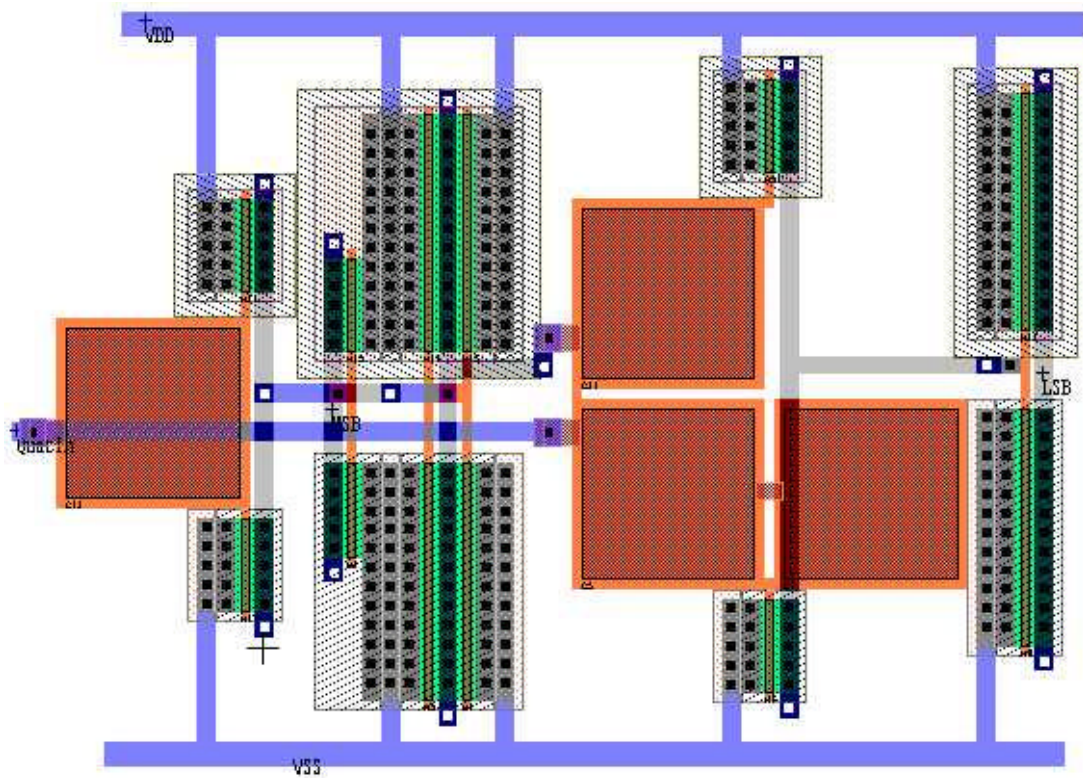
Fig. 4.13: Physical design of the conversion circuit from quaternary logic to binary logic shown in Fig. 4.7.
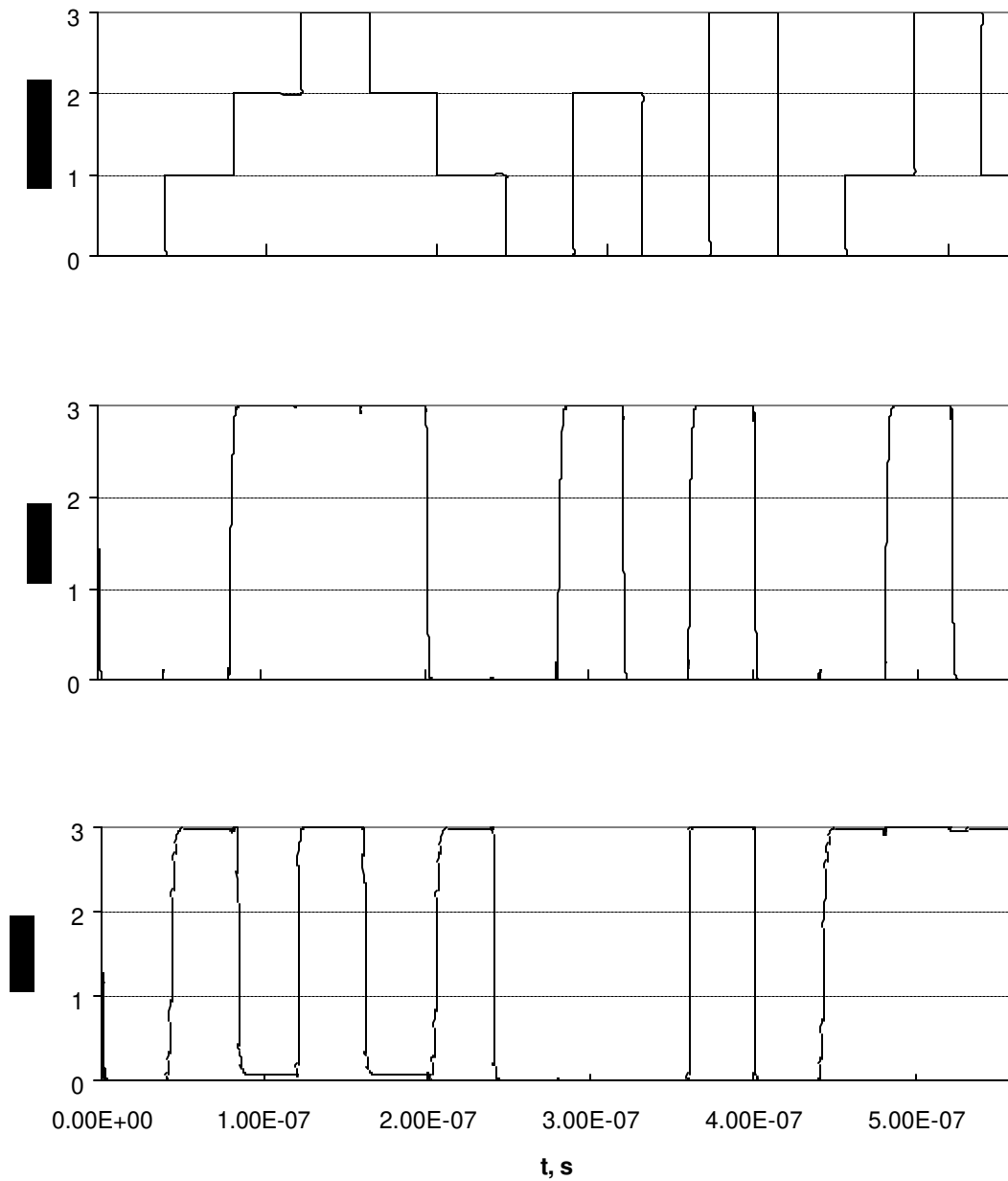
Fig. 4.14: Quaternary input and post layout outputs with 0.1 pF load capacitance.

Table 4.4: Propagation delay time for the layout of Fig. 4.13 with 0.1 pF load capacitance

Logic Level Transition (Quaternary Logic)	MSB (ns)	LSB (ns)
$0 \rightarrow 1$	-	3.46
$1 \rightarrow 2$	1.92	4.97
$2 \rightarrow 3$	-	1.19
$3 \rightarrow 2$	-	2.10
$2 \rightarrow 1$	1.52	6.02
$1 \rightarrow 0$	-	1.02
$0 \rightarrow 2$	2.03	-
$2 \rightarrow 0$	1.14	-
$0 \rightarrow 3$	1.51	0.70
$3 \rightarrow 0$	1.22	0.85
$0 \rightarrow 1$	-	3.45
$1 \rightarrow 3$	1.43	-
$3 \rightarrow 1$	1.63	-

Table 4.5 Comparison of the performance of the present and earlier works

Subject for comparison	Ref. [15]	Ref. [16]	Ref. [18]	Present
CMOS Technology	2µm	-	0.7µm	1.5µm
Voltage Supply	6 volts	5 volts	3 volts	3 volts
Number of V_{th}	1	1	2	1
Transistor Count	28 (30)	30	26	8
Delay in ns (worst case)	36 (13) 0.1pF load	3.8 on-chip	7.9 0.1pF load	6 0.1pF load
Radix	r=4	r=4	r=2^k	r=2^k
Circuit mode	Voltage	Voltage	Voltage	Voltage
Layout Area	-	-	-	$130 \times 175 \mu m^2$
Static power	Yes	Yes	No	Yes

Note: V_{th} is threshold voltage of a transistor.
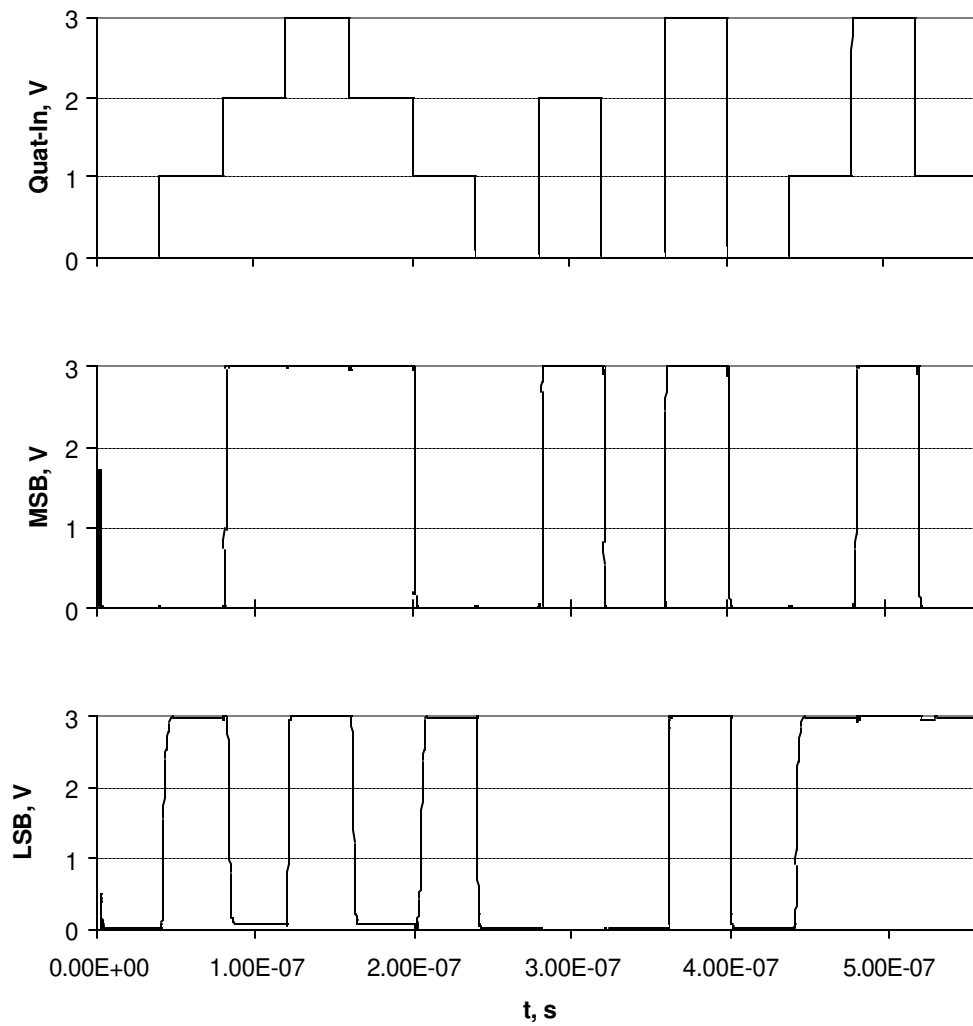
Fig. 4.15: SPICE simulated output of circuit in Fig. 4.7 for all possible combinations of quaternary input (unit capacitance = 365 fF)

4.5   Experimental Results

The design was fabricated in AMI 1.5 µm CMOS process. Fig. 4.16 shows a photomicrograph of the chip. The MOS model parameters of the fabricated chip are obtained from the MOSIS (T1AZ) and are listed in Appendix D. The voltage transfer characteristic of CMOS inverter shown in Fig. 4.1 is simulated with fabricated MOS model parameters and is shown in Fig. 4.17. The value of Φ_{g0} (0.66V) and Φ_{s1} (1.64 V) are obtained from voltage transfer characteristics. The switching threshold voltage (Φ_t) of CMOS inverter is obtained using equation (2.7),

$$\Phi_t = \frac{0.66V + 1.64V}{2} = 1.15V. \tag{4.19}$$

The simulation value of 1.15 V agrees with experimental value of 1.1 V. While the switching threshold voltage with MOS model parameters used for the design is 1.45V (refer equation (4.1)). The voltage on floating gate (Φ_F) of MSB and LSB obtained using equations (4.2- 4.5) and (4.9-4.12) are compared with Φ_t (1.15 V) and tabulated in Tables 4.6 and 4.7, respectively. It is found that for logic 2 (2 V) input, the inequality in equation (4.11) does not satisfy. Φ_F should be less than Φ_t not greater than Φ_t. The extracted design from the layout with parasitic capacitances is resimulated with BSIM3 MOS model parameters of the fabricated design. The simulation output of MSB and LSB for a ramp input of 0 V to 3 V is shown in Fig. 4.18 and Fig. 4.19. The simulation output shows incorrect output at LSB for logic 2 (2 V), which should be LOW instead of HIGH. The fabricated chip is tested for input ranging from 0 V to 3 V and measured values are tabulated.

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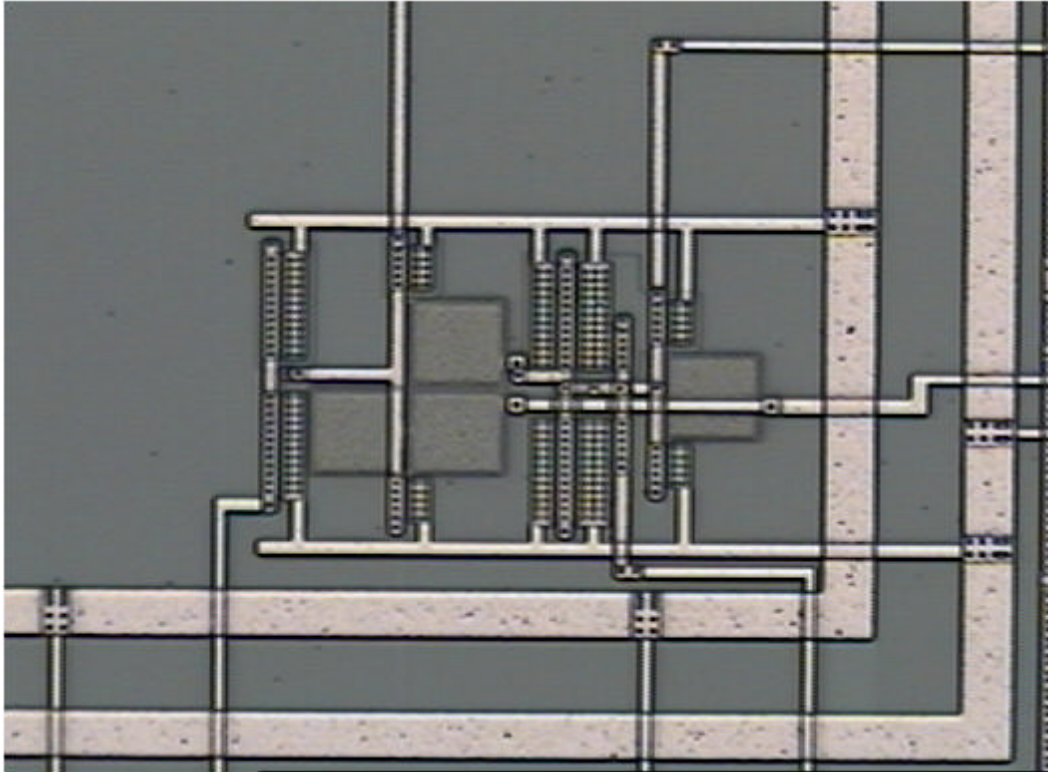
Fig. 4.16: Photomicrograph of chip fabricated by MOSIS in standard double-polysilicon CMOS process.
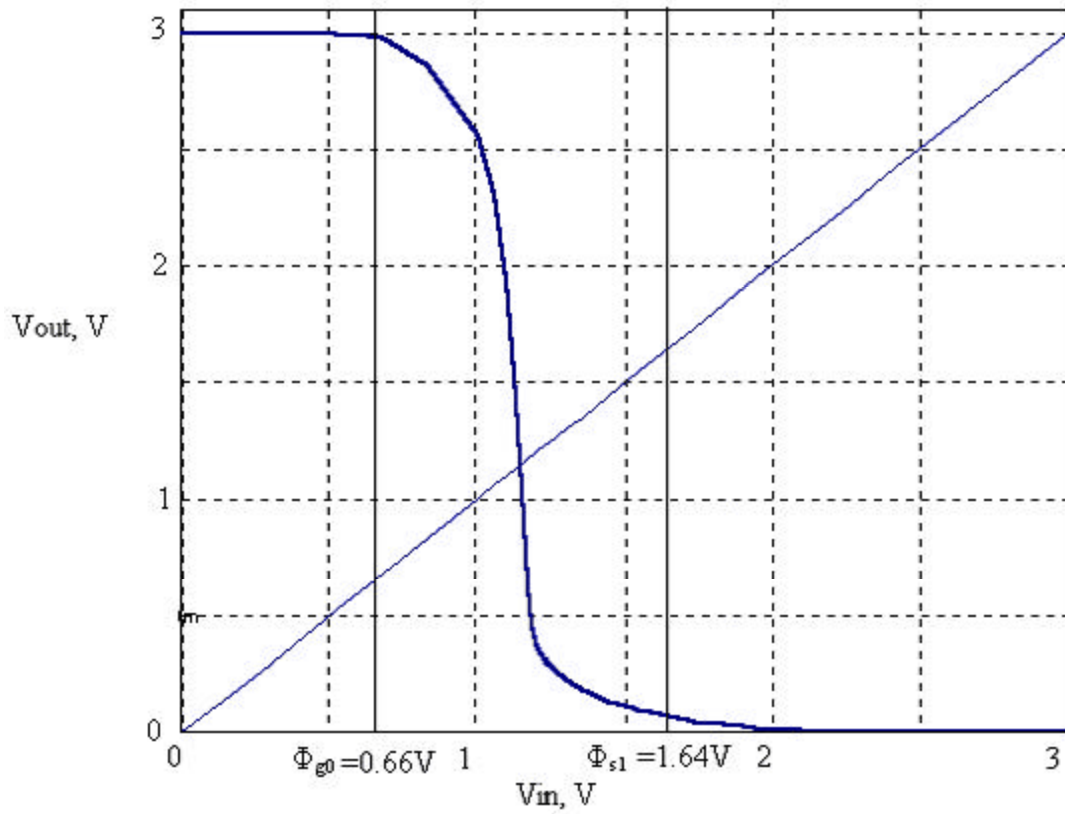
Fig. 4.17: Voltage transfer characteristics of a CMOS inverter with W/L = 16 μm/1.6 μm with MOS model parameters of a fabricated design.
Note: $\Phi_{g0} = 0.66$ V and $\Phi_{s1} = 1.64$ V.

Table 4.6: Voltage on floating gate of MSB for corresponding quaternary inputs (Φ_t= 1.15 V)

Quaternary Input	Voltage on Floating Gate (Φ_F), V	
0	0.15	$\Phi_F < \Phi_t$
1	0.98	$\Phi_F < \Phi_t$
2	1.82	$\Phi_F > \Phi_t$
3	2.65	$\Phi_F > \Phi_t$

Table 4.7: Voltage on floating gate of LSB for corresponding quaternary inputs ($\Phi_t = 1.15$ V)

Quaternary Input	Output of #1	Voltage on Floating Gate (Φ_F), V	
0	HIGH (3 V)	0.96	$\Phi_F < \Phi_t$
1	HIGH (3 V)	1.54	$\Phi_F > \Phi_t$
2	LOW (0 V)	1.25	$\Phi_F > \Phi_t$
3	LOW (0 V)	1.84	$\Phi_F > \Phi_t$
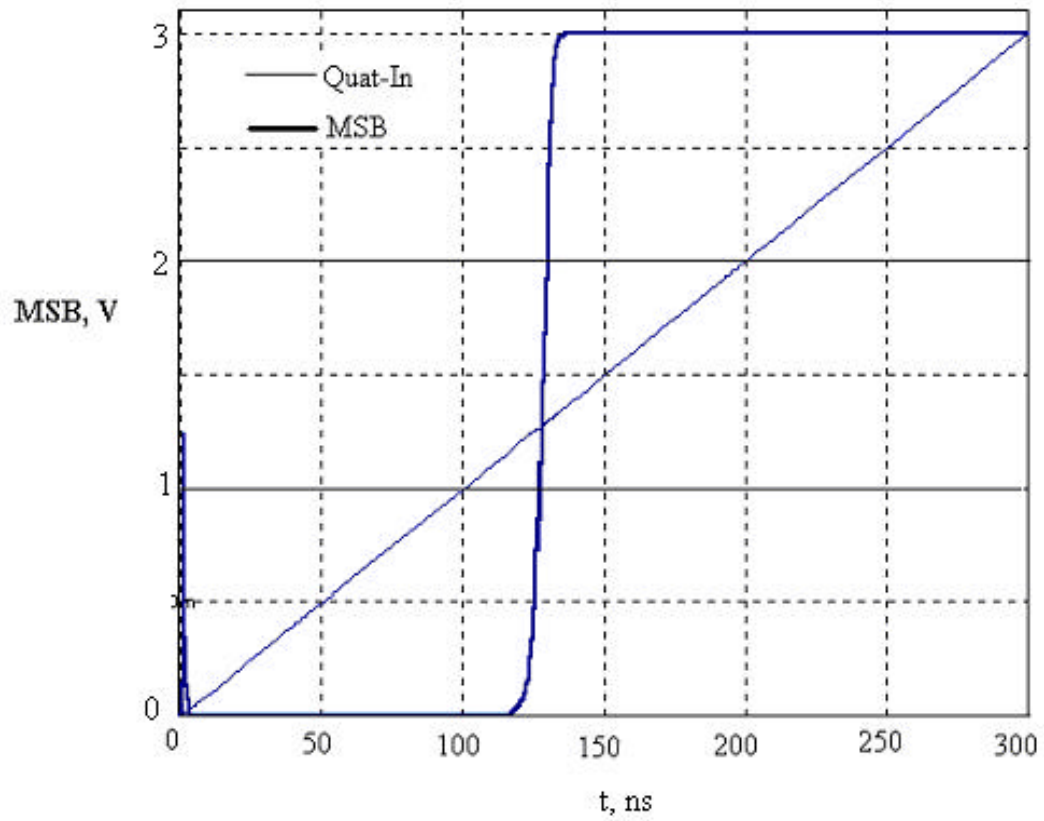
Fig. 4.18. Quaternary input and SPICE simulated output (MSB) for the circuit shown in Fig. 4.7 with MOS model parameters of the fabricated design.
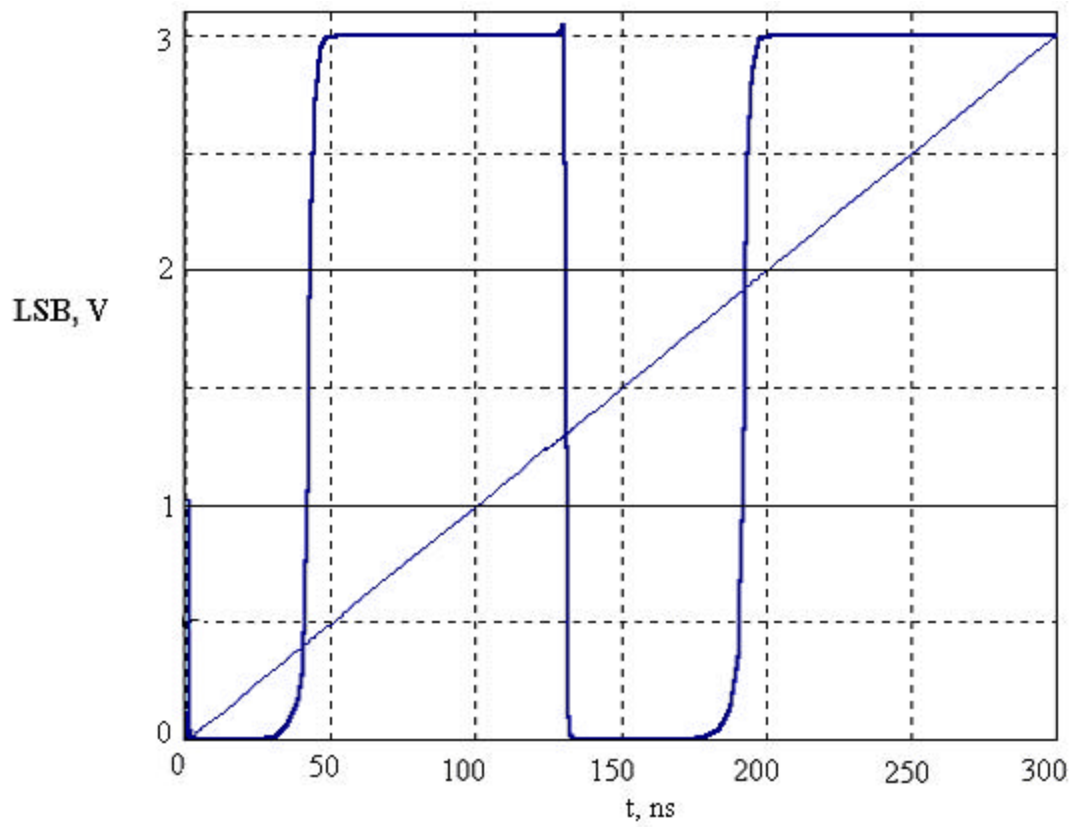
Fig. 4.19. Quaternary input and SPICE simulated output (LSB) for the circuit shown in Fig. 4.7 with MOS model parameters of the fabricated design.

Figure 4.20 shows the experimental results from oscilloscope. The measured values are compared with simulated data with MOS model parameters used for design, MOS model parameters of fabricated chip and are summarized in Tables 4.8 and 4.9, respectively. Figures 4.21 and 4.22 shows the corresponding plots. From measured and simulated data we observe, the maximum voltage that has output corresponding to logic 2 is (1.6 V). Table 4.10 summarizes the voltages of the quaternary logic inputs that give appropriate binary output. With 1.6 V as logic 2, the design is re-simulated with MOS model parameters of fabricated chip for all possible transitions in input and is shown in Fig. 4.23 with 0.1 pF load capacitance. The layout extract is also re-simulated with 1.6 V as logic 2 and is shown in Fig. 4.24. The layout extract is simulated with MOS model parameters of fabricated chip for all possible transitions in input to compare simulated and measured propagation delay. A piece wise linear input with 5 ns rise and fall time and 1 us pulse width is given as input. A 15 pF load capacitance is added at the output as probe capacitance. The output drivers driving the pads are considered for simulations to obtain accurate results. The simulated output of MSB and LSB is shown in Fig. 4.25. The propagation delay of the simulated results from Fig. 4.25 is compared with measured values and is tabulated in Table 4.11.

Quat-In, V

MSB, V

LSB, V

t,μs
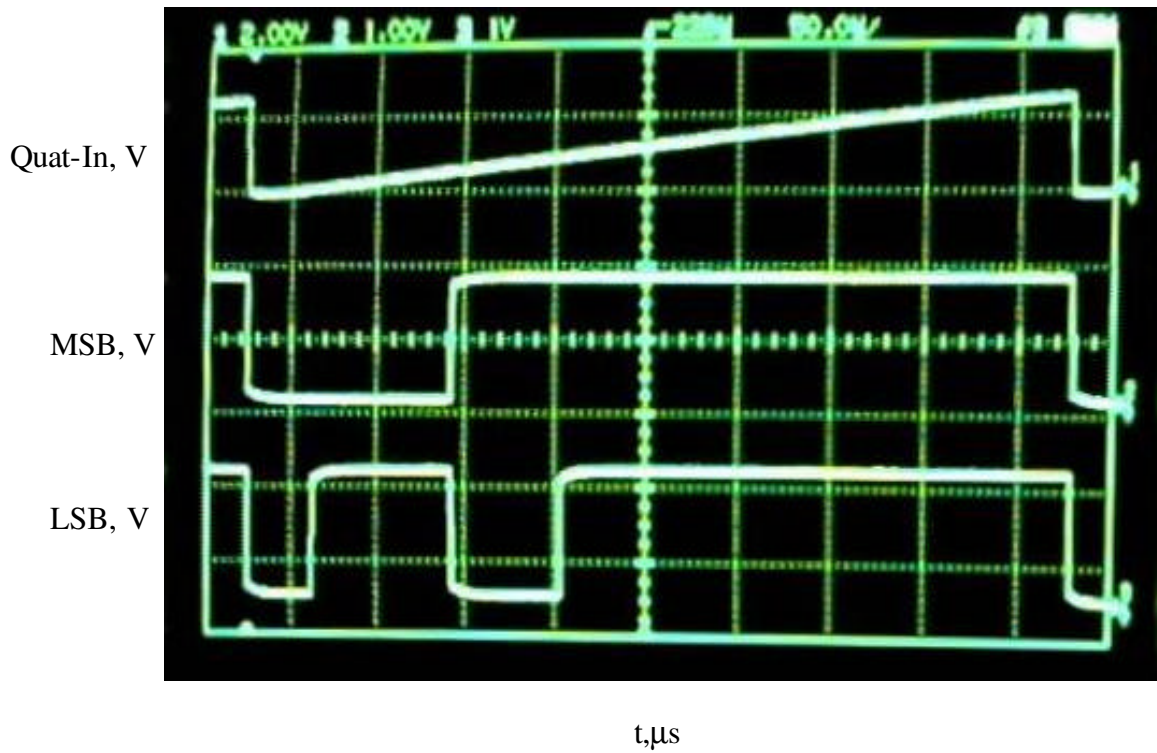
Figure 4.20: Decoder circuit transfer characteristics.

Table 4.8: Output at MSB is compared with simulation data with MOS model parameters used before and after fabrication and fabricated chip

Quaternary Input	Output voltage at MSB		
	Simulated (Design)	Simulated (Fabricated)	Measured
(V)	(V)	(V)	(V)
0.0	0.0	0.0	0.001
0.1	0.001	0.0	0.001
0.2	0.001	0.0	0.001
0.3	0.001	0.0	0.001
0.4	0.001	0.0	0.001
0.5	0.001	0.0	0.001
0.6	0.002	0.0	0.001
0.7	0.002	0.0	0.001
0.8	0.004	0.0	0.001
0.9	0.008	0.0	0.001
1.0	0.015	0.0	0.001
1.1	0.024	0.0	1.02
1.2	0.039	0.034	3.0
1.3	0.057	2.29	3.0
1.4	0.098	2.99	3.0
1.5	0.214	3.0	3.0
1.6	1.415	3.0	3.0
1.7	2.99	3.0	3.0
1.8	3.0	3.0	3.0
1.9	3.0	3.0	3.0
2.0	3.0	3.0	3.0
2.1	3.0	3.0	3.0
2.2	3.0	3.0	3.0
2.3	3.0	3.0	3.0
2.4	3.0	3.0	3.0
2.5	3.0	3.0	3.0
2.6	3.0	3.0	3.0
2.7	3.0	3.0	3.0
2.8	3.0	3.0	3.0
2.9	3.0	3.0	3.0
3.0	3.0	3.0	3.0

Table 4.9: Output at LSB is compared with simulation data with MOS model parameters used before and after fabrication and fabricated chip

Quaternary Input (V)	Output voltage at LSB		
	Simulated (Design) (V)	Simulated (Fabricated) (V)	Measured (V)
0.0	0.0	0.0	0.001
0.1	0.021	0.0	0.001
0.2	0.029	0.0	1.1
0.3	0.034	0.017	3.0
0.4	0.055	0.359	3.0
0.5	0.095	2.99	3.0
0.6	0.100	3.0	3.0
0.7	0.154	3.0	3.0
0.8	0.296	3.0	3.0
0.9	1.810	3.0	3.0
1.0	2.98	3.0	3.0
1.1	2.99	3.0	0.93
1.2	3.0	3.0	0.001
1.3	3.0	2.74	0.001
1.4	3.0	0.0	0.001
1.5	3.0	0.0	0.001
1.6	3.0	0.0	0.001
1.7	0.027	0.0	1.16
1.8	0.041	0.009	3.0
1.9	0.050	0.331	3.0
2.0	0.093	2.997	3.0
2.1	0.100	3.0	3.0
2.2	0.156	3.0	3.0
2.3	0.300	3.0	3.0
2.4	1.841	3.0	3.0
2.5	2.945	3.0	3.0
2.6	2.99	3.0	3.0
2.7	3.0	3.0	3.0
2.8	3.0	3.0	3.0
2.9	3.0	3.0	3.0
3.0	3.0	3.0	3.0
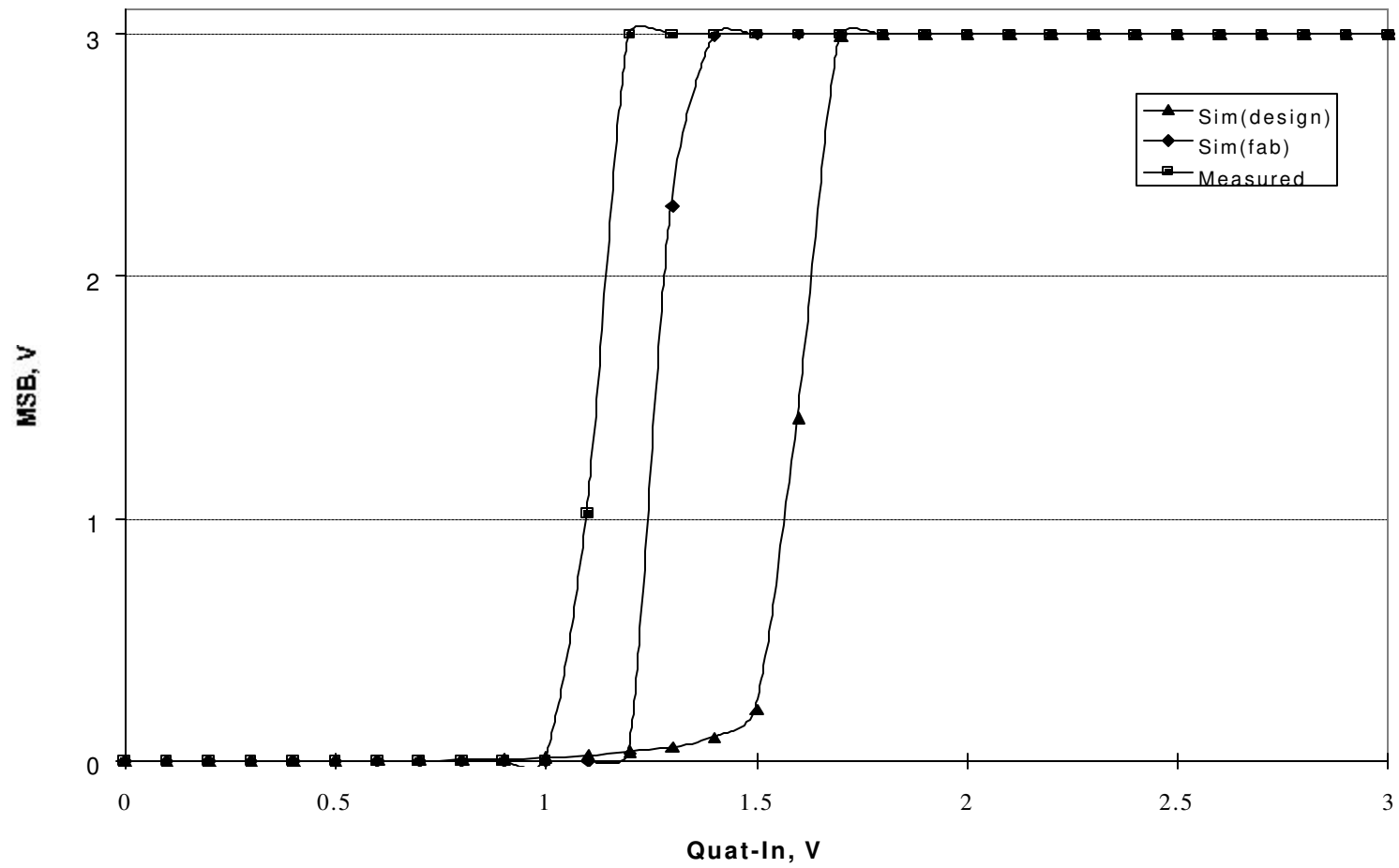
Fig. 4.21: Output MSB is compared with simulated output with MOS model parameters used for (a) design (b) fabricated (c) measured.
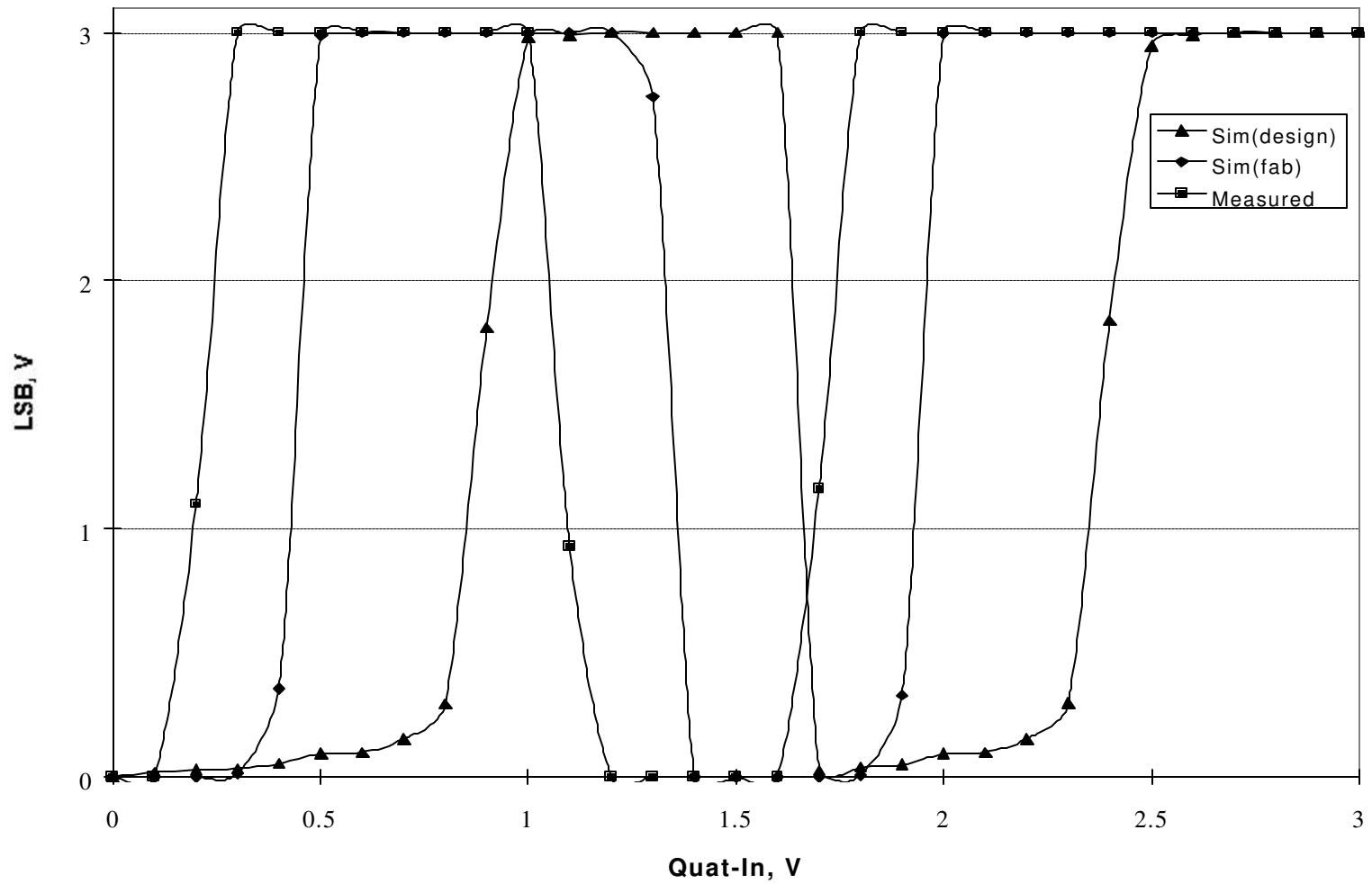
Fig. 4.22: Output LSB is compared with simulated output with MOS model parameters used for (a) design (b) fabricated (c) measured.

Table: 4.10: Summarizes the voltages of quaternary input for design and experiment

Quaternary Input (design) (V)	Quaternary Input (meas) (V)	MSB		LSB	
		simulated (V)	measured (V)	simulated (V)	measured (V)
0.0	0.0	0.0	0.001	0.0	0.0
1.0	1.0	0.01	0.001	3.0	3.0
2.0	1.6	3.0	3.0	0.09	0.001
3.0	3.0	3.0	3.0	3.0	3.0
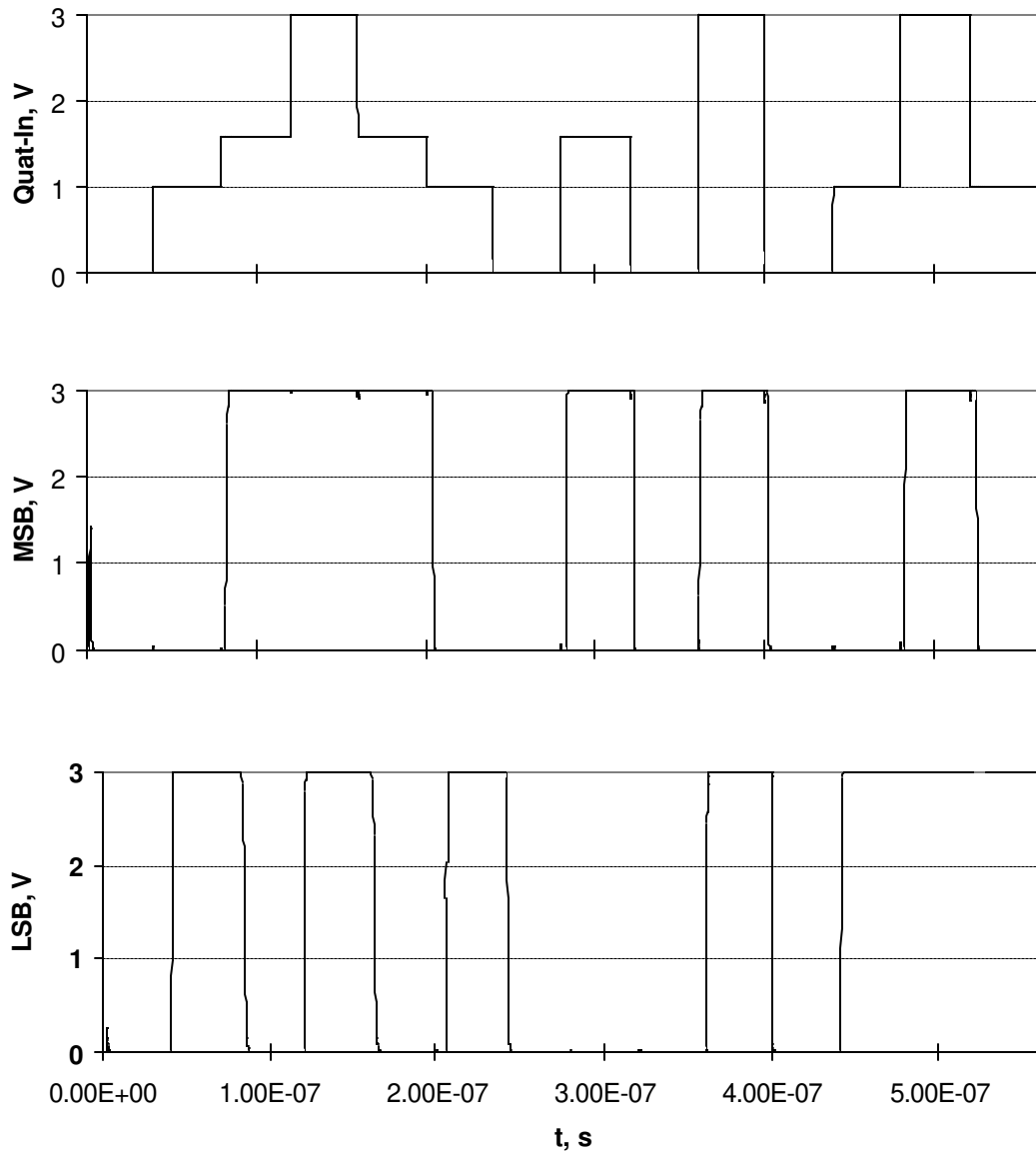
Fig. 4.23: SPICE simulated output of circuit in Fig. 4.7 for all possible combinations
of quaternary input with 0.1 pF load capacitance.
Note: (1) MOS model parameters used for simulation are that of fabricated chip
(2) Logic 2 used for simulation is 1.6 V.
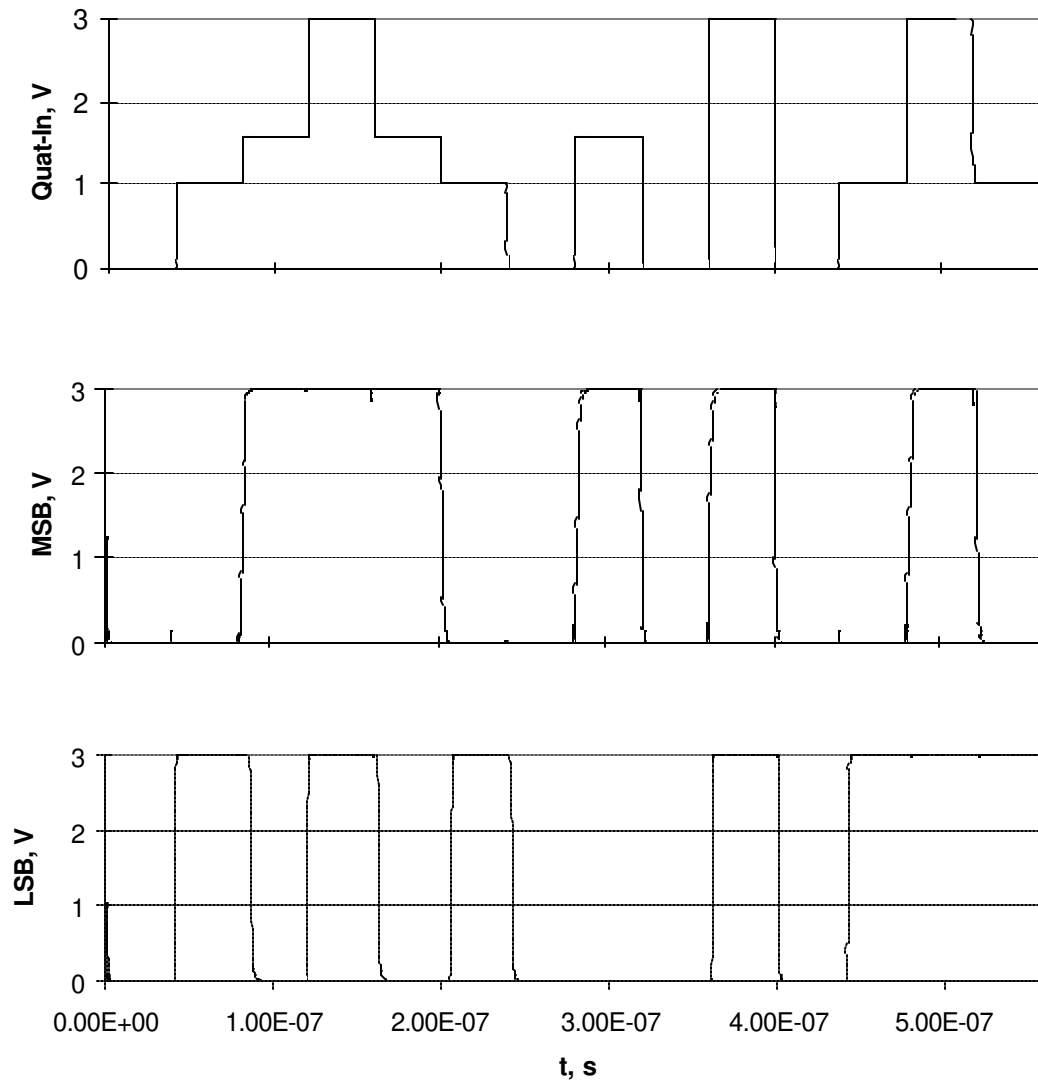
Fig. 4.24: Quaternary input and post layout outputs with 0.1 pF load capacitance.
Note: (1) MOS model parameters used for simulation are of fabricated chip
(2) Logic 2 used for simulation is 1.6 V.
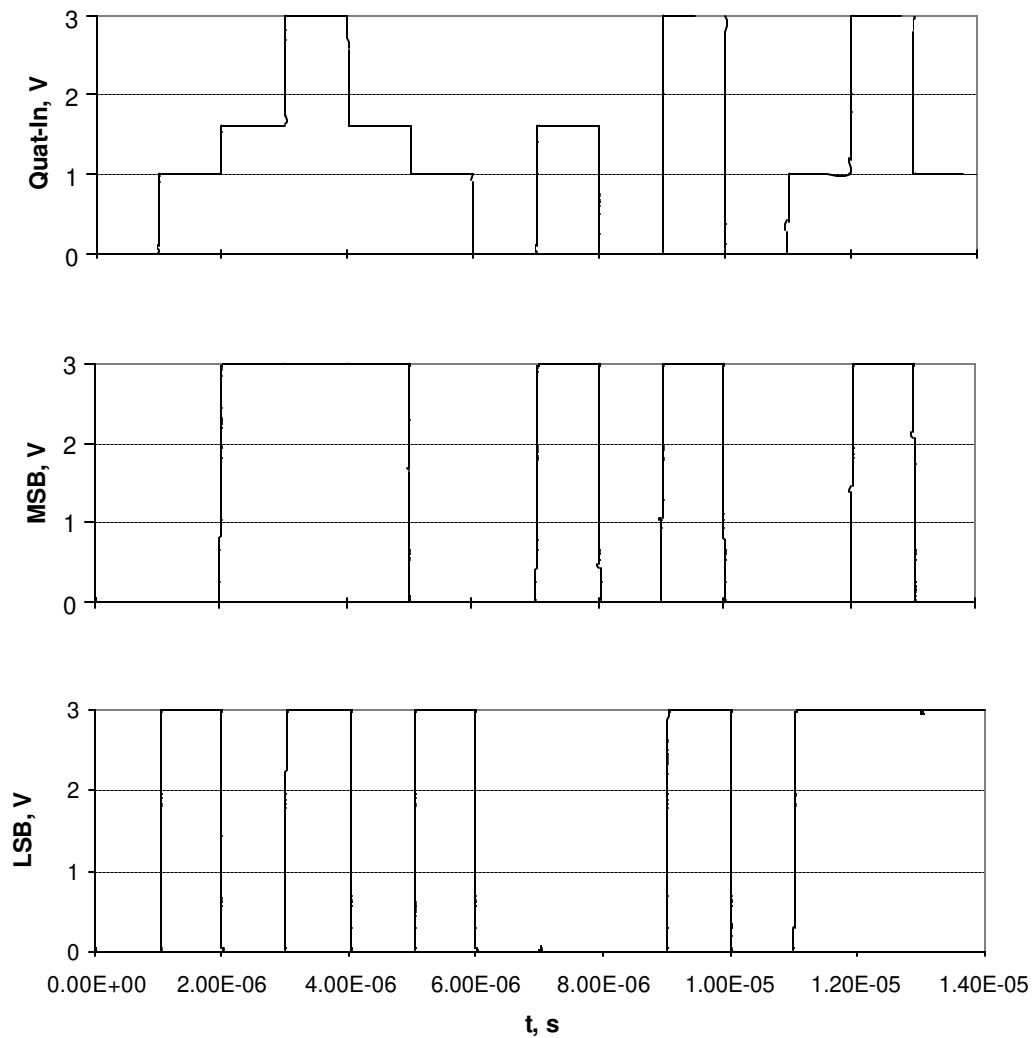
Fig. 4.25: Post layout simulation output with 15 pF load capacitance.
Note: (1) MOS model parameters used for simulation are of fabricated chip
(2) Logic 2 used for simulation is 1.6 V.

Table 4.11: Comparison of propagation delay time between simulation and measured values. Simulated results are on fabricated device

Logic Level Transition Quaternary Logic	MSB		LSB	
	Simulation (ns)	Measured (ns)	Simulation (ns)	Measured (ns)
0→1	-	-	11	13
1→2	11	12	13	-
2→3	-	-	9	10
3→2	-	-	12	15
2→1	11	10	17	20
1→0	-	-	10	11
0→2	12	14	-	-
2→0	8	9	-	-
0→3	11	12	8	9
3→0	8	10	7	9
0→1	-	-	11	13
1→3	11	12	-	-
3→1	10	11	-	-

Chapter 5

Conclusion and Future Work

An integrated circuit design is presented for the conversion of ternary bits into binary bits using multiple-input floating gate MOSFETs. The floating potential diagrams have been used to design different building blocks of the conversion circuit. The principle of MIFG transistor, calculating weighted sum of all inputs at gate level and switching transistor ON or OFF depending upon calculated voltage greater than or less than switching threshold voltage is utilized. The full integrated circuit is designed and simulated in standard 1.5 μm digital CMOS technology. The circuits are simulated in SPICE with MOSIS BSIM3 model parameters. The physical layout for the circuits is drawn using L-EDIT version 8.2. The post layout simulations included interlayer and parasitic nodal capacitance to make the simulation more realistic. The circuits are designed for balanced ternary logic (-1, 0, +1) unlike previous circuit found in literature, which uses (0, 1, 2) ternary logic.

The output bit maximum propagation delay is 8 ns with 0.1 pF simulated capacitive load. With 15 pF simulative capacitive load, the output bit maximum propagation delay is 13 ns. The physical layout of the design occupies an area of 432×908 μm^2.

A simple conversion scheme from quaternary to binary bit is also presented in a standard CMOS process using multiple-input floating gate MOSFETS. The designed circuit was fabricated in AMI 1.5 μm n-well CMOS process and was tested for performance. All quaternary logic levels agree with the corresponding binary bits except the logic 2 (2 V), which was measured at 1.6 V for logic 2 due to

possible process variations. The conversion circuit from quaternary logic to binary logic achieved a great improvement in the number of devices. A reduction of more than 75% in transistor count was obtained over the previous designs. The circuit can be easily embedded in digital CMOS design architectures and used in a sensor readout electronics for transmission of data with reduced bandwidth requirements over a long distance [47]. The output bit maximum propagation delay is 6 ns with 0.1 pF simulated capacitive load and 17 ns with 15 pF load. The physical layout of the design occupies an area of $130 \times 175 \ \mu m^2$.

5.1   Future Work

The circuits were designed for conversion from multivalued (ternary and quaternary) logic to binary logic. An attempt to convert binary logic to multivalued logic using the multiple-input floating gate MOSFETs can be made. In future, the work could be extended to convert multivalued logic (radix $8 = 2^3$) to binary logic. An important aspect of designing circuits using floating gate devices is determining the value of unit capacitance "C", which effects the layout area and performance of the circuit. Thus efforts should be made to determine the optimum value of unit capacitance that can be implemented.

The practical design aspect of simulating floating gate MOSFET in SPICE using low-level models is still an issue. Manufactures do not provide models for simulating floating gate MOSFETs, hence a special technique to simulate these devices with standard MOS models is required.

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Appendix A

Input Circuit Files

* Circuit file to obtain the I-V Characteristics of floating gate nMOS transistor.

* B2 Spice default format (same as Berkeley Spice 3F format)

M1 1 2 0 0 Bsim3_05_nmos l = 1.6u w = 4.0u

C2 2 3 500ff

* Drain to Source voltage (PWL)

V3 1 0 DC 3V PWL (0ns 0v 300ns 3V)

* Different Gate to Source voltages

V4 3 0 DC 0

*V4 3 0 DC 1

*V4 3 0 DC 1.5

*V4 3 0 DC 2

*V4 3 0 DC 2.5

*V4 3 0 DC 3

.model Bsim3_05_nmos nmos (BSIM3 level parameters used shown in Appendix B)

.OPTIONS gmin = 1E-12 reltol = 1E-4 itl1 = 500 itl4 = 500
+ rshunt = 100G

.TRAN 1ns 300ns 0 1ns uic

.IC

.END

* Circuit file used to obtain the I-V Characteristics of floating gate pMOS transistor

* B2 Spice default format (same as Berkeley Spice 3F format)

M1 1 2 0 0 Bsim3_05_pmos l = 1.6u w = 4.0u

C2 2 3 500ff

* Drain to Source voltage (PWL)

V3 1 0 DC 3V PWL (0ns 0v 300ns -3V)

* Different Gate to Source voltages

V4 3 0 DC 0

*V4 3 0 DC -1

*V4 3 0 DC -1.5

*V4 3 0 DC -2

*V4 3 0 DC -2.5

*V4 3 0 DC -3

.model Bsim3_05_pmos pmos (BSIM3 level parameters used shown in Appendix B)

.OPTIONS gmin = 1E-12 reltol = 1E-4 itl1 = 500 itl4 = 500
+ rshunt = 100G

.TRAN 1ns 300ns 0 1ns uic

.IC

.END

* Circuit file to obtain the Transfer Curve for the nMOS floating gate transistor

* B2 Spice default format (same as Berkeley Spice 3F format)

M3 1 2 0 0 Bsim3_05_nmos l = 1.6u w = 4.0u

C3 2 3 500ff

* Gate to Source voltage

V5 3 0 DC 1 PWL (0ns –2v 500ns 3v)

*Different Drain to Source voltage

V6 1 0 DC 1V

* V6 1 0 DC 2V

*V6 1 0 DC 3V

.model Bsim3_05_nmos nmos (BSIM3 level parameters used shown in Appendix B)

.OPTIONS gmin = 1E-12 reltol = 1E-4 itl1 = 500 itl4 = 500
+ rshunt = 100G

.TRAN 1ns 500ns 0 1ns uic

.IC

.END

* Circuit file used to obtain the Transfer Curve of floating gate pMOS transistor

* B2 Spice default format (same as Berkeley Spice 3F format)

M1 1 2 0 1 Bsim3_pmos l = 1.6u w = 4.0u

C2 2 3 500ff

*Gate to Source Voltage

V2 3 0 DC -1 PWL (0ns 2v 500ns -3v)

* Different Drain to Source Voltage

V3 1 0 DC -1V

*V3 1 0 DC -2V

*V3 1 0 DC -3V

.model Bsim3_pmos pmos (BSIM3 level parameters used shown in Appendix B)

.OPTIONS gmin = 1E-12 reltol = 1E-4 itl1 = 500 itl4 = 500
+ rshunt = 100G

.TRAN 1ns 500ns 0 1ns uic

.IC

.END

* Circuit file to obtain the voltage transfer characteristics of floating gate CMOS inverter
* with various capacitors as shown in Fig. 2.14

* B2 Spice default format (same as Berkeley Spice 3F format)

M1 5 4 0 0 Bsim3_05_nmos l = 1.6u w = 8.0u
M2 5 4 22 22 Bsim3_pmos l = 1.6u w = 8.0u

C1 6 4 500ff

* Supply Voltage VDD

V1 22 0 DC 3V

* Gate voltage Vin

V2 6 0 DC 3 PWL (0ns 0v 120ns 3v)

*other capacitors used for obtaining the curves

*C6 0 4 20ff
*C7 0 4 40ff
*C8 22 4 20ff
*C9 22 4 40ff

*output node : 5

.OPTIONS gmin = 1E-12 reltol = 1E-4 itl1 = 500 itl4 = 500
+ rshunt = 100G

.TRAN 1ns 120ns 0 1ns uic

.IC

.END

Appendix B

Design MOSFET Model Parameters

nMOS Model Parameters

.MODEL NMOS NMOS (LEVEL = 49
+VERSION = 3.1   TNOM = 27   TOX = 1.41E-8
+XJ = 1.5E-7   NCH = 1.7E17   VTH0 = 0.6783469
+K1 = 0.8198806   K2 = -0.0815723   K3 = 21.2872824
+K3B = -8.3769938   W0 = 1E-8   NLX = 1E-9
+DVT0W = 0   DVT1W = 0   DVT2W = 0
+DVT0 = 2.9769564   DVT1 = 0.4298091   DVT2 = -0.1314503
+U0 = 459.4465085   UA = 1E-13   UB = 1.566796E-18
+UC = 1.344E-11   VSAT = 1.676264E5   A0 = 0.5671021
+AGS = 0.1157472   B0 = 2.856769E-6   B1 = 5E-6
+KETA = -3.548797E-3   A1 = 5.378248E-4   A2 = 0.3584167
+RDSW = 1.421987E3   PRWG = 0.0206332   PRWB = 0.0174913
+WR = 1   WINT = 2.860502E-7   LINT = 3.762151E-8
+XL = 0   XW = 0   DWG = -1.572821E-8
+DWB = 3.973063E-8   VOFF = 0   NFACTOR = 0.9112552
+CIT = 0   CDSC = 2.4E-4   CDSCD = 0
+CDSCB = 0   ETA0 = 0.0428326   ETAB = -1.388924E-3
+DSUB = 0.317372   PCLM = 2.4796867   PDIBLC1 = -0.5457422
+PDIBLC2 = 2.946108E-3   PDIBLCB = -8.49120E-3   DROUT = 0.726107
+PSCBE1 = 5.402825E8   PSCBE2 = 3.692234E-5   PVAG = 9.248005E-3
+DELTA = 0.01   RSH = 83   MOBMOD = 1
+PRT = 0   UTE = -1.5   KT1 = -0.11
+KT1L = 0   KT2 = 0.022   UA1 = 4.31E-9
+UB1 = -7.61E-18   UC1 = -5.6E-11   AT = 3.3E4
+WL = 0   WLN = 1   WW = 0
+WWN = 1   WWL = -6.554e-20   LL = 0
+LLN = 1   LW = 0   LWN = 1
+LWL = -9.461E-20   CAPMOD = 2   XPART = 0.5
+CGDO = 2.2E-10   CGSO = 2.2E-10   CGBO = 1E-9
+CJ = 4.188753E-4   PB = 0.99   MJ = 0.4464981
+CJSW = 3.196259E-10   PBSW = 0.1   MJSW = 0.1128874
+CJSWG = 1.64E-10   PBSWG = 0.1   MJSWG = 0.1128874
+CF = 0   PVTH0 = -0.0848114   PRDSW = -400.6457406
+PK2 = -0.0250774   WKETA = -0.0208937   LKETA = 2.577922E-3)

pMOS Model Parameters

```
.MODEL PMOS PMOS (          LEVEL = 49
+VERSION = 3.1             TNOM = 27              TOX = 1.41E-8
+XJ = 1.5E-7               NCH = 1.7E17           VTH0 = -0.9341243
+K1 = 0.5370998            K2 = -0.0122252        K3 =3.7496262
+K3B = -0.9286477          W0 = 6.54045E-8        NLX = 1E-9
+DVT0W = 0                 DVT1W = 0              DVT2W = 0
+DVT0 = 2.9562583          DVT1 = 0.5245313       DVT2 = -0.0997267
+U0 = 237.0052372          UA = 3.45997E-9        UB = 1E-21
+UC =-5.45512E-11          VSAT = 2E5             A0 = 0.8887791
+AGS = 0.1458591           B0 = 1.07758E-6        B1 = 5E-6
+KETA = -2.767583E-3       A1 = 0                 A2 = 0.3
+RDSW = 2.565262E3         PRWG = -0.0526966      PRWB = -0.0674531
+WR = 1                    WINT = 3.631054E-7     LINT = 3.573418E-8
+XL = 0                    XW = 0                 DWG = -3.251632E-8
+DWB = 1.114661E-8         VOFF = -0.046905       NFACTOR = 0.9565103
+CIT = 0                   CDSC = 2.4E-4          CDSCD = 0
+CDSCB = 0                 ETA0 = 3.183212E-4     ETAB = 2.302539E-5
+DSUB = 0.0150846          PCLM = 2.4099721       PDIBLC1 = -0.1320417
+PDIBLC2 = 2.588158E-3     PDIBLCB = -0.0999382   DROUT = 0.3140708
+PSCBE1 =7.275362E9        PSCBE2 = 7.138855E-10  PVAG = 0.5287847
+DELTA = 0.01              RSH = 105.1            MOBMOD = 1
+PRT = 0                   UTE = -1.5             KT1 = -0.11
+KT1L = 0                  KT2 = 0.022            UA1 = 4.31E-9
+UB1 = -7.61E-18           UC1 = -5.6E-11         AT = 3.3E4
+WL = 0                    WLN = 1                WW = 0
+WWN = 1                   WWL = -1.205E-20       LL = 0
+LLN = 1                   LW = 0                 LWN = 1
+LWL = 6.268E-21           CAPMOD = 2             XPART = 0.5
+CGDO = 2.36E-10           CGSO = 2.36E-10        CGBO = 1E-9
+CJ = 7.230164E-4          PB = 0.9520106         MJ = 0.4950624
+CJSW = 2.598254E-10       PBSW = 0.99            MJSW = 0.2998526
+CJSWG = 6.4E-11           PBSWG = 0.1            MJSWG = 0.1245165
+CF = 0                    PVTH0 = 5.98016E-3     PRDSW = 14.8598424
+PK2 = 3.73981E-3          WKETA = 4.758951E-3    LKETA = -3.900197E-3 )
```

Appendix C

Simulating Floating Gate MOS Device

One of the practical design issues of using floating gate devices is validation of electrical simulation. Since manufactures do not provide models for floating gate devices, techniques to simulate floating gate devices using standard MOS models must be devised. Other difficulty in simulating floating gate devices is the inability of the simulator to converge when floating nodes exists. Hence an initial operation point of the circuit must be introduced. Few approaches for this problem are given in references [43-46]. In reference [43], the solution was to use an initial condition (.IC) a feature in simulator. While in [44,45] they used additional networks formed by resistors and voltage controlled voltage sources (VCVS) to establish initial voltage on floating gate. Villegas et. al., [46], suggests to initialize all the input voltage sources to zero, before running the simulation, which would allow to set an appropriate operating point when using floating gate devices.

The equivalent circuit of a MIFG inverter when used for electrical simulation is given in Fig. C.1. When the circuit is simulated in SPICE it fails to converge at floating gate. Hence a large resistance in the range of 1E12 ohms was placed from floating gate to ground as shown in Fig. C.2. The resistor gives an initial voltage on floating gate as well as an effect of open circuit from floating gate to ground. The voltage on floating gate from simulations is found to match the theoretical calculations.

When designing circuits using floating gate devices, the switching threshold voltage of the circuits is often changed as explained in section 2.5 and in Fig. 2.15.
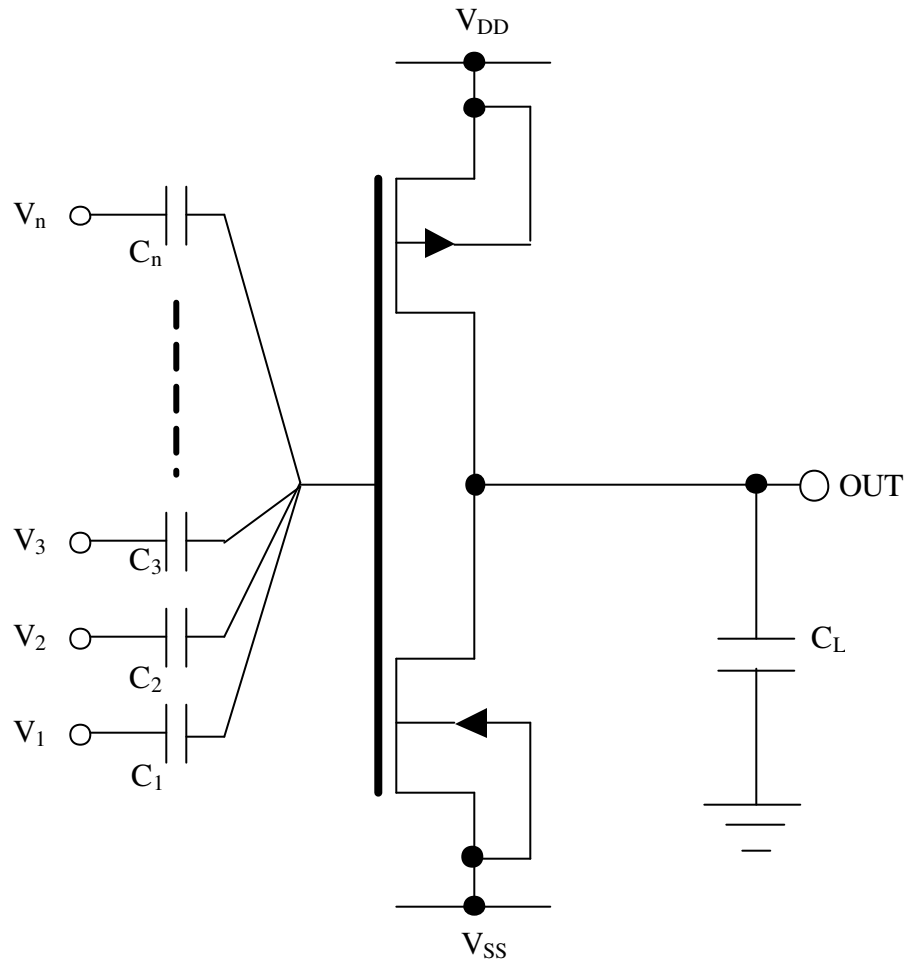
Fig. C.1: Equivalent circuit of a multiple-input floating gate inverter for electrical simulations.
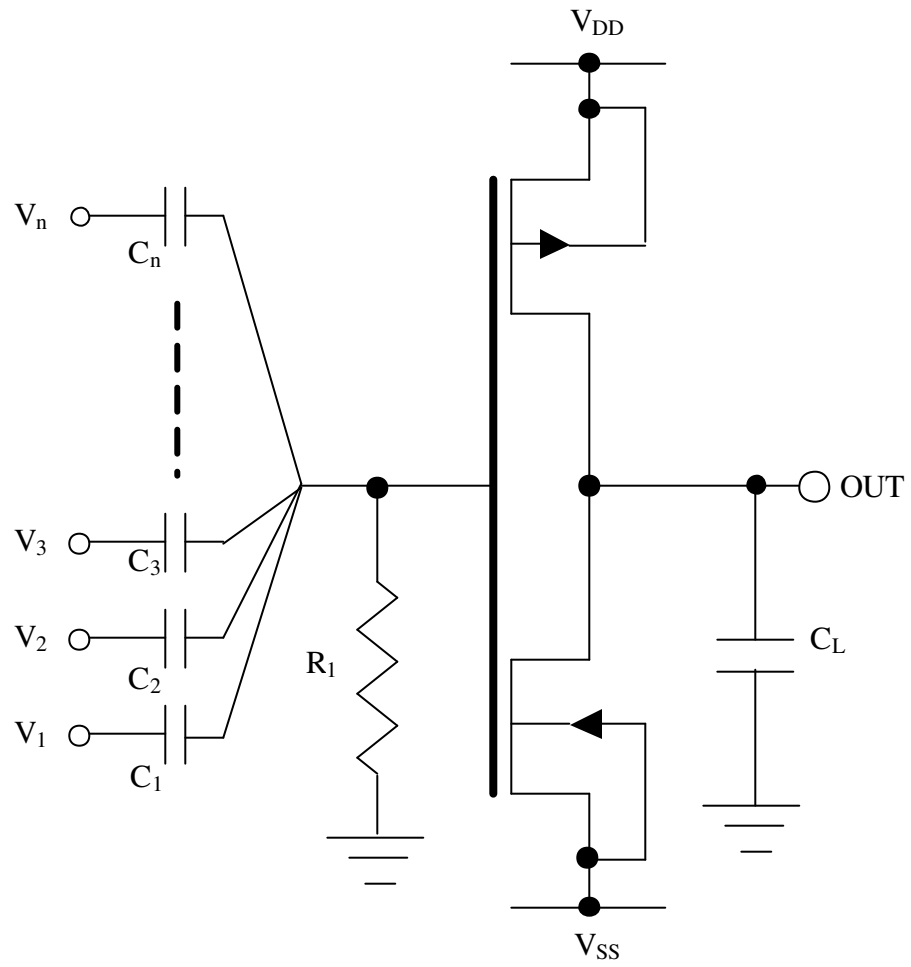
Fig. C.2: Resistor is added to equivalent circuit for simulation purpose.

When capacitor C_1 is used with DC voltage source as input to the capacitance, the simulator recognizes it as a DC storage capacitor, instead of a AC coupling capacitance and blocks the voltage. The DC voltage source is replaced with a piece-wise-linear voltage source by using which the simulator simulates the capacitor as a coupling capacitance. Taken the above considerations for simulating circuits having floating gate devices, the experimental results of circuits failed when MIFG inverters were cascaded.

The circuits are simulated in B2 SPICE with MOSIS BSIM3 MOS model parameters. The B2 SPICE uses an option RSHUNT = 100 G, which places a resistor of 1E11 from every node in the circuit to ground. Thus giving an open circuit effect and as well avoiding floating nodes in the circuit.

Appendix D

MOSFET Model Parameters of the Fabricated Chip

nMOS Model Parameters for 1.5-μm technology (T1AZ)

```
.MODEL NMOS NMOS (          LEVEL = 8
+VERSION = 3.1             TNOM = 27              TOX = 3.07E-8
+XJ = 3E-7                 NCH = 7.5E16           VTH0 = 0.5946428
+K1 = 0.9317355            K2 = -0.0642401        K3 = 8.1988053
+K3B = -1.6036239          W0 = 1E-7              NLX = 1E-8
+DVT0W = 0                 DVT1W = 0              DVT2W = 0
+DVT0 = 0.6287112          DVT1 = 0.3396          DVT2 = -0.3380439
+U0 = 690.3302409          UA = 2.107409E-9       UB = 1.45864E-18
+UC = 5.597668E-11         VSAT = 1.101194E5      A0 = 0.6538174
+AGS = 0.1405777           B0 = 2.36604E-6        B1 = 5E-6
+KETA = -5.491058E-3       A1 = 0                 A2 = 1
+RDSW = 3E3                PRWG =-0.0257109        PRWB = -0.0343409
+WR = 1                    WINT = 7.640524E-7     LINT = 2.383339E-7
+XL = 0                    XW = 0                 DWG = -2.045861E-8
+DWB = 3.86526E-8          VOFF = -0.052426       NFACTOR = 0.7700134
+CIT = 0                   CDSC = 0               CDSCD = 2.966891E-6
+CDSCB = 5.248867E-5       ETA0 = -1              ETAB = -0.4998094
+DSUB = 1                  PCLM = 1.1865082       PDIBLC1 = 7.872555E-3
+PDIBLC2 = 1.779838E-3     PDIBLCB = -0.1         DROUT = 0.0559194
+PSCBE1 = 2.6186E9         PSCBE2 = 5.988929E-10  PVAG = 0.2015173
+DELTA = 0.01              RSH = 51.8             MOBMOD = 1
+PRT = 0                   UTE = -1.5             KT1 = -0.11
+KT1L = 0                  KT2 = 0.022            UA1 = 4.31E-9
+UB1 = -7.61E-18           UC1 = -5.6E-11         AT = 3.3E4
+WL = 0                    WLN = 1                WW = 0
+WWN = 1                   WWL = 0                LL = 0
+LLN = 1                   LW = 0                 LWN = 1
+LWL = 0                   CAPMOD = 2             XPART = 0.5
+CGDO = 1.75E-10           CGSO = 1.75E-10        CGBO = 1E-9
+CJ = 2.922743E-4          PB = 0.9688488         MJ = 0.5144895
+CJSW = 1.31563E-10        PBSW = 0.99            MJSW = 0.1
+CJSWG = 6.4E-11           PBSWG=0.99             MJSWG=0.1
+CF = 0 )
```

pMOS Model Parameters for 1.5-μm technology (T1AZ)

```
.MODEL PMOS PMOS (        LEVEL = 49
+VERSION = 3.1            TNOM = 27              TOX = 3.07E-8
+XJ = 3E-7               NCH = 2.4E16            VTH0 = -0.8476404
+K1 = 0.4513608          K2 = 2.379699E-5        K3 =3.166569E-7
+K3B = -2.2238332        W0 = 9.577236E-7        NLX = 3.166569E-7
+DVT0W = 0               DVT1W = 0               DVT2W = 0
+DVT0 = 0.4531522        DVT1 = 0.6231695        DVT2 = -0.5
+U0 = 236.8923827        UA = 3.833306E-9        UB = 1.487688E-21
+UC =-1.08562E-10        VSAT = 1.275415E5       A0 = 0.6161235
+AGS = 0.2171952         B0 = 2.51061E-6         B1 = 8.008378E-7
+KETA = -7.084748E-3     A1 = 0                  A2 = 0.364
+RDSW = 3E3              PRWG = 0.1936825        PRWB = -0.0872641
+WR = 1                  WINT = 7.565065E-7      LINT = 8.759328E-8
+XL = 0                  XW = 0                  DWG = -2.13917E-8
+DWB = 3.857544E-8       VOFF = -0.0877184       NFACTOR = 0.2508342
+CIT = 0                 CDSC = 2.924806E-5      CDSCD = 1.497572E-4
+CDSCB = 1.091488E-4     ETA0 = 0.15903          ETAB = 6.381554E-3
+DSUB = 0.2873           PCLM = 4.4941362        PDIBLC1 = 6.848725E-3
+PDIBLC2 = 1E-3          PDIBLCB = -1E-3         DROUT = 4.153603E-3
+PSCBE1 =3.341988E9      PSCBE2 = 1E-3           PVAG = 15
+DELTA = 0.01            RSH = 76.4              MOBMOD = 1
+PRT = 0                 UTE = -1.5              KT1 = -0.11
+KT1L = 0                KT2 = 0.022             UA1 = 4.31E-9
+UB1 = -7.61E-18         UC1 = -5.6E-11          AT = 3.3E4
+WL = 0                  WLN = 1                 WW = 0
+WWN = 1                 WWL = 0                 LL = 0
+LLN = 1                 LW = 0                  LWN = 1
+LWL = 0                 CAPMOD = 2              XPART = 0.5
+CGDO = 2.09E-10         CGSO = 2.09E-10         CGBO = 1E-9
+CJ = 2.966784E-4        PB = 0.741159           MJ = 0.4269642
+CJSW = 1.607959E-10     PBSW = 0.99             MJSW = 0.1168473
+CJSWG = 3.9E-11         PBSWG = 0.99            MJSWG = 0.1168473
+CF = 0                  )
```

Vita

Harish Naga Venkata was born on November 30, 1977, in Hyderabad, India. He received his Bachelor of Technology in Electronics and Communication Engineering degree from Sri Venkateswara University, Tirupati, India, in May, 1999. He was enrolled in the Department of Electrical and Computer Engineering at Louisiana State University, Baton Rouge, Louisiana, to attend graduate school. He is presently working for Micron Technology Inc., Allen, Texas. His research interests include multivalued logic, multiple input-floating gate MOSFETs, capacitive based architectures.