Ternary logic implemented on a single dopant atom field effect silicon transistor

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We provide an experimental proof of principle for a ternary multiplier realized in terms of the charge state of a single dopant atom embedded in a fin field effect transistor (Fin-FET). Robust reading of the logic output is made possible by using two channels to measure the current flowing through the device and the transconductance. A read out procedure that allows for voltage gain is proposed. Long numbers can be multiplied by addressing a sequence of Fin-FET transistors in a row. © *2010 American Institute of Physics*. [doi:10.1063/1.3297906]

Increasing computational efficiency and reducing the size and energy cost of computational circuits are central aims in the roadmap of current electronics. We use the stable discrete charge state of a nanosystem (e.g., quantum dot, fullerene, metallic, and semiconducting nanoclusters, coordination compounds, dopant atom, for selected references, see Supporting Materials[1]) and the alteration of the charge state by varying the source drain and gate voltages to implement *ternary* logic. We show that the requirement from the nanosystem is that it has a finite charging energy,[2–5] large compared to the thermal energy at the temperature range of interest and that the *gate potential* can be varied. The essential physics is the measuring of the conductivity with respect to the gate potential, which gives rise to a symmetry of the charge stability map that is needed for ternary logic. The advantages of ternary logic and why balanced ternary notation is particularly advantageous are briefly discussed with more details in the supplementary information. An experimental implementation of a ternary multiplier is reported. Robust reading of the logic output is made possible by using two channels to measure the current flowing through the device and the *transconductance*, which is the derivative of the current with respect to the gate voltage. The experimental results are accompanied by a simulation. For a multiplier one advantage of the balanced ternary notation is that there is no carry digit. Therefore, a sequence of noncoupled transistors enables a number of many ternary digits to be multiplied. A circuit for the readout procedure that allows for voltage gain is proposed.

So called "Non-Boolean" are logic variables that can take more than two values. Following a correspondence that goes back to Shannon (1938), computing devices are assembled as switching networks and therefore use two-valued, say on and off, Boolean variables. There is, however, no reason of principle why two-valued variables must be used. One advantage of multivalued logic is that less space is required to store information, for example, the number nine is denoted as 9 in the usual decimal notation, as 100 in base three, and as 1001 in base two. The complementary aspect is that for a larger radix more states need to be physically distinguishable.

In ternary logic gate implementations,[6–8] ternary variables[9,10] can be encoded in different ways. One is an extension of binary encoding and the three values of the ternary variable are 0, 1, and 2. It is the sensible encoding for nanodevices when the physical variable that is read is the number of electrons in a spatial orbital of a confined system.[8] Another option is called "balanced ternary," in which case the three values of the ternary variable are −1, 0, 1. The use of balanced versus unbalanced ternary encoding depends both on the intended application and on the physical system that will realize the logic operations.

Table S1 in the supplementary information, SI,[1] shows the representation of numbers from −6 to 6 in decimal, binary, ternary unbalanced, and ternary balanced notation. Tables S2 and S3 of the SI compare addition and multiplication for the ordinary (=unbalanced) and balanced ternary encodings. Among the four truth tables shown in Tables S2 and S3, the multiplication in balanced ternary encoding is the most appealing for implementation since it requires no carry digit. This allows in principle for the multiplication of a number several digits long, where each digit multiplication can be treated by a separate unit, without any need of transfer of information from one unit to the next.

Electrical addressing of confined nanosystems for implementing Boolean (meaning binary) logic up to the level of a full adder based on the stability map of a three terminal device has been proposed in.[11] The binary yes/no logic operation is based on the physical distinction between a stable

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and a current carrying region on the stability map. Here we report on the application of the stability map for doing ternary logic. We provide a sketch of the theory that shows the physical origin of the sign, the results of a simulation and two possible experimental realizations. The physics is the quantization of charge for a nanosystem where the charging energy is finite. The two digits to be multiplied are inputed as the source-drain and gate voltages. The readout is the transconductance that can be determined either from the observed current directly or through a lock-in measurement. This allows for a more robust reading of the logic output.

We have previously shown[12] how to perform more elaborate Boolean logic using discrete excited electronic states of a confined nanosystem.[13] Discrete excited states can also be seen in the experimental results reported below.[13,14] It remains to be seen if we can combine charge and energy quantization toward the performance of multidepth *multilevel* logic. The ternary multiplier scheme that we propose here only requires charge quantization and therefore can be implemented on any nanostructure that shows Coulomb blockade. We show below an implementation on a many electron quantum dot and on a single dopant atom in a FinFET.

We consider a three terminal configuration where the drain electrode is grounded, the source voltage is denoted V_b and the gate voltage V_g. The energetics of the electron transfer process to or from a system where the charging energy is independent of the charge state can be described using the "orthodox theory."[2,4,5,15]

We have shown in Ref. 12 how to extend the orthodox theory to taking the discreteness of the excited states of the embedded dopant atom into account. For the logic scheme discussed here, a simple QD orthodox model with a continuous spectrum is sufficient. Equations (1) and (2) of the SI are for the energy differences for electron transfer from the (source or drain) electrode to the charge quantized, CQ, device in terms of the source-drain and gate voltages. See Refs. 5 and 15 for additional discussion. For the electron transfer to be allowed at very low temperature, the process must be exoergic meaning that the energy difference ΔE must be <0. The stability map shows the lines that divide the plane into regions where the charge transfer is ($\Delta E<0$) or is not ($\Delta E>0$) energetically allowed. Equations S3 and S4 of the SI define the boundaries of the region of stability as $\Delta E=0$ and these are the solid lines shown in figure S1 of the SI where the voltages are expressed in reduced units. The result is a diamondlike shape of the region of stability that is generic for a CQ device at low temperature in a three terminal configuration provided that the charging energy is independent of the charge state.

Multiplying two ternary numbers means that there are nine different possible inputs, see Table I below (or tables S2 and S3 of the SI). These nine different inputs are shown as dots in Fig. 1(b) below and also in figure S1.

For a balanced multiplier there is no carry digit so there is only one output digit, -1 or 0 or 1. We read the output as the signed value of the transconductance, meaning positive, zero, or negative. The essential physical point is that the sign of the transconductance alternates as seen in Fig. 1(b) below. The theory shows that the same holds for any CQ device. This alternation corresponds to the symmetry of the truth table, Table I below, of the multiplier.

TABLE I. Truth table for the multiplication of two balanced ternary numbers. The digits to be multiplied are the column and row labels. Note that there is no carry digit. The minus sign of the output is physically encoded by the sign of the transconductance on the four sides of the stability diamond, see Fig. 1(b).

Inputs	−1	0	1
−1	1	0	−1
0	0	0	0
1	−1	0	1

The conductance depends on the rate of electron transfer to and from the CQ device. At temperatures low compared to the charging energy the four rates are, in the lowest approximation, proportional to the respective energy differences: $\Gamma=-\Delta E/\pi\hbar\tilde{R}$ where $\tilde{R}$ is a dimensionless resistance, measured in units of the quantum resistance $\pi\hbar/2e^2=13\ \mathrm{k}\Omega$.[5] A better approximation, when thermal activation is allowed is that at lower temperatures and when $\Delta E>0$, Γ is exponentially small. From the rates of electron transfer, the source to drain current is computed as $I_{SD}\propto\Gamma_S\Gamma_D/(\Gamma_S+\Gamma_D)$.

The different physics of the balanced ternary multiplier is expressed by the unusual symmetry upon reflection of the transconductance, dI/dV_g, with respect to the gate voltage. For the more familiar case of the conductance when the source-drain voltage is varied, dI/dV_b, the sign of the current is the sign of the (source-drain) voltage. $I\,dI/dV_b$ has opposite signs in the upper ($V_b>0$) and lower ($V_b<0$) halves of the plane as shown in Fig. 1(a). Now consider, say, the upper half plane. The current is positive or zero. Start with a very low value of the gate voltage. No current is flowing because

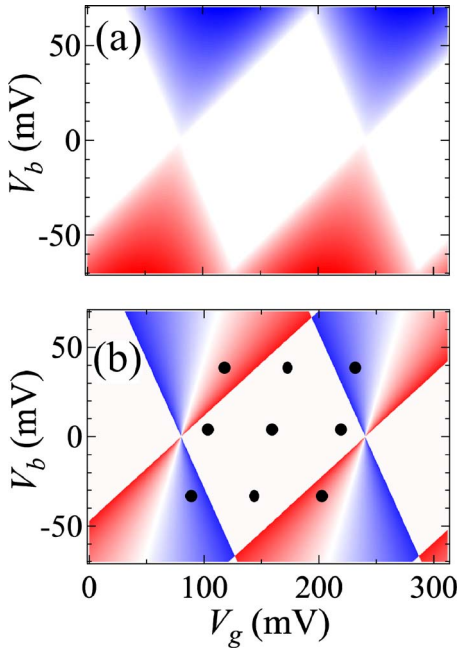

FIG. 1. (Color online) Maps of current, I, (a), and transconductance, dI/dV_g, (b), computed as a function of the gate voltage V_g (abscissa) and the source-drain voltage V_b for $C_g=1$ aF and $C_S=C_g=0.7$ aF. The resistance at either junction is the same. The color coding is a heat map, red is negative, zero is white and blue is positive. The different sign of dI/dV_g on two facing sides of the diamond is clearly seen. In Fig. 1(b) we show the nine points that represent the nine possible inputs for multiplying two ternary numbers. By using reduced voltage variables the plot can be made to look symmetric, see figure S1.

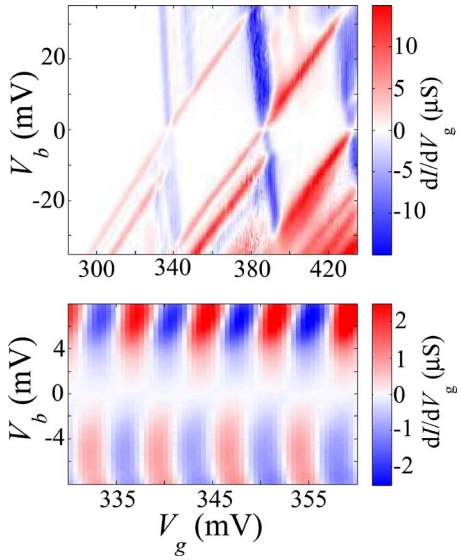

FIG. 2. (Color online) (a) The transconductance, dI/dV_g, stability diagram shows the transport through a single dopant atom embedded in a Fin-FET device at 1.6 K. The region where transport is Coulomb blocked appears in white. Going from left to right, three stable charge states (+1, 0, −1) of the dopant atom are visible. We use the region of stability of the neutral dopant (middle) to implement the multiplier. The regions of positive and negative dI/dV_g appear in light (red online) and dark (blue), respectively. (b) Transconductance of a many electron SET based on complementary metal-oxide semiconductor technology.

a negatively charged state is stable. Increase the gate voltage. Current flows and dI/dV_g is positive, see Fig. 1(b). Increasing the gate voltage further causes the charge state to move out of the Fermi window and the formerly positive current stops. dI/dV_g is negative. Increasing the gate voltage even further moves the next charge state into the Fermi window. Current flows and dI/dV_g is positive, see Fig. 1(a). To determine the transconductance on chip, an ac ripple is added to V_g and the phase difference between this ripple and the modulation of I_d, that corresponds to dI/dV_g is transformed into a dc output voltage. This can be done in a simple five transistors single electron transistor (SET)-FET hybrid circuit and the output voltage can be used as an input the next logic operation.[16]

Two possible implementations on a CQ device are shown in Fig. 2. The transconductance map of a single donor in a Fin-FET is plotted in Fig. 2(a). A detailed analysis verifies that current flows through the lowest level of the dopant that is confined by the surroundings. At higher values of the gate potential interfacial excited states can complicate the picture. By comparing with the computed Fig. 1(b) it is clear that one can read all the nine entries in Table I. Zero output is read as zero conductance (white), 1 is read as a negative conductance (blue), and −1 as a positive value (red). This is the configuration that we favor. As a comparison Fig. 2(b) shows the transconductance of a FET based SET in the many electron limit. No excited states are resolved and the transconductance map is closer to the computed one shown in Fig. 1(b). Note however that the scale in gate voltage here is very much smaller because the charging energy is of the order of a few millivolt. The strength of the transconductance signal is also lower. In comparison to other SET devices, single dopant devices do have the advantage of a device independent charging energy and a wider voltage scale.

In conclusion, we demonstrated the combination of the charge stability map of a nanodevice confined within a three-terminal configuration with the algebra of ternary logic to directly implement a ternary multiplier. The essential physics is the symmetry of the current map as induced by the variation of the current with the gate voltage, the transconductance, dI/dV_g. Two experimental proofs of principle that realize the multiplier in terms of a CQ device are provided. These are a single dopant atom in a Fin-FET and a many electron QD in a SET. We propose a read out procedure that shows voltage gain and transforms the transconductance output into a dc voltage.

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[1]See supplementary material at http://dx.doi.org/10.1063/1.3297906 for more about ternary logic and an additional experimental plot.
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