TEST AND DESIGN-FOR-TEST OF MIXED-SIGNAL INTEGRATED CIRCUITS

Marcelo Lubaszewski[1] and Jose Luis Huertas[2]

[1]*Electrical Engineering Department, Universidade Federal do Rio Grande do Sul (UFRGS), Av. Osvaldo Aranha esquina Sarmento Leite 103, 90035-190 Porto Alegre RS, Brazil;*

[2]*Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica (IMSE-CNM), Universidad de Sevilla, Av. Reina Mercedes s/n, Edificio CICA, 41012 Sevilla, Spain*

Abstract: Although most electronic circuits are almost entirely digital, many include at least a small part that is essentially analog. This is due to the need to interface with the real physical world, that is analog in nature. As demanding market segments require ever more complex mixed-signal solutions, high quality tests become essential to meet circuit design specifications in terms of reliability, time-to-market, costs, etc. In order to lower costs associated to traditional specification-driven tests and, additionally, achieve acceptable fault coverages for analog and mixed-signal circuits, it is reasonable to expect that no other solution than a move towards defect-oriented design-for-test methods will be applicable in the near future. Therefore, testing tends to be dominated by embedded mechanisms to allow for accessibility to internal test points, to achieve on-chip test generation, on-chip test response evaluation, or even to make it possible the detection of errors concurrently to the circuit application. Within this context, an overview of existing test methods is given in this chapter, focusing on design-for-testability, built-in self-test and self-checking techniques suitable for the detection of realistic defects in analog and mixed-signal integrated circuits.

Keywords: Analog and mixed-signal test, fault modelling, fault simulation, test generation, defect-oriented test, design-for-test, design-for-testability, built-in self-test, self-checking circuits.

1. INTRODUCTION

Today's telecommunications, consumer electronics and other demanding market segments, require that more complex, faster and denser circuits are designed in shorter times and at lower costs. Obviously, the ultimate goal is to maximise profits.

Although most electronic circuits are almost entirely digital, many include at least a small part that is essentially analog. This is due to the need to interface with the real physical world, that is analog in nature. Therefore, transducers, signal conditioning and data converter components add to the final circuit architecture, leading to ever more complex mixed-signal chips with an increasing analog-digital interaction.

Nevertheless, the development of reliable products cannot be achieved without high quality methods and efficient mechanisms for testing Integrated Circuits (ICs). If, on one hand, test methods have already reached an important level of maturity in the domain of digital logic, unfortunately, on the other hand, practical analog solutions are still lagging behind their digital counterparts. Analog and mixed-signal testing has traditionally been achieved by functional test techniques, based on the measurement of circuit specification parameters. However, measuring such parameters is a time consuming task, requires costly test equipment and does not ensure that a device passing the test is actually defect-free. Then, to ensure the quality required for product competitiveness, one can no more rely on conventional functional tests: a move is needed towards methods that search for manufacturing defects and faults occurring during a circuit's lifetime. Moreover, to achieve acceptable fault coverages has become a very hard and costly task for external testing: test mechanisms need to be built into integrated circuits early in the design process. Ideally, these mechanisms should be reused to test for internal defects and environmental conditions that may affect the operation of the systems into which the circuits will be embedded. This would provide for amplified payback. To give an estimate about the price to pay for faults escaping the testing process, fault detection costs can increase by a factor of ten, when moving from the circuit to the board level, then from the board to the system level, and lastly, from the final test of the system to its application in the field.

Therefore, design-for-test seems to be the only reasonable answer to the testing challenges posed by state-of-the-art integrated circuits. Mechanisms that allow for accessibility to internal test points, that achieve on-chip test generation, on-chip test response evaluation, and that make it possible the detection of errors concurrently to the application, are examples of structures that may be embedded into circuits to ensure system testability. They

obviously incur penalties in terms of silicon overhead and performance degradation. These penalties must definitely account for finding the best trade off between quality and cost. However, the industrial participation to recent test standardisation initiatives confirms that, in many commercial applications, design-for-test can prove economical.

Within this context, the aim of this chapter is to give a glimpse into the area of design-for-test of analog and mixed-signal integrated circuits. First of all, the test methods of interest to existing design-for-test techniques are revisited. Finally, design-for-testability, built-in self-test and self-checking techniques are discussed and illustrated in the realm of integrated circuits.

2. TEST METHODS

2.1 General background

From the very first design, any circuit undergoes *prototype debugging, production* and periodic *maintenance tests* to simply identify and isolate, or even replace faulty parts. Those are called *off-line tests,* since they are independent of the circuit application and need, in the field, that the application is stopped before the related testing procedures can be run.

In high safety systems, such as automotive, avionics, high speed train and nuclear plants, poor functioning cannot be tolerated and detecting faults concurrently to the application becomes also essential. The *on-line detection* capability, used for checking the validity of undertaken operations, can be ensured by special mechanisms, such as self-checking hardware.

In general, tests must check whether, according to the specifications, the circuit has a correct functional behaviour *(functional testing),* or whether the physical implementation of the circuit matches its schematics *(structural testing).* The former, also called specification-driven test, is based on measuring parameters that are part of the functional specification of the circuit under test. The latter, also called defect-oriented test, is based on catching physical defects that are modelled as *faults* representing, at the level of design description (algorithmic, logic, electrical, etc), the impact of mismatches between the actually implemented and the expected implementation of the device. The structural, opposed to the functional testing, can more easily provide a quantitative measure of test effectiveness *(fault coverage),* due to its fault-based nature. If, for any reason, structural tests cannot reach the required fault coverage, they must be followed by functional tests, although this leads to a longer test time because of redundant testing.

On one hand, test methods have already reached an important level of maturity in the domain of digital systems: *digital testing* has been dominated by structured fault-based techniques and by successfully developed and automated standardised test configurations. On the other hand, practical analog solutions are still lagging behind their digital counterparts: *analog and mixed-signal testing* has traditionally been achieved by functional test techniques, based on the measurement of circuit specification parameters, such as gain, bandwidth, distortion, impedance, noise, etc. Analysing aspects such as size, accuracy, sensitivity, tolerances and modelling, helps understanding why this digital vs. analog testing contrast exists:

Compared to digital logic, analog circuits are usually made up of much fewer elementary devices that interface with the external world through a much smaller number of inputs and outputs. Thus, the difficulties of testing analog circuits do not reside in sizing, but in the precision and accuracy that the measures require. Additionally, analog circuits are much more sensitive to loading effects than digital circuits. The simple flow of an analog signal to an output pin may have an important impact on the final circuit topology and behaviour.

Digital signals have discrete values. Analog signals, however, have an infinite range, and good signal values are referred to certain tolerance margins that depend on process variations and measurement inaccuracies. Absolute tolerances in analog components can be very large (around 20%), but relative matching is usually very good (0.1% in some cases). Although multiple component deviations may occur, in general, analog design methods promote that deviations cancel each other's effect, placing design robustness on the opposite direction of fault detection. Additionally, simulation time very quickly gets prohibitive for multiple component deviations.

For the reasons above, modelling the circuit behaviour is far more difficult in analog than in digital circuits. Furthermore, the function of analog circuits cannot be described by closed-form expressions as in Boolean algebra, that allows for the use of very simple fault models such as the widely accepted digital stuck-at. Instead, the behaviour of an analog circuit depends on the exact behaviour of a transistor, whose model requires a set of complex equations containing lots of parameters. As a consequence, it turns difficult to map defects to suitable fault models and thus, to accurate simulate the circuit behaviour in presence of faults.

Independently of the digital or analog nature of the circuit under test, the application of input stimuli followed by the observation of output voltages has been a widely used test technique. However, it has been shown that such a *voltage testing* cannot detect many physical defects that lead to unusual circuit consumptions. This is the reason why the practice of *current testing,* based on the measurement of the current consumption between the power supplies, has been increasing in importance in the last years. Current testing

has been mostly faced as a complementary technique to the voltage testing approach.

2.2 Defects and fault models

Efficient tests can only be produced if realistic fault models, based on physical failure mechanisms and actual layouts, are considered.

Many defects may be inherent to the silicon substrate on which the integrated structures will be fabricated. Those may result from impurities found in the material used to produce the wafers, for example. Others may be due to problems occurring during the various *manufacturing* steps: the resistivity of contacts, for instance, will depend on the doping quality; the presence of dust particles in the clean room or in the materials may lead to the occurrence of spot defects; the misalignment of masks may result in deviations of transistor sizes, etc. All these defects lead, in general, to faults that simultaneously affect several devices, i.e. *multiple faults.*

Other defects occur during a circuit's *lifetime.* They are usually due to failure mechanisms associated to transport and electromechanical phenomena, thermal weakness, etc. In general, those defects produce *single faults.*

Permanent faults, like interconnect opens and shorts, floating gates, etc, can be produced by defects resulting from manufacturing and circuit usage. *Transient faults,* on the contrary, will appear due to intermittent phenomena, such as electromagnetic interference or space radiations.

Although defects are absolutely the same for digital and analog circuits, fault modelling is a much harder task in the analog case. This is mainly due to a larger number of possible misbehaviours resulting from defects that may affect a circuit dealing with analog signals.

The most intuitive fault model is the one that simply translates the various facets of the expected behaviour of a circuit to a number of parameters that shall conform for the circuit to be considered fault-free. These parameters are obviously extracted from the circuit design specification and measuring all of them equals to checking the whole circuit functionality, at a cost that may approach the one of full device characterisation. In the case of operational amplifiers, such functional fault model may consider accepted intervals for input offset voltage, common-mode rejection ratio, slew-rate, open-loop gain, output resistance and other parameters (Calvano, 2001). In respect to analog filters, functional faults may comprise parameters such as cut-off frequency, pole factor quality, DC-gain, maximum ripple in the pass and reject band, dynamic range, total harmonic distortion, noise, etc (Calvano, 2000). Fault models for Analog-to-Digital (A/D) and Digital-to-Analog (D/A) converters bring up static performance parameters, such as gain, offset, differential and integral non-

linearity, as well as dynamic parameters, such as signal-to-noise and distortion ratio, effective number of bits, total harmonic distortion and spurious free dynamic range (Bernard, 2003).

In terms of structural testing, three categories of faults have been guiding most works on analog testing: *hard faults* (Milor, 1989), *soft* and *large deviations* (Slamani, 1995). Hard faults are serious changes in component values or in circuit topology, usually resulting from catastrophic opens or short circuits. In continuous-time analog integrated circuits, this involves transistors, resistors, capacitors and wires opens and shorts. In discrete-time implementations, switches stuck-on and stuck-open add to the fault model. Figure 1 shows an example of hard faults at the transistor level. Soft faults are small deviations around component nominal values, such as small changes in transistor gains, in capacitor and resistor values, etc. They may cause circuit malfunctions by slightly displacing the cut-off frequency of filters or the output gain of amplifiers, for example. Large deviations are also deviations in the nominal value of components, but of a greater magnitude. They still cause circuit malfunctions, but their effects are quite harder than those observed for soft faults. Some few works also consider interaction faults in analog and mixed-signal circuits (Caunegre, 1996; Cota, 1997). These faults are shorts between nodes of the circuit that are not terminals of the same digital or analog component.

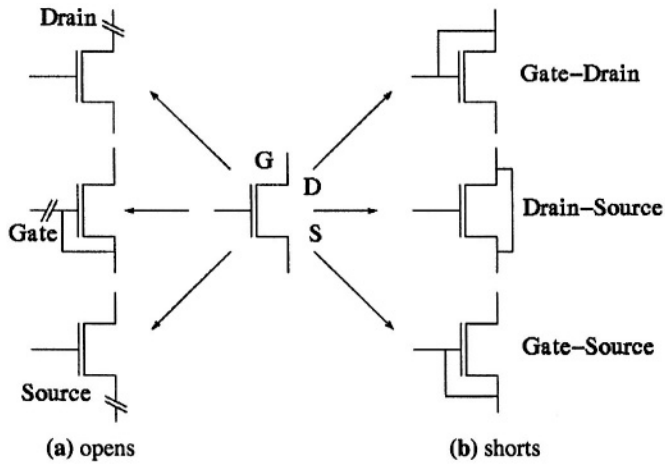

Figure 1. Fault model for hard faults in a MOS transistor.

Finally, from the knowledge about defect sizes and defect occurrences in a process, layouts can be analysed and the probabilities of occurrence of opens, shorts, etc, in different layout portions and layers, can be derived by *inductive fault analysis - IFA* (Meixner, 1991). The IFA technique has the

advantage of considerably reducing the list of faults, by taking into account only those with reasonable chances of occurrence *(realistic faults).*

2.3 Functional Test

In IC industry, most practices for mixed-signal testing are functional and thus, build upon specification-driven procedures. The approaches in use are based on time- or frequency-domain analysis. Many of them make use of Digital Signal Processing (DSP) techniques.

Time-domain analysis is used to check circuit time responses from transient, DC static or AC dynamic measurements. They apply to both filters and data converters.

An example of test procedure based on transient response analysis is given in (Calvano, 2000). That work considers that deviations in the cut-off frequency and in the pole quality factor are the faults to detect in 2^{nd} order sections of analog filters. A pulse, a step or a ramp is applied to a low-pass, band-pass or high-pass filter, respectively, and the peak-time and/or overshoot of the 2^{nd} order dynamic system response is observed. Those parameters prove to be good indirect measures of the filter cut-off frequency and pole quality factor.

For more complex linear (Carro, 1998) and even for non-linear analog circuits (Nácul, 2002), duplication-like testing can be performed by training a digital filter such as it can mimic the expected behaviour of the circuit under test. Once the adaptive filter has all its coefficients determined, then a test stimulus is simultaneously applied to the trained filter and the circuit under test, and the outputs of both circuits are compared to check whether the circuit is faulty or fault free. A broadband test stimulus, such as white noise, is the preferable choice for both the training and the testing phases of the method.

Another example of time-domain analysis is the histogram testing of A/D converters. In this technique, code transition levels are not measured directly, but determined through statistical analysis of converter activity. For a known periodic input stimulus, the histogram of code occurrences (code counts) is computed over an integer number of input waveform periods. Figure 2 shows a *ramp histogram,* also called linear histogram, computed for a linear - typically triangular – waveform. The computation is illustrated for an ideal 3-bit converter. Generally, histograms support analysis of the converter's static performance parameters. A missing code m is easily identified as the corresponding code count $H[m]$ is equal to zero. Also offset is easily identified as a shift in the code counts and gain directly relates to average code count. Finally, the converter linearity can be assessed via the detailed determination of code transition levels.

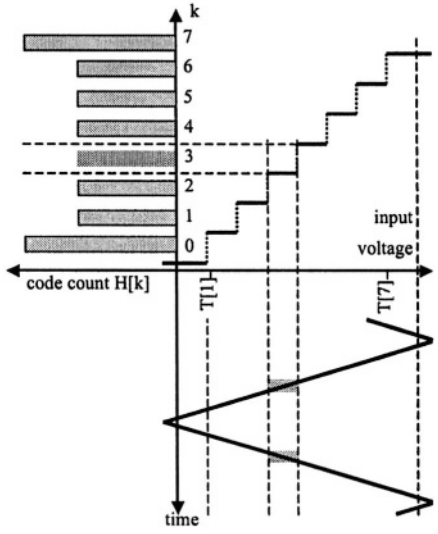

Figure 2. Linear histogram for an ideal 3-bit A/D converter.

A frequency-domain based test typically builds upon a conversion of a signal from the time-domain to a spectral representation.

A Bode plot is the most intuitive and the most frequent representation for the behaviour of a filter in frequency-domain. From a Bode plot, parameters such as gain in the pass and reject band, cut-off frequency and pole quality factor of a filter, can be easily extracted. In practice, a complete frequency sweep is needed to experimentally obtain such a plot, which requires long test application and measurement times.

Another type of frequency-domain test samples signals in the time-domain and then convert to the frequency-domain by applying a Fast Fourier Transform (FFT) or a Discrete Fourier Transform (DFT) to the samples. The resulting spectrum is a plot of frequency component magnitudes over a range of frequency bins. Further details on fundamentals of DSP testing can be found in (Mahoney, 1987; Burns, 2001). Figure 3 illustrates an A/D converter output spectrum obtained from the application of a DFT to the response of the converter to a spectrally pure sine-wave input of frequency f_i. The second to k^{th} harmonic distortion components, A_{H2} to A_{Hk}, occur at frequencies that are integer multiples of f_i. Additionally, spurious components, such as A_{Si} in figure 3, can be seen at other than the input signal or harmonics frequencies. The main dynamic and some static performance parameters can be extracted from the output spectrum in the form of ratios of RMS amplitudes of particular spectral components (Bernard, 2003). Similarly, such a spectrum can be obtained for a filter, for which f_i is usually its cut-off frequency.

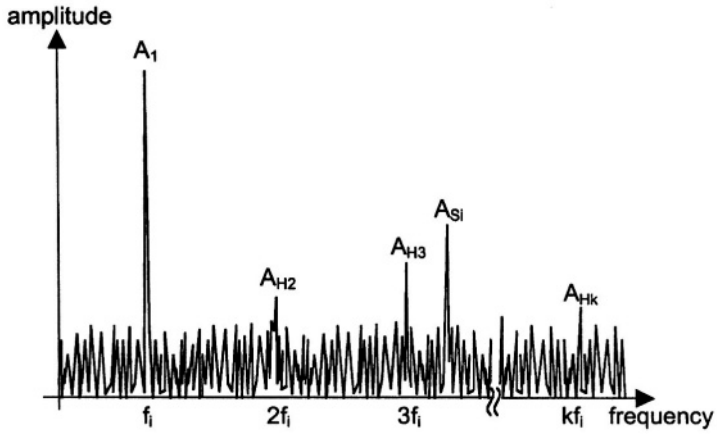

Figure 3. A/D converter output spectrum

2.4 Structural Test

Existing structural fault models give the opportunity of precisely determining input test stimuli that provoke that the faulty circuit behaves differently from the expected fault-free outputs. In next sections, available tools for fault simulation and automatic test generation are described. Those tools make it possible to build structural test sequences for fault detection and fault diagnosis in analog and mixed-signal integrated circuits.

2.4.1 Fault simulation

Fault simulation consists, basically, of simulating the circuit in the presence of the faults of the model, and of comparing the individual results with the fault-free simulations. The goal is to check whether or not these faults are detected by the applied input stimuli. The steps involved in the fault simulation process are:

- fault-free simulation;
- reduction of the fault list *(fault collapsing),* by deleting faults that present the same structure as expected for a particular circuit topology;
- insertion of the fault model into the fault-free circuit description *(fault injection)*;
- simulation of the faulty circuit;
- comparison of the faulty and fault-free simulation results and, in case of mismatch, deletion of the fault from the initial fault list *(fault dropping).*

A typical fault simulation environment is given in figure 4.

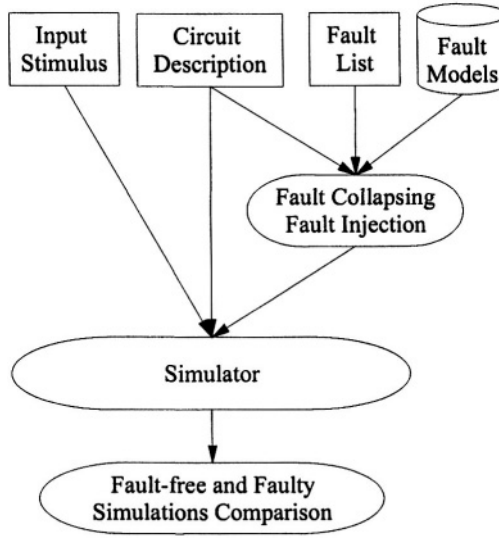

Figure 4. A generic fault simulation procedure.

Fault simulation is widely used for:

- test evaluation, by checking the fault coverage, i.e. the percentage of faults detected by a set of input stimuli;
- fault dropping in test generation, by verifying which faults of the model a computed test stimulus detects; and,
- diagnosis, by making it possible the construction *of fault dictionaries* that identify which faults are detected by every test stimulus.

Contrarily to the digital case, where some degree of parallelism is possible in fault simulation (Abramovici, 1990), in analog and mixed-signal circuits faults are injected and simulated sequentially, making fault simulation a very time consuming task. For analog circuits, fault simulation is traditionally performed at the transistor-level using circuit simulators. For the fault simulation of continuous-time analog circuits, (Sebeke, 1995) proposes a computer-aided testing tool based on a transistor-level hard fault model. This fault model is made up of local shorts, local opens, global shorts and split nodes. The tool injects into the fault-free circuit realistic faults obtained from layouts by an IFA-based fault extractor. For switched-capacitor analog circuits, (Mir, 1997) presents a switch-level fault simulator that models shorts, opens and deviations in capacitors, stuck-on, stuck-open and shorts between analog terminals of switches. An automatic tool is introduced that performs time- and frequency-domain switch-level fault simulations, keeping simulation times orders of magnitude lower than for transistor-level simulations. A behavioural-level fault simulation approach is

proposed in (Nagi, 1993a). It has practical use only for continuos-time linear analog circuits. First of all, the circuit under test, originally expressed as a system of linear state variables, suffers a bilinear transformation from the s-domain equations to the z-domain. Next, the equations are solved to give a discretized solution. In this approach, soft faults in passive components are directly mapped onto the state equations, while hard faults require, in general, that the transfer function is recomputed for the affected blocks. Finally, operational amplifier faults are modelled in the s-domain, before mapping them to the z-domain.

2.4.2 Test generation

Following the choice of a suitable fault model and fault simulator, test generation is the natural step to define an efficient test procedure to apply to the circuit under test.

The problem of generating tests consists, basically, of finding a set of input test stimuli and a set of output measures, which guarantee a maximum fault coverage. If the fault detection goal is extended to include fault diagnosis, the computed test stimuli must, additionally, be capable of distinguishing between faults. A typical test generation environment is given in figure 5.

Over the last decade, some test generation procedures for analog circuits have been proposed in the literature. The technique reported in (Tsai, 1991), one of the earliest contributions to test generation of linear circuits, formulates the analog test generation task as a quadratic programming problem, and it derives pulsed waveforms as input test stimuli. DC test generation is dealt with in (Devarayanadurg, 1994) as a min-max optimisation problem that considers process variations for the detection of hard faults in analog macros. This min-max formulation of the static test problem is extended to the dynamic case (AC) in (Devarayanadurg, 1995). The automatic generation of AC tests has also been addressed in other works (Nagi, 1993b; Slamani, 1995; Mir, 1996a; Cota, 1997). (Nagi, 1993b) uses a heuristic based on sensitivity calculations to choose the circuit frequencies to consider. After each choice, fault simulation is performed as the means to drop from the fault list all detected faults. From a multifrequency analysis, the approach in (Slamani, 1995) selects the test frequencies that maximise the sensitivity of the output parameters measured for each individual faulty component. (Mir, 1996a) also proposes a multifrequency test generation procedure, but computes a minimal set of test measures and a minimal set of test frequencies which guarantee maximum fault coverage and maximal diagnosis. Finally, (Cota, 1997) enlarges the set of faults including interaction shorts, and merges the sensitivity analysis (Slamani, 1995) and the search of minimal sets (Mir, 1996a), with test generation based on fault simulation (Nagi, 1993b). Additionally, it applies the new automatic test

generation procedure to linear and non-linear analog and mixed-signal circuits.

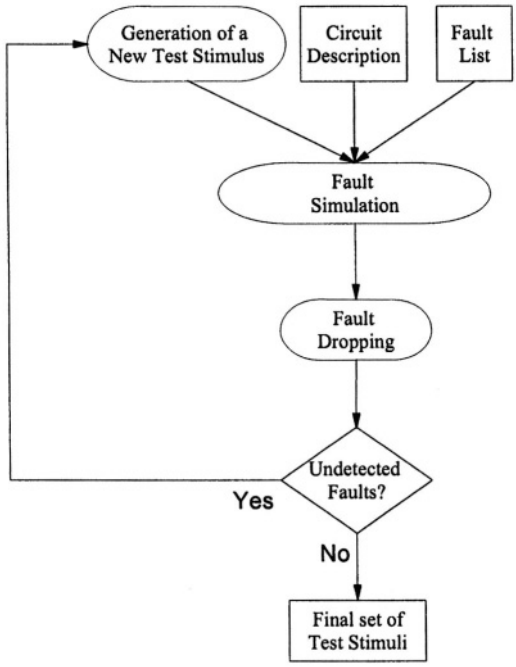

Figure 5. A generic test generation procedure.

3. DESIGN-FOR-TEST

Even though a test generation tool is available for testing, hard-to-detect faults can prevent that a good trade off between fault coverage and testing time is achieved. In these cases, the redesign of parts of the circuit can represent a possible solution to improve the accessibility to hard-to-test elements *(design-for-testability).*

Considering the increasing complexity of integrated circuits, another design-for-test possibility is to build self-test capabilities into circuits *(built-in self-test).* In general, the use of on-chip structures for test generation and test evaluation allows for significant savings in test equipment, reducing the final chip cost.

In case the application requires that faults are detected on-line, the circuit can be made *self-checking* by encoding the outputs of functional blocks and verifying them through embedded checkers. Unlike built-in self-test

approaches, concurrent checking is performed using functional signals, rather than signals specifically generated for testing the circuit.

In the following sections, these three design-for-test approaches, i.e. design-for-testability, built-in self-test and self-checking technique, are further discussed and illustrated. The discussion ends up by the proposal of an unified approach for off-line and on-line testing of analog and mixed-signal integrated circuits.

3.1 Design-for-testability

Design-for-testability approaches aim at improving the capability of observing, at the circuit outputs, the behaviour of internal nodes *(observability),* and at improving the capability of getting test signals from the circuit inputs to internal nodes *(controllability).*

Ad-hoc techniques, that are in general based on partitioning, on the use of multiplexers to give access to hard-to-test nodes, on disabling feedback paths, etc, can be used to enhance the testability of circuits. Nevertheless, structured approaches are far more suitable to face testing problems in highly complex integrated circuits.

In the digital domain, the most successful structured approach is undoubtedly the *scan path* technique (Eichelberger, 1978). In test mode, a set of circuit flip-flops is connected into a shift register configuration, so that scan-in of test vectors and scan-out of test responses are made possible. Similarly, the testability of internal nodes of printed circuit boards can be improved by extending the internal scan path to the interface of integrated circuits. This technique is referred to as *boundary scan* (LeBlanc, 1984) and is the basis of a very successful test standard (IEEE, 1990), implemented in many products available in the market (Maunder, 1994).

In the analog case, the first attempt to apply the idea of the scan path to test filters was made by (Soma, 1990). The basis of this design-for-testability methodology consists of dynamically broadening the bandwidth of each stage of a filter, in order to improve the controllability and observability of circuit internal nodes. This bandwidth expansion is performed by disconnecting the capacitors of the filter stages by using MOS switches. The main drawback of this approach is that the additional switches impact the filter performance. Although in the extension of this technique to switched-capacitor implementations (Soma, 1994) no extra switches are needed in the main signal path, additional control signals and associated circuitry and routing are required. In order to reduce the impact on performance of the additional scan circuitry, operational amplifiers with duplicated input stages have been used in (Bratt, 1995). This technique is illustrated in figure 6: in scan mode, a filter stage can be reprogrammed to work as a voltage follower, and propagate to the next stage the output of the previous stage.

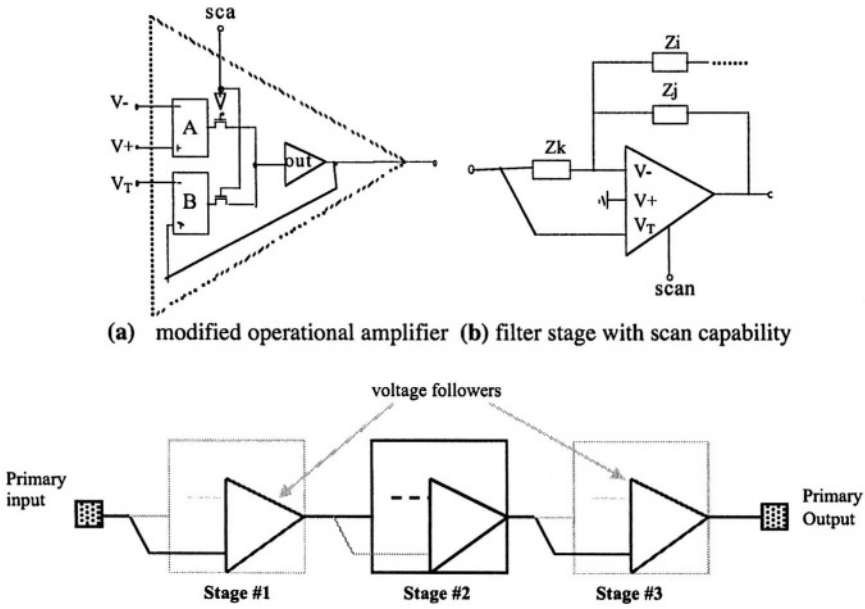

Figure 6. Analog scan based on operational amplifier with duplicated input stage.

At the board level, the main problem to face in testing mixed-signal circuits is the detection and diagnosis of interconnect faults. While shorts and opens in digital wiring can be easily checked by means of boundary scan, analog interconnects (made up of discrete components in addition to wires) require specific mechanisms to measure impedance values. The principle of the most usual impedance measurement technique is shown in figure 7 (Osseiran, 1995). Zx is the impedance to measure. Z1 and Z2 are two other impedances connected to Zx. Zs is the probe impedance of the test stimuli source (including the source output impedance), Zi is the impedance of the probe to the virtual ground of the operational amplifier (including the input impedance of the measuring circuitry) and Zg is the impedance of circuit internal probes connecting Z1 and Z2 to ground. If Zs, Zi and Zg are very low, Zx will be given by the formula in figure 7.

Assuming that the terminals of Zx, Z1 and Z2 are connected to chips (IC1 and IC2 in figure 7), electronic access to these points can be achieved by building into I/O interfaces the *analog boundary modules* (ABM) given in figure 8. While applying the measurement procedure described above, those cells to which Zx is connected will switch on bus AB1 for stimulus application, and switch on bus AB2 for response measurement. The cells connected to the ends of Z1 and Z2 that are opposed to Zx will be pulled

down by switching on VL. All analog boundary scan modules will provide for isolation of integrated circuit cores. The measurement technique in figure 7 and the analog module in figure 8 are part of the IEEE 1149.4 standard for mixed-signal test (IEEE, 1999).

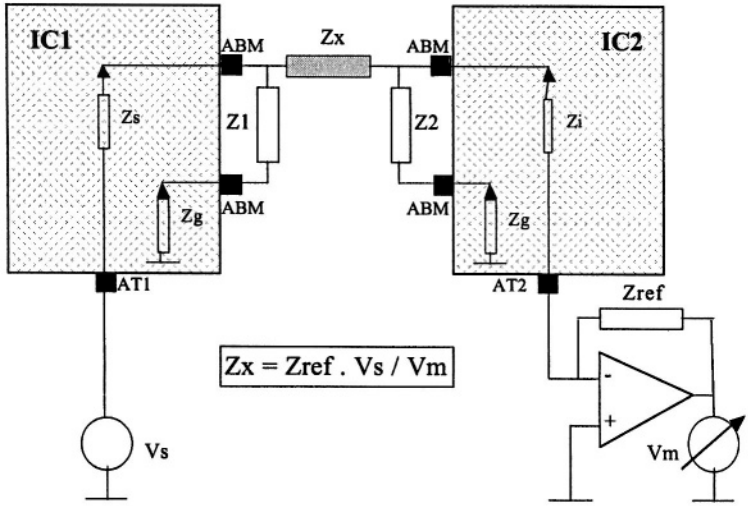

Figure 7. Analog in-circuit test.

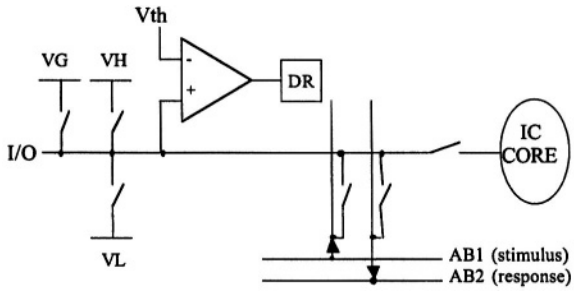

Figure 8. Analog boundary module (ABM).

As it can be seen from figure 9, this test standard extends the IEEE Std. 1149.1 to cope with the test of analog circuitry. The general architecture of the IEEE Std. 1149.4 infrastructure is given in the figure. To comply with the IEEE 1149.1 standard, it comprises a dedicated Test Access Port (TAP) composed of four required pins *TDI, TDO, TMS* and *TCK,* a collection of Digital Boundary Modules (DBM) associated with every digital function pin, and a test control circuitry composed of a TAP controller, an instruction register and an instruction decoder. These features permit loading and unloading of both instructions and test data and provide access to the core

circuitry for application and monitoring of digital test signals. The IEEE 1149.4 standard adds an Analog Test Access Port (ATAP), a Test Bus Interface Circuit (TBIC), Analog Boundary Modules (ABM) associated to every analog function pin and a two-wire internal analog test bus *(AB1/2)*.

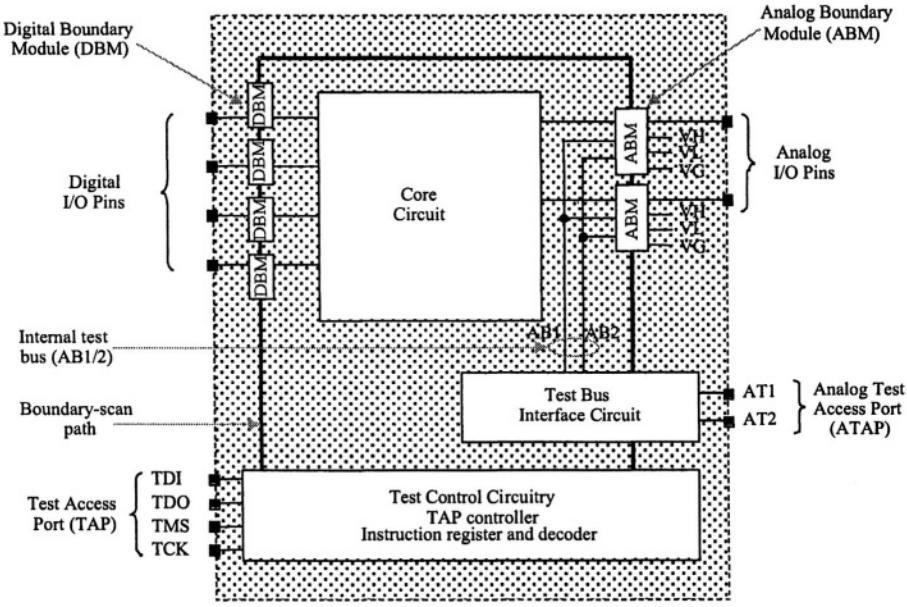

Figure 9. On-chip test architecture of an 1149.4-compliant integrated circuit.

More recently, the problem of ensuring good test accessibility to internal nodes has been considered at a much earlier stage of the IC design process, at the moment of choosing the method for the synthesis of the desired function. (Calvano, 2002), for example, presents a design for testability method that relies on the synthesis of filter transfer functions using partial fraction extraction. The transfer functions are built from 1st order building blocks for which very simple stimuli are disclosed for testing. The resulting filter is partitioned by construction and each individual fraction is made externally accessible through the available infrastructure provided by the IEEE Std.1149.4.

3.2 Built-in self-test

With the advances on integrated circuits, faster and more complex test equipments are needed to meet ever more demanding test specifications. Testers with demanding requirements of speed, precision, memory and noise are in general very expensive. An attractive alternative is to move some or

all of the tester functions onto the chip itself. The use of built-in self-test (BIST) for high volume production of integrated circuits is desirable to reduce the cost per chip during production-time testing.

An ideal BIST scheme should provide means of on-chip test stimulus generation, on-chip test response evaluation, on-chip test control and I/O isolation. The interest in a particular approach depends on its suitability to address the circuit faulty behaviours, and the cost and applicability of the technique.

All BIST methods have some associated cost in terms of area overhead and additional test pins. The additional BIST area required in the chip results in a decrease in yield. This penalty must be compensated by reducing test and maintenance costs. Moreover, by adding circuitry to the signal path, the BIST scheme in use can degrade the circuit performance.

Ideally, a BIST structure would be applicable for any kind of functional circuit. The diversity in design topologies and functional and parametric specifications prevents reaching this aim. However, some structured approaches are applicable to wide classes of circuits. The interest in a BIST technique is also related to the ability to perform diagnosis in the field and the possibility of reusing circuitry already available in the functional design.

3.2.1 Test generation and test compaction

Several BIST approaches were proposed in the past that are now common practice among digital designers. For instance, the merger of at-speed built-in test generation and output response analysis, with the scan path technique, culminated with the proposal of a multifunctional digital BIST structure named BILBO: Built-In Logic Block Observer (Koenemann, 1979).

In the realm of analog circuits, in last years some works have proposed on-chip structures for test generation and response evaluation.

In general, the stimulus generation for analog BIST depends on the type of test measurement to apply (Mir, 1995): DC static, AC dynamic or transient response measurements. DC faults are usually detected by a single set of steady state inputs; AC testing is typically performed using sine-wave forms with variable frequency; finally, pulse signals, ramps or triangular waveforms are the input stimuli for transient response measurements. Relaxation and sine-wave oscillators (Gregorian, 1986) are used for the generation of test signals. Dedicated sine-wave oscillators have already been proposed for multifrequency testing (Khaled, 1995). To minimise the test effort, individual test signals can be combined to form a multi-tone test signal (Lu, 1994; Nagi, 1995). To save hardware, a method to reconvert a sigma-delta D/A converter into a precision analog sine-wave oscillator has been proposed in (Toner, 1993). A practical approach to generate on-chip precise and slow analog ramps, intended for analog testing, has been

prototyped and validated in (Provost, 2003). (Azaïs, 2001) uses a similar on-chip ramp generator to perform histogram based tests of A/D converters. A different way of generating analog test stimuli consists on feeding pseudo-random digital test patterns into a D/A converter. In this method, called hybrid test stimulus generator (Ohletz, 1991), the digital patterns are generated as in a digital BILBO.

An alternative to existing on-chip test stimuli generators is the vectorless technique called Oscillation Test Method, OTM (Arabi, 1997a). In this approach, the Circuit Under Test (CUT) is converted into an oscillator by adding circuitry in a feedback loop, as shown in figure 10. The resulting circuit generates an oscillation frequency that can be expressed as a function of either the CUT components or its important parameters. In order to increase the fault coverage or to make the fault detection easier, the amplitude of the generated signal must be taken as a test measurement complementary to the oscillation frequency (Huertas, 2002a).

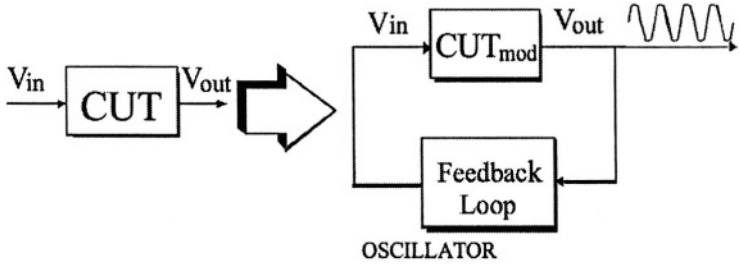

Figure 10. Basic idea of the oscillation test method.

The OTM was successfully applied to filters (Huertas, 2002b) and also to A/D converters (Arabi, 1997b; Huertas, 2003). Figure 11 illustrates the application of this test method to the built-in self-test of a converter (Arabi, 1997b). The oscillating input signal is generated through the charging or discharging of a capacitor with a positive or a negative reference current I, generated on-chip. The reference current is toggled depending on a comparison result between the A/D converter output code, C, and a desired output code, D, after each conversion. If $C < D$, the positive reference current is connected to the capacitor to set a positive slope in the test stimulus. If $C > D$, the negative reference current is chosen to obtain a negative slope in the test stimulus. Testing for the non-linearities of the converter is based on the measurement of the frequency of the signal on the switch control line *(ctrl),* that oscillates around a desired code transition level set by the BIST logic.

For analog circuits, the analysis of the output response is complicated by the fact that analog signals are inherently imprecise. The analysis of the output response can be done by matching the outputs of two identical

circuits. This is possible if the function designed leads to replicated sub-functions or because the circuit is duplicated for concurrent checking (Lubaszewski, 1995). When identical outputs are not available, three main approaches can be considered for analysing the test response (Mir, 1995): In the first approach, the analog BIST includes analog checkers which verify the parameters associated with the analog behaviour (according to the specification) for known input test signals (Slamani, 1993). The second approach consists on the generation of a signature that describes the waveform of the output response. A compaction scheme that uses a digital integrator has been reported in (Nagi, 1994). The third approach is based on the conversion of the analog test responses into digital vectors. This conversion can be performed by available blocks as they appear in the circuit under test or by means of some CUT reconfiguration. Similarly to a digital BILBO, whenever an A/D converter is available, the analog test responses can be fed into an output response analysis register to generate a signature (Ohletz, 1991). A bit-stream can also be obtained as test response output, if there exists in the CUT a block that can be configured as a sigma-delta modulator, for example. This is shown in (Cassol, 2003) for the case of analog filters built from a cascade of second order blocks. In that work, every filter stage is tested using a neighbour block that is reconfigured to work as a sigma-delta converter.

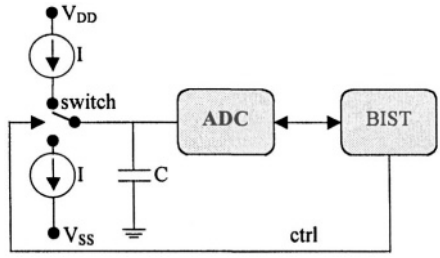

Figure 11. Oscillation BIST applied to A/D converter.

The ability of scanning signals and generating/compacting analog AC-tests using the same hardware has recently led to the proposal of a novel multifunctional BIST structure. This structure, called analog built-in block observer (ABILBO), recreates the digital BILBO versatility in the analog domain (Lubaszewski, 1996). Basically, the ABILBO structure is made up of two analog integrators and one comparator. A switched-capacitor implementation is given in figure 12. Since integrators have duplicated input stages as in figure 6, the operational amplifiers can work as voltage followers and then perform analog scan (model). With the operational amplifiers in the normal mode, switches can be properly programmed, such that either a sine-wave oscillator (mode2) or a double-integration signature analyser (mode3) results. The frequency of the quadrature oscillator obtained

in mode2 depends linearly on the frequency of the switching clock **(Φ1,Φ2).** The signature resulting from the selection of mode3 in the ABILBO structure corresponds to the time for the output of the second integrator to reach a predefined reference voltage **(V_{REF}).** If a counter is used for computing digital signatures, counting must be enabled from the integration start up to the time when the comparator output goes high. In (Renovell, 1997), the ABILBO mode for signature analysis is extended to cope with transient tests. Finally, both integrators can be reset by shorting their integration capacitors (mode4).

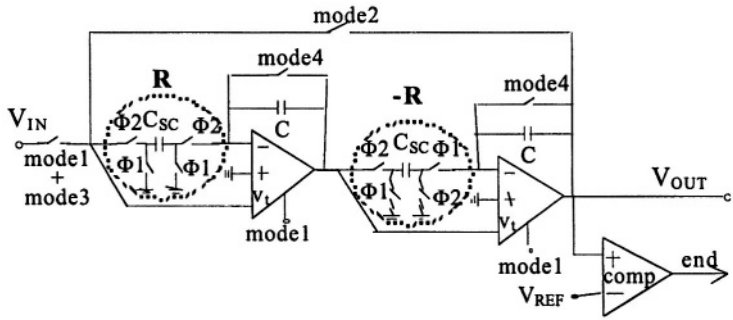

Figure 12. A switched-capacitor analog **BILBO.**

3.2.2 Current testing

Many faults, such as stuck-on transistors and bridging faults, result in higher than normal currents flowing through the power supplies of the circuit under test (Maly, 1988).

In the case of digital CMOS circuits, for example, these faults create a path between VDD and GND that should not exist in the fault-free circuit. Since the quiescent current becomes orders of magnitude higher than the expected leakage currents, these faults can be detected by using off-chip current sensors. This test method simplifies the test generation process, since the propagation of faults to the circuit primary outputs is no more required. In order to lower the evaluation time of the off-chip approach, intrinsically faster *built-in current sensors* can be used.

In the analog world, the same test method may apply to those circuits that present medium to low quiescent currents. For circuits with high quiescent currents, a possibility is to measure transients using specific *built-in dynamic current sensors.* The sensor proposed in (Argüelles, 1994) is shown in figure 13. It can be used to measure the dynamic current across the most sensitive branches of the circuit under test. To avoid performance degradation, this sensor is coupled to the circuit by means of an additional stage to existing current mirrors. As it can be seen from figure 13, in test mode (Enable=1), the transient current is firstly copied, next converted to a voltage and

amplified, and finally digitised. The sensor outputs a signature characterised by the number and width of pulses fitting a predefined time window.

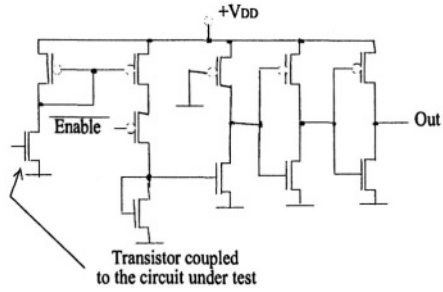

Figure 13. Built-in dynamic current sensor.

Potentially, methods based on current measurements can lead to unified solutions for testing digital and analog parts of mixed-signal integrated circuits (Bracho, 1995).

3.3 Self-checking circuits

In digital self-checking circuits, the concurrent error detection capability is achieved by means of functional circuits, which deliver encoded outputs, and checkers, which verify whether these outputs belong to error detecting codes. The most usual codes are the parity, the Berger and the double-rail code. The general structure of a self-checking circuit is shown in figure 14.

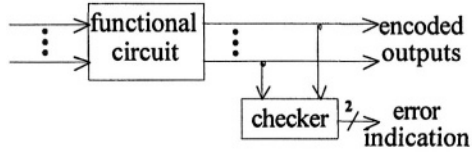

Figure 14. Self-checking circuit.

Most often, self-checking circuits are aimed at reaching the *totally self-checking goal:* the first erroneous output of the functional circuit results in an error indication in the checker outputs.

Similarly to digital self-checking circuits, the aim of designing *analog self-checking circuits* is to meet the totally self-checking goal. This is possible since analog codes can also be defined, for example the differential and duplication codes (Kolarík, 1995). A tolerance is required for checking the validity of an analog functional circuit and this is taken into account within the analog code.

The nodes to be monitored by an analog checker are not necessarily those associated with the circuit outputs, due to commonly used feedback circuitry. In addition, the most important difference is that the input and output code spaces of an analog circuit have an infinite number of elements. Therefore, the hypothesis considered for digital circuits becomes unrealistic, since an infinite number of input signals might be applied within a finite lapse of time. In order to cope with this problem, the self-checking properties are redefined for the analog world in (Nicolaidis, 1993).

In the last years, the self-checking principle has been applied to on-line testing analog and mixed-signal circuits, including filters and A/D converters (Lubaszewski, 1995). The major techniques employed for concurrent error detection are: *partial replication* of modular architectures, e.g. filters based on a cascade of biquads (Huertas, 1992) and pipelined A/D converters (Peralías, 1995); *continuous checksums* in state variable filters (Chatterjee, 1991); *time replication* in current mode A/D converters (Krishnan, 1992); and *balance checking* of fully differential circuits (Mir, 1996b).

The partial replication approach is illustrated in figure 15 for the case of a multistage pipelined A/D converter. Since the converter is built from a *cascade of identical functional modules,* the on-line testing capability can be ensured by an additional *checking module* identical to the converter stages and a multiplexing system. The *multiplexing system* must be such that the outputs of every stage can be compared against the outputs of the checking module, when the latter receives the same input as the former. The *control* gives the sequence of testing that evolves sequentially from the first (1) to the last (L) stage, and then restarts.

Figure 16 illustrates the principle of balance checking applied to fully differential integrated filters. In a correctly balanced fully differential circuit, the operational amplifier inputs are at virtual ground. But, in general, transient faults, deviations in passive components and hard faults in operational amplifier transistors corrupt this balance. In (Mir, 1996b), an analog checker is proposed which is capable of signalling balance deviations, i.e. the occurrence of a common-mode signal at the inputs of fully differential operational amplifiers. This same technique was used for on-line testing A/D converters in (Lubaszewski, 1995) and in (Francesconi, 1996). To improve accuracy of concurrent error detection in fully differential circuits, (Stratigopoulos, 2003a) presented a novel analog checker that dynamically adjusts the error threshold to the magnitude of the input signals. This analog checker was used in (Stratigopoulos, 2003b) to validate a new analog on-line testing approach based on circuit state estimation.

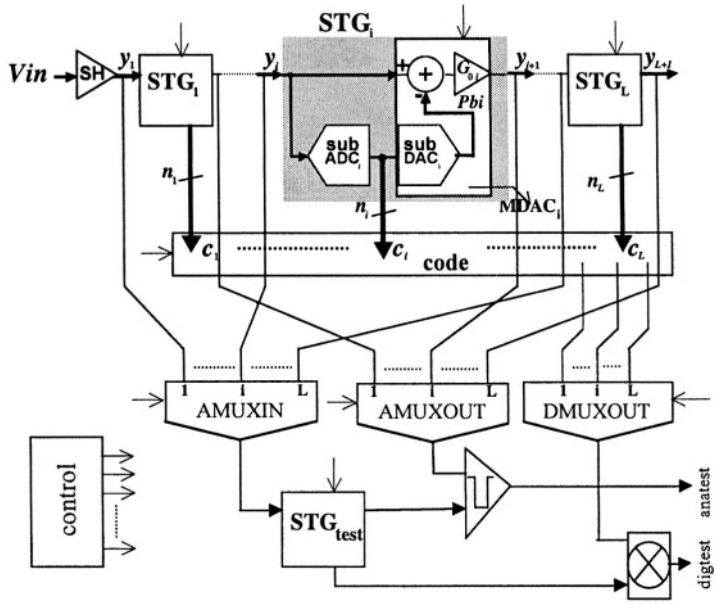

Figure 15. Pipelined A/D converter with on-line test capability.

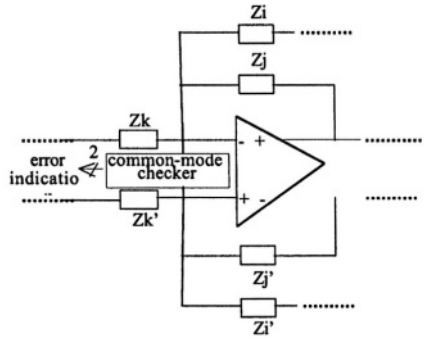

Figure 16. Generic stage of a self-checking fully differential filter.

3.4 Unified built-in self-test

Faults originating from an integrated circuit's manufacture typically manifest as multiple faults. However, conventional self-checking architectures only cover single faults. Besides that, fault latency may lead to the accumulation of faults and can invalidate the self-checking properties. In addition, when the checkers generate an error indication in these circuits, no mechanism exists to recognise if the detected fault is a transient or a permanent one. But this information is important to allow for diagnosis and repair in the field.

A solution to these problems has been given in (Nicolaidis, 1988). Nicolaidis proposes that built-in self-test capabilities similar to those used for production testing are embedded into self-checking circuits. These capabilities must be repeatedly activated, at periods of time no longer than the mean-time between failures. This technique, referred to as *unified built-in self-test (UBIST),* unifies *on-line and off-line tests,* covering all tests necessary during a system's lifetime: manufacturing, field testing and concurrent error detection. Moreover, it simplifies the design of checkers and increases the fault coverage of self-checking circuits.

In the analog domain, the first attempt to couple built-in self-test and self-checking capabilities was made by (Mir, 1996c). Mir proposes the design of a *test master* compliant with the IEEE Std. 1149.1 that efficiently shares hardware between the *off-line and on-line tests of fully differential circuits.* This test master relies on a programmable sine-wave oscillator for test generation and on common-mode analog checkers for test response evaluation. The frequencies to apply to the circuit under test are computed by the test generation tool described in (Mir, 1996a). For concurrent error detection, the checkers monitor the balance of the inputs of fully differential operational amplifiers. To allow for off-line fault detection and fault diagnosis, they additionally observe the balance of operational amplifier outputs (Mir, 1996b).

Another possibility of unifying tests is based on the partial replication scheme presented in the previous section. Assuming the analog filter based on a cascade of biquads shown in figure 17, the multiplexing scheme, the checking module and the comparison mechanism can ensure that *on-line tests* test 1, test 2 and test 3 are applied, in a time-shared manner, to individual filter stages. Since, in this case, the functional modules are not identical but similar, the checking module must be a programmable biquad capable of mimicking the behaviour of every individual filter stage.

The individual biquads can be designed such that they can accommodate, in *off-line test* mode, the *ABILBO structure* of figure 12. Then, off-line tests can be applied in three different phases: In phase test 1, biquad 1 will be tested with biquad 3 working as an oscillator (ABILBO 3) and biquad 2 working as a signature analyser (ABILBO 2). In phase test 2, biquad 2 will be tested with biquad 1 working as an oscillator (ABILBO 1) and biquad 3 working as a signature analyser (ABILBO 3). In phase test 3, biquad 3 will be tested with biquad 2 working as an oscillator (ABILBO 2) and biquad 1 working as a signature analyser (ABILBO 1). A feedback path from the output to the filter input is required to apply the phases test 1 and test 3. In summary, the biquads, while working as test generators, test individual filter stages off-line, and check the ability of the programmable biquad to mimic the filter stages on-line. While working as signature analysers, the biquads check that the test generators work properly, at the same time as they

improve the fault diagnosis capability. This occurs because they make it possible to recognise if a fault affects the stage under test or the programmable biquad. As illustrated by this example, the unification of off-line and on-line tests in modular analog circuits is, in general, expected to result in low performance degradation and low overhead penalty.

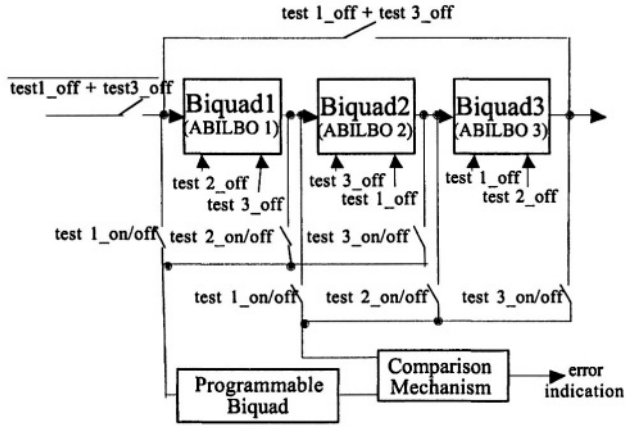

Figure 17. On-line/off-line test merger in a modular analog filter.

The unification of on and off-line tests was also proposed in the realm of data converters built from a cascade of identical functional modules. (Peralías, 1998) addressed the practical implementation of a test technique applicable to digitally-corrected pipelined A/D converters. Because of the self-correction capability, such a kind of converters has some inherent insensitivity to the effect of faults, which represents a disadvantage for testing and diagnosis. Authors show that potentially malfunctioning units can be concurrently identified with low extra circuitry and that the proposed test scheme can also be useful to reduce the time in production-level testing.

4. CONCLUSIONS

Existing design-for-test schemes and related test methods were extensively discussed in this chapter. The analog and mixed-signal cases were addressed, and testing issues were covered at the integrated circuit level. Some of these schemes are natural extensions of digital testing techniques that suffered some adaptations to cope with analog design constraints. Others are based on very specific functional and/or structural properties of particular classes of analog and mixed-signal circuits and signals.

Although structural design-for-test approaches offer, in general, more efficient implementations than specification-driven schemes, they cannot always ensure that the functional performances of the circuit are all met. Then, functional tests are still required, although they are much more time and resource consuming than fault-based approaches. A combination of functional and structural approaches may provide, in many situations, the best quality and cost trade off for analog and mixed-signal testing.

The major advantages of design-for-test over traditional external test methods can be summarised as follows:

- the enhanced accessibility to internal test points makes it possible to develop short test sequences that achieve high fault coverages. This leads to high quality tests, requiring short application times. As a consequence, reliability is improved and time-to-market is shortened;
- cheaper testers can be used, as performance, interfacing and functional requirements are relaxed. Design-for-testability, built-in self-test and self-checking alleviate the probing requirements for the test equipment. Built-in self-test and self-checking alleviate functionality, since test generation and/or response evaluation are performed on-chip.

The main drawbacks that come along with design-for-test are the following:

- an additional time is needed to design the test mechanisms to embed into integrated circuits and systems. However, the test development times for conventional testing methods are often longer. An alternative is to reuse pre-designed test cores;
- extra silicon is required to integrate test capabilities. However, embedded test structures have evolved over the years, and can now achieve very low area overheads. Additionally, the cost of transistors continues to drop.
- the performance of the circuit under test may be degraded by the additional test structures. Again, embedded test structures are expected to evolve, offering more efficient solutions. However, this is still a challenge for analog testing.

Reuse has been the keyword in the domain of integrated systems design. As new synthesis-for-test tools and test standards are developed, reuse tends also to dominate the testing of integrated circuits and systems. In fact, in the test domain this paradigm may not be limited to reuse pre-developed test cores in new designs. It can be further extended to reuse the same embedded test cores to perform different types of tests in different phases of a circuit's lifetime. These tests would allow for prototype debugging, manufacture testing, maintenance checking, and concurrent error detection in the field.

Only mechanisms based on unified off-line and on-line tests can add this dimension to the test reuse.

5. REFERENCES

Abramovici, M., Breuer, M.A. and Friedmann, A.D., 1990, *Digital Systems Testing and Testable Design,* Computer Science Press, New York.

Arabi, K. and Kaminska, B., 1997a, Testing analog and mixed-signal integrated circuits using oscillation-test method, *IEEE Trans. on CAD of Integrated Circuits and Systems* **16**(7).

Arabi, K. and Kaminska, B., 1997b, Oscillation built-in self test (OBIST) scheme for functional and structural testing of analog and mixed-signal circuits, in: *International Test Conference,* Proceedings, pp. 786-795

Argüelles, J., Martínez, M. and Bracho, S., 1994, Dynamic Idd test circuitry for mixed-signal ICs, *Electronics Letters* **30**(6).

Azaïs, F., Bernard, S., Bertrand, Y. and Renovell, M., 2001, Implementation of a linear histrogram BIST for ADCs, in: *Design Automation and Test in Europe,* Proceedings.

Bernard, S., Comte, M., Azaïs, F., Bertrand, Y. and Renovell, M., 2003, A new methodology for ADC test flow optimization, in: *International Test Conference,* Proceedings, pp. 201-209.

Bracho, S., Martínez, M. and Argüelles, J., 1995, Current test methods in mixed-signal circuits, in: *Midwest Symposium on Circuits and Systems,* Proceedings, pp. 1162-1167.

Bratt, A.H., Richardson, A.M.D., Harvey, R.J.A. and Dorey, A.P., 1995, A design-for-test structure for optimising analogue and mixed signal IC test, in: *European Design and Test Conference,* Proceedings, pp. 24-33.

Burns, M. and Roberts, G.W., 2001, *An Introduction to Mixed-Signal IC Test and Measurement,* Oxford University Press.

Calvano, J.V., Castro Alves, V., and Lubaszewski, M., 2000, Fault detection methodology and BIST method for 2^{nd} order Butterworth, Chebyshev and Bessel Filter Approximations, in: *IEEE VLSI Test Symposium,* Proceedings.

Calvano, J.V., Mesquita Filho, A.C., Castro Alves, V. and Lubaszewski, M., 2001, Fault models and test generation for OpAmp circuits – the FFM, *KAP Journal of Electronic Testing: Theory and Applications* **17**:121-138.

Calvano, J.V., Castro Alves, V., Mesquita Filho, A.C. and Lubaszewski, M., 2002, Filters designed for testability wrapped on the mixed-signal test bus, in: *IEEE VLSI Test Symposium,* Proceedings, pp.201-206,

Carro, L, and Negreiros, M., 1998, Efficient analog test methodology based on adaptive algorithms, in: *Design Automation Conference,* pp. 32-37,

Cassol, L., Betat, O., Carro, L. and Lubaszewski, M., 2003, The **ΣΔ-BIST** method applied to analog filters, *KAP Journal of Electronic Testing: Theory and Applications* **19**:13-20.

Caunegre, P. and Abraham, C., 1996, Fault simulation for mixed-signal systems, *KAP Journal of Electronic Testing: Theory and Applications* **8**:143-152.

Chatterjee, A., 1991, Concurrent error detection in linear analog and switched-capacitor state variable systems using continuous checksums, in: *International Test Conference,* Proceedings, pp. 582-591.

Cota, E.F., Lubaszewski, M. and Di Domênico, E.J., 1997, A new frequency-domain analog test generation tool, in: *International Conference on Very Large Scale Integration,* Proceedings, pp. 503-514.

Devarayanadurg, G. and Soma, M., 1994, Analytical fault modelling and static test generation for analog ICs, in: *International Conference on Computer-Aided Design,* Proceedings, pp. 44-47.

Devarayanadurg, G. and Soma, M., 1995, Dynamic test signal design for analog ICs, in: *International Conference on Computer-Aided Design,* Proceedings, pp. 627-629.

Eichelberger, E.B. and Williams, T.W., 1978, A logic design structure for LSI testability, *Journal of Design Automation and Fault-Tolerant Computing* **2**(2): 165-178.

Francesconi, F., Liberali, V., Lubaszewski, M. and Mir, S., 1996, Design of high-performance band-pass sigma-delta modulator with concurrent error detection, in: *International Conference on Electronics, Circuits and Systems,* Proceedings, pp. 1202-1205.

Gregorian, R. and Temes, G.C., 1986, *Analog MOS Integrated Circuits for Signal Processing,* John Wiley and Sons, New York.

Huertas, G., Vázquez, D., Peralías, E.J., Rueda, A. and Huertas, J.L., 2002a, Testing mixed-signal cores: a practical oscillation-based test in an analog macrocell, *IEEE Design and Test of Computers* **19**(6):73-82.

Huertas, G., Vázquez, D., Rueda, A. and Huertas, J.L., 2002b, Practical oscillation-based test of integrated filters, *IEEE Design and Test of Computers* **19**(6):64-72.

Huertas, G., Vázquez, D., Rueda, A. and Huertas, J.L., 2003, Oscillation-based test in oversampling A/D converters, *Elsevier Microelectronics Journal* **34**(10):927-936.

Huertas, J.L., Vázquez, D. and Rueda, A., 1992, On-line testing of switched-capacitor filters, in: *IEEE VLSI Test Symposium,* Proceedings, pp. 102-106.

IEEE Standard 1149.1, 1990, *IEEE Standard Test Access Port and Boundary Scan Architecture,* IEEE Standards Board, New York.

IEEE Standard 1149-4, 1999, *IEEE Standard for a Mixed Signal Test Bus,* IEEE Standards Board, New York.

Khaled, S., Kaminska, B., Courtois, B. and Lubaszewski, M., 1995, Frequency-based BIST for analog circuit testing, in: *IEEE VLSI Test Symposium,* Proceedings, pp. 54-59.

Kolarík, V., Mir, S., Lubaszewski, M. and Courtois, B., 1995, Analogue checkers with absolute and relative tolerances, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* **14**(5): 607-612.

Koenemann, B., Mucha, J. and Zwiehoff, G., 1979, Built-in logic block observation techniques, in: *Test Conference,* Proceedings, pp. 37-41.

Krishnan, S., Sahli, S. and Wey, C.-L., 1992, Test generation and concurrent error detection in current-mode A/D converter, in: *International Test Conference,* Proceedings, pp. 312-320.

LeBlanc, J.J., 1984, LOCST: A built-in self-test technique, *IEEE Design and Test of Computers,* November, pp. 45-52.

Lu, A.K. and Roberts, G.W., 1994, An analog multi-tone signal generator for built-in self-test applications, in: *International Test Conference,* Proceedings, pp. 650-659.

Lubaszewski, M., Mir, S., Rueda, A. and Huertas, J.L., 1995, Concurrent error detection in analog and mixed-signal integrated circuits, in: *Midwest Symposium on Circuits and Systems,* Proceedings, pp. 1151-1156.

Lubaszewski, M., Mir, S. and Pulz, L., 1996, ABILBO: Analog BuILt-in Block Observer, in: *International Conference on Computer-Aided Design,* Proceedings, pp. 600-603.

Mahoney, M., 1987, *DSP-based Testing of Analog and Mixed-Signal Circuits,* IEEE Computer Society Press, 1987.

Maly, W. and Nigh, P., 1988, Built-in current testing - feasibility study, in: *International Conference on Computer-Aided Design,* Proceedings, pp. 340-343.

Maunder, C.M., 1994, The test access port and boundary scan architecture: an introduction to ANSI/IEEE Std. 1149.1 and its applications, in: *Forum on Boundary Scan for Digital and Mixed-Signal Boards,* CERN, Geneva.

Meixner, A. and Maly, W., 1991, Fault modelling for the testing of mixed integrated circuits, in: *International Test Conference,* Proceedings, pp. 564-572.

Milor, L. and Visvanathan, V., 1989, Detection of catastrophic faults in analog integrated circuits, *IEEE Transactions on Computer-Aided Design* **8**(2): 114-130.

Mir, S., Lubaszewski, M., Liberali, V. and Courtois, B., 1995, Built-in self-test approaches for analogue and mixed-signal integrated circuits, in: *Midwest Symposium on Circuits and Systems,* Proceedings, pp. 1145-1150.

Mir, S., Lubaszewski, M. and Courtois, B., 1996a, Fault-based ATPG for linear analog circuits with minimal size multifrequency test sets, *KAP Journal of Electronic Testing: Theory and Applications* **9**:43-57.

Mir, S., Lubaszewski, M., Kolarík, V. and Courtois, B., 1996b, Fault-based testing and diagnosis of balanced filters, *KAP Journal on Analog Integrated Circuits and Signal Processing* **11**:5-19.

Mir, S., Lubaszewski, M. and Courtois, B., 1996c, Unified built-in self-test for fully differential analog circuits, *KAP Journal of Electronic Testing: Theory and Applications* **9**:135-151.

Mir, S., Rueda, A., Olbrich, T., Peralías, E. and Huertas, J.L., 1997, SWITTEST: Automatic switch-level fault simulation and test evaluation of switched-capacitor systems, in: *Design Automation Conference,* Proceedings.

Nácul, A.C., Carro, L., Janner, D. and Lubaszewski, M., 2002, Testing of RF mixers with adaptive filters, *Elsevier Microelectronics Journal* **(33)**10:847-853.

Nagi, N., Chatterjee, A. and Abraham, J.A., 1993a, DRAFTS: Discretized analog circuit fault simulator, in: *Design Automation Conference,* Proceedings, pp. 509-514.

Nagi, N., Chatterjee, A., Balivada, A. and Abraham, J.A., 1993b, Fault-based automatic test generator for linear analog circuits, in: *International Conference on Computer-Aided Design*, Proceedings, pp. 88-91.

Nagi, N., Chatterjee, A. and Abraham, J.A., 1994, A signature analyzer for analog and mixed-signal circuits, in: *International Conference on Computer Design,* Proceedings, pp. 284-287.

Nagi, N., Chatterjee, A., Balivada, A. and Abraham, J.A., 1995, Efficient multisine testing of analog circuits, in: *International Conference on VLSI Design,* Proceedings, pp. 234-238.

Nicolaidis, M., 1988, A Unified Built-in Self-Test Scheme: UBIST, in: *International Symposium on Fault Tolerant Computing,* Proceedings, pp. 157-163.

Nicolaidis, M., 1993, Finitely self-checking circuits and their application on current sensors, in: *IEEE VLSI Test Symposium,* Proceedings, pp. 66-69.

Ohletz, M., 1991, Hybrid Built-In Self-Test (HBIST) for mixed analog/digital integrated circuits, in: *European Test Conference,* Proceedings, pp. 307-316.

Osseiran, A., 1995, Getting to a test standard for mixed-signal boards, in: *Midwest Symposium on Circuits and Systems,* Proceedings, pp. 1157-1161.

Peralías, E., Rueda, A. and Huertas, J.L., 1995, An on-line testing approach for pipelined A/D converters, in: *IEEE International Mixed-Signal Testing Workshop,* Proceedings, pp.44-49.

Peralías, E., Rueda, A., Prieto, J.A. and Huertas, J.L., 1998, DFT & on-line test of high-performance data converters: a practical case, in: *International Test Conference,* Proceedings, pp.534-540.

Provost, B. and Sánchez-Sinencio E., 2003, On-chip ramp generators for mixed-signal BIST and ADC self-test, *IEEE Journal of Solid-State Circuits* **38**(2):263-273.

Renovell, M., Lubaszewski, M., Mir, S., Azais, F. and Bertrand, Y., 1997, A multi-mode signature analyzer for analog and mixed circuits, in: *International Conference on Very Large Scale Integration,* Proceedings, pp. 65-76.

Sebeke, C., Teixeira, J.P. and Ohletz, M.J., 1995, Automatic fault extraction and simulation of layout realistic faults for integrated analogue circuits, in: *European Design and Test Conference,* Proceedings, pp. 464-468.

Slamani, M. and Kaminska, B., 1993, T-BIST: A Built-in Self-Test for analog circuits based on parameter Translation, in: *Asian Test Symposium,* Proceedings, pp. 172-177.

Slamani, M. and Kaminska, B., 1995, Multifrequency analysis of faults in analog circuits, *IEEE Design and Test of Computers* **12**(2):70-80.

Soma, M., 1990, A design-for-test methodology for active analog filters, in: *International Test Conference,* Proceedings, pp. 183-192.

Soma, M. and Kolarík, V., 1994, A design-for-test technique for switched-capacitor filters, in: *VLSI Test Symposium,* Proceedings, pp. 42-47.

Stratigopoulos, H.-G.D. and Makris, Y., 2003a, An analog checker with dynamically adjustable error threshold for fully differential circuits, in: *IEEE VLSI Test Symposium,* Proceedings, pp. 209-214.

Stratigopoulos, H.-G.D. and Makris, Y., 2003b, Concurrent error detection in linear analog circuits using state estimation, in: *International Test Conference,* Proceedings, pp. 1164-1173.

Tsai, S.J., 1991, Test vector generation for linear analog devices, in: *International Test Conference,* Proceedings, pp. 592-597.

Toner, M.F. and Roberts, G.W., 1993, A BIST scheme for an SNR test of a sigma-delta ADC, in: *International Test Conference,* Proceedings, pp. 805-814.