Test Circuits for Substrate Noise Evaluation in CMOS Digital ICs

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Abstract — A Transition Controllable Noise Source (TCNS) generates substrate noises with controlled transitions in size, interstage delay, and direction. The noises are measured in a 100-ps 100-μV resolution by a linear substrate voltage detector that uses a front-end PMOS source follower probing substrate potential and a back-end latch comparator for sampling/digitizing the source follower output. A 0.4-μm CMOS test chip demonstrates the effectiveness of these circuits in performing advanced researches on the substrate noise.

I. Introduction

Mixed-Signal Systems on a Chip (MS-SoC) technology promises further VLSI circuit advancements. However, signal integrity is seriously degraded due to interference of digital switching noise with the analog and also digital circuit operations, which is mainly transmitted through the substrate. Practical requirements arise here in establishing reliable noise management methodologies based on exact and detailed understanding of the substrate noise properties.

II. Substrate Noise Source Circuit Design

Many published articles discuss the substrate noise injection and transmitting processes in a small scale circuit, for example, [1] and [2]. Our approach differing from them is the use of a noise source circuit that can generate the substrate noises under controlled transition distributions within a large digital block, and the interest is placed on a forming process of their waveforms.

A transition controllable noise source shown in Fig. 1 was developed for this purpose. The circuit has a multi-phase clock (Ck[0:10]) generator, which consists of odd delay elements in series, and a matrix of noise source blocks. The delay element has bias voltages V_n and V_p for regulating rise and fall delay, respectively. Inverse or non-inverse transition among the adjacent noise source blocks are selective. The number of noise source blocks to be activated by Ck[0:10] can be 0 to 15, which is set by address signals x[0:3] with 2^x weights. Finally, the circuit can generate substrate noises with controlled transitions in size, inter-stage delay, and direction. The noise source block includes 30 inverters operating in parallel. Each inverter has a 50 fF load capacitor against the substrate, which corresponds to input capacitances of two logic gates and 400 μm AL1 wires, and is designed to have a switching time of 200 ps.

III. Substrate Noise Detector Circuit Design

Another piece for accomplishing the research is a linear substrate voltage detector depicted in Fig. 3. It consists of a P-channel source follower (SF) used as a front-end level shifter and a back-end latch comparator (LC) digitizing the source follower output voltage (V_{sf}) by successive comparisons with an external step reference voltage with ΔV. The source follower is isolated from the substrate by an N-type well and has a P^+ contact probe picking up the substrate voltage. The on-chip latch comparator eliminates parasitic passive elements in assembly and in probes of measurement equipment, that can easily degrade detector bandwidth if attached to the SF's output node. A differential comparator shown in Fig. 3(a) was chosen for the LC because a high temporal resolution could be expected due to the large gain in the positive feedback. The detector realizes a direct probing of the substrate noise with highly linear sensitivity within a designed bandwidth of 2 GHz, and moreover, enables absolute evaluation of the noise, including consideration of polarity. The detector gain can be calibrated by measuring external reference sine waves.

A measurement timing diagram is shown in Fig. 3(b). Clock pulses $\phi_1 \sim \phi_3$ are used for the comparator, where ϕ_1 determines a test point at T_{cmp}, ϕ_2 separates the region of decision from that of offset canceling, and ϕ_3 latches the output. The other clock P_{in} stimulates the multi-phase clock generator of the noise source and is shifted with Δt relatively to the T_{cmp}, and the readout process of V_{sf} is carried out at every timing. The series of V_{sf} reproduces a substrate noise waveform, as is the way similar to that in a sampling oscilloscope. Resolutions of $\Delta V = 100$ μV and $\Delta t = 100$ ps are achieved in our fully automated substrate noise measurement system.

IV. Experimental prototype and measurement examples

Figure 4 shows a microphotograph of a test chip fabricated in a 0.4-μm CMOS, P-type bulk substrate with a single N-well, triple-metal double-poly-Si technology. Circuits were designed with 3.3-V supply voltage. A symmetric axis of the LC faces the TCNS so as to eliminate asymmetry in the noise intensity due to the disparity

in distance. Exclusive pairs of power supply and return wirings with dedicated bond pads are provided for the noise source and for the detector.

A set of typical measured substrate noises is given in Fig. 5, where every delayed edge is in a rise transition. Eleven sub-peaks that coincide with the noise source block action driven by the 11 non-inverse phase clocks (Ck[0:10]) are clearly observed in a 100-ps 100-μV resolution. Sub-peak amplitudes increase with the number of active noise source blocks. The chip has been tested detailedly for general understanding of the substrate noises in CMOS mixed-signal integrated circuits. Results are reported in [3].

V. Conclusions

An advanced experimental methodology for quantifying substrate noise properties is demonstrated.

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References

[1] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE J. Solid-State Circuits*, Vol. 28, No. 4, pp. 420-430, Apr. 1993.

[2] K. M. Fukuda, T. Kikuchi, T. Matsuura, and M. Hotta, "Measurement of Digital Noise in Mixed-Signal Integrated Circuits," *IEEE J. Solid-State Circuits*, Vol. 30, No. 2, pp. 87-92, Feb. 1995.

[3] M. Nagata, J. Nagai, T. Morie, and A. Iwata, "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment," *IEEE Trans. on Computer-Aided Design*, Vol. 19, No. 6, pp. 671-678, Jun. 2000.

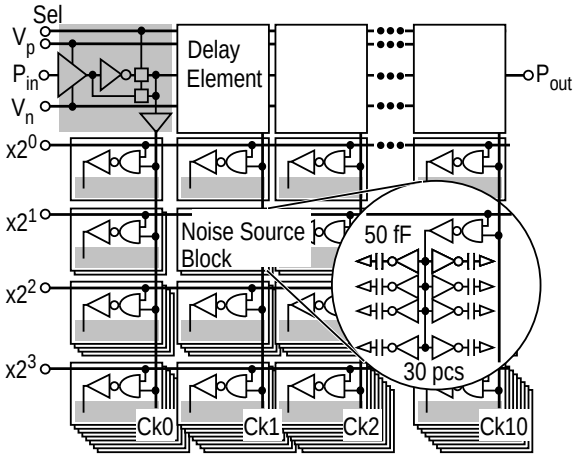

Fig. 1. Transition-controllable noise source circuit.

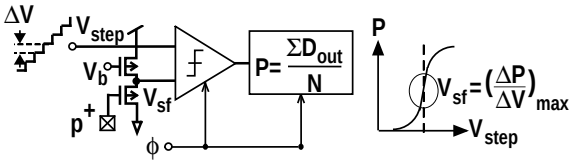

Fig. 2. Linear substrate voltage detector circuit.

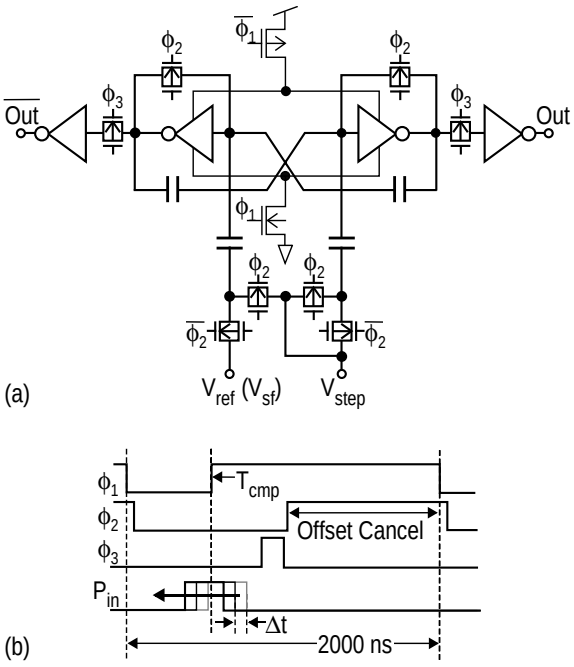

Fig. 3. Latch comparator. (a) Circuit schematic. (b) Timing diagram.

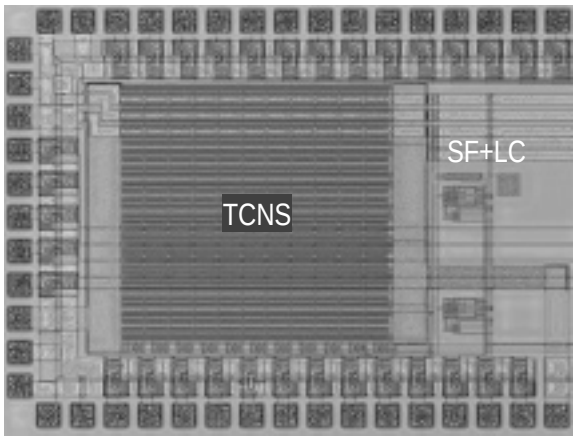

Fig. 4. Microphotograph of 0.4-μm CMOS test chip.

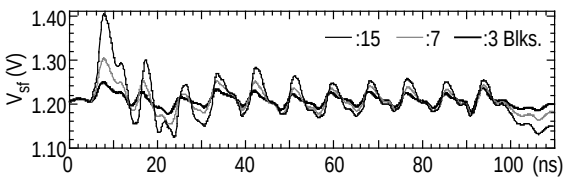

Fig. 5. Measured substrate noise waveforms with a 100-ps 100-μV resolution. All the noise source inverters act in rise transition, and the number of active noise source blocks is taken as a parameter.