Test Infrastructure Design for Mixed-Signal SOCs With Wrapped Analog Cores

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***Abstract*—Many system-on-chips (SOCs) today contain both digital- and analog-embedded cores. Even though the test cost for such mixed-signal SOCs is significantly higher than that for digital SOCs, most prior research in this area has focused exclusively on digital cores. We propose a low-cost test development methodology for mixed-signal SOCs that allows the analog and digital cores to be tested in a unified manner, thereby minimizing the overall test cost. The analog cores in the SOC are wrapped such that they can be accessed using a digital test access mechanism (TAM). We evaluate the impact of the use of analog test wrappers on area overhead and test time. To reduce area overhead, we present an analog test wrapper optimization technique, which is then combined with TAM optimization in a cost-oriented heuristic approach for test scheduling. We also demonstrate the feasibility of using analog wrappers by presenting transistor-level simulations for an analog wrapper and a representative core. We present experimental results for three SOCs from the ITC '02 test benchmarks that have been augmented with three analog cores: an I-Q transmit path pair and an audio CODEC path used in cellular phone applications.**

***Index Terms*—Full-chip testing, mixed-signal SOC testing, SOC testing, test access mechanism (TAM) optimization, test scheduling, wrapper design.**

I. Introduction

ADVANCES in semiconductor technology are contributing to the increasing complexity of system-on-chip (SOC) integrated circuits. Many SOCs in use today are mixed-signal circuits containing both digital and analog embedded cores [1], [2]. There are enormous costs associated with the testing of mixed-signal SOCs [3], [4]. The cumulative test cost for an SOC has three significant components: 1) the cost of the automatic test equipment (ATE); 2) the cost of silicon area overhead due to the on-chip test hardware; and 3) the cost due to test application time. In order to reduce the overall test cost of mixed-signal SOCs, all of the above components of the test cost should be minimized.

Most prior research on test cost reduction for SOCs has focused on digital SOCs. However, since the test cost of a mixed-signal SOC is much higher than that of digital SOCs [3] and many SOCs today have significant analog content, there is a need for efficient test methodologies that can handle mixed-signal SOCs and reduce their test cost. Many consumer electronics products such as MP3 players, PDAs, and audio receivers contain a small number of analog cores that operate in the low- to mid-frequency range; these cores are embedded in a "big-D/small-A" SOC, together with a large number of digital cores. Consumer electronics products belong to a high-volume, low-profit-margin domain, where reducing test cost is of prime importance.

Modular test is increasingly being used to test core-based SOCs [5], [6]. Advantages of modular testing include reduced automatic test pattern generation (ATPG) complexity and greater test reuse. All embedded cores are tested in a stand-alone manner, which is mandatory for embedded non-logic components such as memories and analog modules, as well as black-box third-party cores [6]. In modular test, an on-chip test access infrastructure is used, which consists of test wrappers and test access mechanisms (TAMs). Test wrappers isolate the various modules from their surrounding circuitry during test. TAMs transport test stimuli and responses between SOC pins and module terminals, and *vice versa*. The design of wrappers and TAMs has a significant impact on test application time and the vector memory depth required on the tester.

In this paper, we propose a modular test approach for mixed-signal SOCs. We focus on the optimization of a unified test access architecture that is used for both digital and analog cores. We formulate a global test resource optimization problem for the entire SOC, instead of treating the digital and analog portions separately. In order to provide an efficient interface mechanism, we wrap each analog core by a pair of digital-to-analog converter (DAC) and analog-to-digital (ADC) data converters and a digital configuration circuit. Analog test wrappers (ATWs) reduce test cost in two ways.

1) They convert analog cores into virtual digital cores, which allows the use of digital testers to test the analog cores. This reduces the need for expensive mixed-signal testers, thereby resulting in significant test cost reduction.
2) They allow a unified modular test methodology that results in a substantial reduction in the test application time for the SOC.

ATWs, however, add to the chip area. We propose a new resource optimization technique that reduces the overall area and routing overhead by using shared test wrappers for the time-multiplexed testing of analog cores. We combine the resource optimization approach with a previously developed TAM optimization approach [7]; the combined method leads to a TAM architecture that is efficient in terms of area, routing cost, and overall SOC testing time.

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In the absence of mixed-signal SOC benchmarks, we present results for a "mixed-signal SOC" that has been crafted by adding five analog cores to digital SOCs from the ITC'02 SOC test benchmarks [8]. These results demonstrate that a significant reduction in the overall test cost can be achieved using the proposed approach. We also implement the proposed ATW in a 0.5-μm AMI technology and present transistor-level simulation results.

The rest of this paper is organized as follows. We present related prior work in Section II. We present the proposed analog test wrapper in Section III. In Section IV, we describe conversion of analog test requirements into digital test requirements such that the tests for both the digital and the analog cores are defined in a uniform manner. In Section V, we detail the analog wrapper optimization approach, which is followed by a description of the cost-optimization approach in Section VI. In Section VII, we present experimental results for three ITC'02 benchmark SOCs augmented with five representative analog cores. Finally, we summarize the paper in Section VIII.

II. Prior Work

In this section, we review some test methods that have been proposed for mixed-signal SOCs. We also present the problem of test infrastructure design for the modular test of digital SOCs, and discuss the two TAM optimization methods used in this paper.

A. Mixed-Signal SOC Test

In traditional mixed-signal SOC testing, tests for analog cores are applied either from chip pins through direct test access methods, e.g., via multiplexing, or through a dedicated analog test bus [9], [10]. This strategy requires the use of expensive mixed-signal testers. For mid- to low-frequency analog applications, the data is often digitized at the tester, where it is affordable to incorporate high-quality data converters. In most mixed-signal ICs, analog circuitry accounts for only a small part of the total silicon ("big-D/small-A"). However, the total manufacturing test cost is dominated by analog test cost. This is because expensive mixed-signal testers are employed for extended periods of time, resulting in high overall test cost. A natural solution to this problem is to implement the data converters on-chip. Since most SOC applications do not push the operational frequency limits, the design of such data converters on-chip appears to be feasible. Until recently, such an approach has not been deemed desirable due to its high hardware overhead. However, as the cost of on-chip silicon is decreasing, and the functionality and the number of cores in a typical SOC are increasing, the addition of data converters on-chip for testing analog cores now promises to be cost-efficient. These data converters eliminate the need for expensive mixed-signal test equipment.

The use of on-chip data converters has been proposed in [11]–[16]. In [13], the construction of an analog oscillator based on digital filter design principles is discussed. In [16], an analog oscillator is used to measure the signal-to-noise ratio of a $\Sigma - \Delta$ ADC by taking the fast Fourier transform (FFT) of the digital output signal. In [12], the outputs of several such single-tone signal generators are added to generate a multi-tone signal; this signal generator is then used to measure inter-modulation distortion and frequency response through an on-chip signal processor [17]. In a similar manner, a $\Sigma - \Delta$ DAC and bit streams stored on-chip are used to generate analog signals in [11]. In order to keep the hardware overhead low, a short $\Sigma - \Delta$ bit stream is stored on chip and applied periodically. Several BIST techniques have also been proposed for mixed-signal blocks that cannot be directly tested by an ADC–DAC pair. Such BIST techniques target either data converters themselves [18]–[21] or phase-locked loops (PLLs) [22]–[24].

In [14], the analog circuitry is placed between an ADC and a DAC, and is tested through pseudorandom digital patterns. Such pseudorandom digital patterns are considered to have similar characteristics to white noise, which covers a wide frequency spectrum. The correlation between the output samples and the discretized transfer function is then utilized to determine the pass/fail criteria. In [15], a stand-alone core is used for process monitoring, frequency analysis, linearity testing, and timing measurement.

A considerable amount of research has also been carried out in defining core-level measurement and test methods. In order to reduce the overall testing time for analog circuits, a subset of specifications is selected for test through the use of full specification data on a sample of fabricated chips [25]. In [26] and [27], process distributions, simulation-based methods such as Monte Carlo analysis, and a simple polynomial regression algorithm, are used to eliminate the need for sample production data. The goal is then to select a set of specifications that is most likely to fail under the given process distributions.

Automated generation of test stimuli is the goal of the approaches outlined in [28] and [29], which employ output signal sensitivity to circuit parameters. In [28] and [29], test inputs are defined as single tone sinusoidal signals with frequency as an unknown parameter. The frequency at which the sensitivity of the output voltage (voltage gain) of the circuit is highest to a given component is selected to test it. Sensitivities are determined by manual analysis in [29], and by circuit simulations and the use of the adjoint network method in [28].

From the above discussion of prior work, we note that several test methods have been explored for on-chip analog circuits. However, a unified test methodology for chips containing both analog and digital cores has not been investigated. The test methods thus far, have addressed the test of analog circuits independent of surrounding digital logic.

B. Test Infrastructure Design

In the digital domain, the use of modular test for efficient test of digital SOCs has been widely studied in the literature [30]–[37]. The problem of test access infrastructure optimization to minimize the SOC testing time, has been shown to be $\mathcal{NP}$-hard [38]. As a result, a number of efficient heuristic methods have been proposed [35]–[37], [39]–[41], [43]. Dedicated and scalable TAMs such as Test Bus [42] and TestRail [40] architectures appear to be the most common.

A number of TAM optimization techniques target fixed-width test bus architectures [34], [36], [37], [43]. In a fixed-width architecture, the total TAM width is partitioned among a number

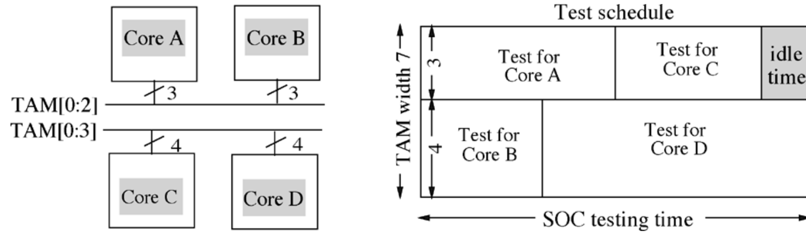

Fig. 1. TAM design using fixed-width test buses [34].

of fixed-width test buses and each core is assigned to one of these TAM partitions (see Fig. 1).

The authors in [34] presented a Test Bus architecture that is optimized using a combination of integer linear programming (ILP) and exhaustive enumeration. Given an SOC with N cores, the optimization problem in [34] is formulated as follows.

Determine: 1) the number B of TAM partitions for the SOC; 2) a partition of the total TAM width W among the TAMs; 3) an assignment of the N cores to TAMs; and 4) a wrapper design for each core, such that SOC testing time is minimized. The problem of test wrapper design was solved in [34] using the *Design_wrapper* algorithm, which is based on the Best Fit Decreasing heuristic [45]. The core assignment problem was solved using an ILP model, formulated as follows.

Consider an SOC with N cores and B TAMs of widths $w_1, w_2, \ldots, w_B$. The time taken in clock cycles to test Core i assigned to TAM j is denoted by $T(w_j)$. Let x_{ij} be a binary variable, defined as follows:

$$x_{ij} = \begin{cases} 1, & \text{if core } i \text{ is assigned to TAM partition } j; \\ 0, & \text{otherwise.} \end{cases}$$

The time taken to test all cores on TAM j is given by $\sum_{i=1}^{N} T_i(w_j)x_{ij}$. Since all the TAMs can be used simultaneously for testing, the system testing time equals $\max_{1\leq j\leq B} \sum_i^N T_i(w_j)x_{ij}$. A mathematical model for core assignment can be formulated as follows.

Objective: Minimize testing time $\mathcal{T}$, subject to:

1) $T \geq \sum_{i=1}^{N} T_i(w_j)x_{ij}, 1 \leq j \leq B$, i.e., $\mathcal{T}$ is the maximum testing time on any TAM;
2) $\sum_{j=1}^{B} x_{ij} = 1, 1 \leq i \leq N$, i.e., every core is assigned to exactly one TAM.

Standard linearization techniques are used in [34] to subsequently obtain an ILP model. It was observed in [34] that the ILP model for core assignment can be solved in reasonable time for a small number of TAM partitions. Hence, a brute-force method, referred to as the ILP/enumerate approach, was used to exhaustively enumerate TAM partitions. A major drawback of this brute-force method is that it does not scale for $B > 3$. The execution time increases exponentially with B and, thus, the algorithm fails to yield results for $B > 3$ in reasonable CPU time.

The optimization approach of [34] was extended in [43], to include a heuristic method for core assignment. The heuristic approach uses three steps for TAM optimization. In the first step, a heuristic algorithm called *Core_assign* is used for assigning cores to TAMs. In the second step, a procedure termed *Partition_evaluate* is used to enumerate and evaluate a large number of TAM partitions. A solution-space-pruning technique is used to limit the number of unique partitions evaluated, thereby ensuring feasible execution times for large problem instances. As a final optimization step, the ILP model is used only once to improve the solution.

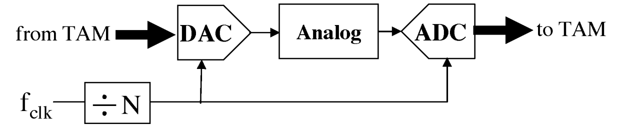

Fig. 2. On-chip digitization of analog test data.

In [7] and [41], methods were presented to integrate TAM design and test scheduling using rectangle packing. In [7], the notion of flexible-width test buses was introduced and a fork-and-merge test bus architecture was used. In this approach, the embedded cores in an SOC are allowed to be connected to any subset of the top-level TAM wires, thereby improving the utilization of the TAM wires. However, a drawback of this approach is that it can potentially increase the complexity of physical design due to more complicated routing of TAM wires. In this paper, we explore the use of both flexible-width and fixed-width TAM architectures for mixed-signal SOC tests; we use the TAM optimization methods presented in [7] and [43].

In all of the above methods, it is assumed that the SOC consists only of digital cores. As a result, these techniques are not directly applicable to mixed-signal SOCs.

III. Test Wrapper for Analog Cores

In order to facilitate a unified test access mechanism for the full-chip testing of SOC, it is necessary to convert analog test signals and responses into the digital domain. Furthermore, the digitized test signals need to be translated into analog signals for the analog core. A flexible-width interface is also required between the digital TAM and the primary I/Os of the analog core. An analog test wrapper can be used to translate the sampled analog test stimuli into continuous analog test signals for the analog core. Similarly, the analog test responses can be translated into digital responses by the wrapper to be analyzed by the digital ATE. The test information for a wrapped analog core includes only digital test patterns, clock frequency, the test configuration, and pass/fail criteria. Thus, the wrapper converts the analog core into a virtual digital core with strictly sequential test patterns, which are the digitized analog signals. In order to utilize test resources efficiently, the analog wrapper needs to provide sufficient flexibility in terms of required resources with respect to all the test needs of the analog core. One way to achieve

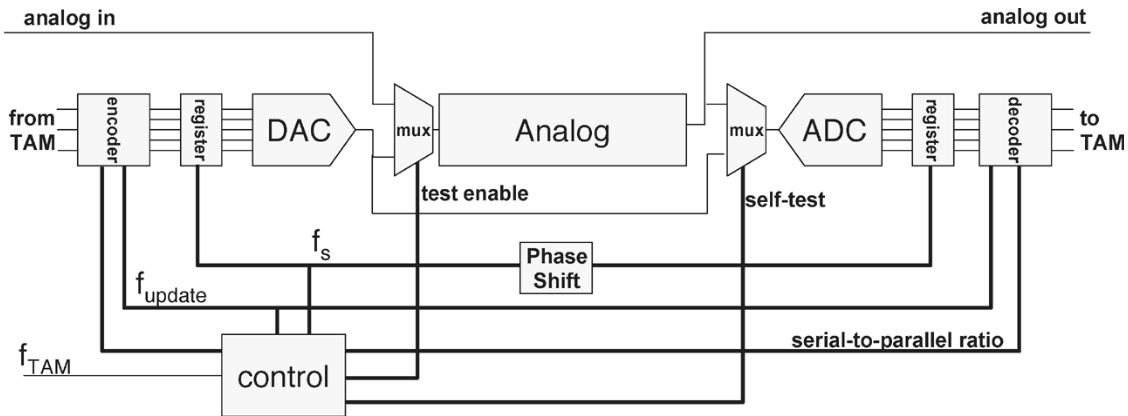

Fig. 3. Block diagram of the analog test wrapper.

this uniform test access scheme for analog cores is to provide an on-chip ADC-DAC pair that can serve as an interface between each analog core and its digital surroundings, as shown in Fig. 2.

Analog tests are provided by the core vendor to the system integrator. In the case of analog testers, these signals are digitized at the high-precision ADCs and DACs of the tester. In case of on-chip digitization, the analog wrapper needs to include the lowest cost data converters that can still provide the required frequency and accuracy for applying the core tests. Thus, on-chip conversion of each analog test to digital patterns imposes requirements on the frequency and resolution of the data converters of the analog wrapper. Thus, the on-chip implementation of data converters can be used for a wide range of low-frequency audio applications. These converters need to be designed to accommodate all the test requirements of the analog core.

Analog tests may also have a high variance in terms of their frequency and test time requirements. While tests involving low-frequency signals require low bandwidth and high test times, tests involving high-frequency signals require high bandwidth and low test time. Keeping the bandwidth assigned to the analog core constant results in under-utilization of the precious test resources. The variance in analog tests has to be fully exploited in order to achieve an efficient test plan. Thus, the analog test wrapper has to be designed to accommodate multiple configurations with varying bandwidth and frequency requirements.

Fig. 3 shows the block diagram of the proposed analog wrapper that can accommodate all the above mentioned requirements. The control and clock signals generated by the test control circuit are highlighted. The registers at each end of the data converters are written and read in a semi-serial fashion depending on the frequency requirement of each test. The digital test control circuit selects the configuration for each test. This configuration includes the divide ratio of the digital TAM clock, the serial to parallel conversion rate of the input and output registers of the data converters, and the test modes.

Some applications may already have on-chip data converters that can be used as part of the ATW architecture in the test mode, thereby reducing the area overhead on the ATW. ATWs can also be used in conjunction with other BIST techniques. Moreover, BIST techniques that may require analog stimuli for start-up can exploit the use of analog test wrappers to transport the stimuli using digital test access mechanisms, thereby reducing the need for mixed-signal testers. Thus, our modular test approach can leverage existing BIST techniques, and *vice versa*.

A. Analog Test Wrapper Modes

In the normal mode of operation, the analog test wrapper is transparent; the primary I/O pins of the analog core are directly accessible in this mode. In contrast, in the test mode, the primary I/Os are connected to the data converters. The ATW has two test modes, namely a *self-test* mode and a *core-test* mode. Before the ATW is configured in the core-test mode, the wrapper data converters have to be characterized for their conversion parameters, such as the nonlinearity and the offset voltage in the self-test mode. The self-test mode is enabled through the analog multiplexer at the input of the wrapper ADC, as shown in Fig. 3. The parameters of the DAC–ADC pair are determined in this mode and are used to calibrate the measurement results. Once the self-test of the test wrapper is complete, core test can be enabled by turning off the self-test bits.

In the test modes, multiple tests can be applied to the core, serially in time. Each test may have a different frequency and TAM width requirements. For each analog test, the encoder is set to the corresponding serial-to-parallel conversion ratio (*cr*), where it shifts the data from the corresponding TAM inputs into the register of the ADC. Similarly, the decoder shifts data out of the DAC register. The update frequency of the input and output registers is $f_{\rm update} = f_s \times cr$, where f_s is the sampling frequency. The serial-to-parallel ratio cr is chosen such that $f_{\rm update}$ is always less than the TAM clock rate, $f_{\rm TAM}$. For example, if the test TAM width requirement is 2 bits and the resolution of the data converters is 12 bits, $cr = 1/6$, i.e., the input and output registers of the data converters are clocked at a rate 6 times less than the clock of the encoder, and the input data is shifted into the encoder and out of the decoder at a 2-bits/cycle rate. The complexity of the encoder and the decoder depends on the number of distinct bandwidth and TAM assignments (the number of possible test configurations). In order to limit the complexity of the encoder-decoder pair, the number of such distinct assignments have to be limited. This requirement can be imposed in the chip-level test scheduling optimization algorithm.

B. Design of Wrapper Data Converters

As in the digital case [6], analog wrappers can be designed either by the core provider or by the system integrator. In the first scenario, the system integrator only needs to know the clock frequency and test patterns. This approach provides the system integrator high flexibility in terms of test resource partitioning, and the core provider the chance to fine-tune the converter design with respect to the core test needs. However, it also results in high test hardware overhead. A more frugal approach is to let the system integrator design the data converters, which can be shared by several cores. In this case, each core provider supplies the information about the test specifications for the analog core such as maximum frequency of operation, power, shape, number of samples, and analysis method. These test specifications of the analog core can be mapped to the parameter specifications of the data converters. In [44], an efficient design methodology is proposed for the design of ATW data converters. The design methodology includes a parameter translation method that maps the analog core's test specifications to the data converter parameters such as resolution, differential nonlinearity (DNL), integral nonlinearity (INL), signal-to-noise ratio (SNR), total harmonic distortion (THD), and spurious-free dynamic range (SFDR). The hardware overhead of the data converters in the ATW can be reduced by added flexibility of sharing data converters among several analog cores. Also, if an application already has an ADC or DAC on-chip, it can be incorporated in an ATW, and can be used for the test of analog cores.

The design of data converters used in SOC applications is challenging due to the need to optimize for speed, resolution, and power consumption. However, the design of test wrappers is relatively easier because power consumption is of lesser concern for test hardware since these converters are turned off during the normal mode of operation.

IV. Analog Tests and Test Requirements

Test requirements are imposed on the digitization of the analog test signals to maintain a certain test accuracy for the analog core. In this section, we elaborate on the various test requirements and present an example of a wrapped analog core test.

In order to utilize an ADC–DAC pair as an interface mechanism for an analog core, its operational frequency must be within the Nyquist frequency of the data converters. In addition, the data converters must provide adequate resolution to apply and observe the weakest test signal given by the core providers. Data converters with a 10-bit resolution that can work at several hundred megahertz are available in CMOS technology today [46]. Thus, the conditions on the frequency and the resolution of the data converters preclude only RF applications from the unified TAM architecture. This is not a stringent limitation since most SOC analog data acquisition and processing is limited to low- to mid-frequencies [1]. An analog test can be represented in terms of a sampling frequency and a number of samples to be taken. The sampling frequency has to be adjusted to meet the Nyquist criterion for the highest frequency signal component. The number of samples are chosen such that at least several full periods of the lowest frequency signal component are sampled. If an analog test contains frequencies ranging from $f_{\min}$ to

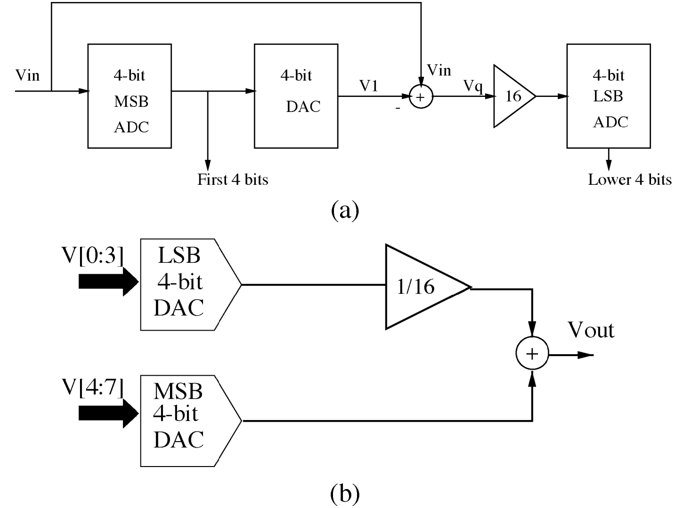

Fig. 4. (a) Block diagram of a modular 8-bit ADC [47]. (b) Block diagram of a modular 8-bit DAC.

$f_{\max}$, the sampling frequency f_s is set higher than $2f_{\max}$. The test time has to be long enough to cover at least two full periods of the lowest frequency signal, thus, it is set higher than $2/f_{\min}$.

In order to prevent any signal distortion, the analog signal is sampled at uniform intervals. As a result, an analog core requires a TAM with a bandwidth that is capable of providing data at the required sampling frequency f_s. In order to incorporate this condition into the test resource allocation algorithm, the cost of assigning a smaller bandwidth to the analog core is set to be infinite. If a TAM with adequate bandwidth is available, the cost is defined in terms of the test time. The test time is expressed in terms of digital clock cycles and it depends on the frequency ratio between the TAM clock and the sampling frequency. As a result, the resource requirements of the analog core are given by

$$T = \frac{N_s \cdot f_{\mathrm{TAM}}}{f_s}; \qquad w \geq \frac{f_s}{f_{\mathrm{TAM}}} \cdot \max\{R_{\mathrm{ADC}}, R_{\mathrm{DAC}}\}$$

where T is the time in clock cycles, f_s is the sampling frequency, f_{TAM} is the TAM clock frequency, N_s is the number of samples to be collected, w is the required TAM width, and R_{ADC} and R_{DAC} represent the number of bits of the data converters. While each analog test has to be applied in a nonpreemptive manner, individual tests can be applied independently of each other without overlap in time, thereby providing greater flexibility in test scheduling.

A. Case Study

We next present implementation details of the analog test wrapper and demonstrate its functionality by applying a test to a wrapped analog core. We design the wrapper using an 8-bit DAC–ADC pair. All simulations and layout are done in a 0.5-μm process technology.

The implementation of the ADC and DAC in a wrapper is critical to the performance and area overhead of the wrapper. We use a modular pipelined architecture for the 8-bit ADC [47], using two 4-bit flash ADCs and one 4-bit DAC. Fig. 4(a) shows a block diagram of the ADC. The modular architecture of the ADC reduces the area overhead significantly. An N-bit flash

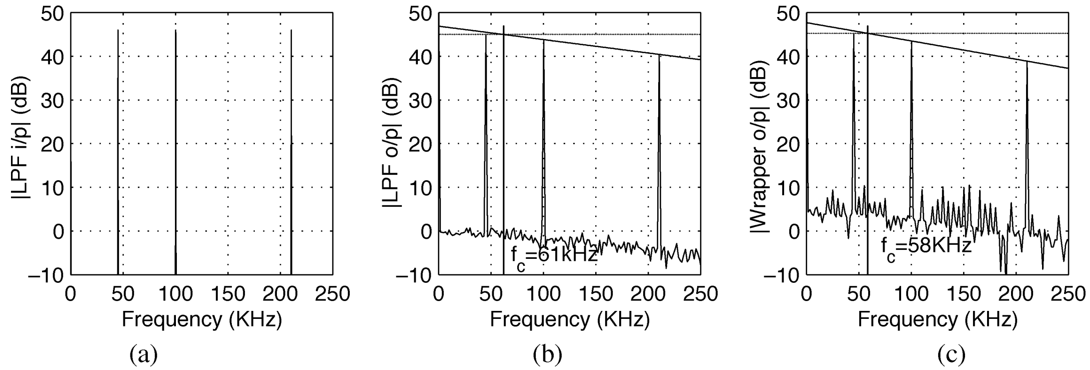

Fig. 5. (a) Frequency spectrum of the applied analog test; (b) frequency spectrum of the analog response of the core; and (c) frequency spectrum of the response of the wrapped analog core.

ADC requires 2^N comparators, thus, an 8-bit flash architecture typically requires 256 comparators. In contrast, the modular approach needs only 32 comparators. The comparators are the primary contributers to the overall area of the ADC. Similarly, we use a modular voltage-steering 8-bit DAC architecture [47], which is constructed from two 4-bit DACs. Fig. 4(b) shows a block diagram of the 8-bit DAC. This modular approach reduces the number of resistors used by a factor of eight. Although the modular approach also adversely impacts the speed of operation of the data converters, it does not prevent us from achieving our desired performance for the low-speed applications that are being targeted here.

To demonstrate the accuracy of using digital test patterns to test wrapped analog cores, we apply a cutoff frequency test f_c to analog core A (a detailed description of the core and its tests is presented in Table II of Section VII). The core is tested for cutoff frequency by applying a multi-tone signal. The frequency spectrum of the resulting signal is used to extrapolate the cutoff frequency of the filter. We compare the frequency spectrum obtained without using a wrapper and doing a direct analog test, to that of the test responses obtained from the wrapped analog core. Fig. 5 shows the HSPICE simulation results for the two scenarios. The error in the response from the wrapped analog core is approximately 5%. This error can be reduced further by using more frequencies in the input signal; for the purpose of illustration, we have chosen an input with only three frequencies. The frequency spectrum is obtained by post-processing the transient analysis data obtained from the simulations. The system clock frequency is 50 MHz and the sampling frequency of the input signal is 1.7 MHz. The number of samples used is 4551. The supply voltage used is 4 V.

We have also implemented a test chip for testing and characterizing an 8-bit analog wrapper. Its area in the 0.5-μm process is only 0.02 mm^2. Preliminary comparison with an industrial core implemented in 0.12-μm technology indicates that the wrapper, even though it is implemented in 0.5-μm technology, is only one-eighth the size of the core. We expect this ratio to be significantly smaller (<1/40) if the wrapper is implemented in the same technology as the core. In this work, we have not considered the overhead of testing the ADC and DAC in the wrapper. Efficient BIST techniques can be used for testing the data converters [18], [20], [21] in the self-test mode of the wrapper.

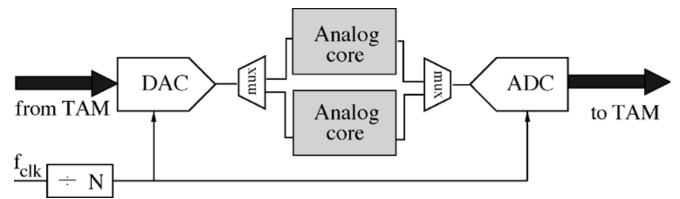

Fig. 6. Shared test wrapper for analog cores.

V. Analog Wrapper Optimization

The ADC–DAC pair, together with the encoder–decoder pair, forms the predominant part of the ATW. The encoder and decoder allow the wrapper to be reconfigured for a set of different tests. We exploit this feature of reconfigurability to optimize the resource utilization and reduce the overall wrapper area.

We propose that an analog test wrapper be designed such that it can support testing of more than one analog core multiplexed in time from one test to another. In the proposed approach, we use the reconfigurability of the analog wrappers to allow the test of multiple analog cores, using a single wrapper, thereby reducing the overall wrapper area significantly. The ATW design can be easily modified to accommodate this feature. Fig. 6 illustrates two analog cores sharing test wrappers (only the ADC–DAC pair of the wrappers are shown for the purpose of illustration). The time-multiplexed testing of the cores can be ensured by the use of multiplexers. Although the use of analog multiplexers may result in additional parasitic noise, the use of analog multiplexers is an accepted practice in analog testing, and design methods exist to alleviate the noise problem [48]–[50]. The sizes of the encoder, decoder, and the ADC-DAC pair in a shared analog wrapper are determined such that they can satisfy the requirements of all the cores sharing the wrapper. The resolution of the ADC–DAC pair in the proposed shared analog wrapper is selected to be the maximum of the ADC–DAC resolution requirements of all the analog cores sharing the wrapper. Similarly, the encoder and decoder are designed for the test with the largest TAM width requirement. The encoders and decoders can be configured to test any of the analog cores. However, a module that requires high-speed and low-resolution data converters cannot share its wrapper with a module that requires high-resolution and low-speed data

converters. It may not be feasible to satisfy the requirements of high-speed and high-resolution with reasonable overhead.

Wrapper sharing results in a certain routing overhead that needs to be accounted for. For analog cores that are separated by a large distance, sharing is less advantageous since the routing overhead will be high. In this work, we evaluate the area overhead due to analog test wrappers as follows. The routing overhead is considered to be a percentage of the wrapper architecture's area overhead. This percentage depends on the relative on-chip location of the analog cores. Typically this location is determined by the functional proximity between the analog core and other cores in the system. Thus, an approximate idea about the proximity of analog wrappers can be obtained prior to layout. The area overhead is estimated as the ratio of the area overhead due to sharing, to the area overhead if there is no sharing of wrappers. When there is no sharing of wrappers between cores, the area overhead is maximum. The area overhead due to test wrappers can be expressed as

$$\mathcal{C}_A = \frac{\sum_i^{N_w} (1 + d_i) \cdot A\max_i}{\sum_j^N A_j} \times 100 \tag{1}$$

where

N_w	number of analog wrappers used;
N	the number of analog cores;
d_i	the routing overhead for shared wrapper i;
A_j	area overhead of analog wrapper j;
$A\max_i$	maximum of the individual wrapper area overheads of the cores for the shared wrapper i.

The cost function defined above is used for preliminary cost analysis. Using the above estimate, it is possible to determine the relative cost of the different sharing combinations among the various analog cores. The routing overhead of a wrapper that serves n cores is defined as $d_i = (n-1) \times p$, where $0 < p \leq 1$ is a factor proportional to the cumulative distance of the n cores from each other. In this paper, without loss of generality, we have considered a representative value of $p = 0.15$ to illustrate the approach. Thus, wrappers that serve only one core have a routing overhead of $d_i = 0$. Note that C_A should always be lower than 100. The sharing combinations that exceed the overhead of the no-sharing case should not be considered.

In order to avoid potential resource conflicts, it is imperative that the tests for cores that share a wrapper do not overlap in time in the test schedule. Thus, we constrain the TAM optimization procedure such that the tests for cores sharing the same wrapper are scheduled serially in time. In this way, the total test time usage of the test wrapper is the sum of the test times of the analog cores that share the wrapper. A lower bound on the overall test time of all the analog cores can now be calculated as the maximum of the usage of every analog test wrapper, i.e., if three analog test wrappers are used to test all the analog cores, then a lower bound t_{LB} on the test time is the maximum of the test time usage of the three analog test wrappers. Table I shows the C_A values for all the combinations of sharing between the five analog cores considered in the experimental setup. The normalized lower bound for each case is also presented; these values have been normalized to the maximum lower bound. A detailed description of the five analog cores labeled A–E is presented in Section VII. (Since Core A and Core B have identical tests, only unique combinations for Core A are presented.)

TABLE I
AREA OVERHEAD COSTS FOR ALL COMBINATIONS OF WRAPPER SHARING

n	C	$\mathcal{C}_A$	t_{LB}	n	C	$\mathcal{C}_A$	t_{LB}
4	{A,C}	83.0	68.5	3	{A,D,E}		31.4
	{C,D}		56.0	2	{A,B,C,D}		98.7
	{C,E}		48.3	2	{A,B,C,E}	49.0	91.1
	{A,B}		42.7	2	{A,C,D,E}		78.6
	{A,D}		30.2	2	{A,B,D,E}		52.8
	{A,E}		22.6	2	{A,B,C}{DE}	46.0	89.8
	{D,E}		10.1	2	{A,C,D}{B,E}		77.3
3	{A,B,C}	66.0	89.8	2	{A,C,E}{B,D}		69.7
	{A,C,D}		77.3	2	{A,D,E}{B,C}		68.5
	{A,C,E}		69.7	2	{C,D,E}{A,B}		57.2
	{A,B,D}		57.2	2	{A,B,E}{C,D}		56.0
	{C,D,E}		51.6	2	{A,B,D}{C,E}		51.6
	{A,B,E}		43.9	1	{A,B,C,D,E}	100	100

n: Number of wrappers; C: Combination of cores that share a wrapper.

VI. TEST COST OPTIMIZATION

In this section, we define the test cost minimization problem for a given TAM width W. The objective is to minimize the test cost in terms of test application time and the area overhead. We use a previously developed TAM optimization technique to obtain the test application time for an SOC. In Section VII, we present experimental results based on the two TAM optimization methods. The first method from [43] optimizes a Test Bus architecture and the second optimization approach from [7] is for a flexible-width TAM architecture.

The test cost for a given SOC-level TAM width W can be minimized as follows. The total test cost is expressed as

$$\mathcal{C}(W) = \omega_T \cdot \mathcal{C}_T(W) + \omega_A \cdot \mathcal{C}_A \tag{2}$$

where ω_T is the cost weighting factor for the test application time $\mathcal{C}_T$, and ω_A is the cost weighting factor for the area overhead cost $\mathcal{C}_A$. The weighting factors are defined such that $\omega_T + \omega_A = 1$. The cost of test application time is expressed as $\mathcal{C}_T(W) = 100 \times T(W)/T_m(W)$, where $T_m(W)$ is the test time of the SOC when all the analog cores share a single analog wrapper. This case represents the most constrained scenario for test scheduling, hence, for any given TAM width, it is likely to yield the highest test time. Essentially, $\mathcal{C}_T$ is the test time normalized to the maximum possible test time. The TAM optimization procedure is used to obtain the value of $T_m(W)$ for a given TAM width W. The area overhead cost includes the cost of the analog core wrappers and the routing overhead of shared wrappers as explained in Section V. Both the costs C_T and C_A have been defined to have values between 1 and 100.

Now, the problem of minimizing the overall test cost of an SOC can be stated as follows.

Problem P_{cost}: Given the test data parameters for the digital cores, the testing time in clock cycles and the core-level TAM widths for the analog cores, the total SOC-level TAM width W, and the test time cost and area overhead cost weights ω_T and ω_A, respectively, determine: 1) the wrapper design for digital

```
Procedure Cost_Optimizer(ωT, ωA, W)
1. Group combinations having the same degree of sharing to form G = G1 ∪ G2 ∪ ··· ∪ Gn;
2. for i := 1 to n do
3.   for j := 1 to (|Gi|) do
4.    Evaluate Ctemp(Gi(j)) := ωT.tLB(Gi(j)) + ωA.CA(Gi(j));
5.   od;
6. od;
7. for i := 1 to n do
8.    Select k ∈ {j |Ctemp(Gi(j)) = max1≤x≤n Ctemp(Gi(x))};
9.    Run TAM_Optimizer procedure to get the test times Ti(W) of
   element Gi(k);od;
10. Tm(W) := max1≤x≤n(Tx(W))
11. for i := 1 to n do
12.   Evaluate cost Ci(W) for selected element;
13. od;
14. Select k ∈ {j |Cmin = min1≤x≤n Cx(W)};
15 for i := 1 to n do
16.   if Ci − Cmin > δ, eliminate group i;
17. od;
18. Evaluate all elements of the groups that have not been eliminated;
19. Return the element that results in the smallest C(W);
```

Fig. 7. Pseudocode for procedure *Cost_Optimizer*.

cores; 2) the groups of analog cores that share analog wrappers; and 3) the TAM width for each core and test schedule for the SOC, such that the total number of TAM wires utilized at any moment does not exceed the overall TAM width W and the total cost $\mathcal{C}(W) = \omega_T.\mathcal{C}_T(W) + \omega_A.\mathcal{C}_A$ is minimized.

The *Design_wrapper* algorithm from [34] is used to design the wrappers for digital cores. Next, the grouping of the analog cores is determined, such that the analog cores grouped together share the same analog test wrapper. Finally, the TAM optimization approach is used to determine a test schedule for the digital and analog cores.

Depending on the specified weights ω_T and ω_A, the analog cores can be grouped such that they share analog wrappers and the overall cost of the wrappers is minimized. The degree of sharing is dictated by the weighting factors in the cost function. If $\omega_T > \omega_A$, the test time is given more weightage in optimization. In this case, the degree of wrapper sharing may be chosen such that the area overhead cost reduction is compromised to achieve better test times. Similarly if $\omega_A > \omega_T$, the degree of sharing is chosen such that the area overhead minimization has priority over test time minimization.

One approach for solving problem P_{cost} is to evaluate the overall cost $\mathcal{C}_T$ for every possible configuration of shared analog wrapper (as presented in Table I) for a given TAM width W and weights ω_T and ω_A. This exhaustive approach requires the TAM optimization procedure to be run for every combination of analog cores to obtain the $\mathcal{C}_T(W)$ values. This is computationally expensive for a larger problem instance with many analog cores since the number of distinct combinations increases exponentially with the number of analog cores.

We propose a heuristic approach that scales well with the increase in the number of analog cores and provides a near optimal result. We use a pruning technique based on the area overhead costs $\mathcal{C}_A$ and analog test time lower bounds t_{LB}, which are available prior to cost optimization. Fig. 7 details the pseudocode for the proposed heuristic procedure *Cost_Optimizer*.

First (in Line 1), all the combinations of analog cores sharing test wrappers are grouped by their degree of sharing, i.e., combinations that have the same area overhead cost $(\mathcal{C}_A)$ are grouped together. Together, all the groups form a set G. The goal is to be able to eliminate an entire group without having to do a complete evaluation. A complete evaluation for a combination entails finding a test schedule by using the TAM optimization procedure.

The next step (line 4) is to estimate preliminary costs for every combination based on area overhead, cost weights, and the lower bounds on analog test times. We calculate the preliminary costs $C\text{temp}$ for every combination as

$$C\text{temp}\left(G_i(j)\right) = \omega_T.t_{LB}\left(G_i(j)\right) + \omega_A.C_A\left(G_i(j)\right) \quad (3)$$

where $G_i(j)$ is combination j of group G_i.

Based on the $C\text{temp}$ values, the combination/element that has the smallest $C\text{temp}$ values is chosen from every group i (Line 8). Next, the *TAM_Optimizer* procedure is used to evaluate the C_T values of the chosen elements of each group. These values are used to determine the $C_i(W)$ value for the chosen elements. The group with the minimum cost $\mathcal{C}_{\min}$ is not eliminated. Next, any group that satisfies the elimination criteria (i.e., $\mathcal{C}_{\min} > \mathcal{C}_i + \delta$) is eliminated. The elimination criteria can be relaxed by making the threshold δ larger.

VII. Experimental Results

In this section, we present the description and specifications of the analog cores used in our mixed-signal SOC circuits. We

TABLE II
TEST REQUIREMENTS FOR THE ANALOG CORES

Test	f_{min}	f_{max}	f_s	T	w
Cores A & B: I-Q transmit					
G_{pb}	50kHz	50kHz	1.5MHz	50,000	1
f_c	45kHz	55kHz	1.5MHz	13,653	4
G_{1MHz}& G_{2MHz}	1MHz	2MHz	8MHz	12,643	2
IIP_3	50kHz	250kHz	8MHz	26,973	2
$V_{off_{DC}}$	DC	DC	10kHz	700	1
Φ_{off}	200kHz	400kHz	15MHz	32,000	4
Core C: CODEC audio					
G_{pb}	20kHz	20kHz	640kHz	80,000	1
f_c	45kHz	55kHz	1.5MHz	136,533	1
THD	2kHz	31kHz	2.46MHz	83,252	1
Core D: Baseband down converter					
IIP_3	3.25MHz	9.75MHz	78MHz	15,754	10
A_v	1MHz	2MHz	26MHz	9,228	4
DR	1MHz	2MHz	26MHz	31,508	4
Core E: General purpose amplifier					
SR	1MHz	2MHz	69MHz	5,400	5
A_v	500KHz	2MHz	8MHz	2,500	1

use three mixed-signal SOCs in our experiments. We present the following sets of experimental results.

- We present a quantitative analysis of test cost reduction due to the use of digital testers in place of expensive mixed-signal testers. We take into account the additional test hardware added to facilitate the use of digital testers for analog test. More specifically, we do a quantitative comparison of the cost of using an analog Test Bus versus a digital Test Bus for testing analog cores.
- We show the impact of using a unified test approach for mixed-signal SOCs on test application time. We compare the SOC testing time obtained using two existing TAM optimization methods for the unified approach, with the testing time obtained using a nonunified test method.
- We also illustrate the impact of using shared test wrappers on overall test cost. We present results for test cost obtained using the proposed test cost optimization approach.
- Finally, we examine the efficiency of the cost optimization approach. We compare the efficiency of the proposed cost optimization method with the exhaustive method described in Section VI.

For our experimental setup, we have used three digital SOCs from the ITC'02 SOC test benchmarks, namely p22810, p93791, and p93791. We have added five analog cores to the SOCs. We refer to the mixed signal SOCs as p22810m, p93791m, and p93791m, respectively. The analog cores consist of a pair of baseband I-Q transmit path with a bandwidth of 500 kHz, a CODEC audio path with a bandwidth of 50 kHz, a baseband down conversion path, and a general purpose amplifier. These analog cores are taken from a commercial baseband cellular phone chip. The test set specifications for each of these analog cores are given in Table II. Due to the lack of a standardized analog test generation tool, analog tests are defined manually based on the core specifications.

For the I-Q transmit path pair, six distinct specification-based tests are defined. These include the pass-band gain (G_{pb}), the cutoff frequency (f_c), the attenuation levels at 1 and 2 MHz ($G_{1\text{ MHz}}$ and $G_{2\text{ MHz}}$), the third-order input intercept (IIP_3), the DC offset (V_{off_DC}), and the phase mismatch (Φ_{off}). For the audio CODEC path, the specifications include G_{pb}, f_c, and the total harmonic distortion (*THD*). The Baseband down conversion path has three specified tests, namely a test for the IIP_3, a test for the gain (A_v), and a test for the dynamic range (*DR*). Lastly, the tests for the general purpose amplifier include a test for the slew rate (*SR*) and a test for the A_v. The TAM width requirements w for each of the analog cores are also presented in Table II. The self-test mode test time has not been considered for both analog and digital cores, thus, Table II presents only the test time on the core-test mode. It should be noted that the analog test wrappers are not limited to the tests listed in Table II. The proposed test wrappers can be used for analog tests that are within the operating frequency and resolution of the data converters in the analog test wrappers.

A. Analog Test Bus Versus Digital Test Bus

In a nonunified test approach for mixed-signal SOCs, the digital and the analog cores are tested separately. The analog cores can be tested using dedicated analog test buses and the digital cores can be tested using digital test buses. The use of an analog test bus requires the use of a mixed-signal tester. An alternative nonunified approach is to sandwich the analog cores between on-chip data converters, thereby obviating the need for a mixed-signal tester. Even with the use of on-chip data converters, however, the analog cores have to be tested on dedicated digital test buses if an ATW is not used. Without the use of an ATW, a dedicated test bus that operates at the data converter frequencies is required. In order to compare the cost of test equipment, we consider three test access architectures. Fig. 8 shows the three TAM architectures. We consider using 1 or 2 separate analog test buses (1 a-bus or 2 a-bus TAM) with a mixed-signal tester, and a 12-bit digital test bus with on-chip data converters and a digital tester (d-bus TAM). As the tests for one analog core cannot be parallelized, the lower bound on analog test time is reached using two analog test buses. Thus, there is no advantage of increasing the number of analog test buses beyond two in the case of using a mixed-signal tester. We use the TAM optimization from [43] to obtain the test time results for the three test bus architectures.

In order to compare the test equipment cost, we make the following assumptions. First, we assume that the digital tester costs 33% less than the mixed-signal tester with all other attributes being the same. This assumption is conservative compared to industrial reports indicating that the mixed-signal tester cost per unit time can be more than twice as much as the digital tester cost [3]. Second, for a fair comparison, we assume that the total pin count allocated for testing remains the same for each experimental case.

Table III compares the test time and cost results for the three SOCs and for various available TAM widths. The cost is calculated as the product of test time with the tester cost per unit time and normalized with respect to the baseline case. The baseline case for each value of W, denoted by 100% refers to the use of either one or two analog test buses (1-abus or 2-abus), whichever yields a smaller testing time. We make the comparison of test time in terms of the cycles of a 50-MHz clock. In order to highlight the comparison, we normalize the test cost to

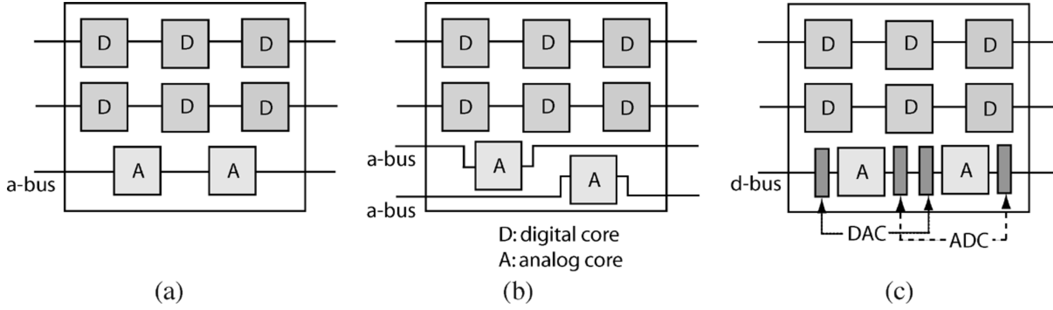

Fig. 8. Test access based on: (a) 1 a-bus TAM; (b) 2 a-bus TAM; and (c) d-bus TAM.

TABLE III
COMPARISON OF TEST TIME (IN CLOCK CYCLES) IN USING ANALOG VERSUS DIGITAL BUS. THE NORMALIZED TEST COST, INCLUDING THE TEST EQUIPMENT COST, IS SHOWN IN PARENTHESIS

	SOC p22810m			SOC p34392m			SOC p93791m		
TAM width W (bits)	1-abus	2-abus	d-bus	1-abus	2-abus	d-bus	1-abus	2-abus	d-bus
24	571823	438619 (100%)	636113 (97%)	876014 (100%)	1033209	1295086 (98%)	1438121 (100%)	1865474	2409601 (112%)
32	636113	299785 (100%)	636113 (142%)	636113 (100%)	685750	876014 (92%)	1032276 (100%)	1185783	1438121 (93%)
40	636113	299785 (100%)	636113 (142%)	636113	583494 (100%)	636113 (73%)	805659 (100%)	918345	1032276 (86%)
48	636113	299785 (100%)	636113 (142%)	636113	544579 (100%)	636113 (78%)	658215 (100%)	735875	8056359 (82%)
56	636113	299785 (100%)	636113 (142%)	636113	544579 (100%)	636113 (78%)	636113	613887 (100%)	658215 (72%)
64	636113	299785 (100%)	636113 (142%)	636113	544579 (100%)	636113 (78.0%)	636113	525828 (100%)	636113 (81%)

a baseline case of using a mixed-signal tester. The testing time is normalized with the relative tester cost to obtain the overall test cost.

These experimental results indicate that for smaller SOCs such as the p22810m, where the analog test time dominates, the use of two analog test buses and a mixed-signal tester results in a lower cost. This result indicates that pushing the signal digitization on-chip is advantageous for SOCs with large digital and small analog content. For p34392m and p93791m, it is clear that using on-chip data converters results in appreciable reduction in the overall test cost, even with a pessimistic cost comparison of mixed-signal ATEs with digital ATEs. The test cost reduction is as high as 25% for several cases.

B. Reduction in Test Application Time

In order to evaluate the proposed analog test wrapper and the unified optimization approach, we compare the test time of using the proposed approach with the test time of the d-bus approach, where only on-chip data converters are used. In the d-bus approach, a TAM width of 12 bits has to be allocated to analog tests for the duration; the remaining available bits are used for digital TAM optimization. In our proposed approach, the analog test requirements are integrated into a global optimization flow where the minimum bandwidth requirements of each analog test is taken into account, and the DAC and ADC registers are updated in a semi-serial fashion.

Since the analog cores are wrapped, we can proceed to solve the TAM optimization problem in a manner identical to solving the problem for digital SOCs. We use two TAM optimization methods based on: a) the fixed-width TAM optimization, which used a Test Bus architecture and b) the flexible-width TAM architecture based on rectangle packing.

For the Test Bus architecture, we use the *Partition_evaluate* heuristic from [43], to arrive at TAM partitions, and the *Core_assign* heuristic [34] to find near optimal core assignments to TAM partitions. For the flexible-width TAM architecture we use the rectangle-packing algorithm from [7].

Table IV shows a comparison of test time using the proposed analog wrapper and the unified test methodology with the test time when only data converters are used in a nonunified approach (d-bus approach). From the results, we observe that the SOC testing time is significantly lower for several TAM width values using the proposed approach. The decrease in testing time is especially significant for small TAM widths. For larger TAM widths ($W > 32$), for p22810 and p34392, a bottleneck core dominates the testing time. Analog Cores A and B are the dominating bottleneck cores in SOC p22810, and digital Core 18 dominates the test time of SOC p34392. In the d-bus approach also, the testing time of the analog cores dominates the overall SOC testing time. Note that the decrease in testing time is further decreased in test cost in addition to the test cost reduction achieved due to the elimination of the expensive mixed-signal tester.

From Table IV, we also observe that the test time for the flexible-width architecture is lower that that of the Test Bus architecture. This is because the flexible-width TAM optimization approach exploits the disparity in the TAM width requirements of digital and analog cores to reduce the overall test time of

TABLE IV
TESTING TIME (IN CLOCK CYCLES) AND PERCENTAGE IMPROVEMENT USING THE PROPOSED APPROACH

W	$T_{\text{d-bus}}$	$T_{\text{fixed-width}}$	$T_{\text{flexible-width}}$	ΔT_1(%)	ΔT_2(%)
SOC p22810m					
24	636113	420652	378532	−33.87	−40.49
32	636113	347131	299785	−45.43	−52.87
40	636113	321660	299785	−49.43	−52.87
48	636113	299785	299785	−52.87	−52.87
56	636113	299785	299785	−52.87	−52.87
64	636113	299785	299785	−52.87	−52.87
SOC p34392m					
24	1294086	807250	838643	−37.62	−35.19
32	876014	622163	575482	−28.98	−34.31
40	636113	584524	544579	−8.1	−14.39
48	636113	544579	544579	−14.39	−14.39
56	636113	544579	544579	−14.39	−14.39
64	636113	544579	544579	−14.39	−14.39
SOC p93791m					
24	2409601	1315625	1345978	−45.40	−44.14
32	1438121	1029681	1023448	−28.40	−28.83
40	1032276	849940	797953	−17.66	−22.70
48	805659	743922	648381	−7.66	−19.52
56	658215	653479	584955	−0.72	−11.13
64	636113	593791	543598	−6.65	−14.54

$\Delta T_1 = \frac{T_{\text{fixed-width}} - T_{\text{d-bus}}}{T_{\text{d-bus}}} \times 100$; $\Delta T_2 = \frac{T_{\text{flexible-width}} - T_{\text{d-bus}}}{T_{\text{d-bus}}} \times 100$

the SOC. The TAM width requirements of an analog core are usually much smaller than that of most digital cores. Moreover, their testing time does not reduce with an increase in the number of digital TAM wires allocated for them. For digital cores, there exists a "staircase variation" of testing time with TAM width [34], hence, their testing time can be reduced with an increase in the TAM width. Thus, there is often a substantial disparity between the TAM width requirements of digital and analog cores. As a result, when analog cores are tested serially with digital cores on the same TAM partition, the analog cores do not use all the TAM wires. Consequently, the overall time taken to test the SOC is not optimized. The flexible-width TAM architecture can handle digital and analog cores in a unified manner, yet bridge the gap in TAM width requirements of digital and analog cores. In the sections that follow, we use the TAM optimization method for flexible-width TAM architecture to obtain the SOC testing time for the various TAM width values.

C. Impact of Shared ATWs on SOC Test Time

Next, we study the impact of wrapper sharing among the analog cores on the overall test time of an SOC. Table V presents results for SOC p93791m. The test time is presented for all the combinations of analog wrapper sharing. The test times are normalized to the case of maximum test time, thus, they are essentially the C_T values for the combinations. As expected, the test time for the case when all the analog cores share the same wrapper, results in the maximum test time. The combinations that result in the lowest test time are highlighted in Table V.

We conclude from the results that as the TAM width increases, the analog core combinations have a greater affect on the overall SOC test time. This is because with an increase in TAM width, the test time of the digital cores decrease and the test time of the analog cores becomes more prominent. Thus,

TABLE V
TEST TIME RESULTS FOR SOC p93791M FOR DIFFERENT COMBINATIONS OF ANALOG WRAPPER SHARING

# of wrappers	Wrapper sharing	$T(W)$		
		$W = 32$	$W = 48$	$W = 64$
4	{A,C}	98.3	**92.6**	86.3
	{C,D}	99.1	**92.6**	85.0
	{C,E}	99.1	**92.6**	87.6
	{A,B}	**97.5**	**92.6**	**82.8**
	{A,D}	99.1	92.8	85.58
	{A,E}	99.1	**92.6**	86.1
	{D,E}	99.1	92.8	85.4
3	{A,B,C}	99.8	92.9	90.1
	{A,C,D}	98.3	92.8	87.2
	{A,C,E}	98.3	**92.6**	86.3
	{A,B,D}	99.1	97.2	85.4
	{C,D,E}	99.1	92.8	85.4
	{A,B,E}	97.9	92.8	**82.8**
	{A,D,E}	99.1	92.9	85.5
2	{A,B,C,D}	99.4	96.4	98.7
	{A,B,C,E}	99.8	98.5	91.1
	{A,C,D,E}	98.3	92.9	87.2
	{A,B,D,E}	98.3	97.2	85.4
2	{A,B,C}{D,E}	99.8	94.9	90.1
	{A,C,D}{B,E}	98.3	92.8	87.2
	{A,D,E}{B,C}	98.3	92.9	87.8
	{C,D,E}{A,B}	98.3	**92.6**	86.8
	{A,B,E}{C,D}	97.9	92.8	86.8
	{A,C,E}{B,D}	98.3	92.8	87.8
	{A,B,D}{C,E}	99.1	97.2	85.4
1	{A,B,C,D,E}	100	100	100

the difference between the lowest and the highest test times of the various combinations for $W = 32$, 48, and 64 are 2.45, 7.36, and 17.18, respectively. It is also seen that the lowest test times are obtained for combinations with a lower degree of sharing. However, for $W = 48$ and $W = 64$, the lowest test times can also be obtained with combinations that have a high degree of sharing. These cases show that some test schedules can result in a low test time, even with a high degree of sharing.

D. Effectiveness of Cost Optimization Approach

Table VI presents the cost of sharing for a set of ω_T and ω_A values. The proposed *Cost_Optimizer* procedure is compared with the exhaustive evaluation approach described in Section VI. (Note that while exhaustive enumeration is possible for these test cases, the high CPU time, notwithstanding, is unlikely to be feasible for larger SOCs.) The C_A values used are the same as those presented in Table I. And the elimination criteria δ for the *Cost_Optimizer* approach is chosen to be zero. Recall that the exhaustive evaluation approach always results in optimal results, although at the expense of greater computation time. It is seen that the *Cost_Optimizer* procedure also gives optimal results for all but one case with a much lower computation time.

In Table VI, η_{exh} and η represent the number of combinations evaluated to arrive at the results, and S represents the combination of core sharing selected. η_{exh} is always 26, since there are a total of 26 combinations. The lower bound on η is four, since the best combinations of four groups have to be evaluated. It is seen that the reduction in the number of combinations evaluated is

TABLE VI
COMPARISON OF *COST_OPTIMIZER* WITH THE EXHAUSTIVE EVALUATION APPROACH

W	$\mathcal{C}_{exh}$	η_{exh}	S	$\mathcal{C}$	η	S	$\Delta\eta$
$w_T = 0.5$, $w_A = 0.5$							
32	71.9	26	{A,B,E}{C,D}	71.9	10	{A,B,E}{C,D}	−61.5
40	69.7	26	{A,B,D}{C,E}	69.7	10	{A,B,D}{C,E}	−61.5
48	69.3	26	{C,D,E}{A,B}	69.3	10	{C,D,E}{A,B}	−61.5
56	68.9	26	{A,B,E}{C,D}	68.9	10	{A,B,E}{C,D}	−61.5
64	65.7	26	{A,B,D}{C,E}	65.7	10	{A,B,D}{C,E}	−61.5
$w_T = 0.8$, $w_A = 0.2$							
32	87.5	26	{A,B,E}{C,D}	88.4	7	{A,C,D,E}	−73.0
40	84.0	26	{A,B,D} {C,E}	84.0	10	{A,B,D} {C,E}	−61.5
48	83.3	26	{C,D,E}{C,E}	83.3	10	{C,D,E}{C,E}	−61.5
56	82.7	26	{A,B,E}{C,D}	82.7	10	{A,B,E}{C,D}	−61.5
64	77.5	26	{A,B,D}{C,E}	77.5	10	{A,B,D}{C,E}	−61.5
$w_T = 0.2$, $w_A = 0.8$							
32	56.4	26	{A,C,D}{B,E}	56.4	10	{A,C,D}{B,E}	−61.5
40	55.5	26	{A,B,D}{C,E}	55.5	10	{A,B,D}{C,E}	−61.5
48	55.3	26	{A,B,E}{C,D}	55.3	10	{A,B,E}{C,D}	−61.5
56	55.1	26	{A,B,E}{C,D}	55.1	10	{A,B,E}{C,D}	−61.5
64	53.8	26	{A,B,D}{C,E}	53.8	10	{A,B,D}{C,E}	−61.5

significant even for the cases where *Cost_Optimizer* yields optimal results. The percentage reduction in the number of evaluations $\Delta\eta$ is also reported $(\Delta\eta = ((\eta - \eta_{\rm exh})/\eta_{\rm exh}) \times 100)$. On an average, the *Cost_Optimizer* procedure takes 6 min to complete on a Sun Ultra 5_10, whereas, the exhaustive approach requires approximately 20 min to complete.

VIII. CONCLUSION

We have presented a new approach for reducing the testing time and test cost for mixed-signal SOCs containing both analog and digital cores. The proposed approach is based on the use of a novel test wrapper for analog cores. We have developed a TAM optimization and test scheduling approach that can handle wrapped analog and digital cores in a unified manner at the SOC level. In addition to reducing testing time, the proposed wrapper obviates the need for expensive mixed-signal testers. We have also presented a resource optimization technique and a cost-oriented optimization heuristic to reduce the overall test cost of mixed-signal SOCs. In the resource optimization approach, we show that multiple analog cores can share analog test wrappers to reduce the area overhead. The cost-oriented optimization approach uses a well known TAM optimization approach together with the analog wrapper optimization technique to give a cost-efficient TAM architecture and test schedule for a mixed-signal SOC. We have presented experimental results for three ITC'02 SOC test benchmarks that have been augmented with five representative analog cores each. The results demonstrate that for "big D/small A" SOCs, compared to a baseline case of ad hoc test planning, the testing time and test cost are reduced significantly using the proposed optimization methods.

REFERENCES

[1] T. Yamamoto *et al.*, "A mixed-signal 0.18-μm CMOS SoC for DVD systems with 432-MSample/s PRML read channel and 16-Mb embedded DRAM," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 1785–1794, Apr. 2001.
[2] H. Kundert *et al.*, "Design of mixed-signal systems-on-a chip," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 19, no. 12, pp. 1561–1571, Dec. 2000.
[3] B. Koupal, T. Lee, and B. Gravens, Bluetooth single chip radios: Holy grail or white elephant [Online]. Available: http://www.signiatech.com/pdf/paper_two_chip.pdf
[4] *"International Technology Roadmap for Semiconductors (ITRS),"* Semiconductor Industry Association, 2003 [Online]. Available: http://public.itrs.net/
[5] S. K. Goel *et al.*, "Test infrastructure design for the Nexperia home platform PNX8550 system chip," in *Proc. Des., Automat., Test Eur. (DATE) Des. Forum*, 2004, pp. 108–113.
[6] Y. Zorian, E. J. Marinissen, and S. Dey, "Testing embedded-core-based system chips," *IEEE Computer*, vol. 32, no. 6, pp. 52–60, Jun. 1999.
[7] V. Iyengar, K. Chakrabarty, and E. J. Marinissen, "Test access mechanism optimization, test scheduling and tester data volume reduction for system-on-chip," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 22, no. 5, pp. 593–604, May 2003.
[8] E. J. Marinissen, V. Iyengar, and K. Chakrabarty, "A set of benchmarks for modular testing of SOCs," in *Proc. IEEE Int. Test Conf. (ITC)*, 2002, pp. 519–528 [Online]. Available: http://www.extra.research.philips.com/itc02socbenchm/
[9] A. Cron, "IEEE P1149.4—Almost a standard," in *Proc. IEEE Int. Test Conf. (ITC)*, 1997, pp. 174–182.
[10] S. Sunter, "Cost/benefit analysis of the P1149.4 mixed-signal test bus," *Inst. Elect. Eng. Proc., Circuits, Devices Syst.*, vol. 143, no. 6, pp. 393–398, Dec. 1996.
[11] B. Dufort and G. W. Roberts, "On-chip analog signal generation for mixed-signal built-in self-test," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 318–330, Mar. 1999.
[12] A. Lu and G. W. Roberts, "An oversampling based analog multitone signal generator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 45, no. 3, pp. 391–394, Mar. 1998.
[13] A. Lu, G. W. Roberts, and D. J. Johns, "A high quality analog oscillator using oversampling D/A conversion techniques," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 41, no. 7, pp. 437–444, Jul. 1994.
[14] C. Y. Pan and K. T. Cheng, "Pseudorandom testing for mixed-signal circuits," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 16, no. 10, pp. 1173–1189, Oct. 1997.
[15] M. Hafed *et al.*, "A stand-alone integrated test core for time and frequency domain measurements," in *Proc. IEEE Int. Test Conf. (ITC)*, 2000, pp. 1031–1040.
[16] M. F. Toner and G. W. Roberts, "A BIST scheme for an SNR test of a Sigma-Delta ADC," in *Proc. IEEE Int. Test Conf. (ITC)*, 1993, pp. 805–814.
[17] ——, "A BIST technique for a frequency response and intermodulation distortion test of a Sigma-Delta ADC," in *Proc. IEEE VLSI Test Symp. (VTS)*, 1994, pp. 60–65.
[18] Y.-J. Chang *et al.*, "Built-in high resolution signal generator for testing ADC and DAC," in *Proc. IEEE Int. Symp. VLSI Technol., Syst., Appl.*, 2003, pp. 231–234.
[19] Y. Cong and R. L. Geiger, "A 1.5 14 b 100 MS/s self-calibrated DAC," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 2051–2060, Dec. 2003.
[20] J.-L. Huang *et al.*, "A BIST scheme for on-chip ADC and DAC testing," in *Proc. Des., Automat., Test Eur. (DATE)*, 2000, pp. 216–220.
[21] L. Jin *et al.*, "Linearity testing of precision analog-to-digital converters using stationary nonlinear inputs," in *Proc. IEEE Int. Test Conf. (ITC)*, 2003, pp. 218–227.
[22] Y.-J. Chang *et al.*, "A testable BIST design for PLL," in *Proc. IEEE VLSI Test Symp. (VTS)*, 2003, pp. 204–207.
[23] S. Kim, M. Soma, and D. Risbund, "An effective defect-oriented BIST architecture for high-speed phase-locked loops," in *Proc. IEEE VLSI Test Symp. (VTS)*, 2000, pp. 231–236.
[24] S. Sunter and A. Roy, "BIST for phase-locked loops in digital applications," in *Proc. IEEE Int. Test Conf. (ITC)*, 1999, pp. 532–540.
[25] S. D. Huss and R. S. Gyurcsik, "Optimal ordering of analog integrated circuit tests to minimize test time," in *Proc. ACM/IEEE Des. Automat. Conf. (DAC)*, 1991, pp. 494–499.
[26] L. Milor and A. L. Sangiovanni-Vincentelli, "Optimal test set design for analog circuits," in *Proc. Int. Conf. Comput.-Aided Des. (ICCAD)*, 1990, pp. 294–297.
[27] ——, "Minimizing production test time to detect faults in analog circuits," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 13, no. 6, pp. 796–813, Jun. 1994.
[28] K. Saab, D. Marche, N. B. Hamida, and B. Kaminska, "LIMsoft: Automated tool for sensitivity analysis and test vector generation," *Inst. Elect. Eng. Proc., Circuits, Devices, Syst.*, vol. 143, no. 6, pp. 386–392, Dec. 1996.
[29] M. Slamani and B. Kaminska, "Multifrequency testability analysis for analog circuits," in *Proc. IEEE VLSI Test Symp. (VTS)*, 1994, pp. 54–59.

[30] Z. S. Ebadi and A. Ivanov, "Time domain multiplexed TAM: implementation and comparison," in *Proc. Des., Automat., Test Eur. (DATE)*, 2003, pp. 732–737.
[31] S. K. Goel and E. J. Marinissen, "SOC test architecture design for efficient utilization of test bandwidth," *ACM Trans. Des. Automat. Electron. Syst.*, vol. 8, no. 4, pp. 399–429, Oct. 2003.
[32] H.-S. Hsu *et al.*, "Test scheduling and test access architecture optimization for system-on-chip," in *Proc. IEEE Asian Test Symp. (ATS)*, 2002, pp. 411–416.
[33] Y. Huang, S. M. Reddy, and W.-T. Cheng, "Core-clustering based SOC test scheduling optimization," in *Proc. IEEE Asian Test Symp. (ATS)*, 2002, pp. 405–410.
[34] V. Iyengar, K. Chakrabarty, and E. J. Marinissen, "Co-optimization of test wrapper and test access architecture for embedded cores," *J. Electron. Testing: Theory Appl.*, vol. 18, no. 2, pp. 213–230, Apr. 2002.
[35] S. Koranne, "A novel reconfigurable wrapper for testing of embedded core-based SOC's and its associated scheduling algorithm," *J. Electron. Testing: Theory Appl.*, vol. 18, no. 4-5, pp. 415–434, Aug. 2002.
[36] E. Larsson and Z. Peng, "An integrated framework for the design and optimization of SOC test solutions," *J. Electron. Testing: Theory Appl.*, vol. 18, no. 4-5, pp. 385–400, Aug. 2002.
[37] Q. Xu and N. Nicolici, "On reducing wrapper boundary register cells in modular SOC testing," in *Proc. IEEE Int. Test Conf. (ITC)*, 2003, pp. 622–631.
[38] K. Chakrabarty, "Optimal test access architectures for system-on-a-chip," *ACM Trans. Des. Automat. Electron. Syst.*, vol. 6, no. 1, pp. 26–49, Jan. 2001.
[39] M. Benabdenbi, W. Maroufi, and M. Marzouki, "CAS-BUS: A test access mechanism and a toolbox environment for core-based system chip testing," *J. Electron. Testing: Theory Appl.*, vol. 18, no. 4-5, pp. 455–473, Aug. 2002.
[40] S. K. Goel and E. J. Marinissen, "Effective and efficient test architecture design for SOCs," in *Proc. IEEE Int. Test Conf. (ITC)*, 2002, pp. 529–538.
[41] Y. Huang *et al.*, "Optimal core wrapper width selection and SOC test scheduling based on 3-D bin packing algorithm," in *Proc. IEEE Int. Test Conf. (ITC)*, 2002, pp. 74–82.
[42] P. Varma and S. Bhatia, "A structured test re-use methodology for core-based system chips," in *Proc. IEEE Int. Test Conf. (ITC)*, 1998, pp. 294–302.
[43] V. Iyengar, K. Chakrabarty, and E. J. Marinissen, "Efficient test access mechanism optimization for system-on-chip," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 22, no. 5, pp. 635–643, May 2003.
[44] A. Sehgal, S. Ozev, and K. Chakrabarty, "A flexible design methodology for analog test wrappers in mixed-signal SOCs," in *Proc. IEEE Int. Conf. Comput. Des. (ICCD)*, 2005, pp. 50–55.
[45] E. G. Coffman, Jr., M. R. Garey, and D. S. Johnson, "An application of bin-packing to multiprocessor scheduling," *SIAM J. Comput.*, vol. 7, no. 1, pp. 7–17, Feb. 1978.
[46] Y. T. Wang and B. Razavi, "An 8-bit 150-MHz CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 308–317, Mar. 2000.
[47] D. A. Johns and K. Martin*, Analog Integrated Circuit Design*. New York: Wiley, 1997.
[48] C. Su and Y.-T. Chen, "Intrinsic response extraction for the removal of the parasitic effects in analog test buses," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 19, no. 4, pp. 437–445, Apr. 2000.
[49] ——, "Crosstalk effect removal for analog measurement in analog test bus," in *Proc. IEEE VLSI Test Symp. (VTS)*, 2000, pp. 403–408.
[50] S. Sunter, "A low cost 100 MHz analog test bus," in *Proc. IEEE VLSI Test Symp. (VTS)*, 1995, pp. 60–65.

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