

Test Strategies for Low Power Devices

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Abstract

Ultra low-power devices are being developed for embedded applications in bio-medical electronics, wireless sensor networks, environment monitoring and protection, etc. The testing of these low-cost, low-power devices is a daunting task. Depending on the target application, there are stringent guidelines on the number of defective parts per million shipped devices. At the same time, since such devices are cost-sensitive, test cost is a major consideration. Since system-level power-management techniques are employed in these devices, test generation must be power-management-aware to avoid stressing the power distribution infrastructure in the test mode. Structural test techniques such as scan test, with or without compression, can result in excessive heat dissipation during testing and damage the package. False failures may result due to the electrical and thermal stressing of the device in the test mode of operation, leading to yield loss. This paper considers different aspects of testing low-power devices and some new techniques to address these problems.

1. Introduction

With the arrival of wireless communication and battery-operated mobile devices, the push for low-power electronics has been tremendous. Ultra low-power devices are necessary in applications like bio-medical electronics and wireless sensor networks, where battery replacement is either impossible or too expensive. Examples of such applications are devices which are inserted into the human body, e.g. a pace maker. Similarly, devices mounted on protected natural resources such as trees depend on scavenged energy from wind, sun-light, and ambient heat. RFID chips are being developed for tracking objects, such as grocery items.

Designers have invented a number of circuit-level and system-level techniques to reduce power dissipation and elongate battery life. A high-level of system integration is important to reduce size and cost of these devices. For example, it is common to integrate Analog/Digital and Digital/Analog converters and RF transceivers along with microprocessors/microcontrollers/digital signal processors. The testing strategy for these devices should find the right synergy with the design techniques.

This paper deals with test strategies for low-power and ultra low-power devices. The paper is organized as follows. Section 2 enumerates the various challenges in

testing of low-power and ultra low-power devices. Section 3 considers test-mode power dissipation as a challenge in testing low-power devices. Scan-based structural testing is assumed as the basic test strategy, and we define ways to reduce average and peak test power during scan shift and scan capture, respectively. In Section 4, hierarchical scan test is considered for the testing of low-power devices. New techniques published in the literature for hierarchical scan test are reviewed. Section 5 considers the automation of test solutions for low-power and ultra low-power devices.

2. Test Challenges for Low-Power Devices

As mentioned in the previous section, system-on-chip (SoC) integration is used to build low-cost devices. While SoC design poses many big challenges, but the testing of these low-cost, low-power devices is even more daunting.

- System integration aggravates the problem of controllability and observability.
- The stress on low cost calls for test cost reduction, which can only be achieved through the use of low-cost testers and multi-site testing.
- The system designer defines several functional modes, during which a subset of the system components are active. For example, in a chip for wireless sensor networks, the authors use 6 low-power modes other than the active mode [1]. However, scan test modes typically have no relation to these functional modes, and are guided by considerations such as scan chain balancing. As a result, during a scan test mode, the power dissipation may exceed the peak power for which the packaging has been designed, resulting in circuit damage or circuit reliability problems.
- Fortunately, hierarchical test, which is mainly a strategy to reduce test generation complexity, can also help reduce test power if we can ensure that untested circuit components in a test mode are either turned off through power switches or receive constant logic values as inputs and do not dissipate dynamic power. Thus, partitioning the system for hierarchical testing must also consider power constraints.
- System integrators cannot avoid glue logic, which may receive inputs from and feed data to one or more IP cores. Test access to the glue logic will require that the IP cores be wrapped. Core wrappers may not be acceptable due to the associated area and speed penalties. In such a case, the DFT engineers tend to

include a top-up scan test mode, where all the scan flops in the circuit are made part of the scan chains.

- IDDQ testing becomes difficult to practice since system-level stand-by power for a good part is quite high by itself and hard to distinguish from that of a defective part. Similarly, dynamic burn-in testing though scan patterns can be a challenge since leakage power is high at elevated temperatures and excessive dynamic power during scan shift/capture aggravates the problem. This forces us to reduce the scan frequency during burn-in, which impacts the test time and effectiveness of testing.
- On-line test methods, which typically use BIST, have an additional requirement that they must not drain too much energy.
- Analog, mixed-signal, and RF circuits are very sensitive to addition of DFT logic not only from the view point of area, performance and power overhead, but also from the impact the DFT circuitry may have on the functionality. For example, probing may result in malfunctioning of an RF circuit [2], which is a motivation for using some form of self-test.
- Sensors are often integrated on the chip and these are MEMS based. Testing them is a specialized art.
- On-chip clock generation is required in systems which have to be tested in the field without the use of a tester. Since a reference clock through a crystal may be difficult to provide due to cost or environmental considerations, alternate techniques such as MEMS may have to be explored for clock generation [3].

3. Power Issues during Test

3.1 Test Power and Its Impact

There are two types of test power: *average test power* and *peak test power*. The former is the ratio between the total energy consumed during test and the test time, while the latter is the maximum power consumed during test [4].

High average test power leads to high heat dissipation, which is the cause of chip or package damage as well as reliability degradation due to hot spots [5-7]. This is especially a serious problem for low-power devices, which usually have low heat dissipation limits. On the other hand, high peak test power may cause excessive circuit noise and result in false failures during test [8]. This is intolerable since it lowers the manufacturing yield of low-power devices, pushing up their costs.

From the viewpoint of scan test, test power can be divided into *shift power* and *capture power*, corresponding to shift mode and capture mode, respectively. In shift mode, many clock pulses are applied to load a test vector and unload a test response. Therefore, average shift power dominates heat dissipation during scan shift. Excessive peak shift power may cause scan chain failures [9], resulting in yield

loss. In capture mode, where only one or two clock pulses are needed, the contribution towards test heat is negligible. However, as shown in Fig. 1, in the widely-used launch-off-capture-based scan-based transition-delay test scheme, excessive capture power can cause incorrect capture of test responses, resulting in yield loss [10].

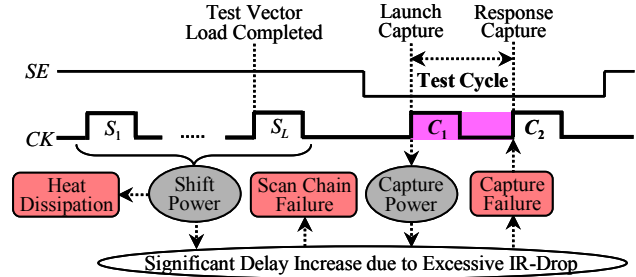


Fig. 1 Test power impact in at-speed scan testing.

Test power problems are becoming more and more serious due to the following reasons:

- (1) Aggressive use of power management in low-power devices is widening the gap between functional and test power. Power grid and package design capable of handling such lowered functional power is often too weak to handle the higher test power due to non-functional operations and parallelism in testing.
- (2) At-speed testing is mandatory for achieving required test quality. However, the short test cycle (Fig. 1) due to high system speeds, long sensitized paths for small-delay detection, and low supply voltage in low-power devices are making it highly susceptible to dynamic noise such as IR-drop in the power grid, severely challenging its applicability.

3.2 Basic Scan Test Power Reduction Techniques

Table 1 lists some basic power reduction techniques.

Table 1 Basic Techniques for Test Power Reduction

	Shift Power Reduction	Capture Power Reduction
DFT	<ul style="list-style-type: none"> • Shift Impact Blocking (blocking gate, special scan cell, first-level power supply gating, selective blocking) • Scan Chain Modification (scan cell reordering, scan chain segmentation, scan chain disabling) • Scan Clock Manipulation (splitting, staggering) 	<ul style="list-style-type: none"> • Partial Capture (circuit modification, scan chain disabling, one-hot clocking, capture clock staggering)
ATPG	<ul style="list-style-type: none"> • Blocking Test Generation • Low-Power Compaction • X-Filling (0-fill, 1-fill, minimum-transition-fill) 	<ul style="list-style-type: none"> • Test Generation (internal constraint checking, external constraint checking, target fault restriction) • FF-Oriented X-Filling (probability-based, justification-based, hybrid) • Node-Oriented X-Filling (internal-switching-activity-aware, critical-path-aware)

Generally, average shift power should be dramatically reduced to meet the package's stringent heat dissipation limits of low-power devices, and peak capture power should be reduced to such an extent that dynamic power supply noise in the weak power grid of low-power devices will not cause any false failures in capture mode.

In the following, we show two example techniques: one for shift power reduction and one for capture power reduction. Details on other techniques can be found in [4-7].

- **Shift Chain Segmentation: Shift Power Reduction**

As shown in Fig. 2, a scan chain is divided into n segments and only one segment is active at a time in shift mode. It has the potential of reducing shift power by $1/n$.

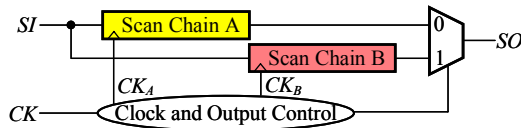


Fig. 2 Scan chain segmentation.

- **Probability-Based X-Filling: Capture Power Reduction**

As shown in Fig. 3, the 0 and 1 probabilities of each PPO X-bit are calculated, based on which the logic value for the corresponding PPT X-bit is determined. This helps reduce the capture switching activity at FFs [11].

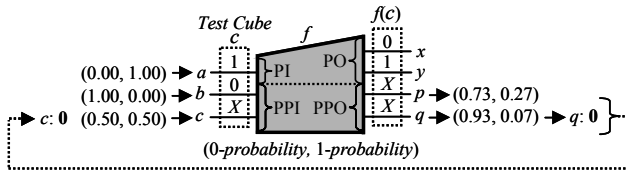


Fig. 3 Probability-based X-filling.

In addition, the power management infrastructure in low-power devices, such as *gated clocks* and *multiple power domains*, can be used to reduce test power. Furthermore, for a core-based design, power-aware test scheduling can take the power constraint of each core into consideration to guarantee that the total power of concurrently tested cores does not exceed the given power rating.

Test engineers need to select proper test power reduction techniques to build their own low-power DFT and ATPG flows, by considering the design, quality, and application characteristics of the target products, as well as EDA tool availability. In addition, it should be noticed that capture mode is more delicate than shift mode, in that circuit or clocking change in capture mode may trigger ATPG change, fault coverage loss, test data inflation, etc.

The effect of a test power reduction technique needs to be assessed by test power analysis. There is a need to improve the current gate-level dynamic power analysis flow that is expensive due to huge data volume and long run time. In addition, easy-to-compute yet highly-relevant test metrics, preferably at the gate-level, need to be established for

guiding choices in the techniques. Furthermore, the impact of power on timing also needs to be efficiently analyzed in order to make test power reduction more effective.

3.3 Other Test Power Reduction Issues

- **Low-Power Logic BIST**

Logic BIST is an attractive solution for test cost reduction and mission-critical applications. However, since logic BIST usually operates at system speeds and applies pseudo-random test stimuli, its power consumption is usually too high for low-power devices. Major techniques [7] for low-power logic BIST includes *LFSR modification*, *vector filtering*, *circuit partitioning*, and *test scheduling*.

- **Low-Power Memory Test**

Embedded memory blocks in a low-power device are often tested by memory BIST, in which test scheduling is needed to ensure that the power consumption of any group of concurrently-tested memory blocks does not cause any heat or IR-drop problem. In addition, the test power of each BISTed memory block can be reduced by power-aware memory test algorithms [7]. For example, original tests can be reordered to minimize the switching activity on each address line while retaining the fault coverage.

- **Leakage Test Power Reduction**

Leakage (subthreshold and gate) power increases rapidly with shrinking feature sizes and decreasing supply voltages, making leakage power reduction an important design issue for low-power devices. During test, gate leakage power can be reduced by DFT or ATPG techniques [14]. For example, the inputs of a gate can be carefully set so that the number of the on-transistors in the gate is reduced, without changing its output value.

4. Hierarchical Test Strategies for Low-Power Devices

Functional testing is one of the common alternatives for testing low-power devices for several reasons. Functional vectors are guaranteed to respect the test constraints of the device. Functional tests are also ideal for at-speed testing, since they do not over-exercise the power distribution infrastructure, resulting in false failures. For testing on-chip analog and mixed-signal circuits, functional tests are often the method of choice. Test-benches developed for functional verification can be converted into functional tests. There are several disadvantages of using functional vectors. They demand a lot of tester memory – this has several negative connotations: a low-cost tester cannot be used and the device cannot be made self-testable. Converting the outputs of simulation of a functional test-bench into functional patterns is a demanding task.

For the digital logic on the chip, scan-based testing using automatically generated test patterns is widely used. When the digital logic is large (several million gates), scan test

generation will have to be done hierarchically since the run-time and memory requirement of pattern generation does not scale linearly with gate count. When there are several digital IP cores, they can be tested one at a time. Test access mechanisms (TAM) such as test busses can be provided to gain controllability and observability access to the cores. Since testing the cores one after another may increase run-time, concurrent testing of cores is recommended, provided the TAM and tester constraints permit. Power dissipation constraints must be considered in concurrent test scheduling; this leads to a constrained optimization problem, where test application time is the objective under power/tester/TAM constraints [12].

Unfortunately, in hierarchical testing, testing of glue logic can pose a challenge if the cores are not wrapped for performance considerations [13]. A common solution in the industry is to provide a mop-up or daisy-scan mode, where all the scan cells in the design take part in a scan test. Modern-day SoC use test compression to reduce the test data volume; compressed test application is used for individual IP cores and daisy-scan is used for covering the faults in glue logic. Even though the number of patterns in daisy-scan are not expected to be high, the test application time and test power are significant in this mode. So much so that the benefits of hierarchical testing can be significantly diminished. Devanathan et al. have proposed a way to analyze the interactions among the cores and define test modes that can virtually eliminate the daisy mode [13]. For example, if there are 3 cores A, B, and C, and there is no direct interaction between cores A and C, the test modes can include the independent test modes A, B, C, and the modes A->B and B->C. This eliminates the daisy mode A->B->C, which is power-intensive.

The daisy scan mode is also a problem from the view point of test application time. It would be advisable to run the daisy scan patterns at a higher scan shift frequency to reduce the test application time. But this may be difficult since dynamic power dissipation during scan shift is directly proportional to the scan shift frequency. To overcome this difficulty, a new scan architecture is proposed in [14] which uses the on-chip power management infra-structure to reduce the voltage during scan shift. The authors show that both leakage power and dynamic power are considerably reduced through voltage scaling, permitting faster shift. In [15], the author explores a way to use frequency scaling to tradeoff shift power and test application time; the author suggests that if the total tolerable power in a test mode is P_{max} and the actual test power is lower, then the shift frequency can be increased to reduce test time.

IDDQ testing is almost always applied in the full-chip mode. However, the leakage power in daisy mode can be high, making it difficult to distinguish good parts from defective parts through measurement of standby current.

The authors of [16] propose a hierarchical IDDQ strategy where power supply can be turned off to individual cores during the individual phases of IDDQ test. The PMScan architecture of [14] is also applicable for IDDQ and burn-in tests, although PMScan has not been applied for reliability tests so far.

5. Low Power and Test: An EDA Perspective

Today, EDA vendors provide low power solution flows where low power intent is considered at each design stage [17]. EDA tools have been constantly challenged with problems related to integrating DFT insertion with logical/physical synthesis and timing closure. Building power and DFT solutions on a common synthesis platform enables optimal implementation of power management and DFT structures and maximizes productivity. This is easier said than done. Power management structures might introduce testability problems while test might increase the power consumption of the design. Test automation products have to fit in design synthesis flows, understand the designer's power intent and make designs testable by adding adequate DFT structures. At the same time, they need to drive down test application time and reduce test data volume while keeping power consumption under control.

5.1 Low Power Design Methodology

A low-power design may comprise the following design concepts and capabilities: (i) Multiple supplies, and probably multiple voltages, across different parts (also referred to as power domains) of the chip; (ii) Power-down of selective power domains while ensuring proper isolation between shutdown and live parts, as well as ensuring proper retention of flip-flop states; (iii) Supply voltage scaling/switching, together with frequency scaling/switching, across multiple scenarios (operation modes); (iv) Clock-gating of flip-flops; (v) Mapping of technology cells from libraries with different threshold voltage, and so on. Figure 4 shows a schematic of a typical low-power design where dedicated cells (isolation cells, power switches, level shifters, enabled-level shifters) are used along with a power controller. A standard is shaping up for users to specify the structural aspects of their power intent [18]. The operating environment details (process, temperature, voltage data, leakage power calculation, switching activity) are provided separately.

5.2 Support of Power Management Techniques

As part of the synthesis-based flows, test automation products need to understand the power related constraints and management structures. For a DFT product, this translates into the following considerations: (i) Each step in the DFT insertion process has to be made low-power aware; (ii) Additional work has to be done in order to test the power management structures themselves; (iii) The

tool has to allow the user make the best trade-offs between DFT architecture options and their impact on power management structure needs. On the other hand, an ATPG tool has to be guided by a power budget, usually in term of toggling activity. It needs to support the power management structures themselves. Finally, it also has to help the user make trade-off decisions in the area of pattern count, test application time and power consumption. Due to lack of space, this section only reviews the impact on DFT insertion.

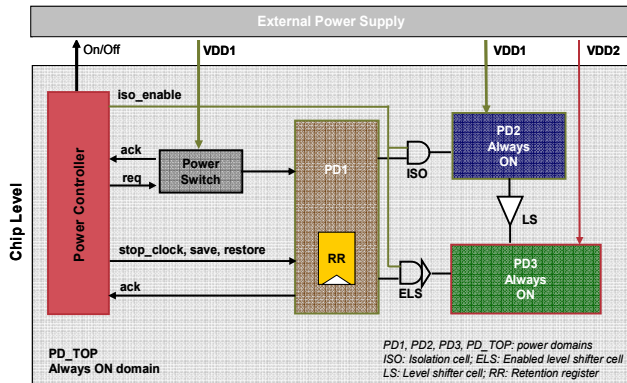


Fig. 4 Multi-voltage concepts

5.2.1 Impact on Test Design Rule Checking

Test design rules checking aims to verify that the design meets requirements for DFT insertion. The support for low power brings a new set of rules to be considered [19]. It includes the following: (i) Avoid unwanted power down during scan shift and capture; (ii) Avoid toggling of isolation clamp signals during scan shift and capture; (iii) Avoid retention state corruption during scan shift and capture; (iv) Scan chains must not span power domains that could be independently powered on/down; (v) Make sure power down/up of power domains could be activated.

5.2.2 Impact on DFT Architecting

A DFT product should be open in order to handle different DFT methodologies. It needs to offer orthogonal options regarding mixing of scan structures across different voltage domains and/or different power domains. It also needs to allow informed architecting iterations with the user so that this one could make the best trade-offs in term of scan chain budgeting/balancing versus voltage domain and/or power domain crossings. When DFT structures span different domains, the tool has to make sure the number of crossings is the minimum possible.

5.2.3 Impact on DFT Implementation

DFT Implementation is a one-step process that modifies the design by realizing a given DFT architecture. It inserts the DFT logic, routes scan chains, performs logic mapping and local design optimizations. In the low power environment, it also has to insert the power management

structures such as level shifters and isolation cells based on the designer's power intent. To cost-effectively achieve these tasks, DFT implementation has to be tightly integrated with design synthesis so that it relies on the same engines synthesis uses. In addition, it has to deal with the following considerations: (i) It needs to re-use existing power management structures whenever it is possible; (ii) It inserts DFT logic in order to facilitate test of power management structures; (iii) It should produce testable designs and test protocols compliant with the test design rules described above; (iv) Logic mapping and optimization should not violate voltage and/or power domain constraints such as using a non-always-ON cell on an always-ON path; (v) It should generate test models with power annotation for hierarchical flows support.

5.2.4 Test of Power Management Structures

There is no universal approach that tests all the power management structures. Each structure needs a specific test method: (i) An isolation cell is tested by adding DFT logic to provide access to the isolation cell control; (ii) Manufacturing test of retention registers requires both '0' and '1' to be saved and then restored [19]; (iii) The power control logic might need test points to be inserted in order to provide observability to output pins. This will force the outputs of the controller to the appropriate state during test which avoids toggling power meshes up and down; (iv) The production test of power switches is by far the most challenging task. A design could require a high number of switches, usually implemented in a daisy-chained manner. The power up of power domains faces rush current that could damage the chip. Usually, this is done in sequence and takes some time to get a power domain to its stable state. Many switches are used for given power domain and assembled in "fault-tolerant" scheme [20]. A defective switch (stuck-ON/OFF) usually results in performance degradation. Delay fault testing seems to be the right way to handle this situation.

5.2.5 Power Annotation and Hierarchical Design Flows

Hierarchical flows are used as a way of designing very large designs and core-based systems. In this context, the gates of block or core that has DFT implemented in it might not be used. Instead, only a test model is used for DFT insertion. Power details about DFT architecting should also be annotated on the model, the same way scan chain related clocks are abstracted [21].

5.3 Techniques to Reduce Power Consumption

Since power is becoming a huge concern, the first approach that comes to mind is to disable any DFT logic, particularly the test dedicated clocks, when this is not used. This applies to the gating of XOR tree in scan compressor IPs, core wrapping clocks, test points, etc. When DFT structures are active, they should help keep power

consumption under control. Today, there are no power-budget guided system-level planning tools available in the industry. However, there are many DFT techniques available to users that are designed to reduce power. Depending on their designs, users could use one or a combination of these solutions based on tradeoffs between test constraints and power consumption.

5.3.1 ATPG-level solutions

ATPG techniques could contribute to power reduction, but their results are not predictable as they are design dependent. One cannot quantify how much shift or capture power savings could be achieved. Examples of such techniques include low power fill of patterns and toggling-activity guided ATPG [11, 24], which are used to reduce average power and peak shift power.

5.3.2 Multi-mode DFT techniques

Existing techniques such as special scan cells [25], modified test data decompressor IP [22], etc., help reduce power dissipation but may not always yield optimal results as some of the benefits may be local and not propagated across the system. Intelligent DFT architecture and test scheduling can provide substantial system-wide power optimization. Multi-mode DFT architectures [23] provide several modes of operation of a design in which test patterns can be applied. Each mode targets different portions of the design or different DFT techniques and is associated with its own set of test constraints and procedures. For example, consider a SoC design encapsulating 4 cores. The design could have 4 different test modes where each core is individually tested. The cores that are not tested in a mode can be bypassed or rendered inactive through wrappers or other glue logic. This will reduce power dissipation by reducing switching activity in the inactive cores. In addition, there could be modes where combinations of cores are tested in parallel to reduce test application time. The optimal combinations are determined through intelligent power-aware test scheduling algorithms.

6. Conclusions

In this paper, we looked at the problems in the testing of low-power and ultra low-power devices and reviewed several existing solutions for these problems. We believe that this is an active area of research and development, which will see further growth in the coming years. While considerable effort has been spent towards developing scan-based test compression techniques for reducing pattern volume, we need to consider test power as a metric in developing these solutions. Process and temperature variability add a new dimension to the testing of low-power devices. Statistical techniques will be required in test generation to avoid pessimism and yield loss. Frequency and power binning will become necessary.

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